Datasheet

Boundary Conduction Mode

Power Factor Correction Controller IC

BD7692FJ

General Description

BD7692FJ is Power Factor Correction for AC/DC supplies the system which is suitable for all the products needing power factor improvement. The PFC adopts boundary conduction mode (BCM), and switching loss reduction and noise reduction are possible by Zero Current Detection (ZCD). ZCD detects by resistance, the auxiliary winding is unnecessary.

Key Specifications

- Input Voltage Range: 10 V to 26 V
- Operating Current: 470 µA (Typ)
- Maximum Frequency: 450 kHz (R_{RT}120 kΩ)
- Operating Temperature Range: -40 °C to +105 °C

Package

Package	W(Typ) x D(Typ) x H(Max)
SOP-J8	4.90 mm x 6.00 mm x 1.65 mm

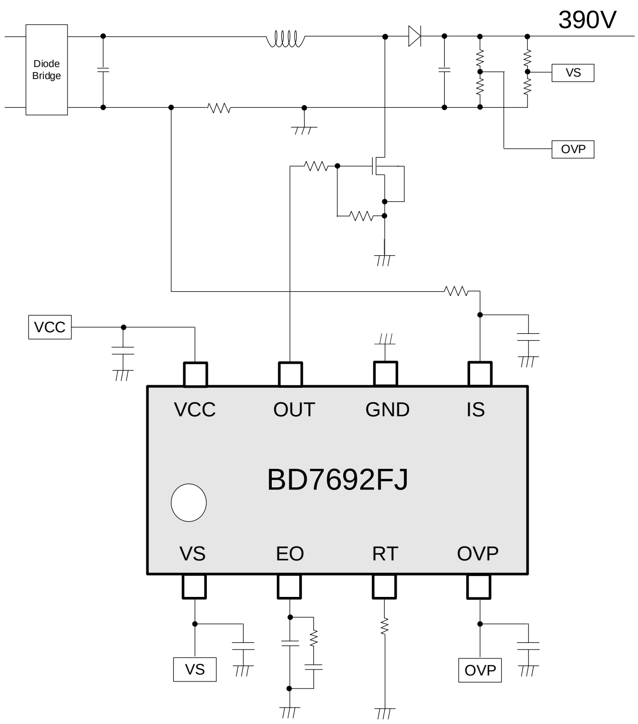
Features

- Boundary Conduction Mode
- Low Power Consumption
- VCCUVLO
- Resister Detection for ZCD
- Switching Loss Reduction, Noise Reduction by ZCD
- Dynamic and Static OVP by the VS Pin
- High Accuracy Over Current Detection (±4 %)
- Error Amplifier Input Short Protection
- Stable MOSFET Gate Drive by the Clamper
- Protection Function by the OVP Pin
- Over Voltage Reduce by Soft Start
- Safe Design by the IS-GND Short Timer Operation

Applications

- AC Adopter, TV, Lighting Equipment, Refrigerator, etc.

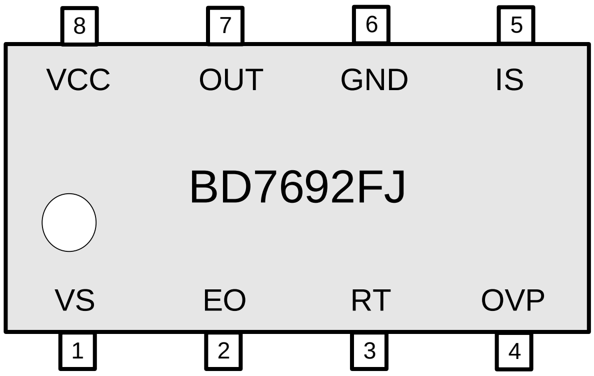
Typical Application Circuit



〇Product structure : Silicon integrated circuit 〇This product has no designed protection against radioactive rays

Pin Configuration

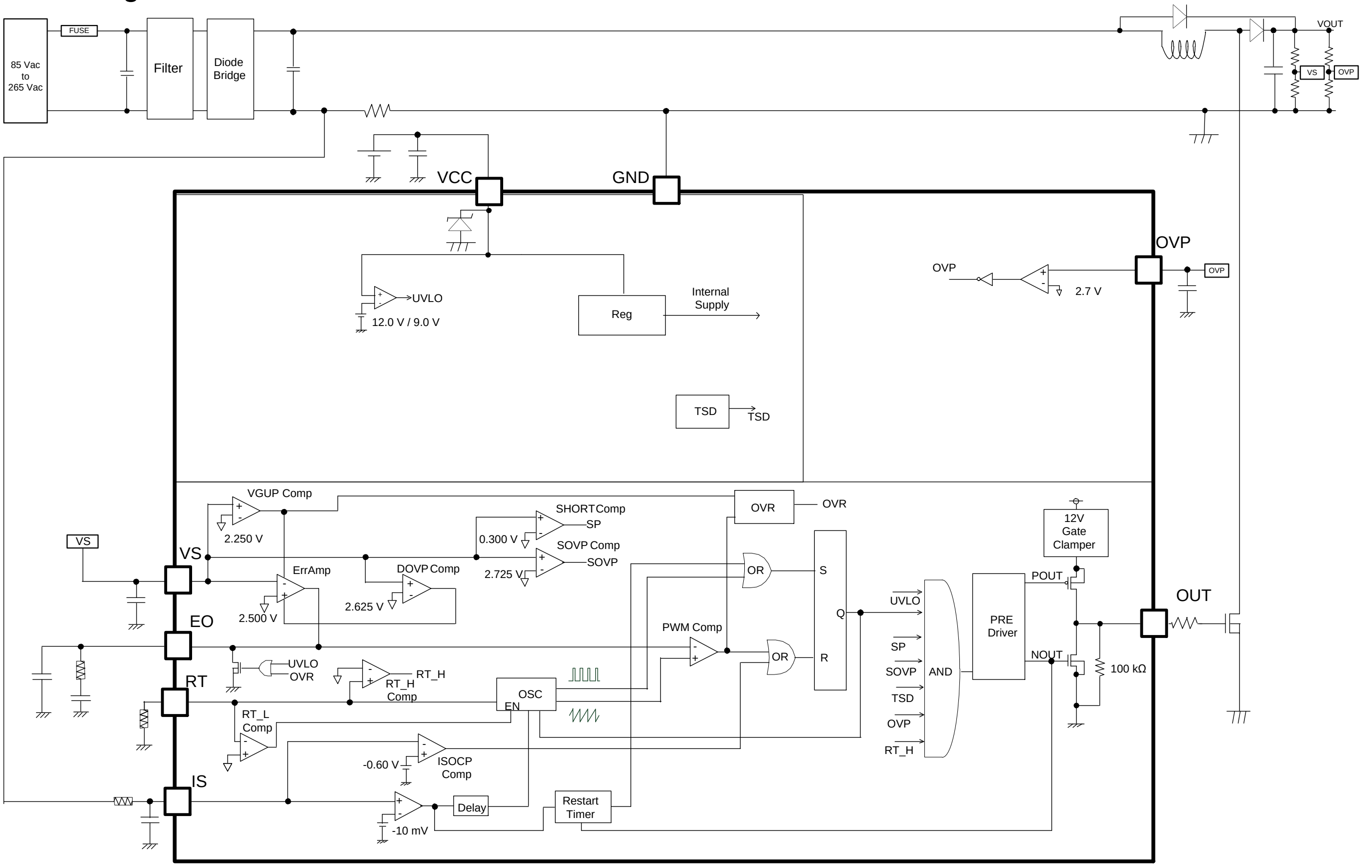
(TOP VIEW)



Pin Descriptions

Pin No.	Pin Name	I/O	Function	ESD Diode	
				VCC	GND
1	VS	I	Feedback input	-	○
2	EO	I/O	Error amp output	-	○
3	RT	I/O	Maximum frequency setting	-	○
4	OVP	I	Over voltage protection	-	○
5	IS	I	Zero current and over current detection	-	○
6	GND	-	GND	○	-
7	OUT	O	External MOSFET gate control	-	○
8	VCC	I	VCC	-	○

Block Diagram



Description of Blocks

1 VCC Protection

This IC has VCC UVLO (Under Voltage Lock Out) of the VCC pin. Switching stops at the time of VCC voltage drop.

2 Power Factor Correction

The power factor improvement circuit is a voltage control method of Boundary Conduction Mode.
The outline operation circuit diagram is shown in Figure 1. The switching operation is shown in Figure 2.

Switching Operation

1. MOSFET is turned on, and I_L increases.
2. The IC compares V_{EO} with V_{RAMP} slope decided in RT pin, and MOSFET is off when the V_{RAMP} voltage higher than V_{EO}.
3. MOSFET is off, and I_L decreases.
4. The IS pin detects a zero point of the I_L and turns on MOSFET.

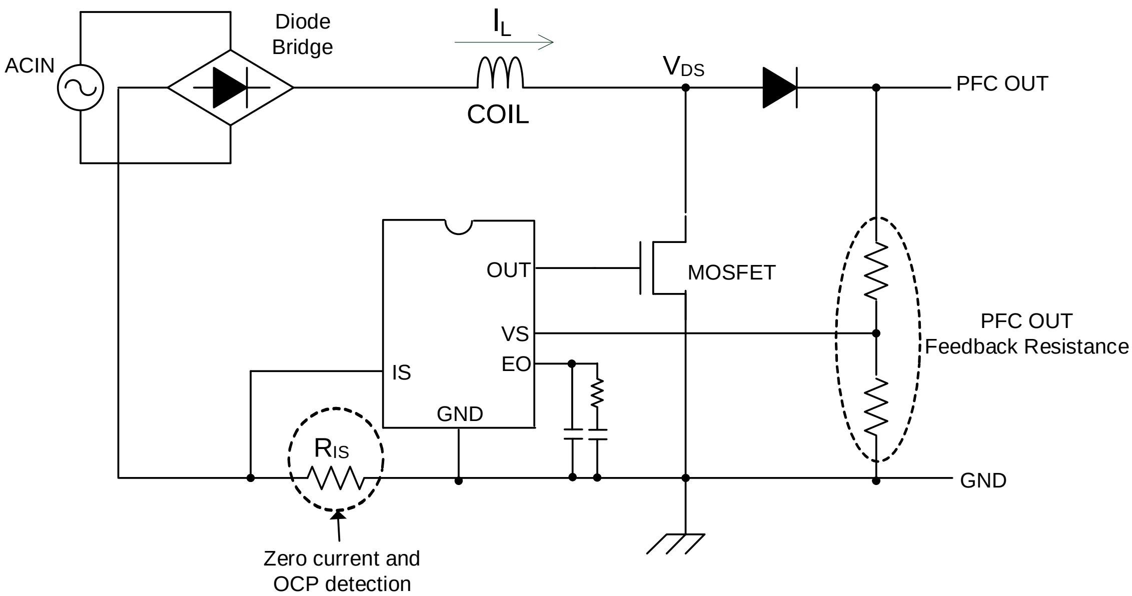


Figure 1. Operation Circuit Outline

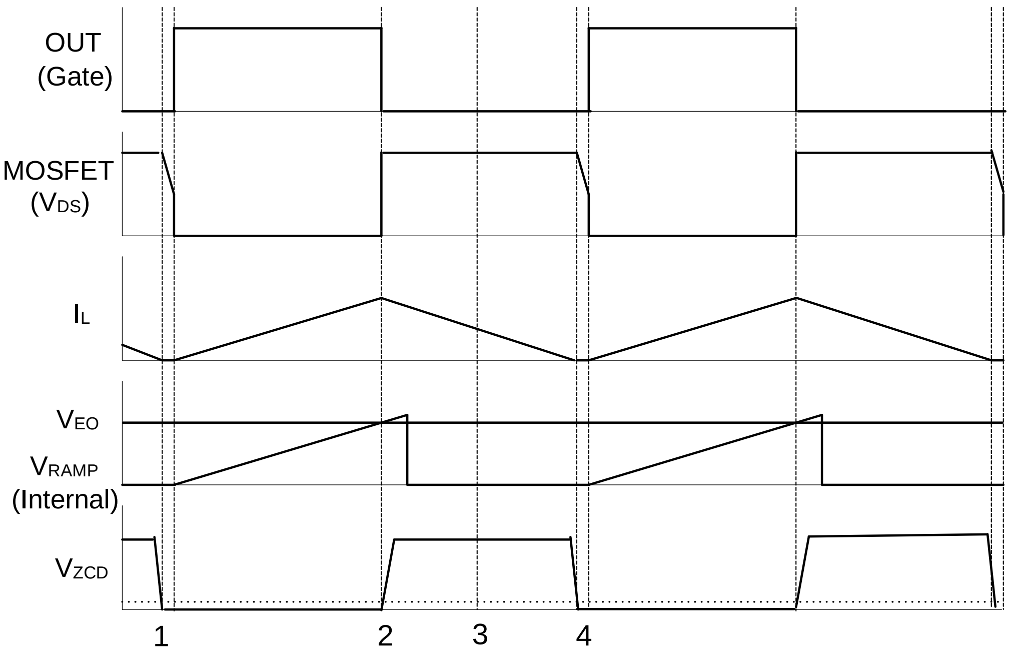


Figure 2. Switching Operation Timing Chart

Description of Blocks - continued

3 About ErrAMP

3.1 GmAMP

The VS pin monitors a divided point for resistance of the output voltage. The ripple voltage of AC frequency (50 Hz/60 Hz) overlaps with the VS pin. GmAMP removes this ripple voltage. GmAMP compares V_{AMP} (2.500 V Typ) with the removed voltage, GmAMP controls the EO voltage by this gap. When the EO pin voltage rises, ON width of the OUT pin becomes wide. When the EO voltage less than V_{OFF_TH} (0.30 V Typ), the IC stops switching. Therefore, it can stop switching operation when the EO pin connects to the GND.
Please set the external parts number of the error amplifier so that AC frequency does not overlap in EO pin. And, please confirm it by an actual board.

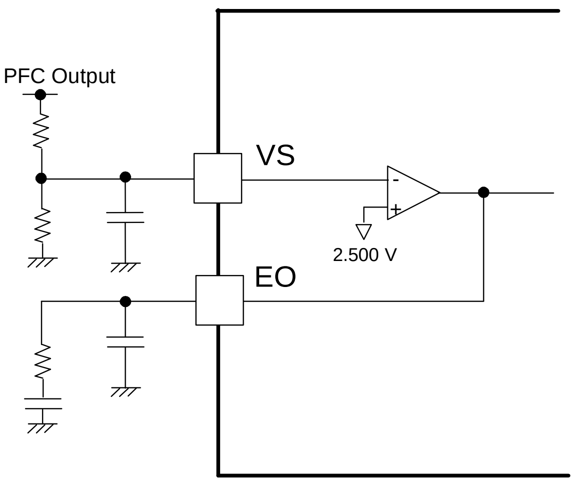


Figure 3. GmAMP Block Diagram

3.2 VS Short Protection

The VS pin has a short protection function.
A state of VS pin voltage < V_{SHORT} (0.300 V Typ) continues t_{VS_SH} (150 µs Typ) or more, it stops switching.
Figure 4 shows the operation.

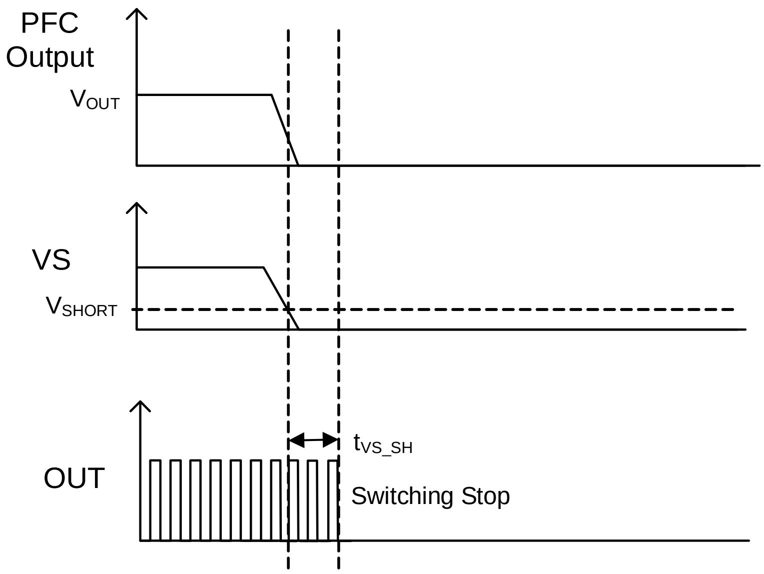


Figure 4. Operation of VS Short Protection

3.3 VS Low Voltage Gain Increase Function

When output voltage decreases by output load sudden changes, an output voltage drop period becomes long because a voltage control loop is slow. The VS pin voltage becomes lower than V_{GUP} (2.250 V Typ) (equivalent to -10 % of output voltage), the error amplifier increases the speed of the voltage control loop. ON width of OUT increases and prevents a long-term drop of the output voltage. When the VS pin voltage rises from V_{GUP} (2.250 V Typ), this operation stops.

3 About ErrAMP - continued

3.4 VS Overvoltage Gain Increase Function (DOVP)

When output voltage rises by startup or a rapid change of the output load, output voltage rises for a long term because a voltage control loop is slow. The VS pin voltage becomes V_{OVP} (2.625 V Typ) (equivalent to +5 % of output voltage), the error amplifier increases the speed of the voltage control loop. By this operation, it reduces ON width of OUT and prevents a long-term rise of the output voltage. When the VS pin voltage decreases under V_{OVP} (2.625 V Typ), this operation stops.

3.5 VS Overvoltage Protection Function (SOVP)

IC has static OVP for the time when VS is above the overvoltage gain increase function voltage V_{OVP}.
The VS pin voltage rises from V_{OVP1} (2.725 V Typ), it stops switching immediately. The VS pin voltage less than V_{OVP2} (2.600 V Typ), it starts switching. Figure 5 shows the operation.

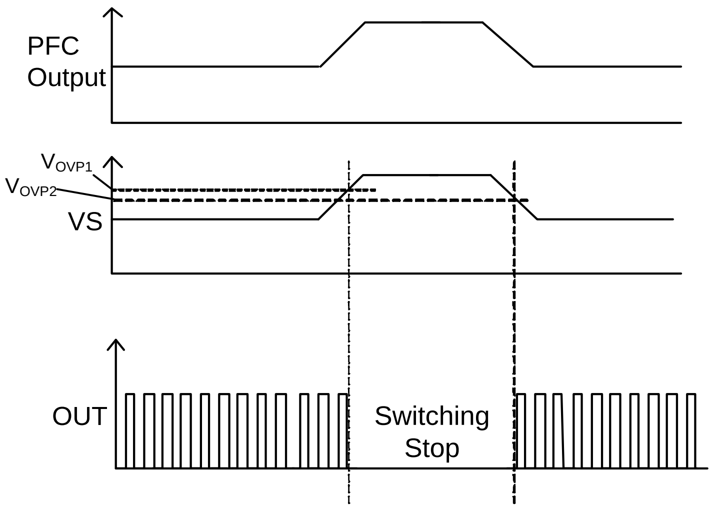


Figure 5. VS Overvoltage Protection Operation

3.6 Over Voltage Reduce Function at Start Up (OVR)

When the VS pin voltage performs a rise in startup to V_{GUP} (2.250 V Typ) (equivalent to -10 % of output voltage), it discharges the EO voltage to the off threshold voltage forcibly. OUT pulse width is narrows when the EO voltage falls, through rate of output voltage becomes slow and reduces over voltage in the startup.
This function is effective only once after VCCUVLO cancellation.

4 OVP Pin Over Voltage Protection

The OVP pin is an overvoltage protection function to use when VS feedback circuit is above static OVP (cf. Figure 6) at the time of abnormality. When the OVP pin voltage rises over V_{OVP3} (2.7 V Typ), it stops switching operation after t_{OVP3} (60 µs Typ) (cf. Figure 7). If the OVP pin becomes V_{OVP4} (2.6 V Typ) or less, it restarts operation.

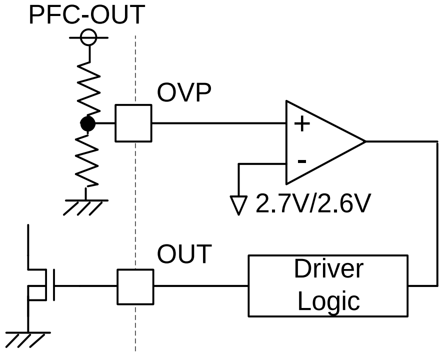


Figure 6. OVP Over Voltage Protection

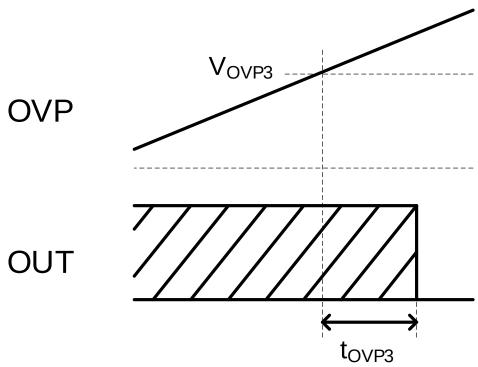


Figure 7. Timing Chart

Description of Blocks - continued

5 IS Pin

5.1 Zero Current Detection and Overcurrent Detection Function

The zero current detection circuit is a function to detect a zero cross of the inductor current (I_L) (cf. Figure 8).
When the voltage of the IS pin becomes higher than the zero current detection voltage, the OUT output becomes High after progress at zero current detection delay time (t_{ZCDD} 1.35 µs Typ). Please set the R_{IS} value about the overcurrent detection of the inductor current (I_L) so that the IS pin voltage becomes V_{IS_OCP} (-0.60 V Typ) or less. In addition, it recommends that to add CR filter for switching noise reduction. Figure 9 shows the operation.

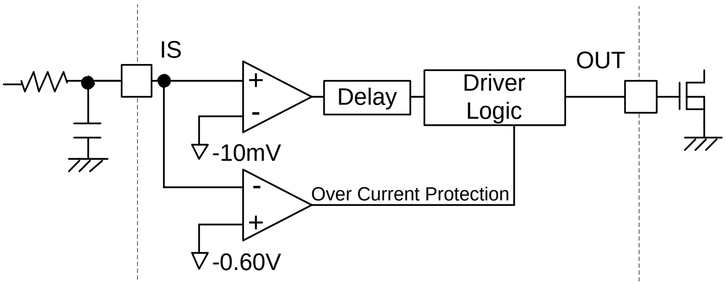


Figure 8. IS Current Detection Circuit

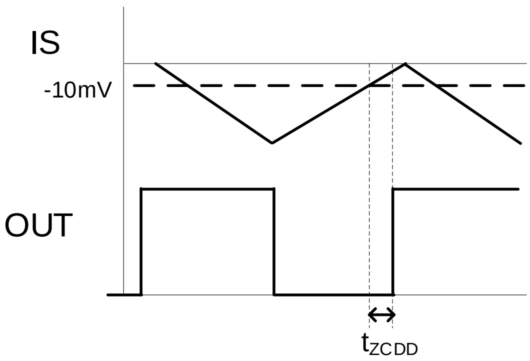


Figure 9. IS Zero Current Detection Delay Time

5.2 IS-GND Short Function

When the IS pin short-circuits with the GND pin, zero current detection is not possible. It is the IS voltage > -10 mV in off timing of the OUT pin in the case of -10 mV, IC operates the restart timer. It can prevent CCM operation by discharging the current which collected to the coil in a restart time.

6 RT Pin

This pin sets frequency of the slope voltage formed in the IC inside by external resistance. Figure 10 shows RT resistor value and relations of the maximum frequency. The maximum ON width on the application is calculated in the following formula. Figure 11 shows relations of RT resistor value and maximum ON width.

$$t_{ON\_MAX} = \frac{2 \times L \times P_{O\_PFC}}{V_{INMIN}{}^2 \times \eta_{\_PFC}} \quad [s]$$

Where:
V_{INMIN} is the minimum input voltage.
L is the inductance.
P_{O_PFC} is the maximum output power.
$\eta_{\_PFC}$ is the efficiency.

Necessary t_{ON_MAX} on application can be check as upper formula. Please set ON width in the RT pin t_{ON_MAX} or more.
In addition, it shows relations of RT resistor value and PFC zero current detection Delay in Figure 12.
The high-speed frequency in the light load is limited by RT pin to improve efficiency in the light load.
External resistance of the RT pin can set only 39 kΩ, 68 kΩ, 120 kΩ, 220 kΩ, 470 kΩ.
Do not set the fixed number except the designated value for RT external resistance.
The IC reads RT resistor value at the time of VCCUVLO cancellation and establishes setting. The setting is not changed even if it changes RT resistor value after VCCUVLO cancellation.

6 RT Pin - continued

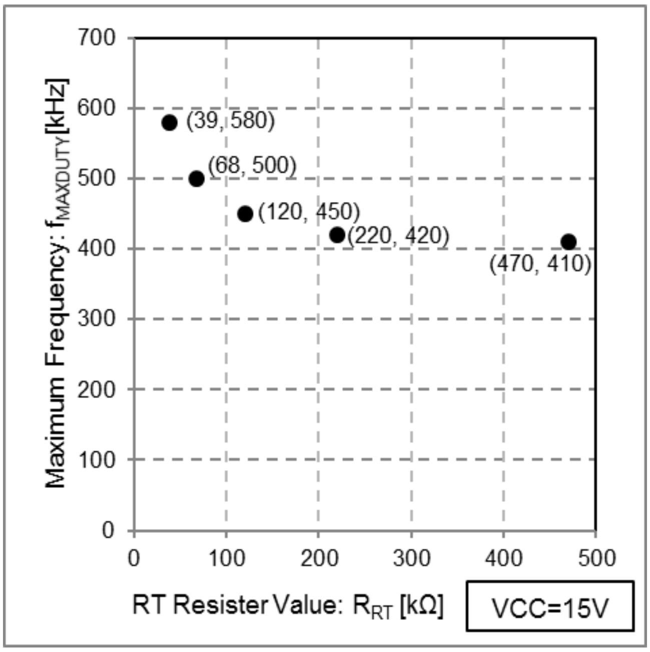


Figure 10. Maximum Frequency vs RT Resister Value

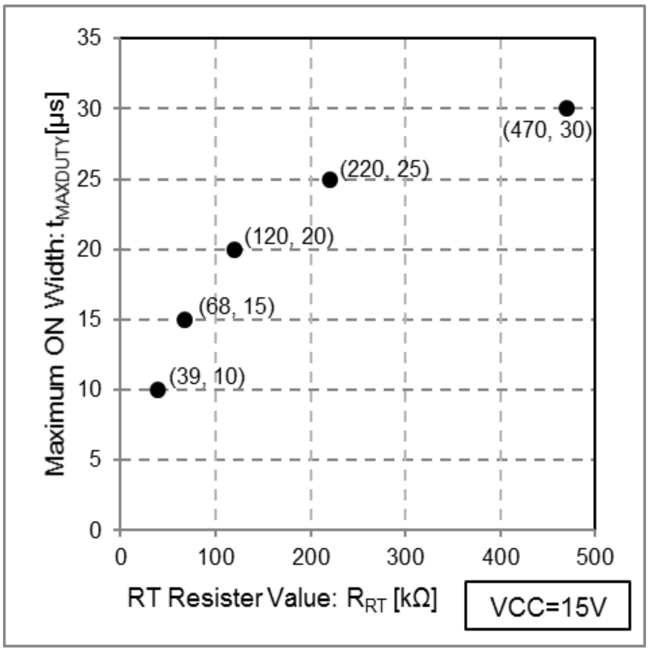


Figure 11. Maximum ON Width vs RT Resister Value

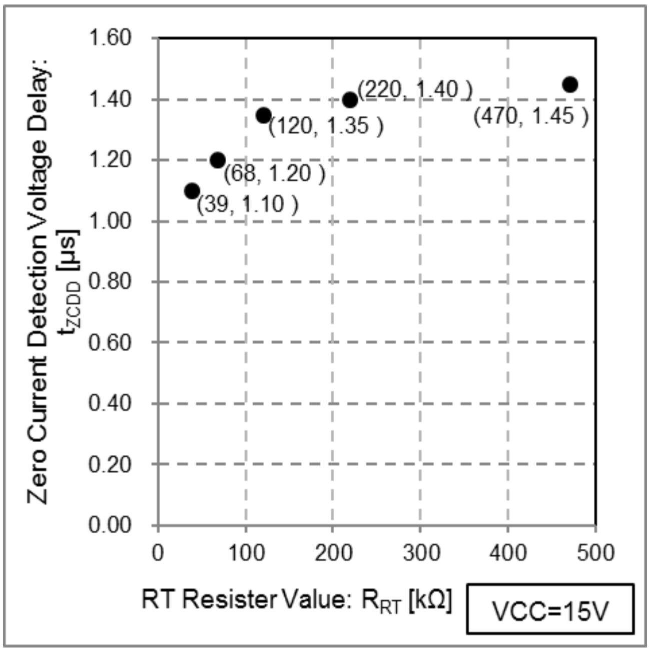


Figure 12. Zero Current Detection Voltage Delay vs RT Resister Value

Table 1. RT Resister Value Characteristics (reference value)

R_{RT} (kΩ)	$f_{MAXDUTY}$ (kHz)	$t_{MAXDUTY}$ (µs)	t_{ZCDD} (µs)
39	580	10	1.10
68	500	15	1.20
120	450	20	1.35
220	420	25	1.40
470	410	30	1.45

*These table and graph mentioned above are reference value. After the confirmation of the actual board, please set the fixed number.

*The characteristic kind to fluctuate by RT resistance is only five kinds. When RT resistance is set other than the resistor value mentioned above, it becomes the factor of the unstable operation.

Operation Mode of the Protective Circuit

Table2 shows the operation mode of each protection function.

Table 2. Operation Mode of Each Protective Circuit

Parameter	Contents	Protection mode			
		Detection Method	Detect Operation	Cancellation Method	Cancellation Operation
VCCUVLO	VCC Pin Low Voltage Protection	VCC<9.0 V(Typ) (VCC Drop)	OUT Stop EO Discharge	VCC>12.0 V(Typ) (VCC Rise)	Startup Operation
IS OCP	IS Pin Over Current Protection	IS<-0.60 V(Typ) (IS Drop)	OUT Stop	IS>-0.60 V(Typ) (IS Rise)	Normal Operation
VS Short Protection	VS Pin Short Protection	VS<0.300 V(Typ) (VS Drop)	OUT Stop EO Discharge	VS>0.300 V(Typ) (VS Rise)	Normal Operation
VS Gain Increase	VS Pin Low Voltage Gain Increase	VS<2.250 V(Typ) (VS Drop)	Gm Amplifier GAIN Increase	VS>2.250 V(Typ) (VS Rise)	Normal Operation
VS Dynamic OVP	VS Pin Overvoltage Protection 1	VS>2.625 V(Typ) (VS Rise)	Gm Amplifier GAIN Increase	VS<2.625 V(Typ) (VS Drop)	Normal Operation
VS Static OVP	VS Pin Overvoltage Protection 2	VS>2.725 V(Typ) (VS Rise)	OUT Stop	VS<2.600 V(Typ) (VS Drop)	Normal Operation
OVP	OVP Pin Overvoltage Protection 3	OVP>2.700 V(Typ) (OVP Rise)	OUT Stop	OVP<2.600 V(Typ) (OVP Drop)	Normal Operation

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit	Condition
Maximum Voltage 1	V_{MAX1}	-0.3 to +28.0	V	VCC
Maximum Voltage 2	V_{MAX2}	-0.3 to +15.0	V	OUT
Maximum Voltage 3	V_{MAX3}	-0.3 to +6.5	V	OVP, RT, VS, EO
Maximum Voltage 4	V_{MAX4}	-6.5 to +0.3	V	IS(Exclude 20 ms after input voltage injection)
IS Pin Maximum Current	I_{IS}	-20	mA	IS(20 ms or less after input voltage injection)
OUT Pin Output Peak Current 1	I_{OUT1}	-0.5	A	Source current
OUT Pin Output Peak Current 2	I_{OUT2}	+1.0	A	Sink current
Maximum Junction Temperature	Tjmax	+150	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
SOP-J8				
Junction to Ambient	θ_{JA}	149.3	76.9	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	18	11	°C/W

(Note 1) Based on JESD51-2A(Still-Air)
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

Recommended Operating Conditions

Parameter	Symbol	Rating			Unit	Condition
		Min	Typ	Max		
Supply Voltage	VCC	10.0	15.0	26.0	V	VCC Voltage
Operation Temperature	Topr	-40	+25	+105	°C	

Recommended Range of the External Component (Ta=25 °C)

Parameter	Symbol	Rating	Unit
VCC Pin Connection Capacity	C_{VCC}	10.0 or more	μF
RT Resister Value	R_{RT}	39, 68, 120, 220, 470	kΩ

Do not set the fixed number except the designated value for RT external resistance.

Electrical Characteristics (Unless otherwise specified Ta = 25 °C, VCC = 15 V)

Parameter	Symbol	Specifications			Unit	Condition
		Min	Typ	Max		
[Circuit Current]						
Circuit Current(ON)1	I_{ON1}	-	470	1000	µA	VS=1.0 V, EO=OPEN, R_{RT}=120 kΩ, OVP=OPEN
Circuit Current (ON)2	I_{ON2}	-	530	1200	µA	VS=1.0 V, EO=OPEN, R_{RT}=120 kΩ, OVP=0 V (PULSE operation)
Start Up Current	I_{ON3}	-	55	110	µA	VCC=11 V
[VCC Pin Protection]						
VCC UVLO Voltage1	V_{UVLO1}	11.0	12.0	13.0	V	VCC rise
VCC UVLO Voltage2	V_{UVLO2}	8.0	9.0	10.0	V	VCC drop
VCC UVLO Hysteresis	V_{UVLO3}	-	3.0	-	V	$V_{UVLO3} = V_{UVLO1} - V_{UVLO2}$
[Gm Amplifier Block]						
VS Pin Pull-up Current	I_{VS}	-	0.7	-	µA	
Gm Amplifier Reference Voltage 1	V_{AMP}	2.465	2.500	2.535	V	
Gm Amplifier Line Regulation	V_{AMP_LINE}	-20	-1	-	mV	VCC=10 V to 26 V
Gm Amplifier Trans Conductance	T_{VS}	45	70	95	µA/V	EO=2.5 V V_{GUP} <VS< V_{OVP}
Gm Amplifier Source Current	I_{EO_SOURCE}	30	50	70	µA	VS=1.0 V
Gm Amplifier Sink Current	I_{EO_SINK}	30	50	70	µA	VS=3.5 V
[EO Block]						
Off Threshold Voltage	V_{OFF_TH}	0.15	0.30	0.60	V	
EO Discharge Current	I_{EO}	1	2	4	mA	VCC=11 V, EO=1.0 V
[OSC Block]						
Maximum ON Width1	$t_{MAXDUTY1}$	8	10	12	µs	R_{RT}=39 kΩ, EO=4.0 V
Maximum ON Width2	$t_{MAXDUTY2}$	16	20	24	µs	R_{RT}=120 kΩ, EO=4.0 V
Maximum ON Width3	$t_{MAXDUTY3}$	24	30	36	µs	R_{RT}=470 kΩ, EO=4.0 V
Maximum Frequency1	$f_{MAXDUTY1}$	493	580	667	kHz	R_{RT}=39 kΩ, EO=0.3 V
Maximum Frequency2	$f_{MAXDUTY2}$	382	450	518	kHz	R_{RT}=120 kΩ, EO=0.3 V
Maximum Frequency3	$f_{MAXDUTY3}$	348	410	472	kHz	R_{RT}=470 kΩ, EO=0.3 V
RT Output Voltage	V_{RT}	0.9	1.2	1.8	V	R_{RT}=120 kΩ
[IS Block]						
Zero Current Detection Voltage	V_{ZCD}	-15	-10	-5	mV	
Zero Current Detection Voltage Delay	t_{ZCDD}	0.65	1.35	2.05	µs	R_{RT}=120 kΩ
IS Overcurrent Detection Voltage	V_{IS_OCP}	-0.62	-0.60	-0.58	V	
Restart Timer	t_{REST}	15	30	45	µs	IS = GND
[VS Protection Block]						
VS Short Protection Detection Voltage	V_{SHORT}	0.200	0.300	0.400	V	
VS Shortstop Protection Detection Time	t_{VS_SH}	50	150	300	µs	
VS Overvoltage Gain Increase Voltage	V_{OVP}	1.025 x V_{AMP}	1.050 x V_{AMP}	1.075 x V_{AMP}	V	
VS Overvoltage Protection Detection Voltage 1	V_{OVP1}	1.075 x V_{AMP}	1.090 x V_{AMP}	1.105 x V_{AMP}	V	VS rise
VS Overvoltage Protection Detection Voltage 2	V_{OVP2}	1.020 x V_{AMP}	1.040 x V_{AMP}	1.060 x V_{AMP}	V	VS drop
VS Overvoltage Protection Detection Voltage Hysteresis	V_{HYS}	0.030 x V_{AMP}	0.050 x V_{AMP}	0.070 x V_{AMP}	V	
VS Low Voltage Gain Increase Voltage	V_{GUP}	0.840 x V_{AMP}	0.900 x V_{AMP}	0.960 x V_{AMP}	V	
[OVP Block]						
OVP Detection Voltage 1	V_{OVP3}	2.6	2.7	2.8	V	OVP rise
OVP Detection Voltage 2	V_{OVP4}	2.5	2.6	2.7	V	OVP drop
OVP Detect Time	t_{OVP3}	20	60	150	µs	
[OUT Block]						
OUT H Voltage	V_{POUTH}	10.8	12.0	13.2	V	OUT=-20 mA
OUT L Voltage	V_{POUTL}	-	-	1.00	V	OUT=+20 mA
OUT Pull-down Resistance	R_{PDOUT}	75	100	125	kΩ	

Typical Performance Curves

(Reference data)

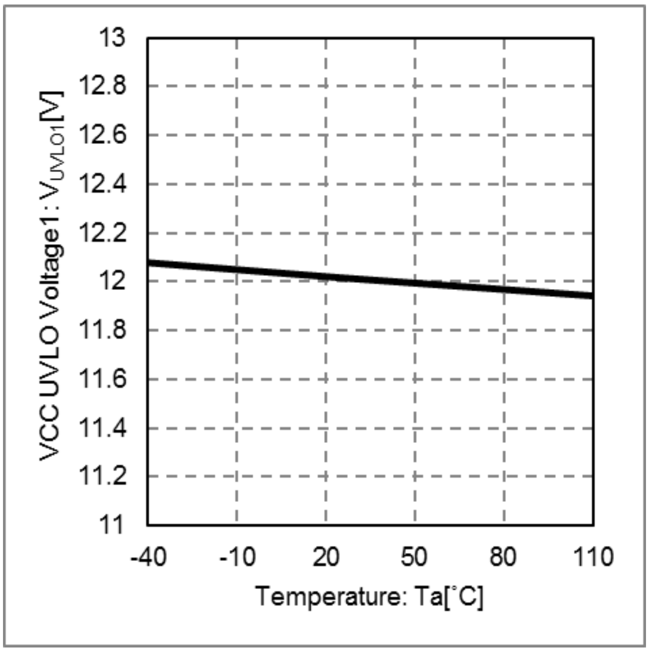


Figure 13. VCC UVLO Voltage1 vs Temperature

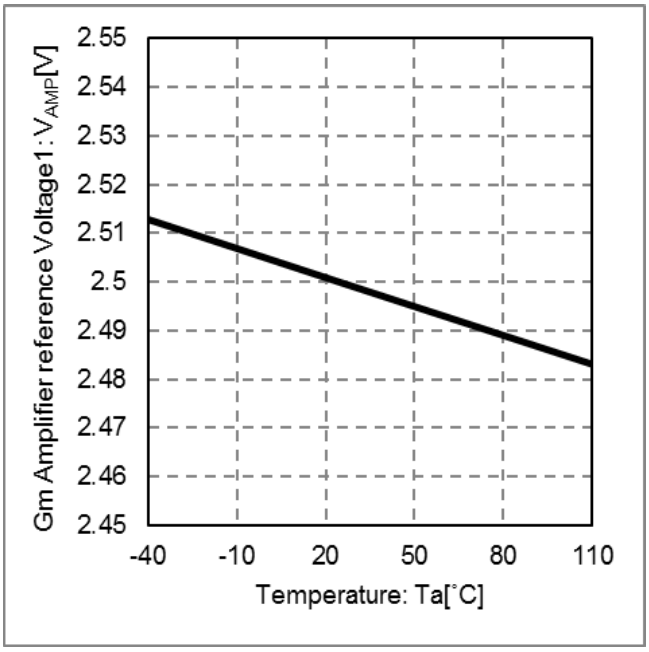


Figure 14. Gm Amplifier Reference Voltage1 vs Temperature

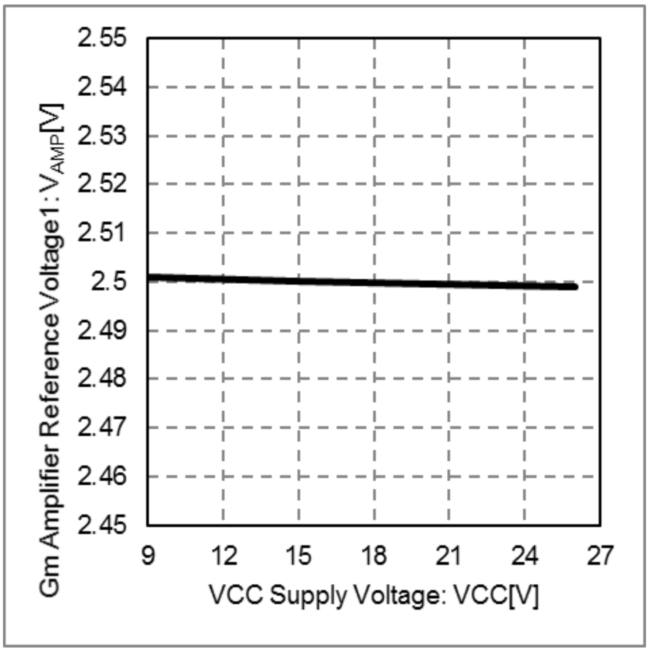


Figure 15. Gm Amplifier Reference Voltage1 vs VCC Supply Voltage

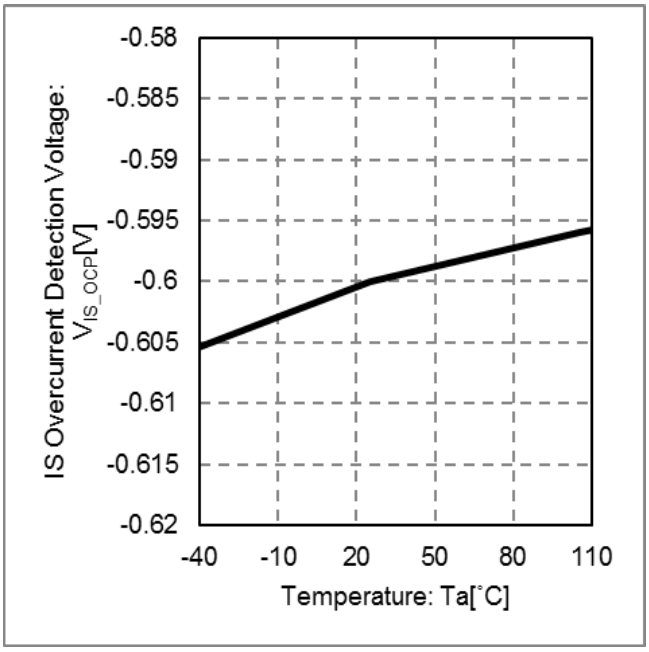


Figure 16. IS Overcurrent Detection Voltage vs Temperature

Typical Performance Curves - continued

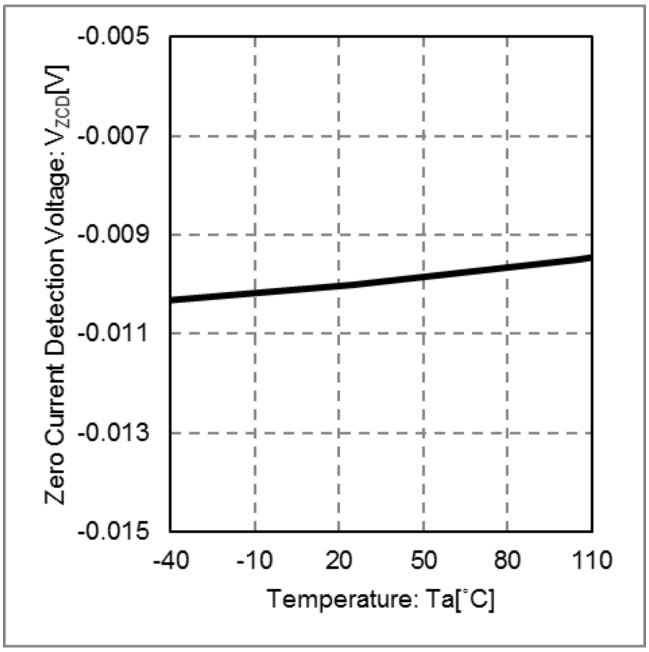


Figure 17. Zero Current Detection Voltage vs Temperature

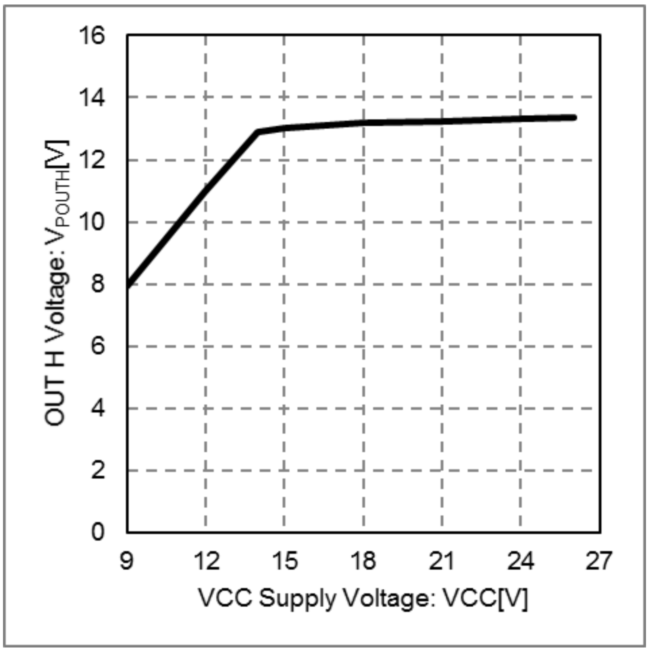


Figure 18. OUT H Voltage vs VCC Supply Voltage

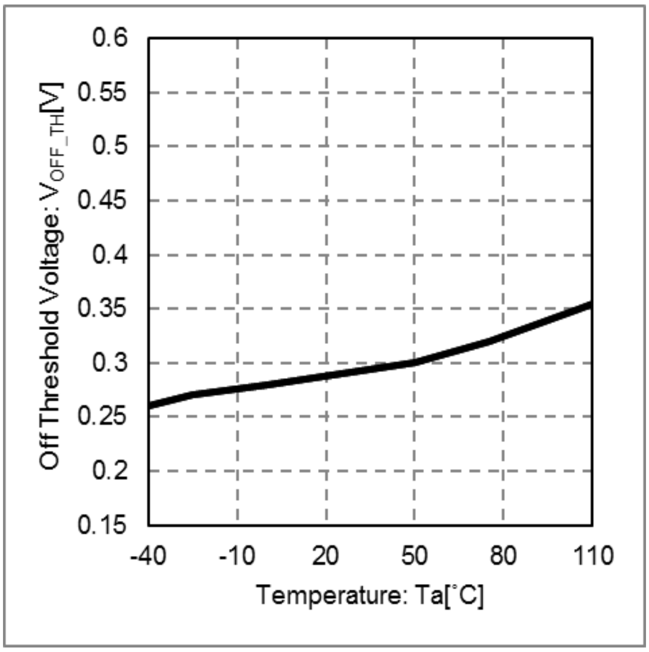


Figure 19. Off Threshold Voltage vs Temperature

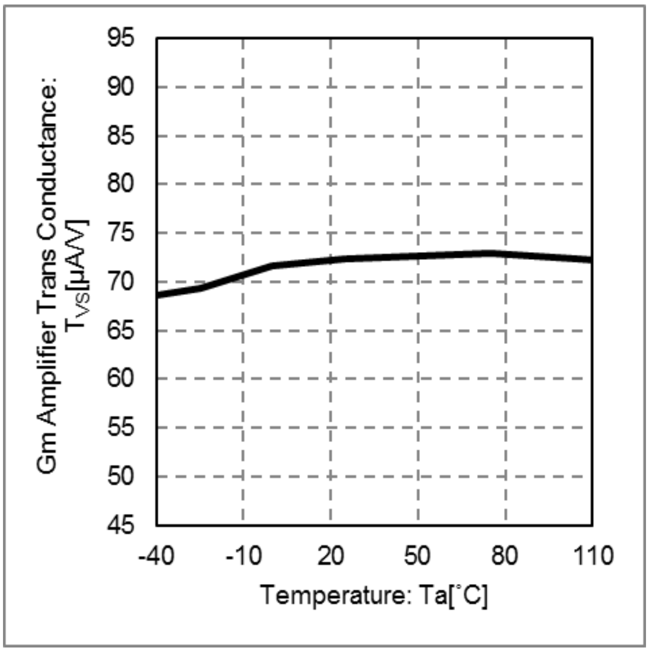


Figure 20. Gm Amplifier Trans Conductance vs Temperature

Timing Chart

The startup sequence is shown below.

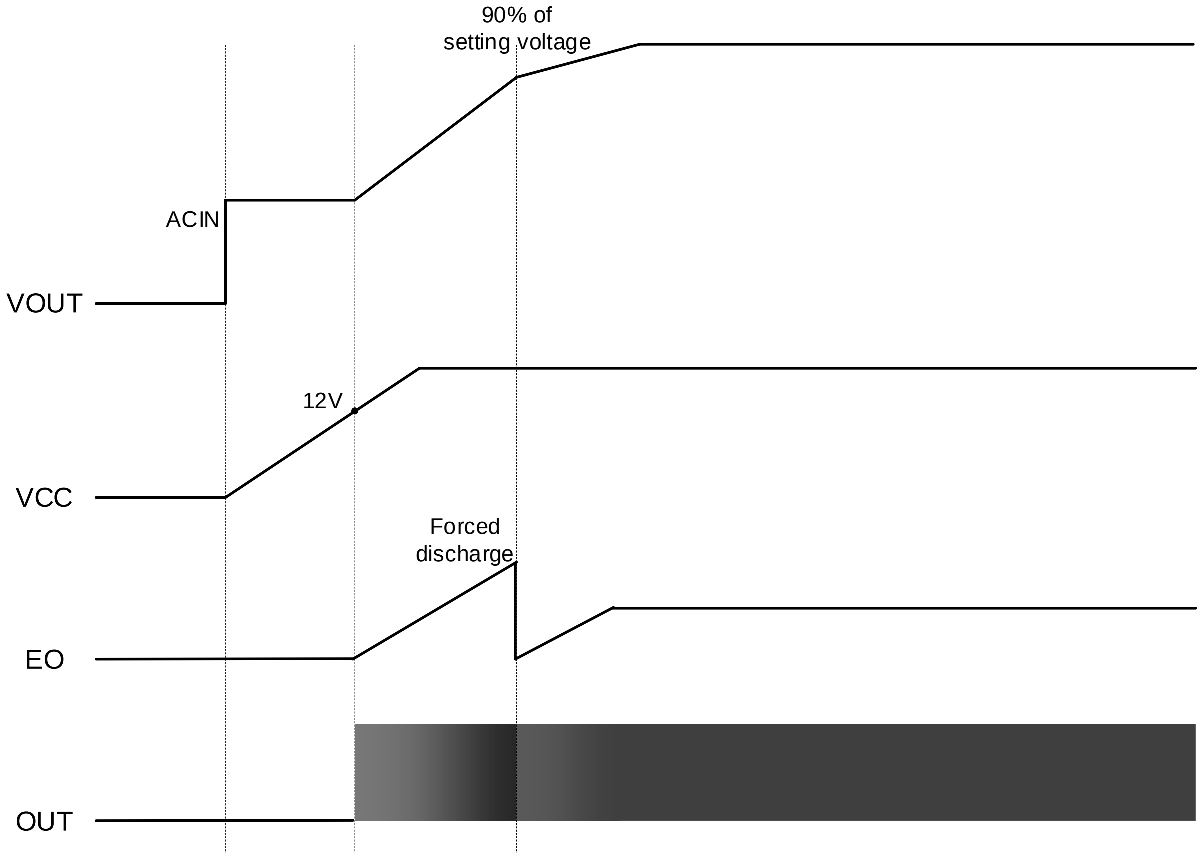


Figure 21. Startup Sequence

Application Example

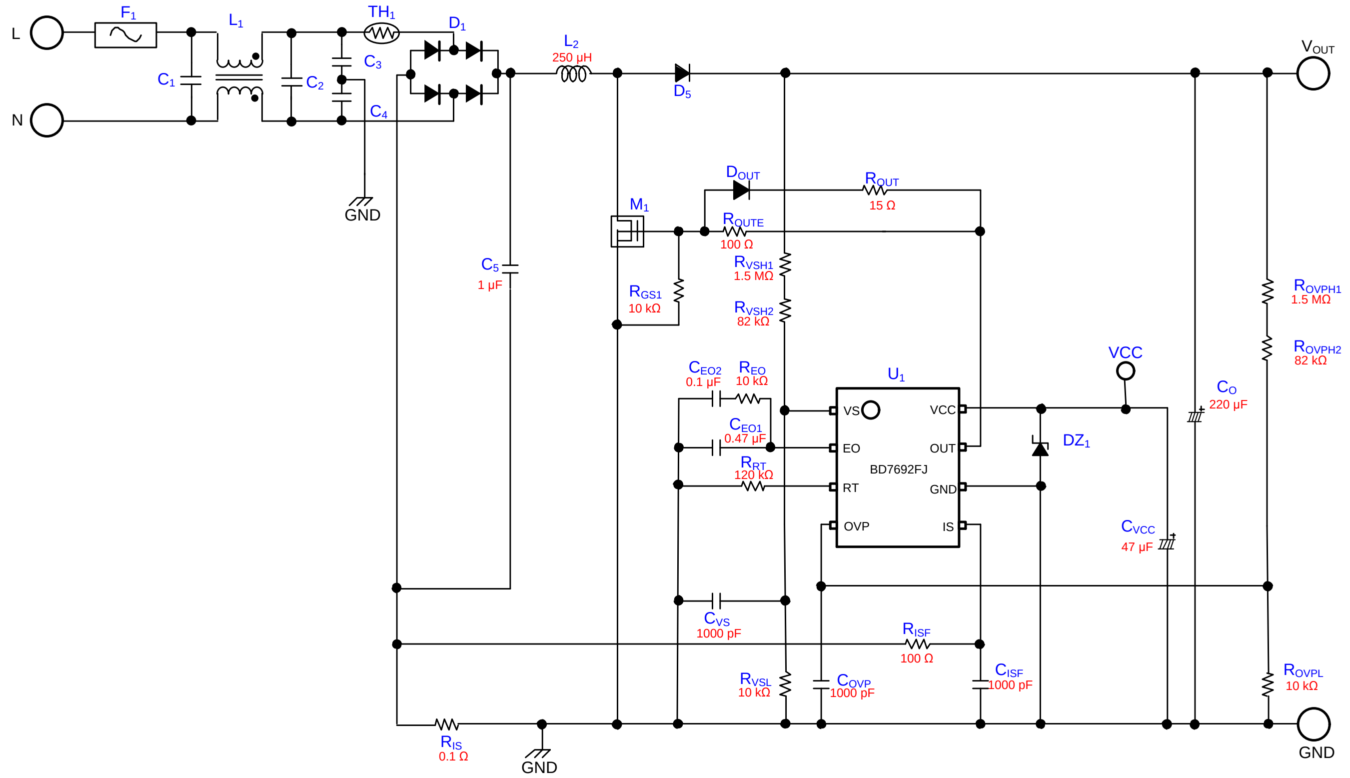


Figure 22. Application Example

Application Example – continued

1 Output Voltage Setting

The output voltage is decided in resistor value of R_{VSH} and R_{VSL}.

$$V_{OUT} = \left(1 + \frac{R_{VSH}}{R_{VSL}}\right) \times V_{AMP} = \left(1 + \frac{1582\ k\Omega}{10\ k\Omega}\right) \times 2.5\ V = 398 \quad \text{[V]}$$

Where:
R_{VSH} is the high side resister value of output feedback line.
R_{VSL} is the low side resister value of output feedback line.
V_{AMP} is the Gm Amplifier Reference Voltage 1

2 Decision of Minimum Frequency f_{SW}

The switching frequency of PFC

$$f_{SW} = \frac{\eta_{\_PFC} - {V_{IN}}^2}{2 \times P_{O\_PFC} \times L} \times \frac{V_{OUT} - \sqrt{2} \times V_{IN}}{V_{OUT}} \quad \text{[V]}$$

Where:
V_{IN} is the input voltage.
L is the inductance.
P_{O_PFC} is the maximum output power.
$\eta_{\_PFC}$ is the efficiency.

The frequency is minimized in the minimum input voltage. Slow frequency is effective about loss and noise. However, it is necessary to make inductance large when frequency is too slow. In addition, it enters the audible band when frequency lowers to 20 kHz or less, and sound banging occurs. It designs the minimum frequency as 50 kHz this time.

3 Calculation of the Inductance

$$L = \frac{\eta_{\_PFC} - {V_{IN}}^2}{2 \times P_{O\_PFC} \times fsw} \times \frac{V_{OUT} - \sqrt{2} \times V_{IN}}{V_{OUT}} \quad \text{[V]}$$

e.g. V_{IN}=AC90 V, V_{OUT}=400 V, P_{O_PFC}=200 W, $\eta_{\_PFC}$=0.9, f_{SW}=50 kHz

$$L = 248.5\ \mu H \approx 250 \quad [\mu\text{H}]$$

4 Calculation of the Inductor Current

$$I_{PK} = \frac{\sqrt{2} \times V_{IN}}{L} \times t_{ON} = \frac{2\sqrt{2} \times P_{O\_PFC}}{\eta_{\_PFC} \times V_{IN}} = 6.98 \quad \text{[A]}$$

5 Calculation of the ON Width

$$t_{ON\_MAX} = \frac{2 \times L \times P_{O\_PFC}}{{V_{INMIN}}^2 \times \eta_{\_PFC}} \quad \text{[s]}$$

ON width is short at the high AC voltage. Therefore, the ON width is decided with the minimum AC voltage.
It recommends RT setting such as the maximum ON width is just covered at the minimum AC voltage when an AC input voltage range is wide. ON width is short when the high AC voltage. And the EO voltage range is small. EO voltage band width is the large then the ON width setting by the RT resistance is short.

6 VCC External Capacitor

The VCC pin can reduce VCC voltage change at the time of the switching by attaching capacitor.
This IC drives gate capacitor of the external MOSFET by the OUT pin. The VCC capacitor recommends electric field capacitor 10 µF or more withstand pressure 35 V or more.
When the OUT pin outputs H, the gate capacitor charge current of the MOSFET flows from VCC in the OUT pin direction. When there is not VCC capacitor, the VCC voltage descends. The VCC voltage descent may become the factor of a switching stop by the VCCUVLO detection and the unstable operation. In order to avoid this, VCC capacitor is necessary. The VCC voltage descent depends on external MOSFET, operation frequency (output load) and the AC voltage.
Please confirm whether there is not VCC voltage descent which causes the VCCUVLO false detection at the time of MOSFET drive under the assumed situation with an actual board.

Attention in the Board Design

About parts placement

Please locate the parts in the Figure 23 inside dot line near the IC. In addition, please do parts placement to avoid the interference with switching lines and high current lines such as inductor, DRAIN.

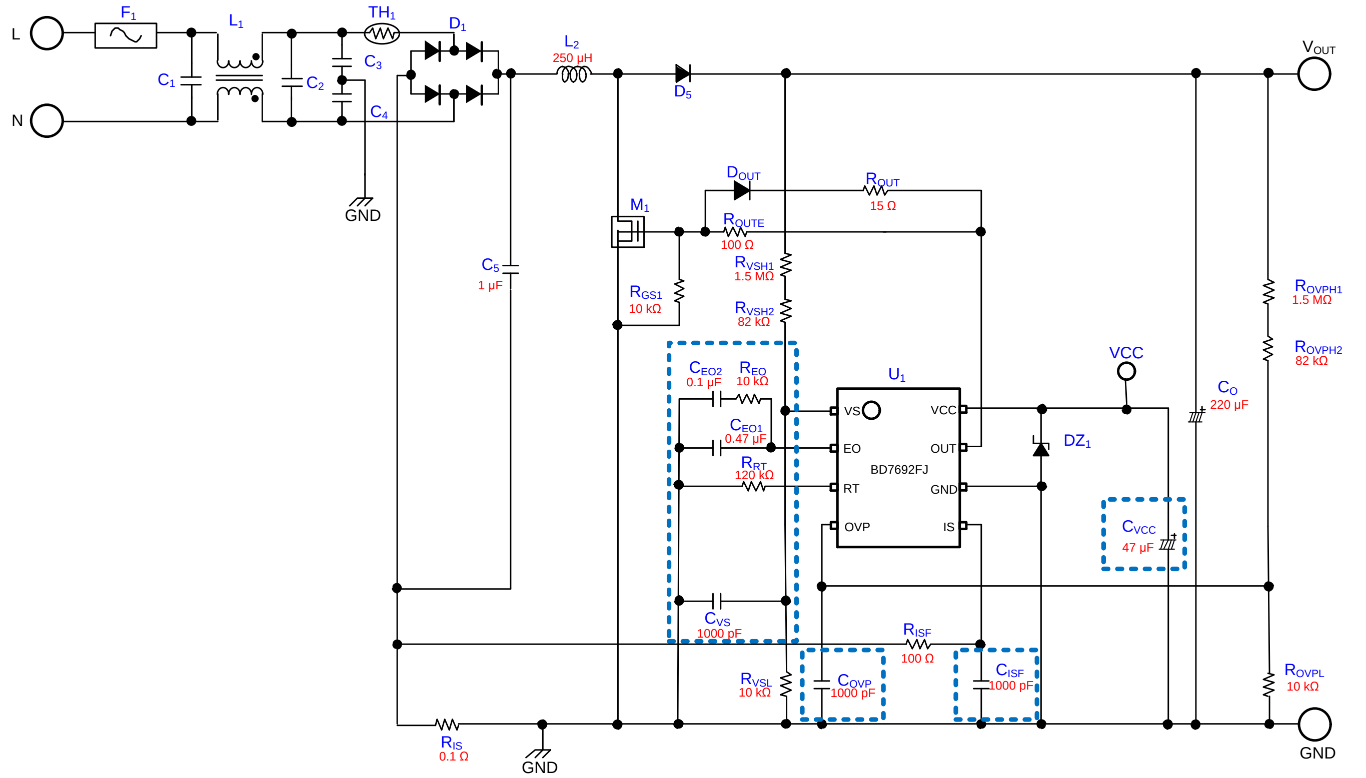


Figure 23. Parts Placement

About GND wiring guidance

The red line of Figure 24 is the GND lines which large current flows. Each line independence wires it, and please wire it short and thickly. A blue line is ICGND. Please make a common use ICGND and GND of IC around parts.

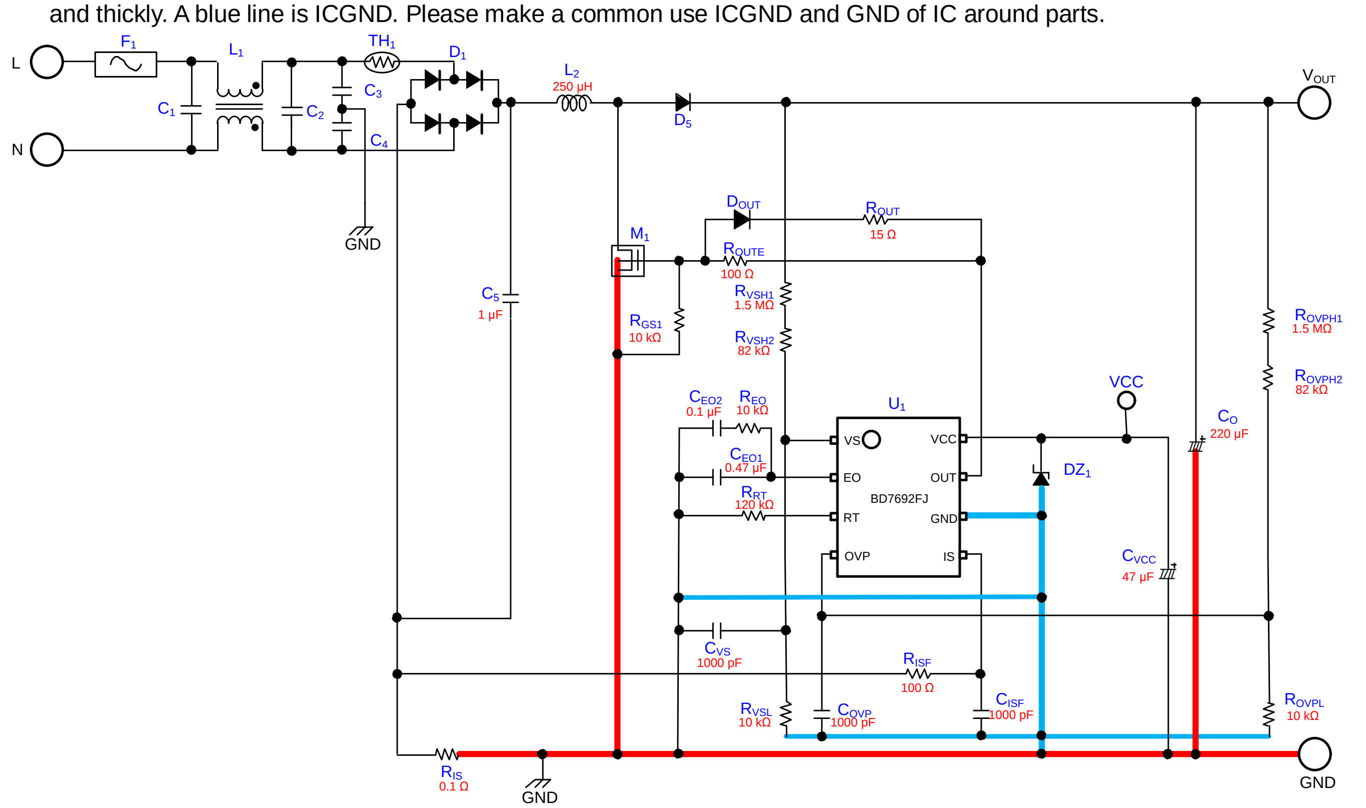


Figure 24. GND Line Layout

Attention in the Board - continued

About large current line
Large circuit current flows through the part of the red line of Figure 25. Please wire it short and thickly. Do not place IC and high impedance line near the red line because it has large noise.

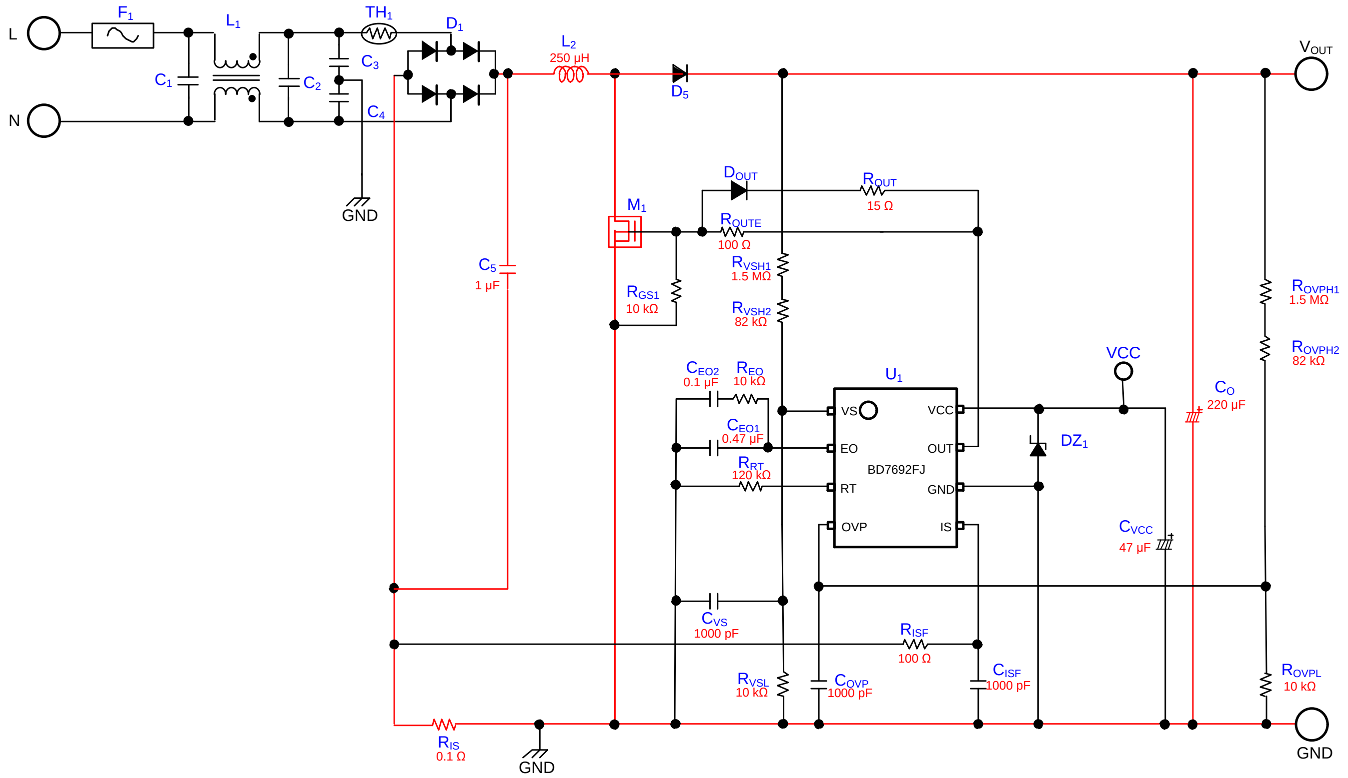
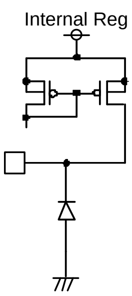
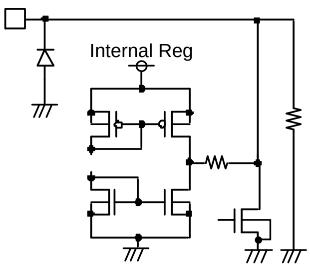
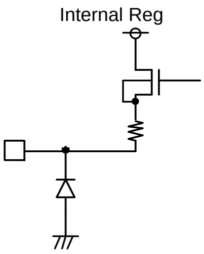
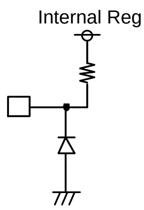
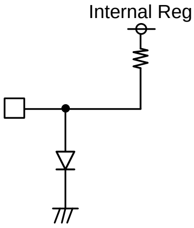
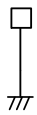
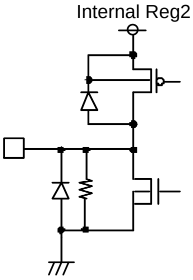
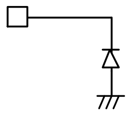


Figure 25. High Current Line Layout

I/O Equivalence Circuits

<table>
<tr><td>1</td><td>VS</td><td>2</td><td>EO</td><td>3</td><td>RT</td><td>4</td><td>OVP</td></tr>
<tr><td colspan="2">
</td><td colspan="2">
</td><td colspan="2">
</td><td colspan="2">
</td></tr>
<tr><td>5</td><td>IS</td><td>6</td><td>GND</td><td>7</td><td>OUT</td><td>8</td><td>VCC</td></tr>
<tr><td colspan="2">
</td><td colspan="2"></td><td colspan="2">
</td><td colspan="2"></td></tr>
</table>

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

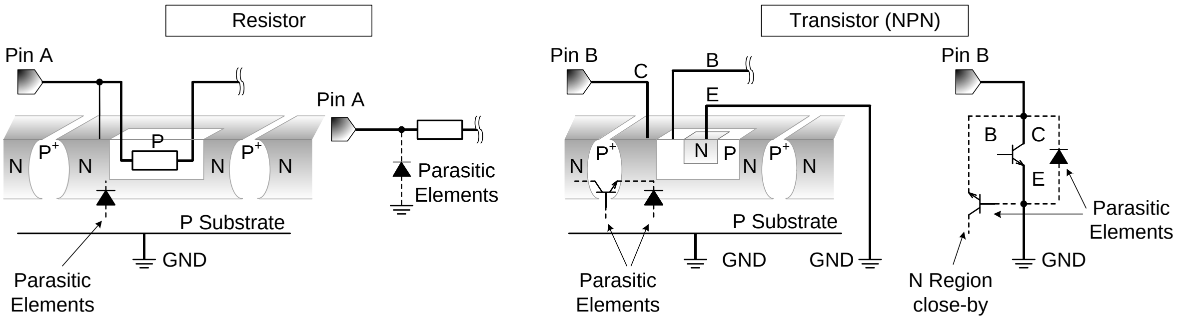


Figure 26. Example of monolithic IC structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

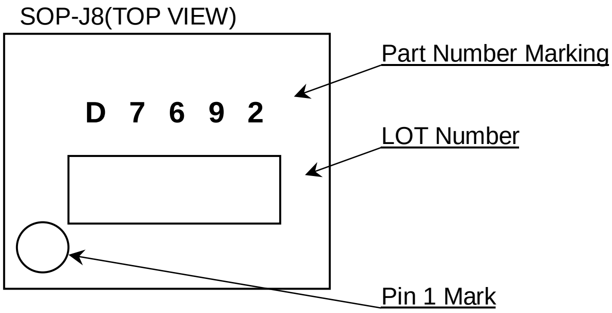
Ordering Information

B D 7 6 9 2 F J - E2

Package
FJ: SOP-J8

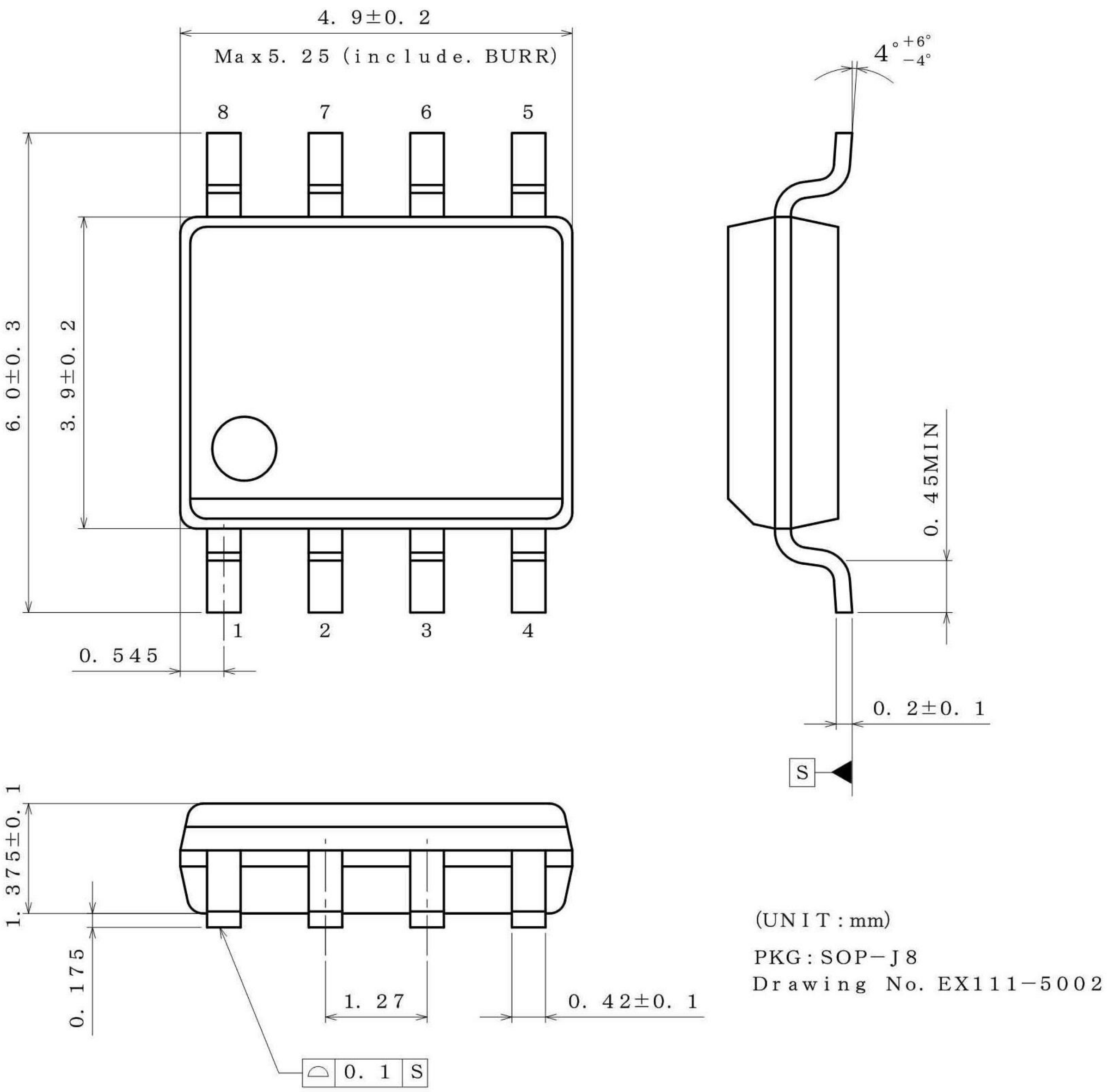
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagrams



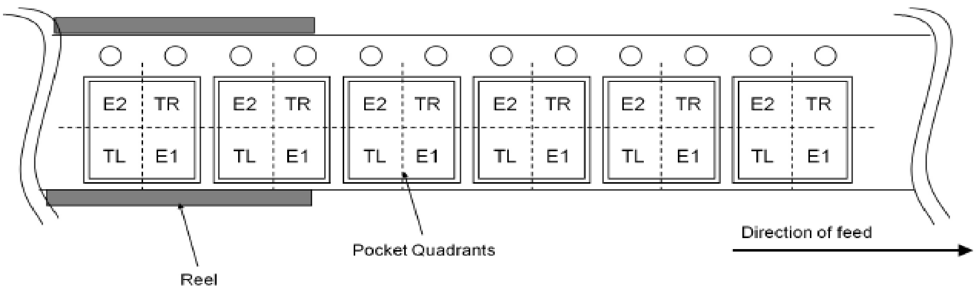
Physical Dimension and Packing Information

Package Name	SOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
04.Oct.2018	001	Release

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precaution for Storage / Transportation

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
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2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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