MULTI-CHIP PACKAGE (MCP) MEMORY

1.8V 2G-BIT (16M-WORD x 8-BIT)
SLC NAND FLASH MEMORY
&
1.8V 1G-BIT (256K- WORD x 8 BANK x 32-BIT)
LOW POWER DDR2 (LPDDR2) SDRAM

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1 GENERAL DESCRIPTION

The W71NW series is a Multi-Chip Package (MCP) memory product family that consists of a 1.8V NAND Flash Memory device and a 1.8V Low Power SDRAM device in one convenient Thin VFBGA package.

W71NW20GF3FW consists of:

- W29N02GZ - 1.8V 2G-Bit x8-BIT NAND Flash Memory
- W97AH2KK - 1.8V 1G-Bit x32-BIT Low Power DDR2 SDRAM
- 162 Ball VFBGA - Dimension 8x10.5x1.0mm, ball pitch 0.50-mm, ball diameter 0.30mm

2 FEATURES

W29N02GZ NAND Flash Memory

- **Basic Features**
  - – Density : 2Gbit (Single chip solution)
  - – Vcc : 1.7V to 1.95V
  - – Bus width : x8
  - – Operating temperature
    - ▪ Industrial: -40°C to 85°C
- **Single-Level Cell (SLC) technology.**
- **Organization**
  - – Density: 2G-bit/256M-byte
  - – Page size
    - ▪ 2,112 bytes (2048 + 64 bytes)
  - – Block size
    - ▪ 64 pages (128K + 4K bytes)
- **Highest Performance**
  - – Read performance (Max.)
    - ▪ Random read: 25us
    - ▪ Sequential read cycle: 25ns
  - – Write Erase performance
    - ▪ Page program time: 250us(typ.)
    - ▪ Block erase time: 2ms(typ.)
  - – Endurance 100,000 Erase/Program Cycles(2)
  - – 10-years data retention
- **Command set**
  - – Standard NAND command set
  - – Additional command support
    - ▪ Copy Back
    - ▪ Two-plane operation
  - – Contact Winbond for OTP feature
  - – Contact Winbond for block Lock feature
- **Lowest power consumption**
  - – Read: 25mA(typ.3V),T.B.D(typ.1.8V)
  - – Program/Erase: 10mA(typ.1.8V)
  - – CMOS standby: 10uA(typ.)

W97AH2KK Low Power DDR2 SDRAM

- **VDD1 = 1.7~1.95V**
- **VDD2/VDDCA/VDDQ = 1.14V ~ 1.30V**
- **Data width: x32**
- **Clock rate: up to 533MHz**
- **Four-bit prefetch DDR architecture**
- **Eight internal banks for concurrent operation**
- **Programmable READ and WRITE latencies (RL/WL)**
- **Programmable burst lengths: 4, 8, or 16**
- **Per Bank Refresh**
- **Partial Array Self-Refresh(PASR)**
- **Deep Power Down Mode (DPD Mode)**
- **Programmable output buffer driver strength**
- **Data mask (DM) for write data**
- **Clock Stop capability during idle periods**
- **Double data rate for data output**
- **Differential clock inputs**
- **Bidirectional differential data strobe**
- **Interface: HSUL_12**
- **JEDEC LPDDR2-S4B compliance**
- **Operating Temperature Range**

  -40 ~ 85 °C

Note:

1. **Endurance specification is based on 1bit/528 byte ECC (Error Correcting Code).**

3 BALL CONFIGURATION

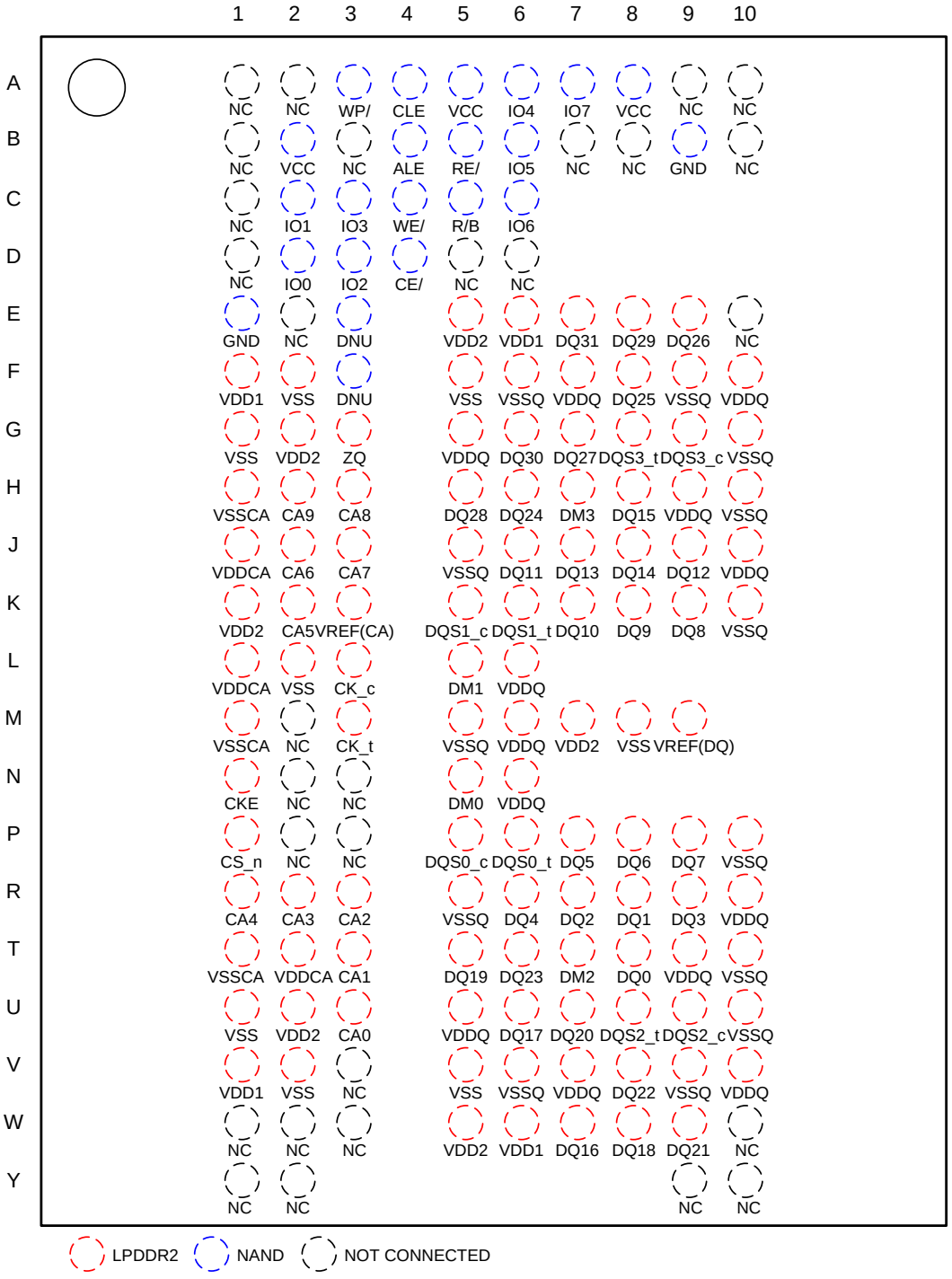


Figure 3-1 W71NW20GF3FW, 162 Ball VFBGA Package (Top View, balls facing down)

3.1 162-Ball Description for W29N02GZ NAND Flash Memory

Ball NO.	BALL NAME	I/O	FUNCTION
A3	WP#	I	Write Protect
C4	WE#	I	Write Enable
B4	ALE	I	Address Latch Enable
A4	CLE	I	Command Latch Enable
D4	CE#	I	Chip Enable
B5	RE#	I	Read Enable
C5	R/B#	I	Ready/#Busy
D2	IO0	I/O	Data Input Output 0
C2	IO1	I/O	Data Input Output 1
D3	IO2	I/O	Data Input Output 2
C3	IO3	I/O	Data Input Output 3
A6	IO4	I/O	Data Input Output 4
B6	IO5	I/O	Data Input Output 5
C6	IO6	I/O	Data Input Output 6
A7	IO7	I/O	Data Input Output 7
B2,A5,A8	VCC		Power Supply NAND
E1,B9	VSSn		Ground NAND
E3,F3	DNU		Do Not Use
Multiple	NC		No Connection

Table 3-1 W29N02GZ VFBGA-162 Ball Description

3.2 162-Ball Description for W97AH2KK Low Power DDR2 SDRAM

BALL NO.	BALL NAME	I/O	FUNCTION
P1	CS_n	I	Chip Select
N1	CKE	I	Clock Enable
L3	CLK_c	I	CK_t and CK_c are differential clock inputs
M3	CLK_t	I	CK_t and CK_c are differential clock inputs
U3	CA0	I	DDR Command/Address Input 9
T3	CA1	I	DDR Command/Address Input
R3	CA2	I	DDR Command/Address Input
R2	CA3	I	DDR Command/Address Input
R1	CA4	I	DDR Command/Address Input
K2	CA5	I	DDR Command/Address Input

BALL NO.	BALL NAME	I/O	FUNCTION
J2	CA6	I	DDR Command/Address Input
J3	CA7	I	DDR Command/Address Input
H3	CA8	I	DDR Command/Address Input
H2	CA9	I	DDR Command/Address Input
N5	DM0	I	Input Data Mask
L5	DM1	I	Input Data Mask
T7	DM2	I	Input Data Mask
H7	DM3	I	Input Data Mask
P5	DQS0_c	I/O	Data Strobe (Bi-directional, Differential)
P6	DQS0_t	I/O	Data Strobe (Bi-directional, Differential)
K5	DQS1_c	I/O	Data Strobe (Bi-directional, Differential)
K6	DQS1_t	I/O	Data Strobe (Bi-directional, Differential)
U9	DQS2_c	I/O	Data Strobe (Bi-directional, Differential)
U8	DQS2_t	I/O	Data Strobe (Bi-directional, Differential)
G9	DQS3_c	I/O	Data Strobe (Bi-directional, Differential)
G8	DQS3_t	I/O	Data Strobe (Bi-directional, Differential)
T8	DQ0	I/O	Data Inputs/Output
R8	DQ1	I/O	Data Inputs/Output
R7	DQ2	I/O	Data Inputs/Output
R9	DQ3	I/O	Data Inputs/Output
R6	DQ4	I/O	Data Inputs/Output
P7	DQ5	I/O	Data Inputs/Output
P8	DQ6	I/O	Data Inputs/Output
P9	DQ7	I/O	Data Inputs/Output
K9	DQ8	I/O	Data Inputs/Output
K8	DQ9	I/O	Data Inputs/Output
K7	DQ10	I/O	Data Inputs/Output
J6	DQ11	I/O	Data Inputs/Output
J9	DQ12	I/O	Data Inputs/Output
J7	DQ13	I/O	Data Inputs/Output
J8	DQ14	I/O	Data Inputs/Output
H8	DQ15	I/O	Data Inputs/Output
W7	DQ16	I/O	Data Inputs/Output
U6	DQ17	I/O	Data Inputs/Output
W8	DQ18	I/O	Data Inputs/Output
T5	DQ19	I/O	Data Inputs/Output

BALL NO.	BALL NAME	I/O	FUNCTION
U7	DQ20	I/O	Data Inputs/Output
W9	DQ21	I/O	Data Inputs/Output
V8	DQ22	I/O	Data Inputs/Output
T6	DQ23	I/O	Data Inputs/Output
H6	DQ24	I/O	Data Inputs/Output
F8	DQ25	I/O	Data Inputs/Output
E9	DQ26	I/O	Data Inputs/Output
G7	DQ27	I/O	Data Inputs/Output
H5	DQ28	I/O	Data Inputs/Output
E8	DQ29	I/O	Data Inputs/Output
G6	DQ30	I/O	Data Inputs/Output
E7	DQ31	I/O	Data Inputs/Output
G3	ZQ	I/O	Reference Pin for Output Drive Strength Calibration
F1,V1,E6,W6	VDD1		Core Power Supply 1
K1,G2,U2,E5,W5,M7	VDD2		Core Power Supply 2
G5,U5,L6,M6,N6,F7, V7,H9,T9,F10,J10,R10,V10	VDDQ		I/O Power Supply
J1,L1,T2	VDDCA		Input Receiver Power Supply
G1,U1,L2,V2,F5,F2,V5,M8	VSS		Ground
J5,M5,R5,F6,V6,F9,V9,G10,H10,K10,P10, T10,U10	VSSQ		I/O Ground
H1,M1,T1	VSSCA		Ground for CA Input Receivers
K3	VREF(CA)		Reference Voltage for CA Command and Control Input Receiver
M9	VREF(DQ)		Reference Voltage for DQ Input Receiver

Table 3-2 W97AH2KK VFBGA-162 Ball Description

4 Block Diagram

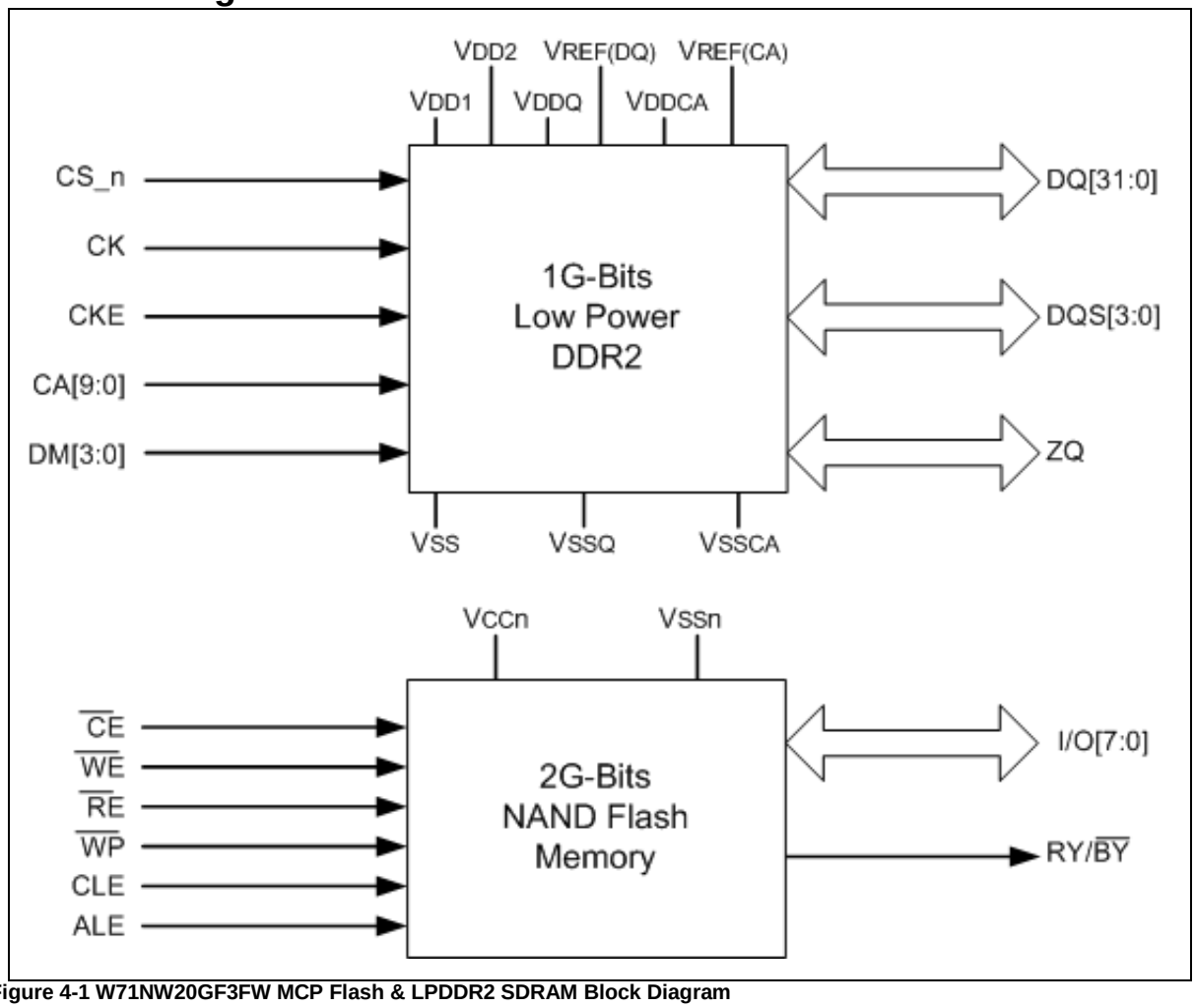
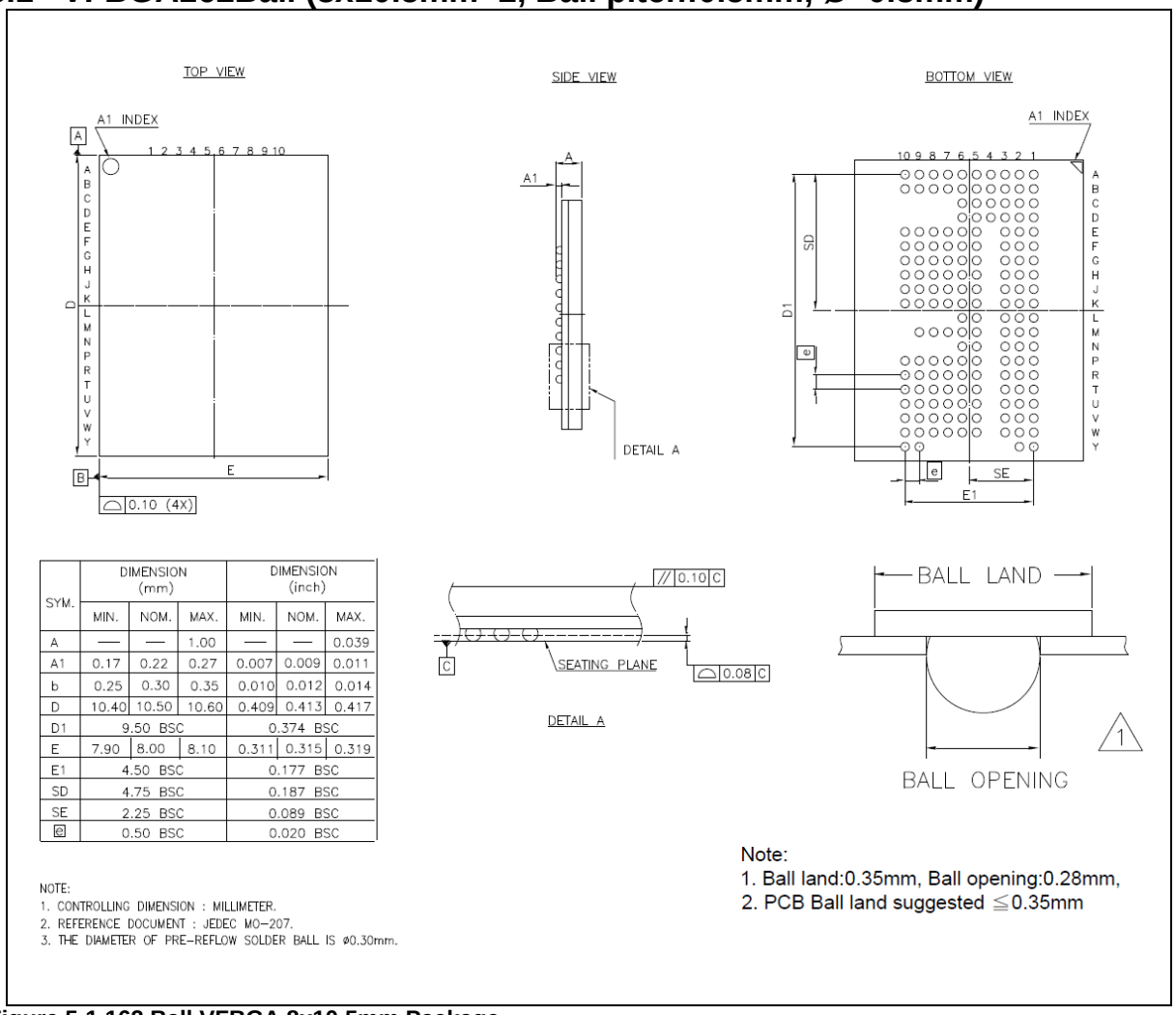


Figure 4-1 W71NW20GF3FW MCP Flash & LPDDR2 SDRAM Block Diagram

5 Package Specification

5.1 VFBGA162Ball (8x10.5mm^2, Ball pitch:0.5mm, Ø=0.3mm)



SYM.	DIMENSION (mm)			DIMENSION (inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.00	—	—	0.039
A1	0.17	0.22	0.27	0.007	0.009	0.011
b	0.25	0.30	0.35	0.010	0.012	0.014
D	10.40	10.50	10.60	0.409	0.413	0.417
D1	9.50 BSC			0.374 BSC		
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	4.50 BSC			0.177 BSC		
SD	4.75 BSC			0.187 BSC		
SE	2.25 BSC			0.089 BSC		
e	0.50 BSC			0.020 BSC		

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.
3. THE DIAMETER OF PRE-REFLOW SOLDER BALL IS ø0.30mm.

Note:
1. Ball land:0.35mm, Ball opening:0.28mm,
2. PCB Ball land suggested ≦0.35mm

Figure 5-1 162 Ball VFBGA 8x10.5mm Package

6 MCP ORDERING INFORMATION

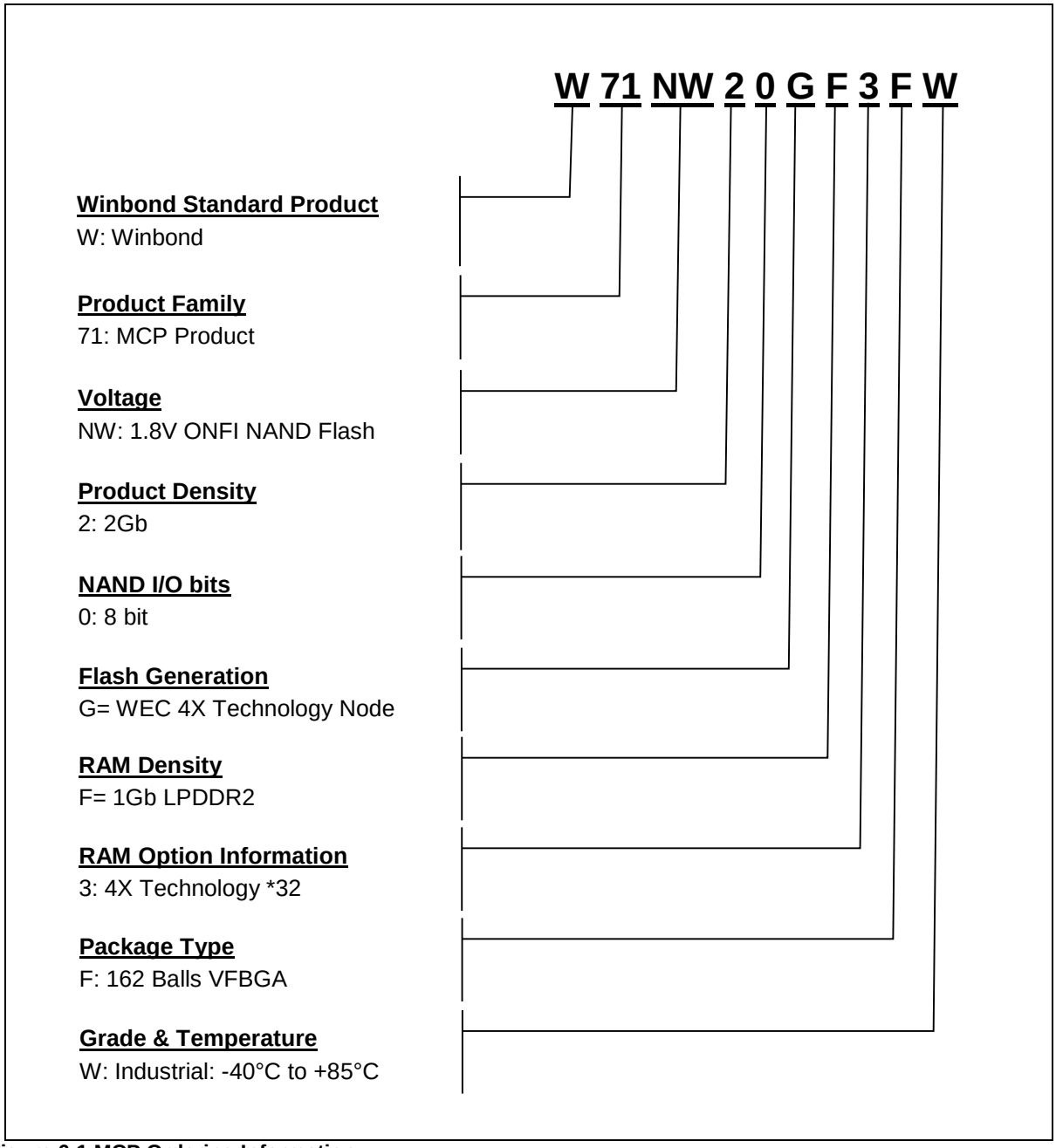


Figure 6-1 MCP Ordering Information

7 Revision History

VERSION	DATE	PAGE	DESCRIPTION
A	07/15/2014		New Create Preliminary
B	11/26/2014	3	Corrected W29N02GZ BUS Width to x8
C	06/09/2015	3 10 N/A	Added new W29N02GZ description Temperature Grade Correction Added updated W29N02GZ Datasheet

Table 7-1 Revision History

Preliminary Designation

The "Preliminary" designation on a *Winbond* datasheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *Winbond* or an authorized sales representative should be consulted for current information before using this product.

Trademarks

Winbond and *SpiFlash* are trademarks of *Winbond Electronics Corporation.*
All other marks are the property of their respective owner.

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, *Winbond* products are not intended for applications wherein failure of *Winbond* products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify *Winbond* for any damages resulting from such improper use or sales.

W29N02GW/Z
2G-BIT 1.8V
NAND FLASH MEMORY

winbond

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1. GENERAL DESCRIPTION

The W29N02GW/Z (2G-bit) NAND Flash memory provides a storage solution for embedded systems with limited space, pins and power. It is ideal for code shadowing to RAM, solid state applications and storing media data such as, voice, video, text and photos. The device operates on a single 1.7V to 1.95V power supply with active current consumption as low as 13mA at 1.8V and 10uA for CMOS standby current.

The memory array totals 276,824,064bytes, and organized into 2,048 erasable blocks of 135,168 bytes (135,168 words). Each block consists of 64 programmable pages of 2,112-bytes (1056 words) each. Each page consists of 2,048-bytes (1024 words) for the main data storage area and 64-bytes (32words) for the spare data area (The spare area is typically used for error management functions).

The W29N02GW/Z supports the standard NAND flash memory interface using the multiplexed 8-bit (16-bit) bus to transfer data, addresses, and command instructions. The five control signals, CLE, ALE, #CE, #RE and #WE handle the bus interface protocol. Also, the device has two other signal pins, the #WP (Write Protect) and the RY/#BY (Ready/Busy) for monitoring the device status.

2. FEATURES

- **Basic Features**
  - – Density : 2Gbit (Single chip solution)
  - – Vcc : 1.7V to 1.95V
  - – Bus width : x8 x16
  - – Operating temperature
    - ▪ Industrial: -40°C to 85°C
- **Single-Level Cell (SLC) technology.**
- **Organization**
  - – Density: 2G-bit/256M-byte
  - – Page size
    - ▪ 2,112 bytes (2048 + 64 bytes)
    - ▪ 1,056 words (1024 + 32 words)
  - – Block size
    - ▪ 64 pages (128K + 4K bytes)
    - ▪ 64 pages (64K + 2K words)
- **Highest Performance**
  - – Read performance (Max.)
    - ▪ Random read: 25us
    - ▪ Sequential read cycle: 25ns
  - – Write Erase performance
    - ▪ Page program time: 250us(typ.)
    - ▪ Block erase time: 2ms(typ.)
  - – Endurance 100,000 Erase/Program Cycles(2)
  - – 10-years data retention
- **Command set**
  - – Standard NAND command set
  - – Additional command support
    - ▪ Copy Back
    - ▪ Two-plane operation
  - – Contact Winbond for OTP feature
  - – Contact Winbond for block Lock feature
- **Lowest power consumption**
  - – Read: 25mA(typ.3V),T.B.D(typ.1.8V)
  - – Program/Erase: 10mA(typ.1.8V)
  - – CMOS standby: 10uA(typ.)
- **Space Efficient Packaging**
  - – Contact Winbond for stacked packages/KGD

Note:

1. **Endurance specification is based on 1bit/528 byte ECC (Error Correcting Code).**

3. PACKAGE TYPES AND PIN CONFIGURATIONS

3.1 Pin Descriptions

PIN NAME	I/O	FUNCTION
#WP	I	Write Protect
ALE	I	Address Latch Enable
#CE	I	Chip Enable
#WE	I	Write Enable
RY/#BY	O	Ready/Busy
#RE	I	Read Enable
CLE	I	Command Latch Enable
I/O[0-7] I/O[0-15]	I/O	Data Input/Output (x8,x16)
Vcc	Supply	Power supply
Vss	Supply	Ground
DNU	-	Do Not Use.
N.C	-	No Connect

Table 3-1 Pin Descriptions

Note:

1. **Connect all Vcc and Vss pins to power supply or ground. Do not leave Vcc or Vss disconnected.**

4. PIN DESCRITPIONS

4.1 Chip Enable (#CE)

#CE pin enables and disables device operation. When #CE is high the device is disabled and the I/O pins are set to high impedance and enters into standby mode if not busy. When #CE is set low the device will be enabled, power consumption will increase to active levels and the device is ready for Read and Write operations.

4.2 Write Enable (#WE)

#WE pin enables the device to control write operations to input pins of the device. Such as, command instructions, addresses and data that are latched on the rising edge of #WE.

4.3 Read Enable (#RE)

#RE pin controls serial data output from the pre-loaded Data Register. Valid data is present on the I/O bus after the tREA period from the falling edge of #RE. Column addresses are incremented for each #RE pulse.

4.4 Address Latch Enable (ALE)

ALE pin controls address input to the address register of the device. When ALE is active high, addresses are latched via the I/O pins on the rising edge of #WE.

4.5 Command Latch Enable (CLE)

CLE pin controls command input to the command register of the device. When CLE is active high, commands are latched into the command register via I/O pins on the rising edge of #WE.

4.6 Write Protect (#WP)

#WP pin can be used to prevent the inadvertent program/erase to the device. When #WP pin is active low, all program/erase operations are disabled.

4.7 Ready/Busy (RY/#BY)

RY/#BY pin indicates the device status. When RY/#BY output is low, it indicates that the device is processing either a program, erase or read operations. When it returns to high, those operations have completed. RY/#BY pin is an open drain.

4.8 Input and Output (I/Ox)

I/Ox bi-directional pins are used for the following; command, address and data operations.

5. BLOCK DIAGRAM

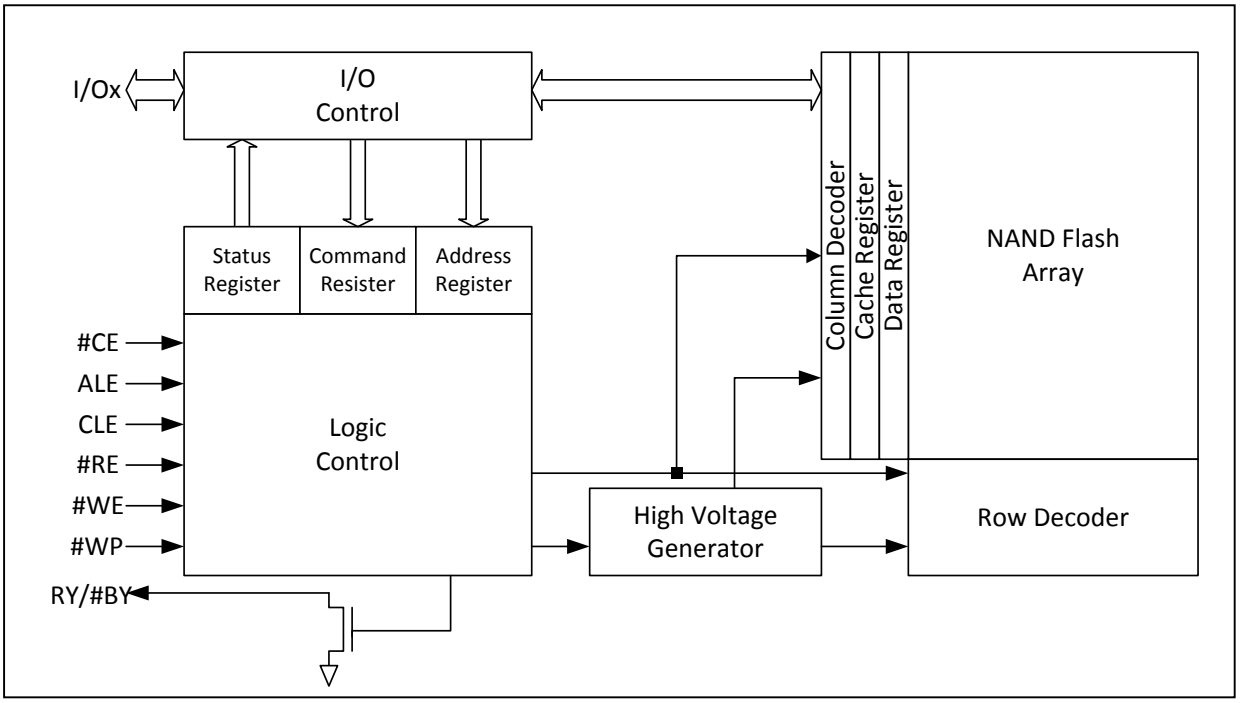

Figure 5-1 NAND Flash Memory Block Diagram

6. MEMORY ARRAY ORGANIZATION

6.1 Array Organization (x8)

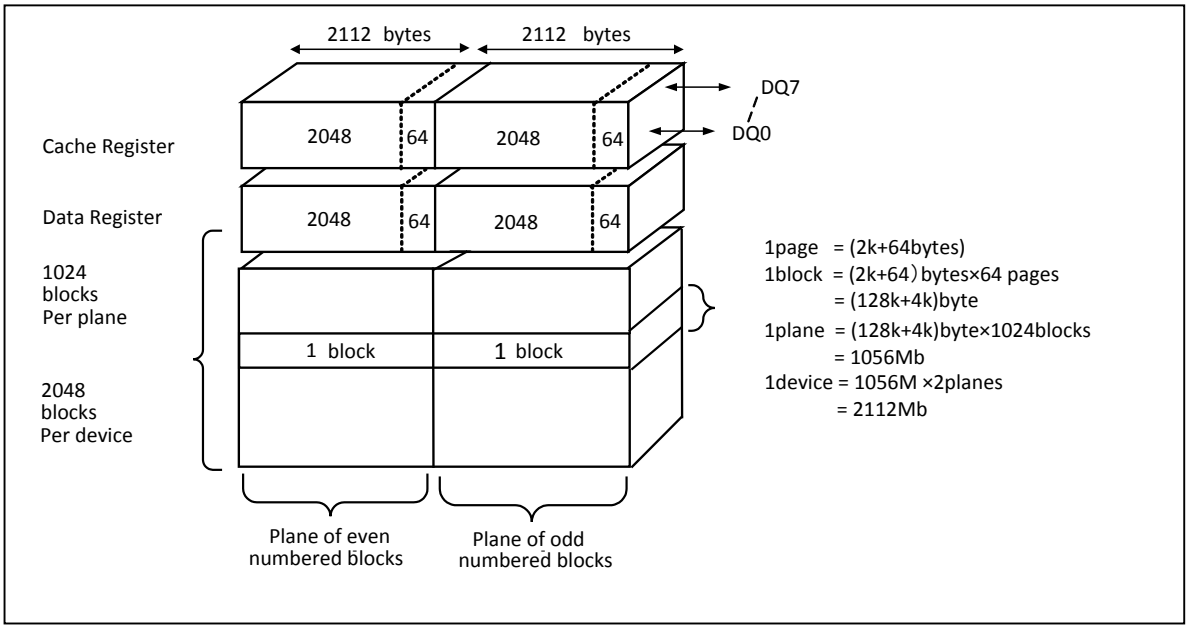

Figure 6-1 Array Organization

	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st cycle	A7	A6	A5	A4	A3	A2	A1	A0
2nd cycle	L	L	L	L	A11	A10	A9	A8
3rd cycle	A19	A18	A17	A16	A15	A14	A13	A12
4th cycle	A27	A26	A25	A24	A23	A22	A21	A20
5th cycle	L	L	L	L	L	L	L	A28

Table 6-1 Addressing

Notes:

1. **"L" indicates a low condition, which must be held during the address cycle to insure correct processing.**
2. **A0 to A11 during the 1st and 2nd cycles are column addresses. A12 to A28 during the 3rd, 4th and 5th cycles are row addresses.**
3. **A18 is plane address**
4. **The device ignores any additional address inputs that exceed the device's requirement.**

6.2 Array Organization (x16)

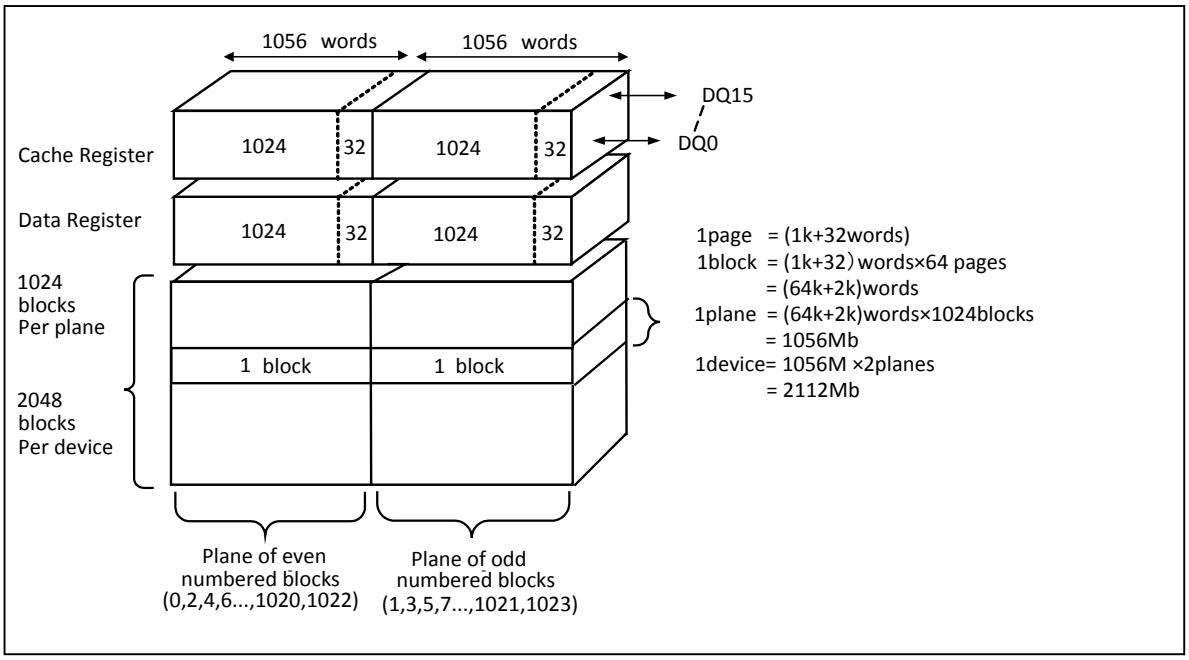

Figure 6-2 Array Organization

	I/O[15:8]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st cycle	L	A7	A6	A5	A4	A3	A2	A1	A0
2ndcycle	L	L	L	L	L	L	A10	A9	A8
3rd cycle	L	A18	A17	A16	A15	A14	A13	A12	A11
4th cycle	L	A26	A25	A24	A23	A22	A21	A20	A19
5th cycle	L	L	L	L	L	L	L	L	A27

Table 6-2 Addressing

Notes:

1. **"L" indicates a low condition, which must be held during the address cycle to insure correct processing.**
2. **A0 to A10 during the 1st and 2nd cycles are column addresses. A11 to A27 during the 3rd, 4th and 5th cycles are row addresses.**
3. **A17 is plane address**
4. **The device ignores any additional address inputs that exceed the device's requirement.**

7. MODE SELECTION TABLE

MODE		CLE	ALE	#CE	#WE	#RE	#WP
Read mode	Command input	H	L	L		H	X
	Address input	L	H	L		H	X
Program Erase mode	Command input	H	L	L		H	H
	Address input	L	H	L		H	H
Data input		L	L	L		H	H
Sequential Read and Data output		L	L	L	H		X
During read (busy)		X	X	X	X	H	X
During program (busy)		X	X	X	X	X	H
During erase (busy)		X	X	X	X	X	H
Write protect		X	X	X	X	X	L
Standby		X	X	H	X	X	0V/Vcc

Table 7-1 Mode Selection

Notes:

1. **"H" indicates a HIGH input level, "L" indicates a LOW input level, and "X" indicates a Don't Care Level.**
2. **#WP should be biased to CMOS HIGH or LOW for standby.**

8. COMMAND TABLE

COMMAND	1ST CYCLE	2ND CYCLE	3rd CYCLE	4th CYCLE	Acceptable during busy
PAGE READ	00h	30h			
READ for COPY BACK	00h	35h			
READ ID	90h				
READ STATUS	70h				Yes
RESET	FFh				Yes
PAGE PROGRAM	80h	10h			
PROGRAM for COPY BACK	85h	10h			
BLOCK ERASE	60h	D0h			
RANDOM DATA INPUT*1	85h				
RANDOM DATA OUTPUT*1	05h	E0h			
READ PARAMETER PAGE	ECh				
READ UNIQUE ID	EDh				
GET FEATURES	EEh				
SET FEATURES	EFh				
READ STATUS ENHANCED	78h				Yes
TWO PLANE READ PAGE	00h	00h	30h		
TWO PLANE READ FOR COPY BACK	00h	00h	35h		
TWO PLANE RANDOM DATA READ	06h	E0h			
TWO PLANE PROGRAM(TRADITIONAL)	80h	11h	81h	10h	
TWO PLANE PROGRAM(ONFI)	80h	11h	80h	10h	
TWO PLANE PROGRAM FOR COPY BACK(TRADITIONAL)	85h	11h	81h	10h	
TWO PLANE PROGRAM FOR COPY BACK(ONFI)	85h	11h	85h	10h	
TWO PLANE BLOCK ERASE(TRADITIONAL)	60h	60h	D0h		
TWO PLANE BLOCK ERASE(ONFI)	60h	D1h	60h	D0h	

Table 8-1 Command Table

Notes:

1. **RANDOM DATA INPUT and RANDOM DATA OUTPUT command is only to be used within a page.**
2. **Any commands that are not in the above table are considered as undefined and are prohibited as inputs.**
3. **Do not cross plane address boundaries when using Copy Back Read and Program for copy back.**

9. DEVICE OPERATIONS

9.1 READ operation

9.1.1 PAGE READ (00h-30h)

When the device powers on, 00h command is latched to command register. Therefore, system only issues five address cycles and 30h command for initial read from the device. This operation can also be entered by writing 00h command to the command register, and then write five address cycles, followed by writing 30h command. After writing 30h command, the data is transferred from NAND array to Data Register during tR. Data transfer progress can be done by monitoring the status of the RY/#BY signal output. RY/#BY signal will be LOW during data transfer. Also, there is an alternate method by using the READ STATUS (70h) command. If the READ STATUS command is issued during read operation, the Read (00h) command must be re-issued to read out the data from Data Register. When the data transfer is complete, RY/#BY signal goes HIGH, and the data can be read from Data Register by toggling #RE. Read is sequential from initial column address to the end of the page. (See Figure 9-1)

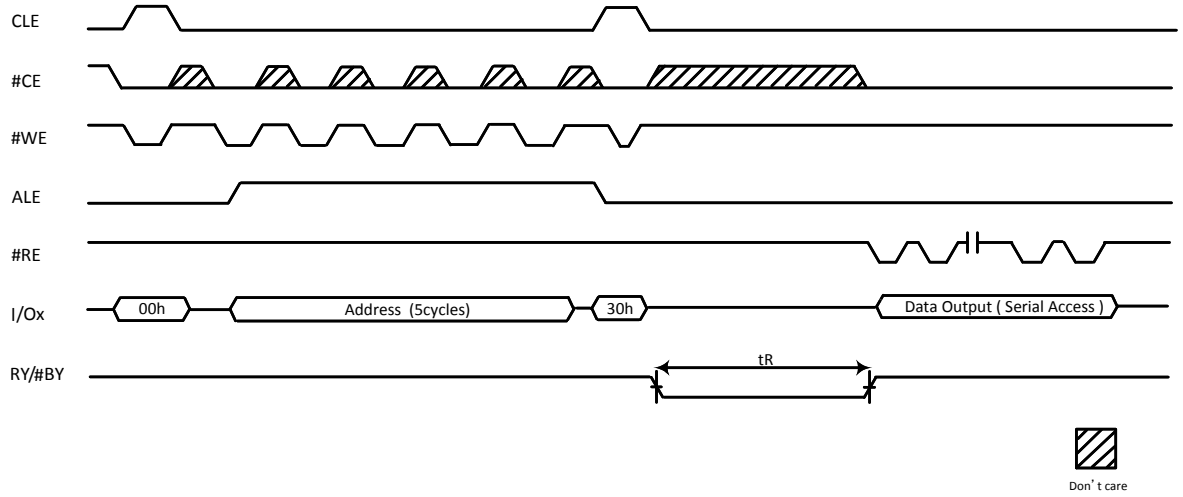

Figure 9-1 Page Read Operations

9.1.2 TWO PLANE READ (00h-00h-30h)

TWO PLANE READ (00h-00h-30h) transfers two pages data from the NAND array to the data registers. Each page address have to be indicated different plane address.

To set the TWO PLANE READ mode, write the 00h command to the command register, and then write five address cycles for plane 0. Secondly, write the 00h command to the command register, and five address cycles for plane 1. Finally, the 30h command is issued. The first-plane and second-plane addresses must be identical for all of issued address except plane address.

After the 30h command is written, page data is transferred from both planes to their respective data registers in tR. RY/#BY goes LOW While these are transfered,. When the transfers are complete, RY/#BY goes HIGH. To read out the data, at first, system writes TWO PLANE RAMDOM DATA READ (06h-E0h) command to select a plane, next, repeatedly pulse #RE to read out the data from selected plane. To change the plane address, issues TWO PLANE RANDOM DATA READ (06h-E0h)

command to select the another plane address, then repeatedly pulse #RE to read out the data from the selected plane data register.

Alternatively, data transfers can be monitored by the READ STATUS (70h). When the transfers are complete, status register bit 6 is set to 1. To read data from the first of the two planes even when READ STATUS ENHANCED (78h) command is used, the system must issue the TWO PLANE RANDOM DATA READ (06h-E0h) command at first and pulse #RE repeatedly.

Write a TWO PLANE RANDOM DATA READ (06h-E0h) command to select the other plane ,after the data cycle is complete. pulse #RE repeatedly to output the data beginning at the specified column address. During TWO PLANE READ operation,the READ STATUS ENHANCED (78h) command is prohibited .

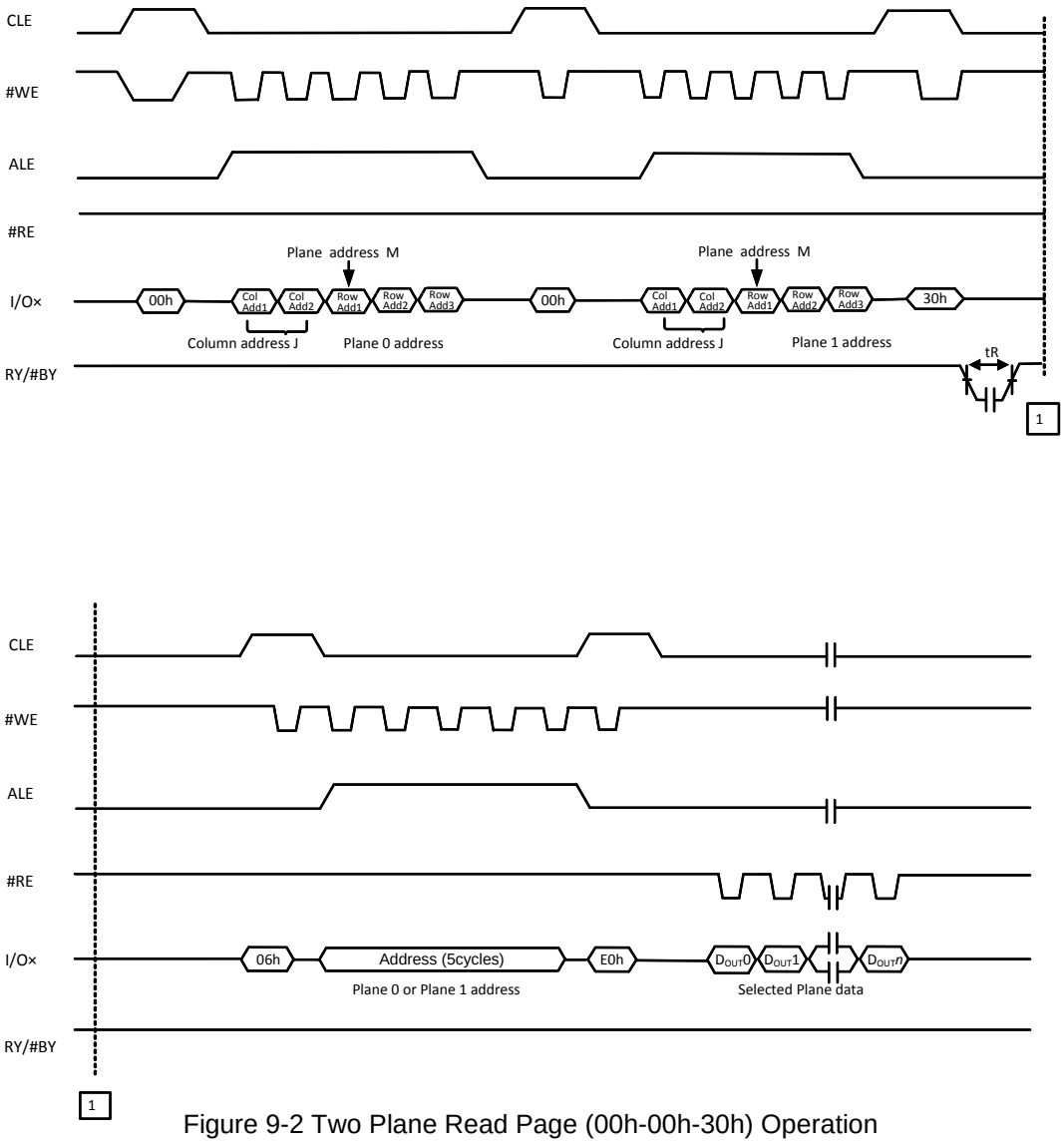

Figure 9-2 Two Plane Read Page (00h-00h-30h) Operation

9.1.3 RANDOM DATA OUTPUT (05h-E0h)

The RANDOM DATA OUTPUT allows the selection of random column addresses to read out data from a single or multiple of addresses. The use of the RANDOM DATA OUTPUT command is available after the PAGE READ (00h-30h) sequence by writing the 05h command following by the two cycle column address and then the E0h command. Toggling #RE will output data sequentially. The RANDOM DATA OUTPUT command can be issued multiple times, but limited to the current loaded page.

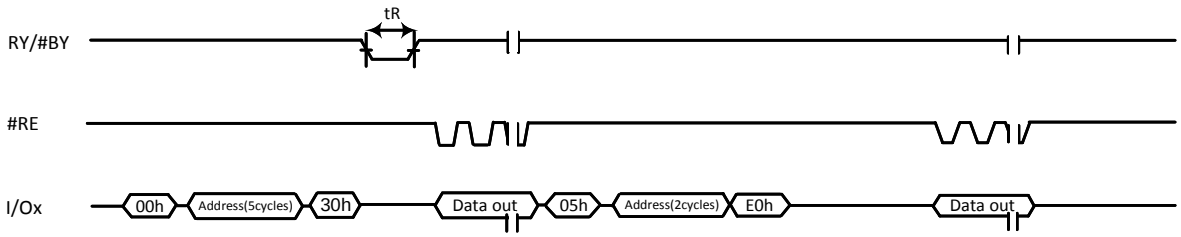

Figure 9-3 Random Data Output

9.1.3.1. TWO PLANE RANDOM DATA OUTPUT (06h-E0h)

TWO PLANE RANDOM DATA READ (06h-E0h) command can indicate to specified plane and column address on data register . This command is accepted by a device when it is ready.

Issuing 06h to the command register, two column address cycles, three row address cycles, E0h are followed, this enables data output mode on the address device's data register at the specified column address. After the E0h command , the host have to wait at least tWHR before requesting data output. The selected device is in data output mode until another valid command is issued.

The TWO PLANE RANDOM DATA READ (06h-E0h) command is used to select the data register to be enabled for data output. When the data output is complete on the selected plane, the command can be issued again to start data output on another plane.

If there is a need to update the column address without selecting a new data register, the RANDOM DATA READ (05h-E0h) command can be used instead.

Figure 9-4 Two Plane Random Data Read (06h-E0h) Operation

9.1.4 READ ID (90h)

READ ID command is comprised of two modes determined by the input address, device (00h) or ONFI (20h) identification information. To enter the READ ID mode, write 90h to the Command Register followed by a 00h address cycle, then toggle #RE for 5 single byte cycles, W29N02GW/Z. The pre-programmed code includes the Manufacturer ID, Device ID, and Product-Specific Information (see Table 9.1). If the READ ID command is followed by 20h address, the output code includes 4 single byte cycles of ONFI identifying information (See Table 9.2). The device remains in the READ ID Mode until the next valid command is issued.

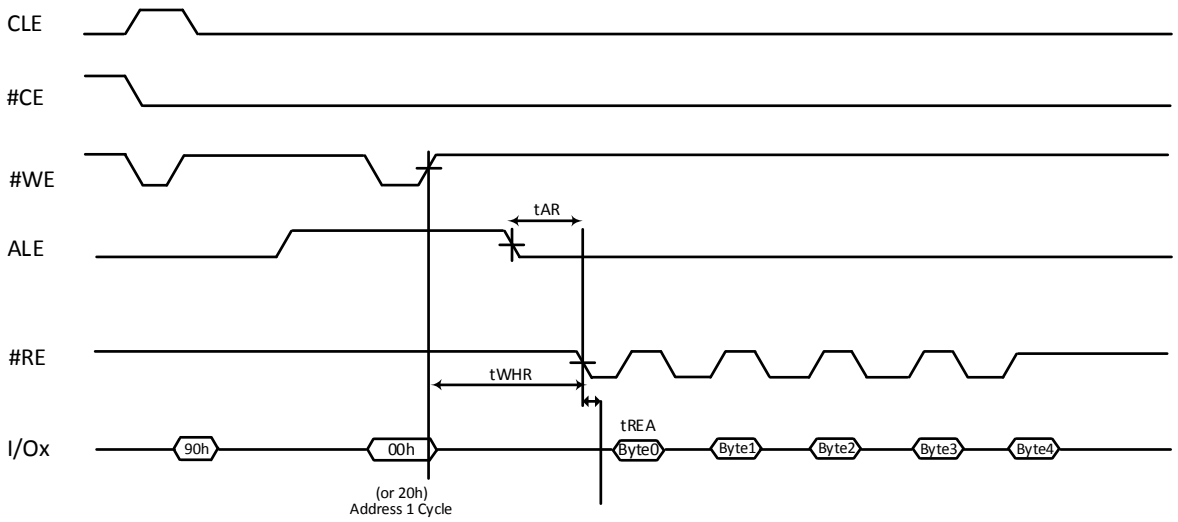

Figure 9-5 Read ID

# of Byte/Cycles	1st Byte/Cycle	2nd Byte/Cycle	3rd Byte/Cycle	4th Byte/Cycle	5th Byte/Cycle
W29N02GZ	EFh	AAh	90h	15h	04h
W29N02GW	EFh	BAh	90h	55h	04h
Description	MFR ID	Device ID	Cache Programming not Supported	Page Size:2KB Spare Area Size:64b BLK Size w/o Spare:128KB Organized:x8 or x16 Serial Access:25ns	

x16 device : the ID is outputted at word units, and defined lower-byte (IO0-7). ID table shows only lower-byte ID.

Table 9-1 Device ID and configuration codes for Address 00h

# of Byte/Cycles	1st Byte/Cycle	2nd Byte/Cycle	3rd Byte/Cycle	4th Byte/Cycle
Code	4Fh	4Eh	46h	49h

Table 9-2 ONFI identifying codes for Address 20h

9.1.5 READ PARAMETER PAGE (ECh)

READ PARAMETER PAGE can read out the device's parameter data structure, such as, manufacturer information, device organization, timing parameters, key features, and other pertinent device parameters. The data structure is stored with at least three copies in the device's parameter page. Figure 9-9 shows the READ PARAMETER PAGE timing. The RANDOM DATA OUTPUT (05h-E0h) command is supported during data output.

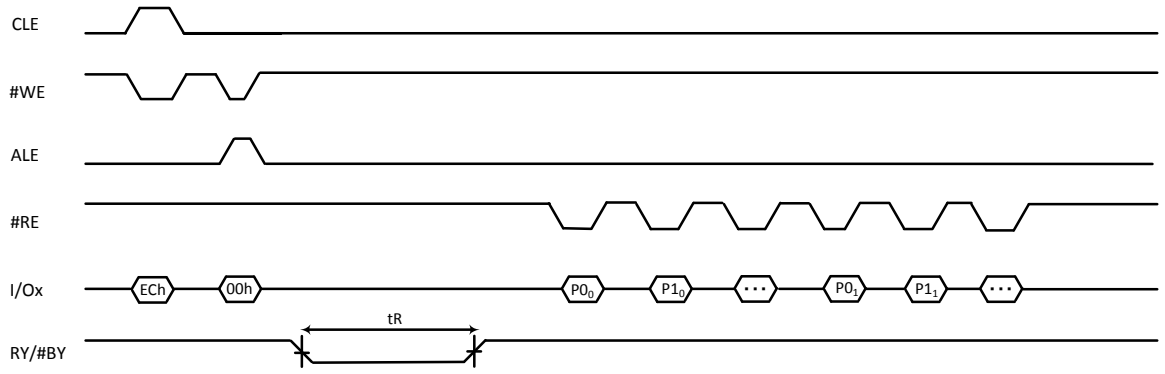

Figure 9-6 Read Parameter Page

Byte	Description		Value
0-3	Parameter page signature		4Fh, 4Eh, 46h, 49h
4-5	Revision number		02h, 00h
6-7	Features supported	W29N02GZ	18h,00h
		W29N02GW	19h,00h
8-9	Optional commands supported		3Fh,00h
10-31	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
32-43	Device manufacturer		57h, 49h, 4Eh, 42h, 4Fh, 4Eh, 44h, 20h, 20h, 20h, 20h, 20h
44-63	Device model	W29N02GZ	57h,32h,39h,4Eh,30h,32h,47h,5Ah,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h
		W29N02GW	57h,32h,39h,4Eh,30h,32h,47h,57h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h,20h
64	Manufacturer ID		EFh
65-66	Date code		00h, 00h
67-79	Reserved		00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
80-83	# of data bytes per page		00h, 08h, 00h, 00h

Byte	Description	Value
84-85	# of spare bytes per page	40h, 00h
86-89	# of data bytes per partial page	00h, 02h, 00h, 00h
90-91	# of spare bytes per partial page	10h, 00h
92-95	# of pages per block	40h, 00h, 00h, 00h
96-99	# of blocks per unit	00h, 08h, 00h, 00h
100	# of logical units	01h
101	# of address cycles	23h
102	# of bits per cell	01h
103-104	Bad blocks maximum per unit	28h, 00h
105-106	Block endurance	01h, 05h
107	Guaranteed valid blocks at beginning of target	01h
108-109	Block endurance for guaranteed valid blocks	00h, 00h
110	# of programs per page	04h
111	Partial programming attributes	00h
112	# of ECC bits	01h
113	# of interleaved address bits	01h
114	Interleaved operation attributes	0Ch
115-127	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
128	I/O pin capacitance	0Ah
129-130	Timing mode support	1Fh, 00h
131-132	Program cache timing	00h, 00h
133-134	Maximum page program time	BCh, 02h
135-136	Maximum block erase time	10h, 27h
137-138	Maximum random read time	19h, 00h
139-140	tCCS minimum	46h, 00h
141-163	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
164-165	Vendor specific revision #	01h,00h
166-253	Vendor specific	00h
254-255	Integrity CRC	Set at shipment
256-511	Value of bytes 0-255	

Byte	Description	Value
512-767	Value of bytes 0-255	
>767	Additional redundant parameter pages	

x16 device : the ID is outputted at word units, and defined lower-byte (IO0-7). ID table shows only lower-byte ID.

Table 9-3 Parameter Page Output Value

9.1.6 READ STATUS (70h)

The W29N02GW/Z has an 8-bit Status Register which can be read during device operation. Refer to Table 9.3 for specific Status Register definitions. After writing 70h command to the Command Register, read cycles will only read from the Status Register. The status can be read from I/O[7:0] outputs, as long as #CE and #RE are LOW. Note; #RE does not need to be toggled for Status Register read. The Command Register remains in status read mode until another command is issued. To change to normal read mode, issue the PAGE READ (00h) command. After the PAGE READ command is issued, data output starts from the initial column address.

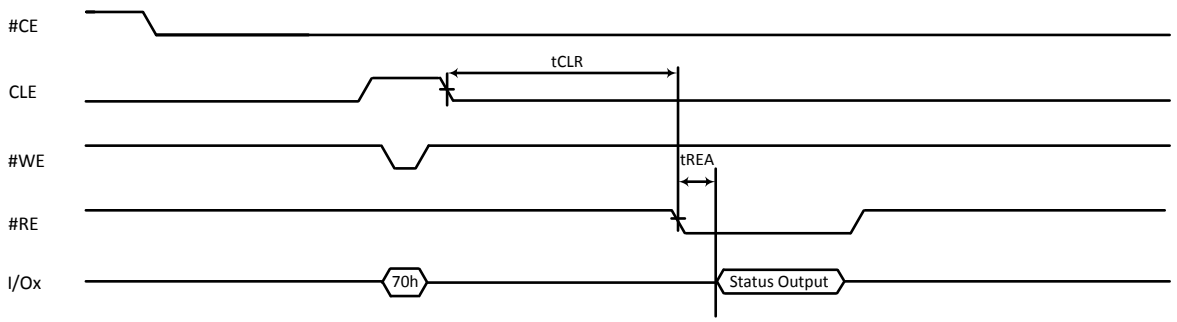

Figure 9-7 Read Status Operation

SR bit	Page Read	Page Program	Block Erase	Definition
I/O 0	Not Use	Pass/Fail	Pass/Fail	0=Successful Program/Erase 1=Error in Program/Erase
I/O 2	Not Use	Not Use	Not Use	0
I/O 3	Not Use	Not Use	Not Use	0
I/O 4	Not Use	Not Use	Not Use	0
I/O 5	Ready/Busy	Ready/Busy	Ready/Busy	Ready = 1 Busy = 0
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Ready = 1 Busy = 0
I/O 7	Write Protect	Write Protect	Write Protect	Unprotected = 1 Protected = 0

Table 9-4 Status Register Bit Definition

9.1.7 READ STATUS ENHANCED (78h)

The READ STATUS ENHANCED (78h) command returns the status of the addressed plane on a target even when it is busy (SR BIT 6 = 0).

Writing 78h to the command register, followed by three row address cycles containing the page, plane and block addresses that is same as executed addresses, puts the device into read status mode. The device stays in this mode until another valid command is issued

The device status is returned when the host requests data output. The SR BIT 6 and SR bit 5 bits of the status register are shared for all planes on the device. The SR BIT 1 and SR BIT 0 (SR bit0) bits are specific to the plane specified in the row address.

The READ STATUS ENHANCED (78h) command also enables the device for data output. To begin data output following a READ operation after the device is ready (SR BIT 6 = 1), issue the READ MODE (00h) command, then begin data output. If the host needs to change the data register that will output data, use the TWO PLANE RANDOMDATA READ (06h-E0h) command after the device is ready.

Use of the READ STATUS ENHANCED (78h) command is prohibited when OTP mode is enabled. It is also prohibited following some of the other reset, identification.

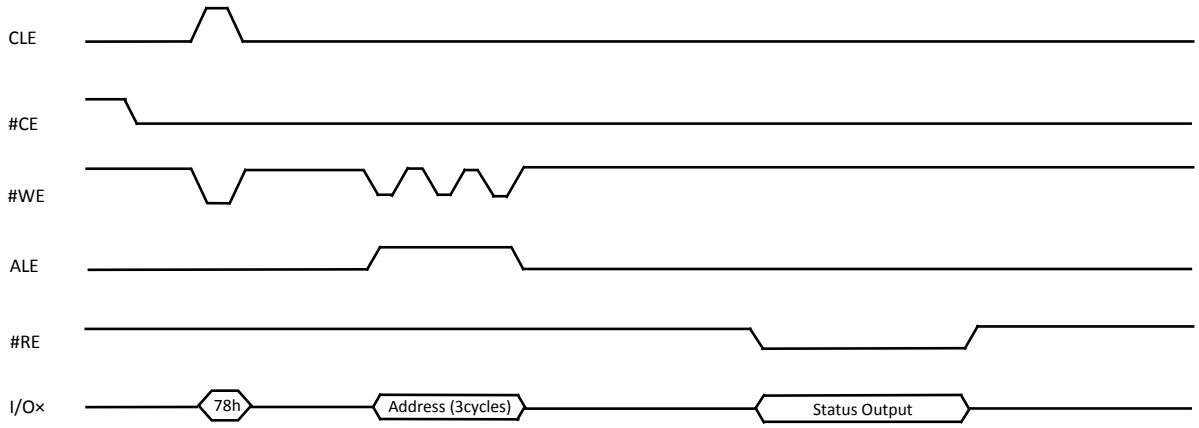

Figure 9-8 Read Status Enhanced (78h) Operation

9.1.8 READ UNIQUE ID (EDh)

The W29N02GW/Z NAND Flash device has a method to uniquely identify each NAND Flash device by using the READ UNIQUE ID command. The format of the ID is limitless, but the ID for every NAND Flash device manufactured, will be guaranteed to be unique.

Numerous NAND controllers typically use proprietary error correction code (ECC) schemes. In these cases Winbond cannot protect unique ID data with factory programmed ECC. However, to ensure data reliability, Winbond will program the NAND Flash devices with 16 bytes of unique ID code, starting at byte 0 on the page, immediately followed by 16 bytes of the complement of that unique ID. The combination of these two actions is then repeated 16 times. This means the final copy of the unique ID will resides at location byte 511. At this point an XOR or exclusive operation can be performed on the first copy of the unique ID and its complement. If the unique ID is good, the results should yield all the bits as 1s. In the event that any of the bits are 0 after the XOR operation, the procedure can be repeated on a subsequent copy of the unique ID data.

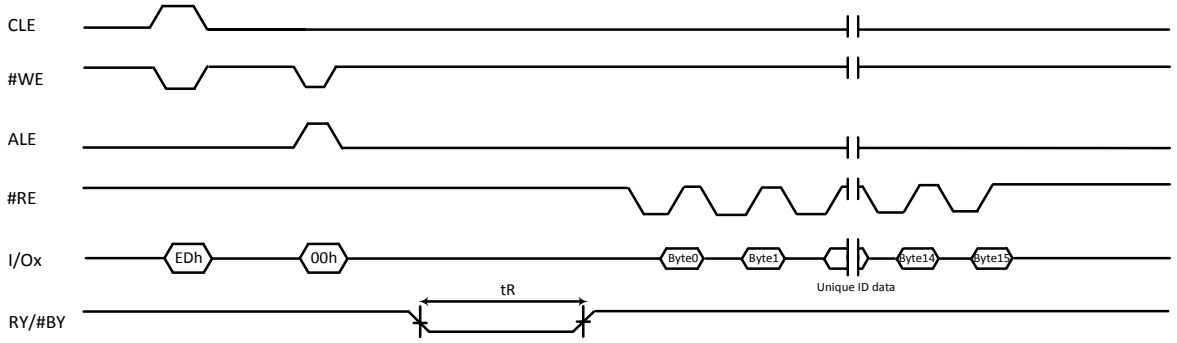

Figure 9-9 Read Unique ID

9.2 PROGRAM operation

9.2.1 PAGE PROGRAM (80h-10h)

The W29N02GW/Z Page Program command will program pages sequentially within a block, from the lower order page address to higher order page address. Programming pages out of sequence is prohibited. The W29N02GW/Z supports partial-page programming operations up to 4 times before an erase is required if partitioning a page. Note; programming a single bit more than once without first erasing it is not supported.

9.2.2 SERIAL DATA INPUT (80h)

Page Program operation starts with the execution of the Serial Data Input command (80h) to the Command Register, following next by inputting five address cycles and then the data is loaded. Serial data is loaded to Data Register with each #WE cycle. The Program command (10h) is written to the Command Register after the serial data input is finished. At this time the internal write state controller automatically executes the algorithms for program and verifies operations. Once the programming starts, determining the completion of the program process can be done by monitoring the RY/#BY output or the Status Register Bit 6, which will follow the RY/#BY signal. RY/#BY will stay LOW during the internal array programming operation during the period of (tPROG). During page program operation, only two commands are available, READ STATUS (70h) and RESET (FFh). When the device status goes to the ready state, Status Register Bit 0 (I/O0) indicates whether the program operation passed (Bit0=0) or failed (Bit0=1), (see Figure 9-13). The Command Register remains in read status mode until the next command is issued.

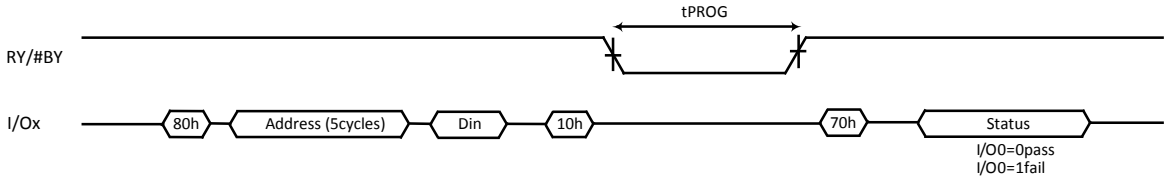

Figure 9-10 Page Program

9.2.3 RANDOM DATA INPUT (85h)

After the Page Program (80h) execution of the initial data has been loaded into the Data Register, if the need for additional writing of data is required, using the RANDOM DATA INPUT (85h) command can perform this function to a new column address prior to the Program (10h) command. The RANDOM DATA INPUT command can be issued multiple times in the same page (See Figure 9-14).

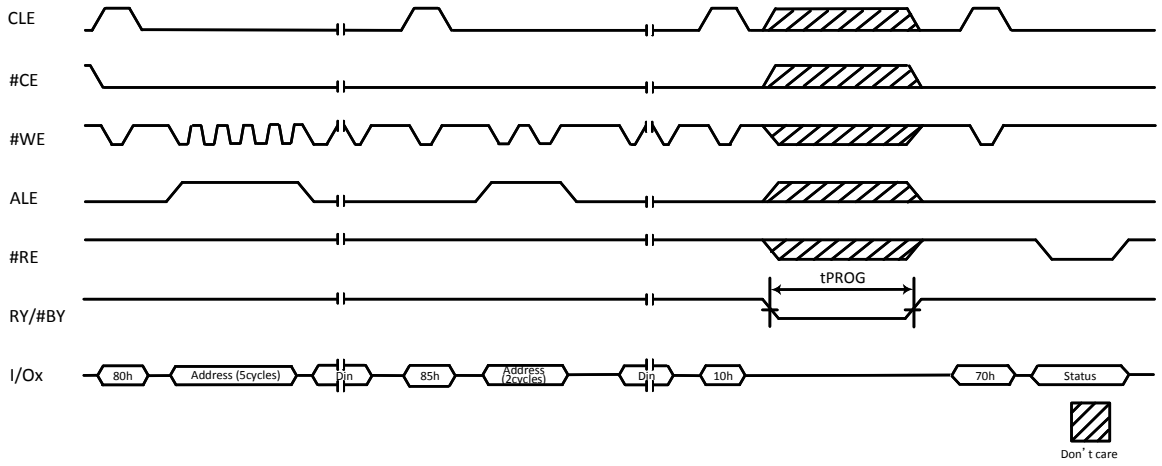

Figure 9-11 Random Data Input

9.2.4 TWO PLANE PAGE PROGRAM

TWO PLANE PAGE PROGRAM command make it possible for host to input data to the addressed plane's data register and queue the data register to be moved to the NAND Flash array.

This command can be issued several times. Each time a new plane address is specified that plane is also queued for data transfer. To input data for the final plane and to begin the program operation for all previously queued planes, the PAGE PROGRAM command has to be issued. All of the queued planes will move the data to the NAND Flash array. when it is ready (SR BIT 6 = 1),this command is accepted.

At the block and page address is specified, input a page to the data register and queue it to be moved to the NAND Flash array ,the 80h is issued to the command register. Unless this command has been preceded by a TWO PLANE PAGE PROGRAM command, issuing the 80h to the command register clears all of the data registers' contents on the selected target. Write five address cycles containing the column address and row address; data input cycles follow. Serial data is input beginning at the column address specified. At any time, while the data input cycle, the RANDOM DATA INPUT (85h) command can be issued. When data input is complete, write 11h to the command register. The device will go busy (SR BIT 6 = 0, SR BIT 5 = 0) for tDBSY.

To ascertain the progress of tDBSY, the host can monitor the target's RY/#BY signal or, the status operations (70h, 78h) can be used alternatively,. When the device status shows that it is ready (SR BIT 6 = 1), additional TWO PLANE PAGE PROGRAM commands can be issued to queue additional planes for data transfer, then, the PAGE PROGRAM commands can be issued.

When the PAGE PROGRAM command is used as the final command of a two plane program operation, data is transferred from the data registers to the NAND Flash array for all of the addressed

planes during tPROG. When the device is ready (SR BIT 6 = 1, SR BIT 5 = 1), the host should check the status of the SR BIT 0 for each of the planes to verify that programming completed successfully.

When system issues TWO PLANE PAGE PROGRAM and PAGE PROGRAM commands, READ STATUS (70h) command can confirm whether the operation(s) passed or failed. If the status after READ STATUS (70h) command indicates an error (SR BIT 0 = 1 and/or SR BIT 1 = 1), READ STATUS ENHANCED (78h) command can be determined which plane is failed.

TWO PLANE PROGRAM commands require five-cycle addresses, one address indicates the operational plane. These addresses are subject to the following requirements:

• The column address bits must be valid address for each plane

• The plane select bit, A18, must be set to “L” for 1st address input, and set to “H” for 2nd address input.

• The page address (A17-A12) and block address (A28-A19) of first input are don’t care. It follows secondary inputted page address and block address.

Two plane operations must be same type operation across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

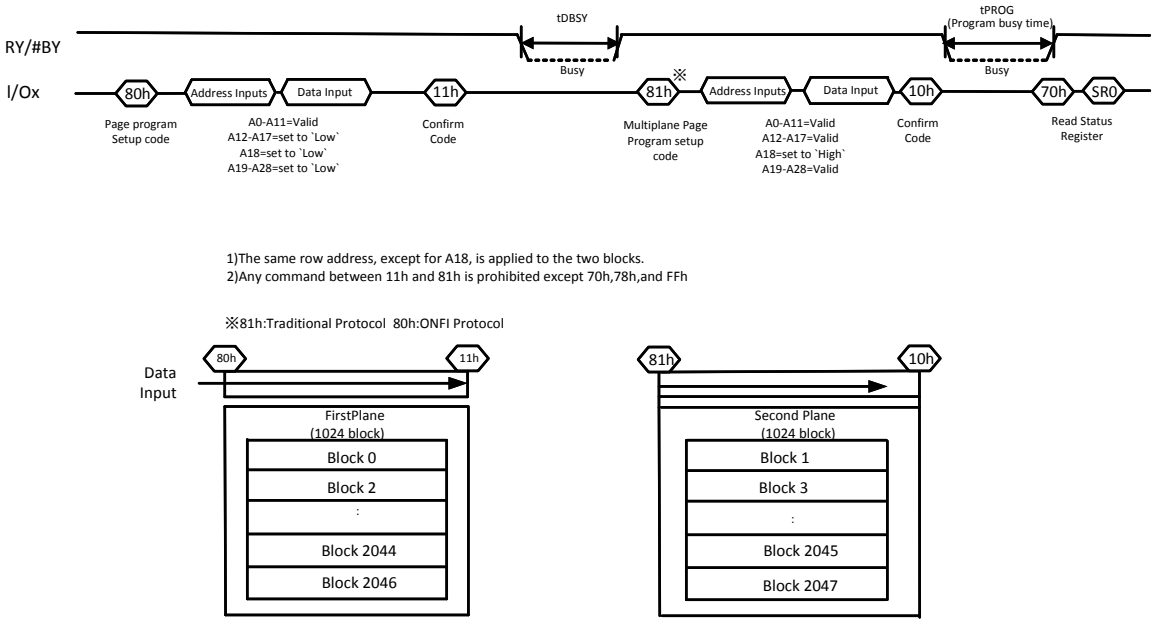

Figure 9-12 Two Plane Page Program

9.3 COPY BACK operation

Copy Back operations require two command sets. Issue a READ for COPY BACK (00h-35h) command first, then the PROGRAM for COPY BACK (85h-10h) command. Copy back operations are only supported within a same plane.

9.3.1 READ for COPY BACK (00h-35h)

The READ for COPY BACK command is used together with the PROGRAM for COPY BACK (85h-10h) command. To start execution, READ for COPY BACK (00h) command is written to the Command Register, followed by the five cycles of the source page address. To start the transfer of the selected page data from the memory array to the data register, write the 35h command to the Command Register.

After execution of the READ for COPY BACK command sequence and RY/#BY returns to HIGH marking the completion of the operation, the transferred data from the source page into the Data Register may be read out by toggling #RE. Data is output sequentially from the column address that was originally specified with the READ for COPY BACK command. RANDOM DATA OUTPUT (05h-E0h) commands can be issued multiple times without any limitation after READ for COPY BACK command has been executed (see Figures 9-19 and 9-20).

At this point the device is in ready state to accept the PROGRAM for COPY BACK command.

9.3.2 PROGRAM for COPY BACK (85h-10h)

After the READ for COPY BACK command operation has been completed and RY/#BY goes HIGH, the PROGRAM for COPY BACK command can be written to the Command Register. The command results in the transfer of data to the Data Register, then internal operations start programming of the new destination page. The sequence would be, write 85h to the Command Register, followed by the five cycle destination page address to the NAND array. Next write the 10h command to the Command Register; this will signal the internal controller to automatically start to program the data to new destination page. During this programming time, RY/#BY will LOW. The READ STATUS command can be used instead of the RY/#BY signal to determine when the program is complete. When Status Register Bit 6 (I/O6) equals to “1”, Status Register Bit 0 (I/O0) will indicate if the operation was successful or not.

The RANDOM DATA INPUT (85h) command can be used during the PROGRAM for COPY BACK command for modifying the original data. Once the data is copied into the Data Register using the READ for COPY BACK (00h-35h) command, follow by writing the RANDOM DATA INPUT (85h) command, along with the address of the data to be changed. The data to be changed is placed on the external data pins. This operation copies the data into the Data Register. Once the 10h command is written to the Command Register, the original data and the modified data are transferred to the Data Register, and programming of the new page commences. The RANDOM DATA INPUT command can be issued numerous times without limitation, as necessary before starting the programming sequence with 10h command.

Since COPY BACK operations do not use external memory and the data of source page might include a bit errors, a competent ECC scheme should be developed to check the data before programming data to a new destination page.

9.3.3 TWO PLANE READ for COPY BACK

To improve read through rate, TWO PLANE READ for COPY BACK operation is copied data concurrently from one or two plane to the specified data registers.

TWO PLANE PROGRAM for COPY BACK command can move the data in two pages from the data registers to different pages. This operation improves system performance than PROGRAM for COPY BACK operation.

9.3.4 TWO PLANE PROGRAM for COPY BACK

Function of TWO PLANE PROGRAM for COPY BACK command is equal to TWO-PLANE PAGE PROGRAM command, except that when 85h is written to the command register, then data register contents are not cleared. Refer to TWO-PLANE PAGE PROGRAM for more details features.

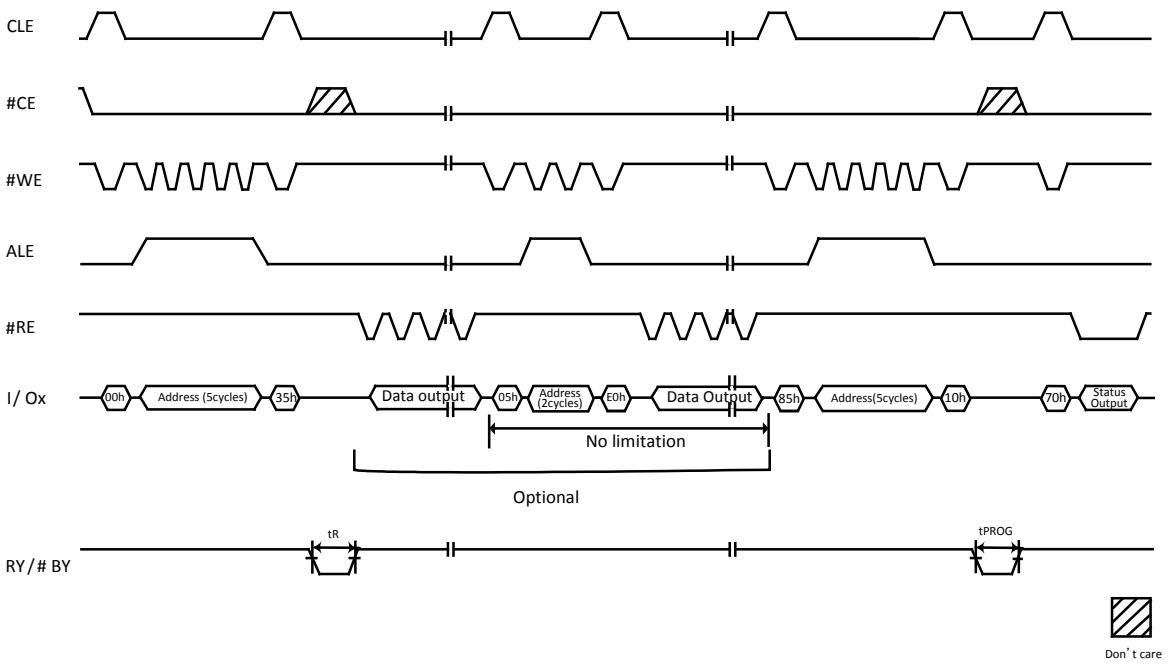

Figure 9-13 Program for copy back Operation

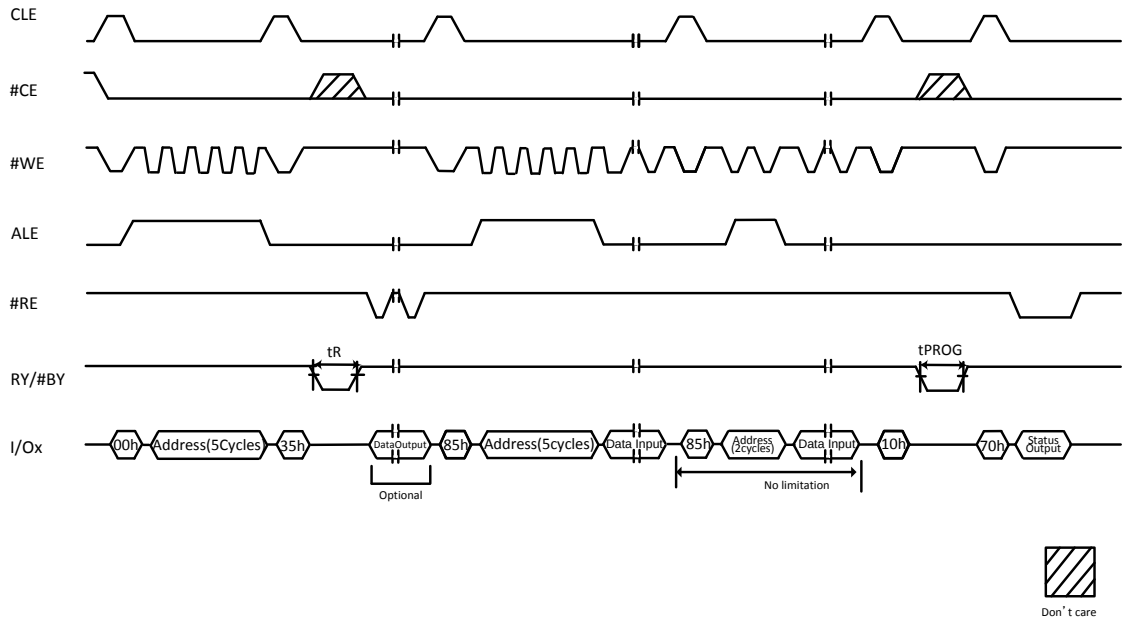

Figure 9-14 Copy Back Operation with Random Data Input

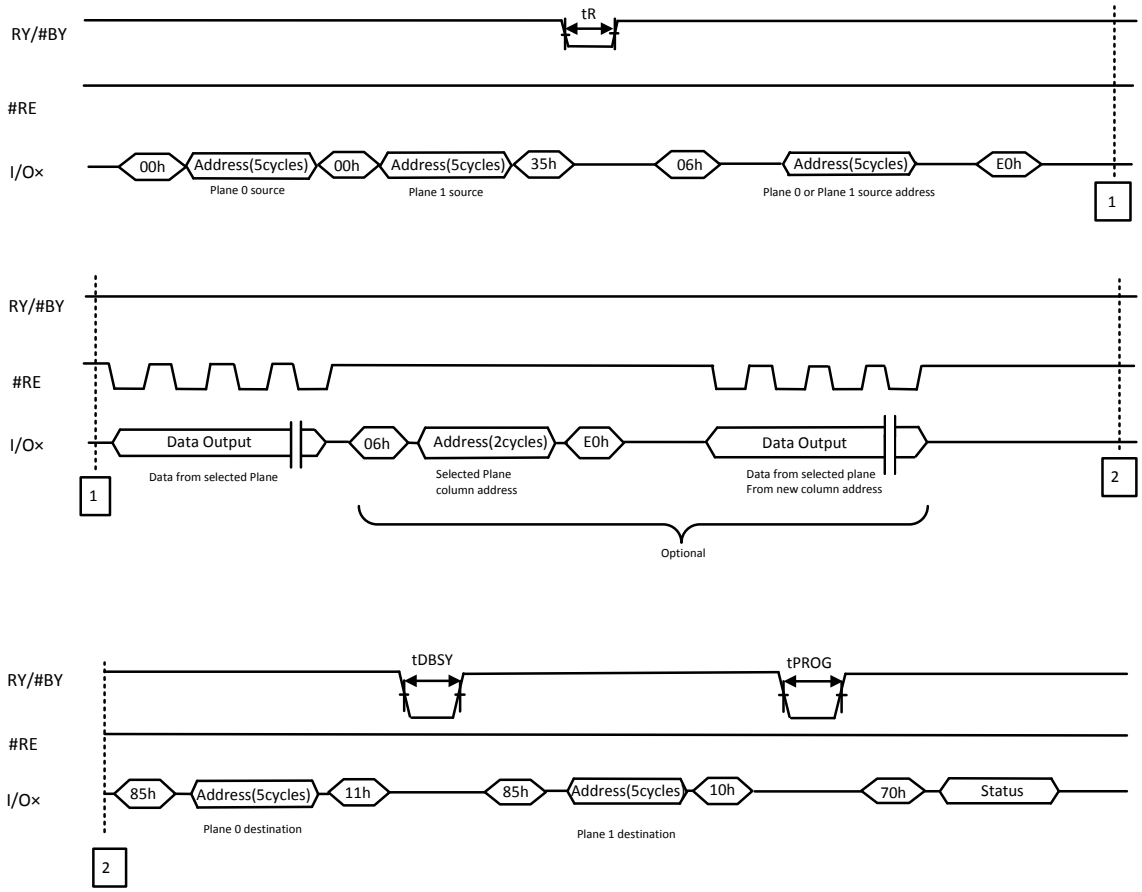

Figure 9-15 Two Plane Copy Back

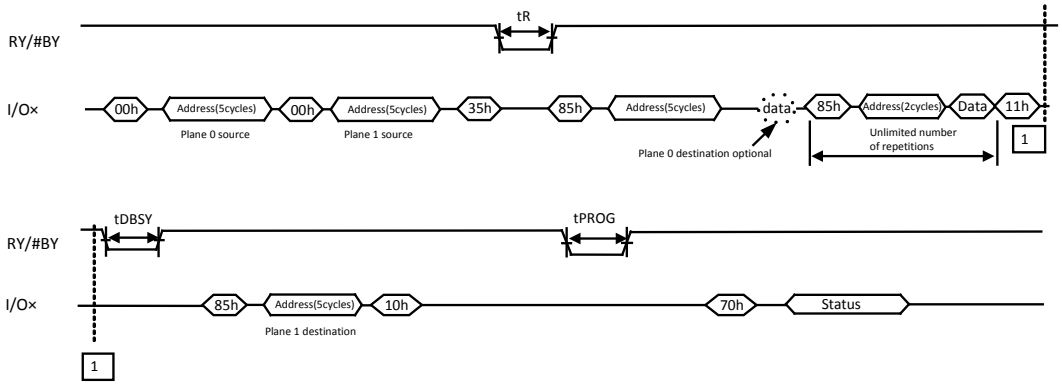

Figure 9-16 Two Plane Copy Back with Random Data Input

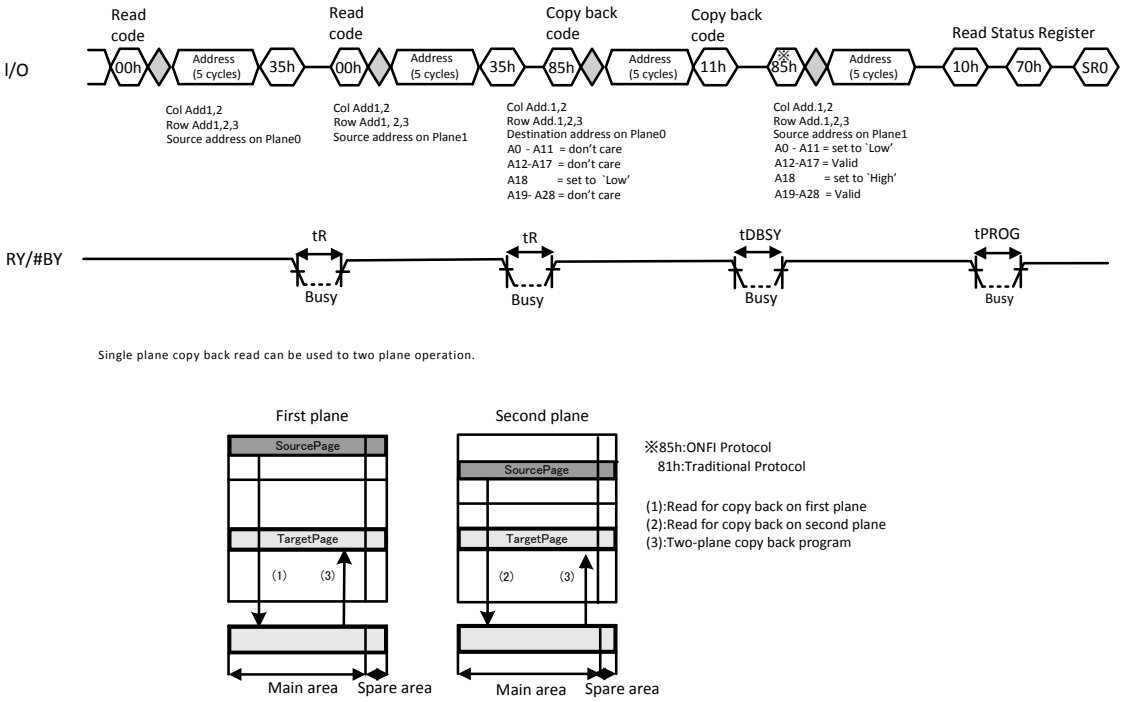

Figure 9-17 Two Plane Program for copy back

9.4 BLOCK ERASE operation

9.4.1 BLOCK ERASE (60h-D0h)

Erase operations happen at the architectural block unit. This W29N02GW/Z has 2048 erase blocks. Each block is organized into 64 pages (x8:2112 bytes/page, x16:1056 words/page), 132K bytes (x8:128K + 4K bytes, x16:64 K+ 2Kwords)/block. The BLOCK ERASE command operates on a block by block basis.

Erase Setup command (60h) is written to the Command Register. Next, the three cycle block address is written to the device. The page address bits are loaded during address block address cycle, but are ignored. The Erase Confirm command (D0h) is written to the Command Register at the rising edge of #WE, RY/#BY goes LOW and the internal controller automatically handles the block erase sequence of operation. RY/#BY goes LOW during Block Erase internal operations for a period of tBERS,

The READ STATUS (70h) command can be used for confirm block erase status. When Status Register Bit6 (I/O6) becomes to “1”, block erase operation is finished. Status Register Bit0 (I/O0) will indicate a pass/fail condition (see Figure 9-24).

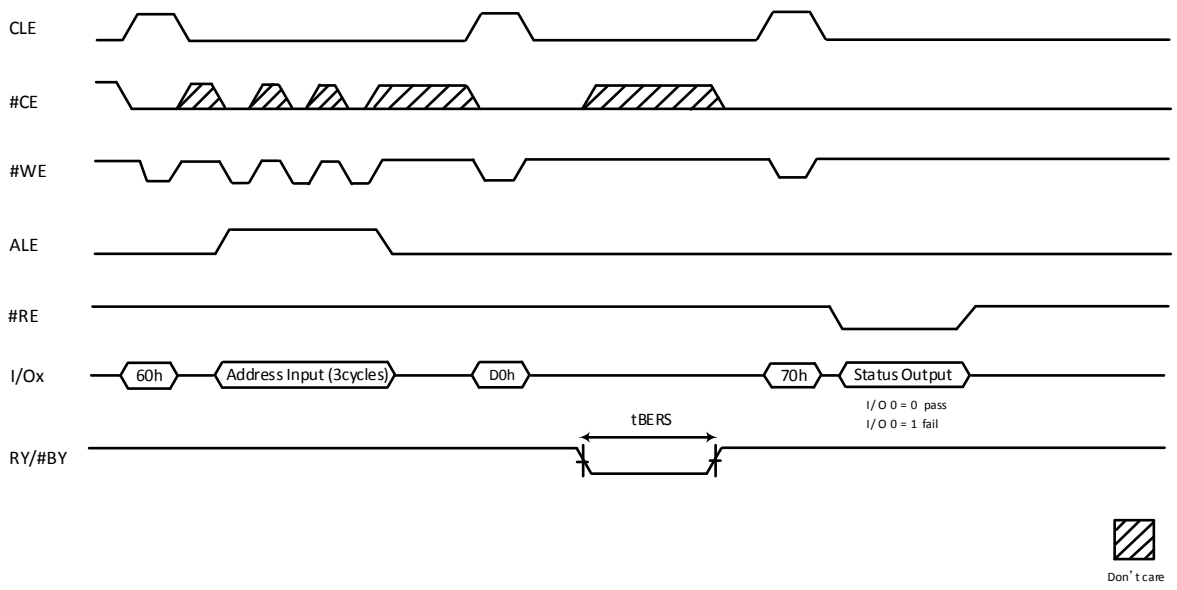

Figure 9-18 Block Erase Operation

9.4.2 TWO PLANE BLOCK ERASE

TWO PLANE BLOCK ERASE (60h-D1h) command indicates two blocks in the specified plane that is to be erased. To start ERASE operation for indicated blocks in the specified plane, write the BLOCK ERASE (60h-D0h) command.

To indicate a block to be erased, writing 60h to the command register, then, write three address cycles containing the row address, the page address is ignored. By writing D1h command to command register, the device will go busy (SR BIT 6 = 0, SR BIT 5 = 0) for tDBSY.

To confirm busy status during tDBSY, the host can monitor RY/#BY signal. Instead, system can use READ STATUS (70h) or READ STATUS ENHANCED (78h) commands. When the status shows ready (SR BIT 6 = 1, SR BIT 5 = 1), additional TWO PLANE BLOCK ERASE commands can be issued for erasing two blocks in a specified plane.

When system issues TWO PLANE BLOCK ERASE (60h-D1h), and BLOCK ERASE (60h-D0h) commands, READ STATUS (70h) command can confirm whether the operation(s) passed or failed. If the status after READ STATUS (70h) command indicates an error (SR BIT 0 = 1), READ STATUS ENHANCED (78h) command can be determined which plane is failed.

TWO PLANE BLOCK ERASE commands require three cycles of row addresses; one address indicates the operational plane. These addresses are subject to the following requirements:

• The plane select bit, A18, must be different for each issued address.

• Block address (A28-A19) of first input is don't care. It follows secondary inputted block address.

Two plane operations must be same type operation across the planes; for example, it is not possible to perform a PROGRAM operation on one plane with an ERASE operation on another.

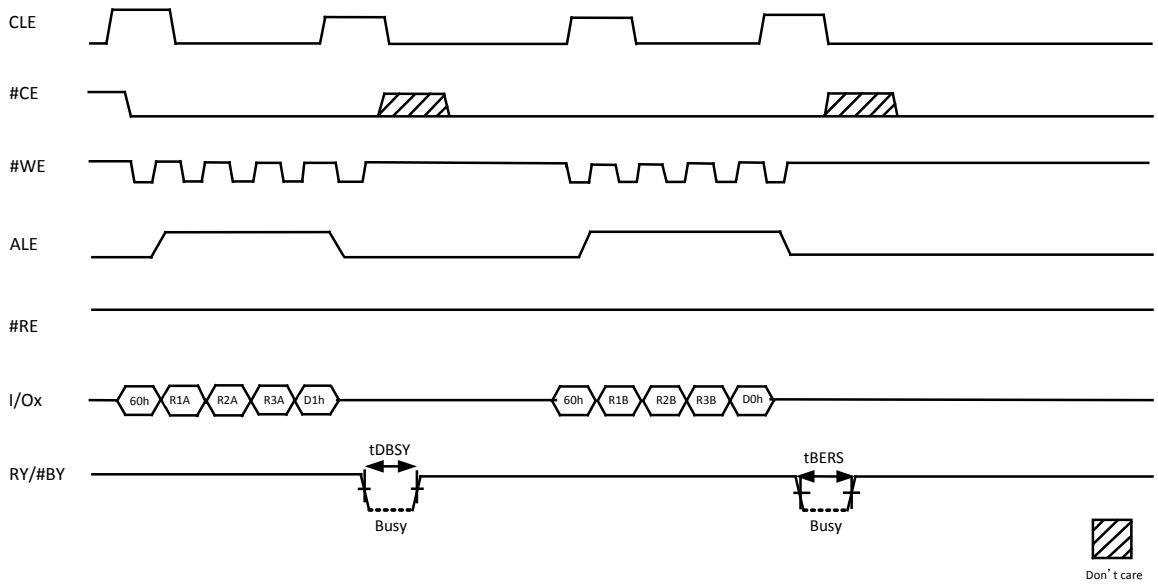

Figure 9-19 Two Plane Block Erase Operation

9.5 RESET operation

9.5.1 RESET (FFh)

READ, PROGRAM, and ERASE commands can be aborted by the RESET (FFh) command during the time the W29N02GW/Z is in the busy state. The Reset operation puts the device into known status. The data that is processed in either the programming or erasing operations are no longer valid. This means the data can be partially programmed or erased and therefore data is invalid. The Command Register is cleared and is ready to accept next command. The Data Register contents are marked invalid.

The Status Register indicates a value of E0h when #WP is HIGH; otherwise a value of 60h is written when #WP is LOW. After RESET command is written to the command register, RY/#BY goes LOW for a period of tRST (see Figure 9-26).

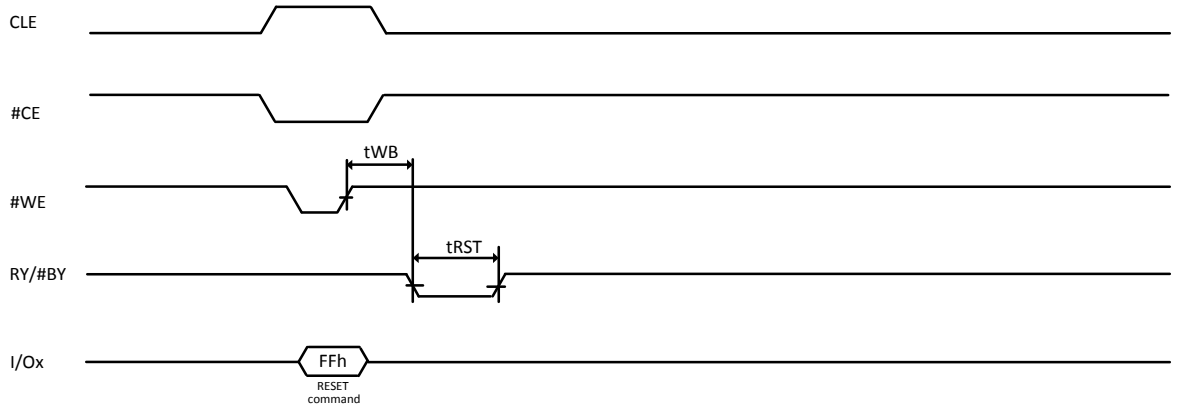

Figure 9-20 Reset Operation

9.6 FEATURE OPERATION

The GET FEATURES (EEh) and SET FEATURES (EFh) commands are used to change the NAND Flash device behavior from the default power on settings. These commands use a one-byte feature address to determine which feature is to be read or modified. A range of 0 to 255 defines all features; each is described in the features table (see Table 9.5 thru 9.7). The GET FEATURES (EEh) command reads 4-Byte parameter in the features table (See GET FEATURES function). The SET FEATURES (EFh) command places the 4-Byte parameter in the features table (See SET FEATURES function).

When a feature is set, meaning it remains active by default until the device is powered off. The set feature remains the set even if a RESET (FFh) command is issued.

Feature address	Description
00h	N.A
02h-7Fh	Reserved
80h	Vendor specific parameter : Programmable I/O drive strength
81h	Vendor specific parameter : Programmable RY/#BY pull-down strength
82h-FFh	Reserved

Table 9-5 Features

Feature Address 80h: Programmable I/O Drive Strength

Sub feature parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
I/O drive strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Table 9-6 Feature Address 80h

Note:

1. **The default drive strength setting is Full strength. The Programmable I/O Drive Strength mode is used to change from the default I/O drive strength. Drive strength should be selected based on expected loading of the memory bus. This table shows the four supported output drive-strength settings. The device returns to the default drive strength mode when a power cycle has occurred. AC timing parameters may need to be relaxed if I/O drive strength is not set to full.**

Feature Address 81h: Programmable RY/#BY Pull-down Strength

Sub feature parameter	Options	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Value	Notes
P1											
RY/#BY pull-down strength	Full (default)	Reserved (0)						0	0	00h	1
	Three-quarters	Reserved (0)						0	1	01h	
	One-half	Reserved (0)						1	0	02h	
	One-quarter	Reserved (0)						1	1	03h	
P2											
		Reserved (0)								00h	
P3											
		Reserved (0)								00h	
P4											
		Reserved (0)								00h	

Table 9-7 Feature Address 81h

Note:

1. **The default programmable RY/#BY pull-down strength is set to Full strength. The pull-down strength is used to change the RY/#BY pull-down strength. RY/#BY pull-down strength should be selected based on expected loading of RY/#BY. The four supported pull-down strength settings are shown. The device returns to the default pull-down strength when a power cycle has occurred.**

9.6.1 GET FEATURES (EEh)

The GET FEATURES command returns the device feature settings including those previously set by the SET FEATURES command. To use the Get Feature mode write the command (EEh) to the Command Register followed by the single cycle byte Feature Address. RY/#BY will goes LOW for the period of tFEAT. If Read Status (70h) command is issued for monitoring the process completion status, Read Command (00h) has to be executed to re-establish data output mode. Once, RY/#BY goes HIGH, the device feature settings can be read by toggling #RE. The device remains in Feature Mode until another valid command is issued to Command Register. See Figure 9-27.

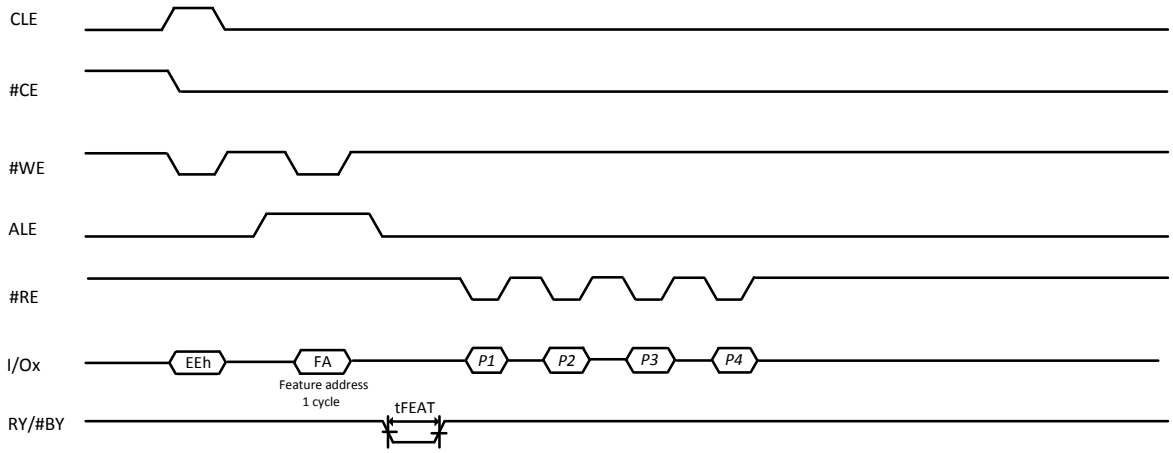

Figure 9-21 Get Feature Operation

9.6.2 SET FEATURES (EFh)

The SET FEATURES command sets the behavior parameters by selecting a specified feature address. To change device behavioral parameters, execute Set Feature command by writing EFh to the Command Register, followed by the single cycle feature address. Each feature parameter (P1-P4) is latched at the rising edge of each #WE. The RY/#BY signal will go LOW during the period of tFEAT while the four feature parameters are stored. The Read Status (70h) command can be issued for monitoring the progress status of this operation. The parameters are stored in device until the device goes through a power on cycle. The device remains in feature mode until another valid command is issued to Command Register.

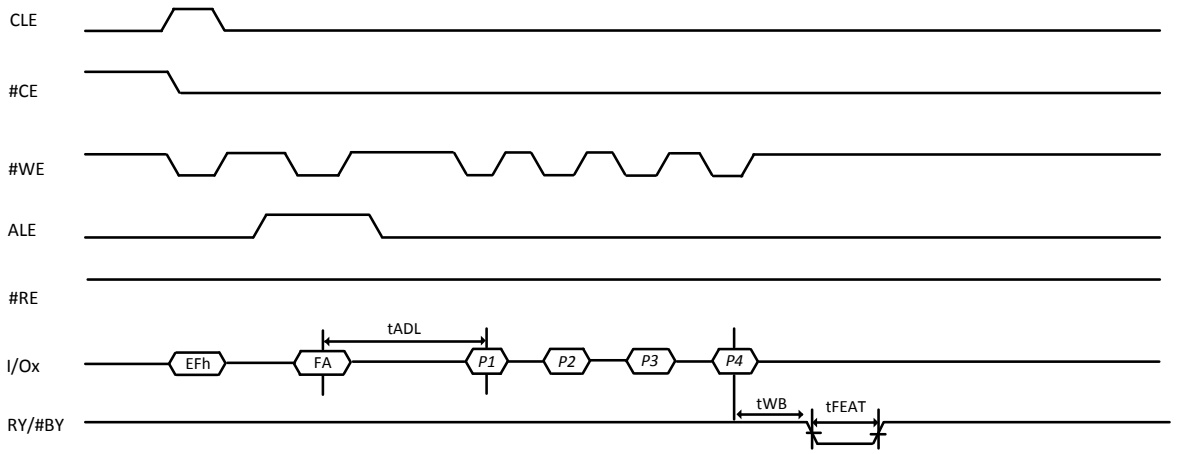

Figure 9-22 Set Feature Operation

9.7 ONE TIME PROGRAMMABLE (OTP) area

The device has One-Time Programmable (OTP) memory area comprised of a number of pages (2112 bytes/page) (1056words/page). This entire range of pages is functionally guaranteed. Only the OTP commands can access the OTP area. When the device ships from Winbond, the OTP area is in an erase state (all bits equal “1”). The OTP area cannot be erased, therefore protecting the area only prevent further programming. Contact to Winbond for using this feature.

9.8 WRITE PROTECT

#WP pin can enable or disable program and erase commands preventing or allowing program and erase operations. Figure 9-29 to 9-34 shows the enabling or disabling timing with #WP setup time (tWW) that is from rising or falling edge of #WP to latch the first commands. After first command is latched, #WP pin must not toggle until the command operation is complete and the device is in the ready state. (Status Register Bit5 (I/O5) equal 1)

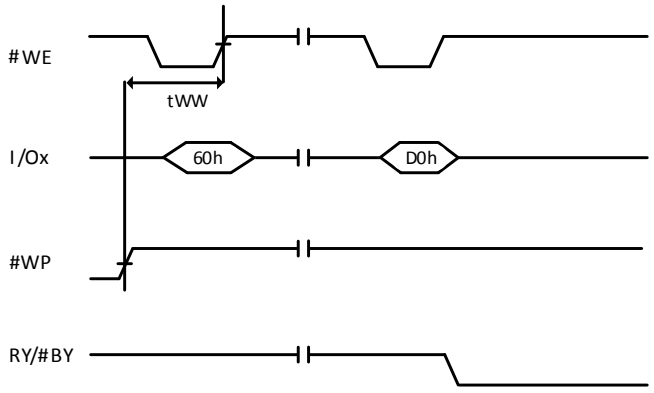

Figure 9-23 Erase Enable

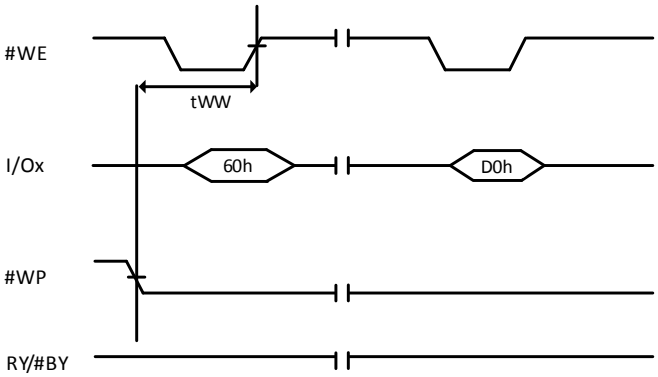

Figure 9-24 Erase Disable

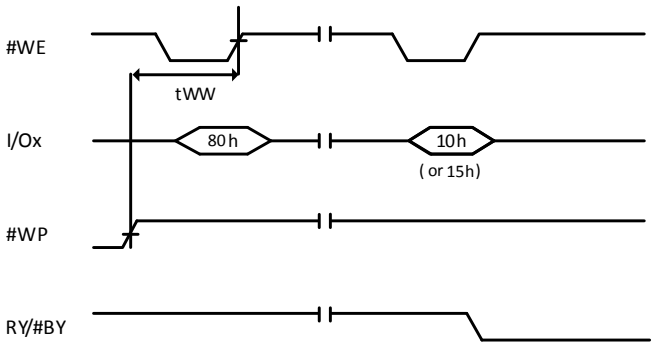

Figure 9-25 Program Enable

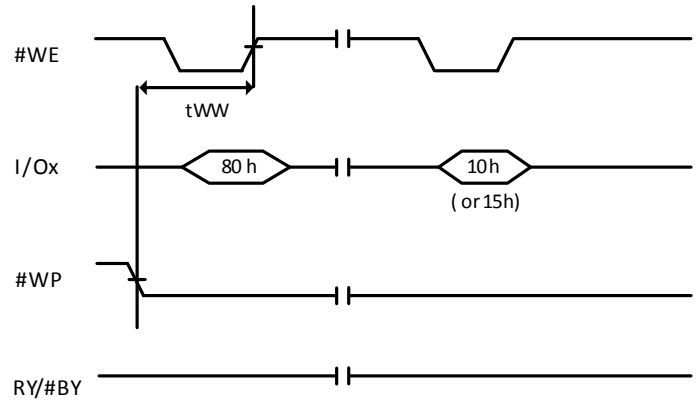

Figure 9-26 Program Disable

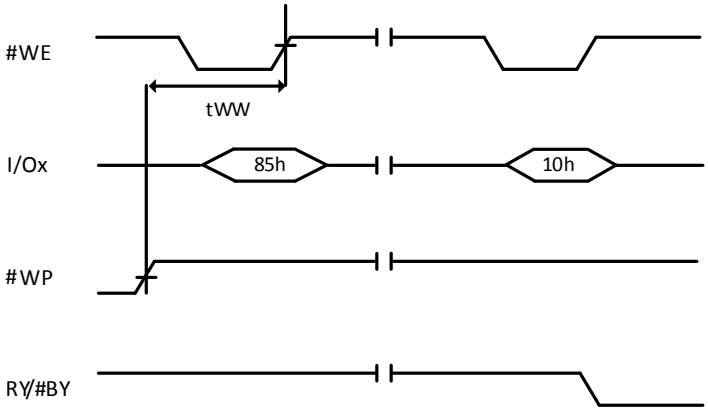

Figure 9-27 Program for Copy Back Enable

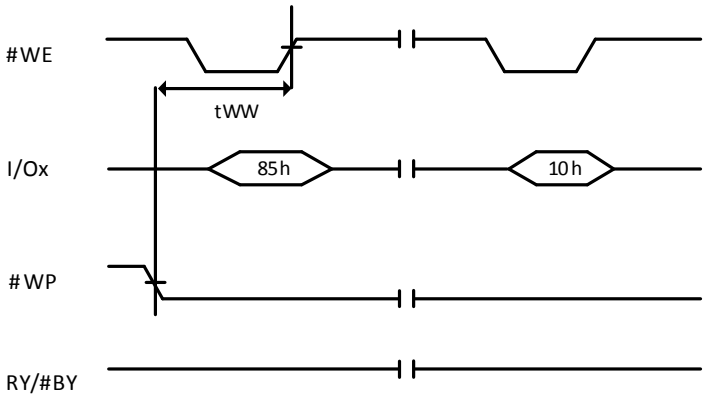

Figure 9-28 Program for Copy Back Disable

9.9 BLOCK LOCK

The device has block lock feature that can protect the entire device or user can indicate a ranges of blocks from program and erase operations. Using this feature offers increased functionality and flexibility data protection to prevent unexpected program and erase operations. Contact to Winbond for using this feature.

10. ELECTRICAL CHARACTERISTICS

10.1 Absolute Maximum Ratings (1.8V)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +2.4	V
Voltage Applied to Any Pin	VIN	Relative to Ground	–0.6 to +2.4	V
Storage Temperature	TSTG		–65 to +150	°C
Short circuit output current, I/Os			5	mA

Table 10-1 Absolute Maximum Ratings

Notes:

1. **Specification for W29N02GW/Z is preliminary. See preliminary designation at the end of this document.**
2. **This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.**

10.2 Operating Ranges (1.8V)

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage	VCC		1.7	1.95	V
Ambient Temperature, Operating	TA	Industrial	-40	+85	°C

Table 10-2 Operating Ranges

10.3 Device power-up timing

The device is designed to avoid unexpected program/erase operations during power transitions. When the device is powered on, an internal voltage detector disables all functions whenever Vcc is below about 1.1V at 1.8V device. Write Protect (#WP) pin provides hardware protection and is recommended to be kept at VIL during power up and power down. A recovery time of minimum 1ms is required before internal circuit gets ready for any command sequences (See Figure 10-1).

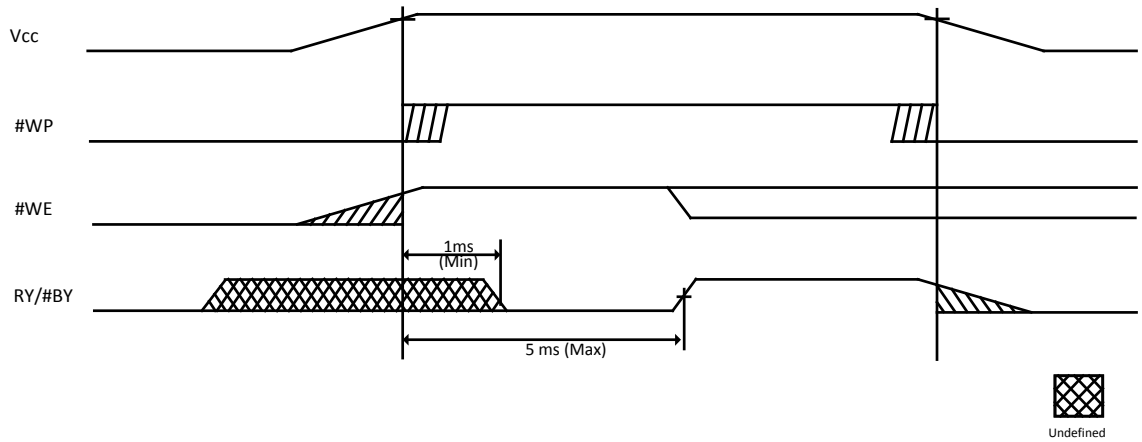

Figure 10-1 Power ON/OFF sequence

10.4 DC Electrical Characteristics (1.8V)

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	

Sequential Read current	Icc1	tRC= tRC MIN
		#CE=VIL
		IOUT=0mA
			-	13	20	mA

Program current	Icc2	-	-	10	20	mA
Erase current	Icc3	-	-	10	20	mA
Standby current (TTL)	ISB1	#CE=VIH #WP=0V/Vcc	-	-	1	mA
Standby current (CMOS)	ISB2	#CE=Vcc – 0.2V #WP=0V/Vcc	-	10	50	µA
Input leakage current	ILI	VIN= 0 V to Vcc	-	-	±10	µA
Output leakage current	ILO	VOUT=0V to Vcc	-	-	±10	µA
Input high voltage	VIH	I/O15~0, #CE,#WE,#RE, #WP,CLE,ALE	0.8 x Vcc	-	Vcc + 0.3	V
Input low voltage	VIL	-	-0.3	-	0.2 x Vcc	V
Output high voltage(1)	VOH	IOH=-100µA	Vcc -0.1	-	-	V
Output low voltage(1)	VOL	IOL=+100µA	-	-	0.1	V
Output low current	IOL(RY/#BY)	VOL=0.2V	3	4		mA

Table 10-3 DC Electrical Characteristics

Note:

1. **VOH and VOL may need to be relaxed if I/O drive strength is not set to full.**

10.5 AC Measurement Conditions (1.8V)

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Input Capacitance(1), (2)	CIN	-	10	pF
Input/Output Capacitance(1), (2)	CIO	-	10	pF
Input Rise and Fall Times	TR/TF	-	2.5	ns
Input Pulse Voltages	-	0 to VCC		V
Input/Output timing Voltage	-	Vcc/2		V
Output load (1)	CL	1TTL GATE and CL=30pF		-

Table 10-4 AC Measurement Conditions

Notes:

1. **Verified on device characterization , not 100% tested**
2. **Test conditions TA=25'C, f=1MHz, VIN=0V**

10.6 AC timing characteristics for Command, Address and Data Input (1.8V)

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
ALE to Data Loading Time	tADL	70	-	ns
ALE Hold Time	tALH	5	-	ns
ALE setup Time	tALS	10	-	ns
#CE Hold Time	tCH	5	-	ns
CLE Hold Time	tCLH	5	-	ns
CLE setup Time	tCLS	10	-	ns
#CE setup Time	tCS	20	-	ns
Data Hold Time	tDH	5	-	ns
Data setup Time	tDS	10	-	ns
Write Cycle Time	tWC	25	-	ns
#WE High Hold Time	tWH	10	-	ns
#WE Pulse Width	tWP	12	-	ns
#WP setup Time	tWW	100	-	ns

Table 10-5 AC timing characteristics for Command, Address and Data Input

Note:

1. **tADL is the time from the #WE rising edge of final address cycle to the #WE rising edge of first data cycle.**

10.7 AC timing characteristics for Operation (1.8V)

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
ALE to #RE Delay	tAR	10	-	ns
#CE Access Time	tCEA	-	25	ns
#CE HIGH to Output High-Z(1)	tCHZ	-	50	ns
CLE to #RE Delay	tCLR	10	-	ns
#CE HIGH to Output Hold	tCOH	15	-	ns
Output High-Z to #RE LOW	tIR	0	-	ns
Data Transfer from Cell to Data Register	tR	-	25	µs
READ Cycle Time	tRC	25	-	ns
#RE Access Time	tREA	-	22	ns
#RE HIGH Hold Time	tREH	10	-	ns
#RE HIGH to Output Hold	tRHOH	15	-	ns
#RE HIGH to #WE LOW	tRHW	100	-	ns
#RE HIGH to Output High-Z(1)	tRHZ	-	100	ns
#RE LOW to output hold	tRLOH	3	-	ns
#RE Pulse Width	tRP	12	-	ns
Ready to #RE LOW	tRR	20	-	ns
Reset Time (READ/PROGRAM/ERASE)(2)	tRST	-	5/10/500	µs
#WE HIGH to Busy(3)	tWB	-	100	ns
#WE HIGH to #RE LOW	tWHR	80	-	ns

Table 10-6 AC timing characteristics for Operation

Notes: AC characteristics may need to be relaxed if I/O drive strength is not set to "full."

1. **Transition is measured ±200mV from steady-state voltage with load. This parameter is sampled and not 100 % tested**
2. **Do not issue new command during tWB, even if RY/#BY is ready.**

10.8 Program and Erase Characteristics

PARAMETER	SYMBOL	SPEC		UNIT
		TYP	MAX	
Number of partial page programs	NoP	-	4	cycles
Page Program time	tPROG	250	700	µs
Busy Time for SET FEATURES /GET FEATURES	tFEAT	-	1	µs
Busy Time for program/erase at locked block	tLBSY	-	3	µs
Busy Time for OTP program when OTP is protected	tOBSY	-	30	µs
Block Erase Time	tBERS	2	10	ms
Last Page Program time (1)	tLPROG	-	-	-
Busy Time for Two Plane page program and Two Plane Block Erase	tDBSY	0.5	1	µs

Table 10-7 Program and Erase Characteristics

Note:

1. **tLPROG = Last Page program time (tPROG) + Last -1 Page program time (tPROG) – Last page Address, Command and Data load time.**

11. TIMING DIAGRAMS

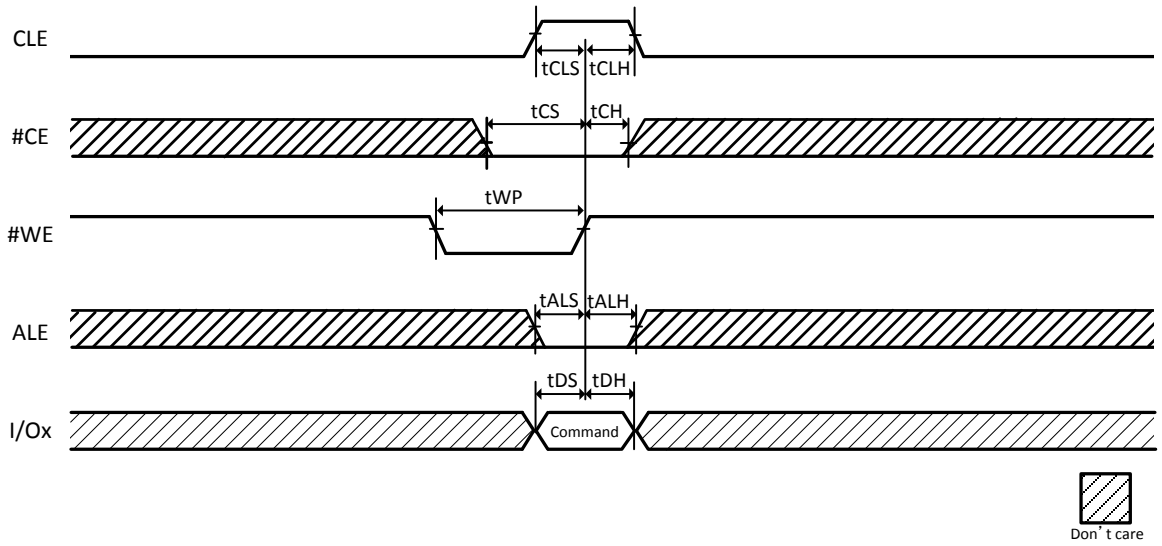

Figure 11-1 Command Latch Cycle

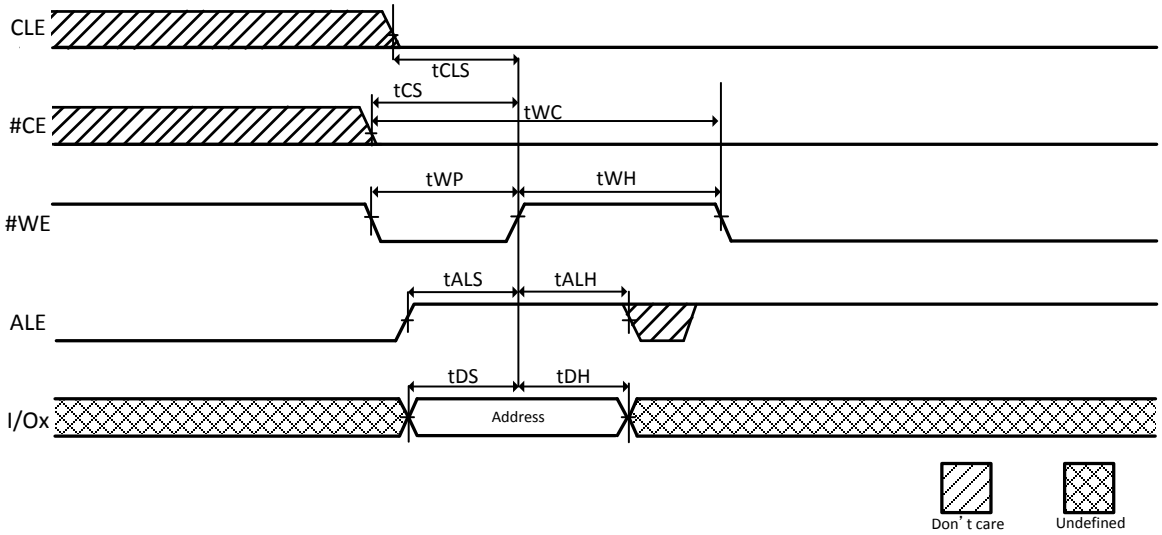

Figure 11-2 Address Latch Cycle

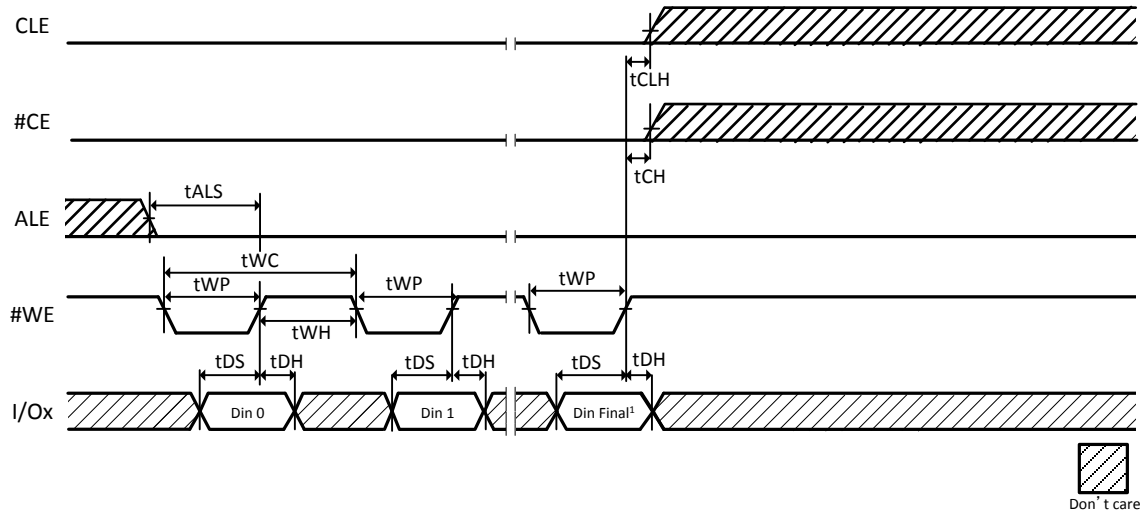

Figure 11-3 Data Latch Cycle

Note:

1. **Din Final = 2,111(x8)**

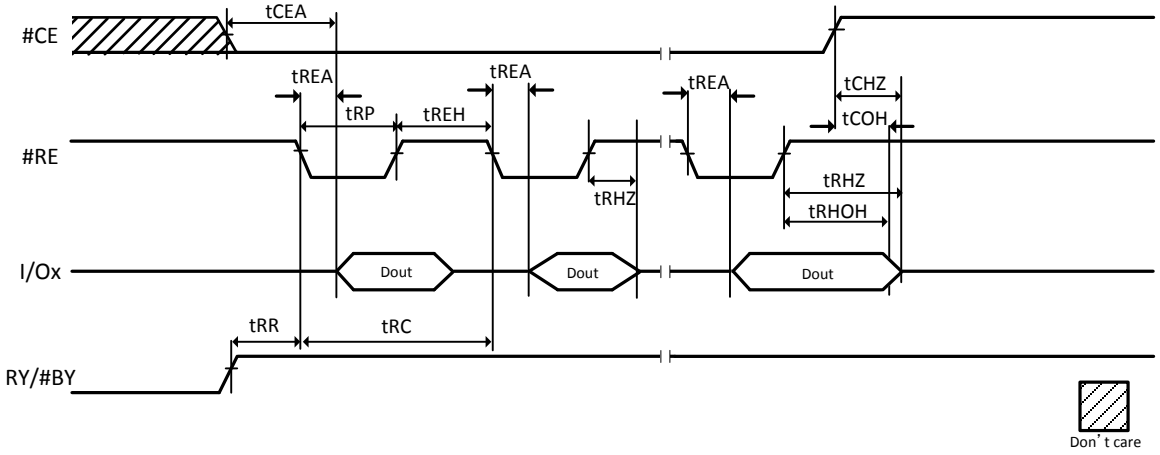

Figure 11-4 Serial Access Cycle after Read

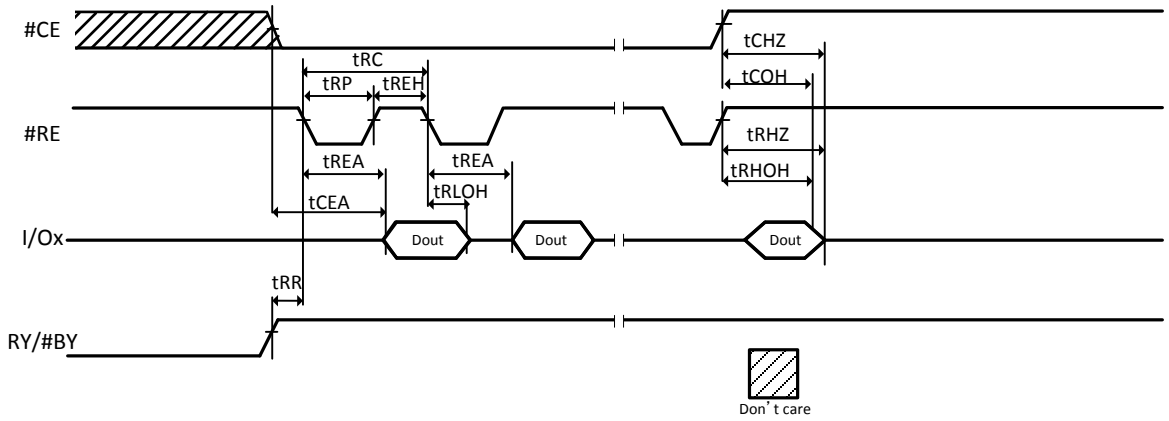

Figure 11-5 Serial Access Cycle after Read (EDO)

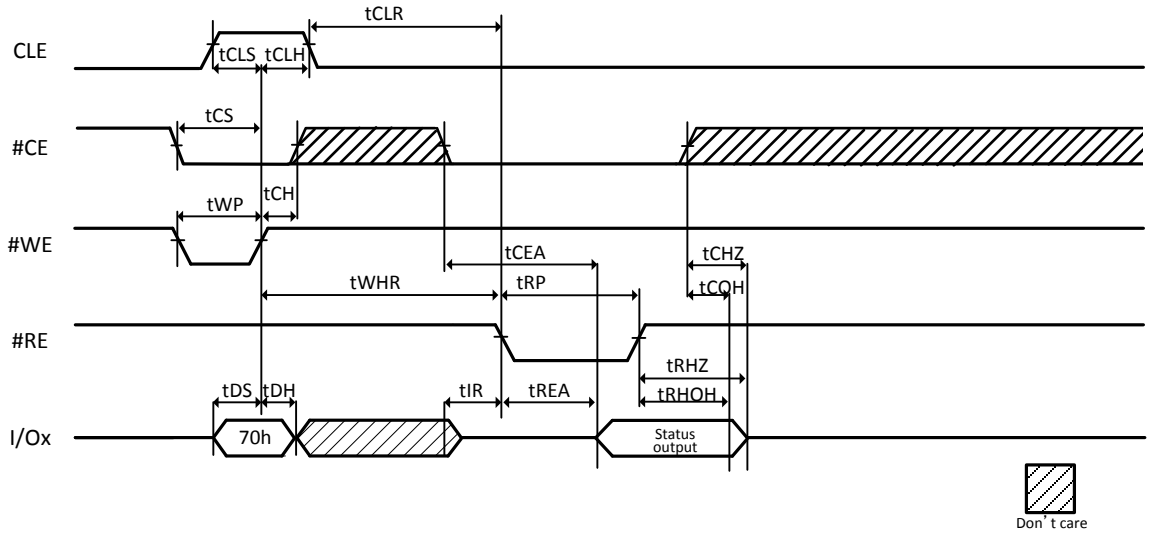

Figure 11-6 Read Status Operation

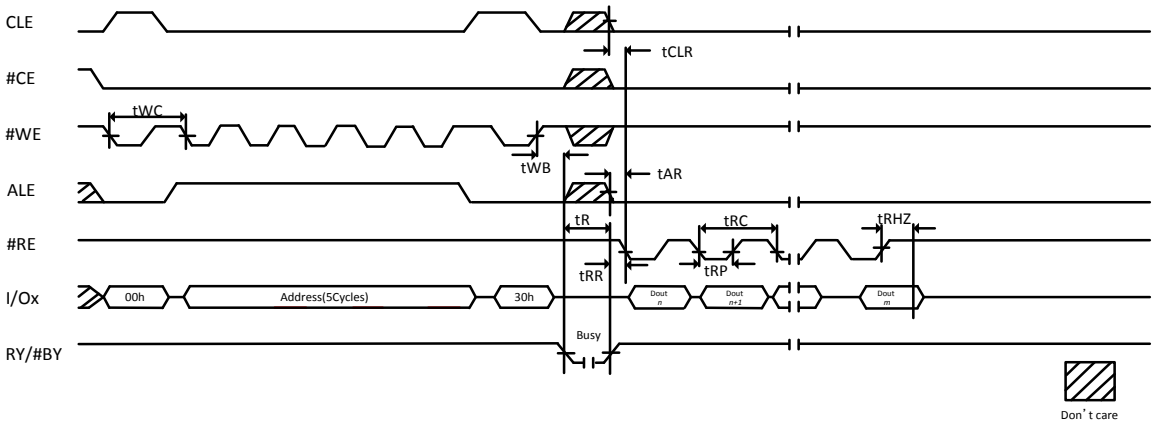

Figure 11-7 Page Read Operation

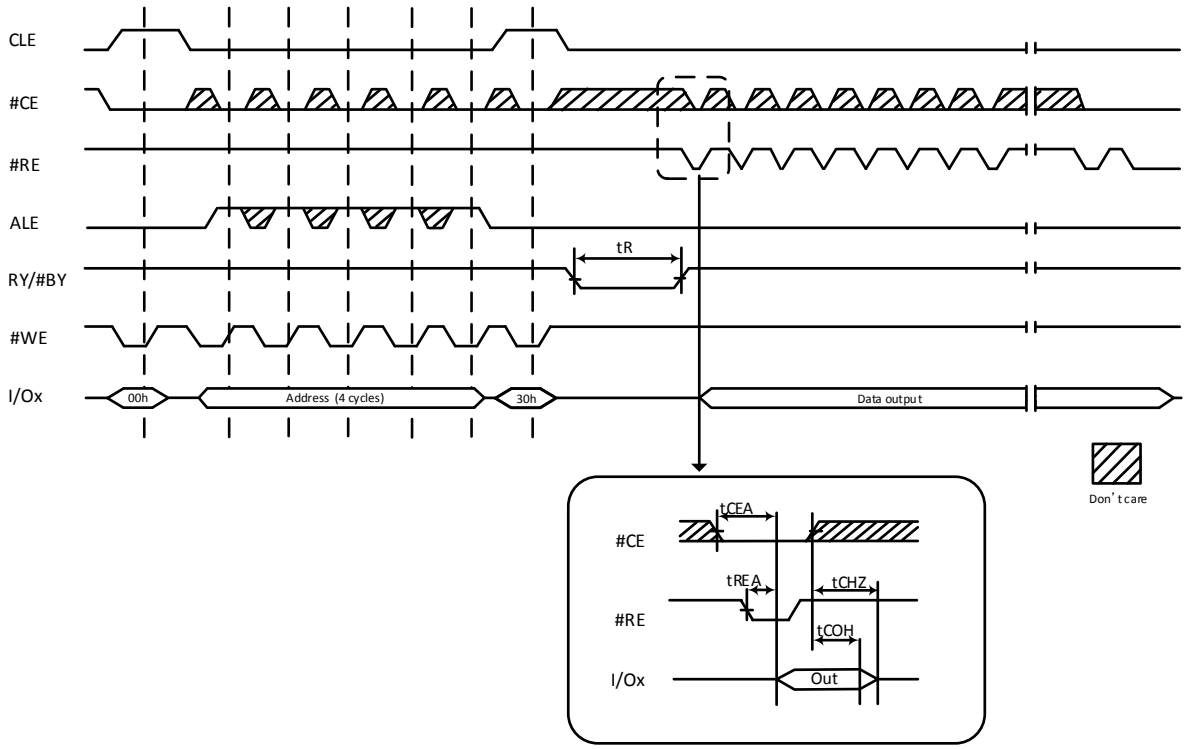

Figure 11-8 #CE Don't Care Read Operation

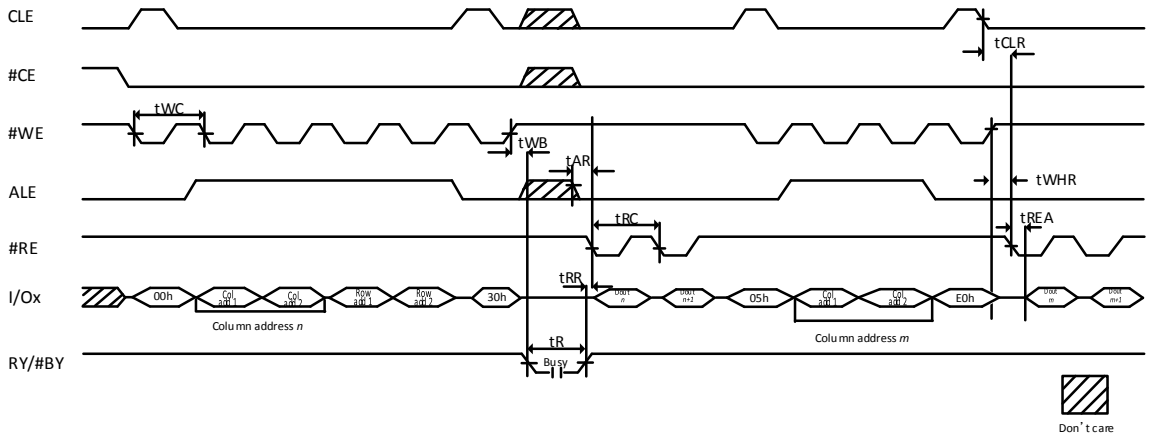

Figure 11-9 Random Data Output Operation

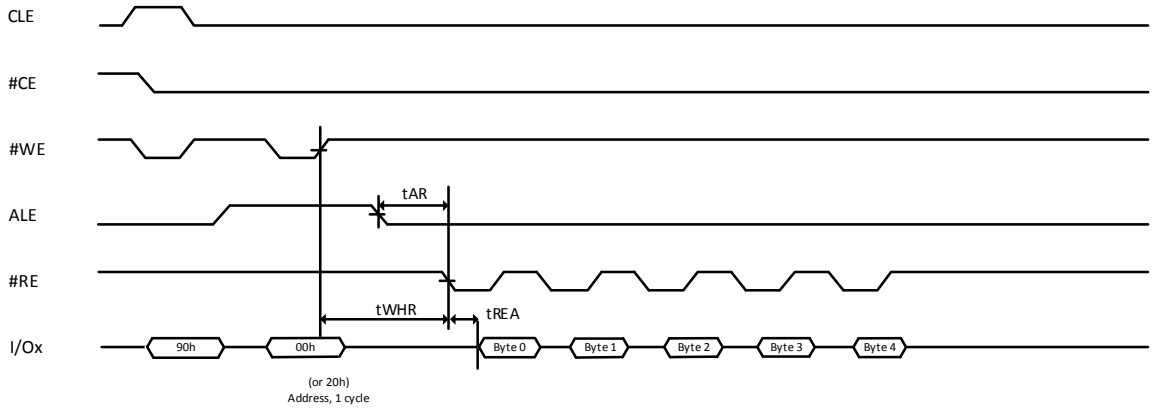

Figure 11-10 Read ID

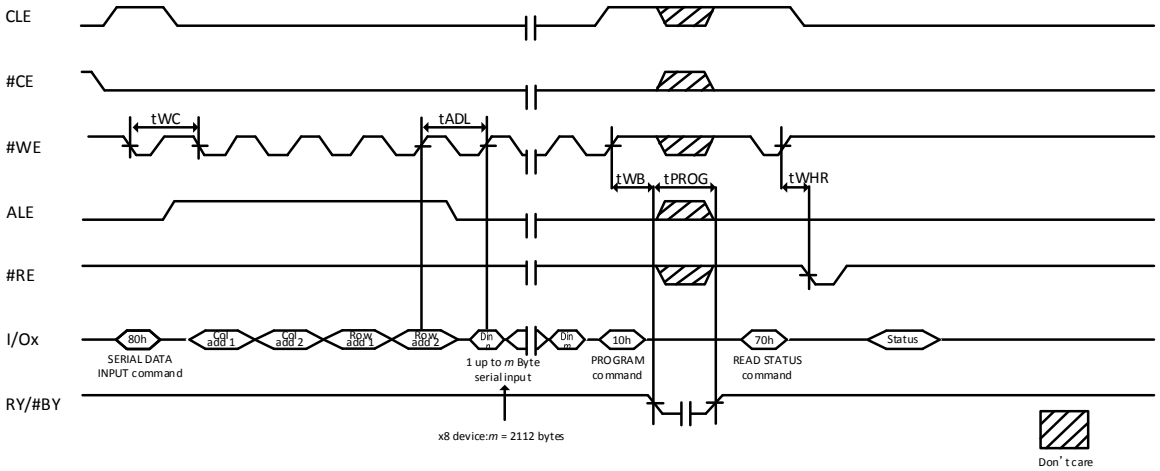

Figure 11-11 Page Program

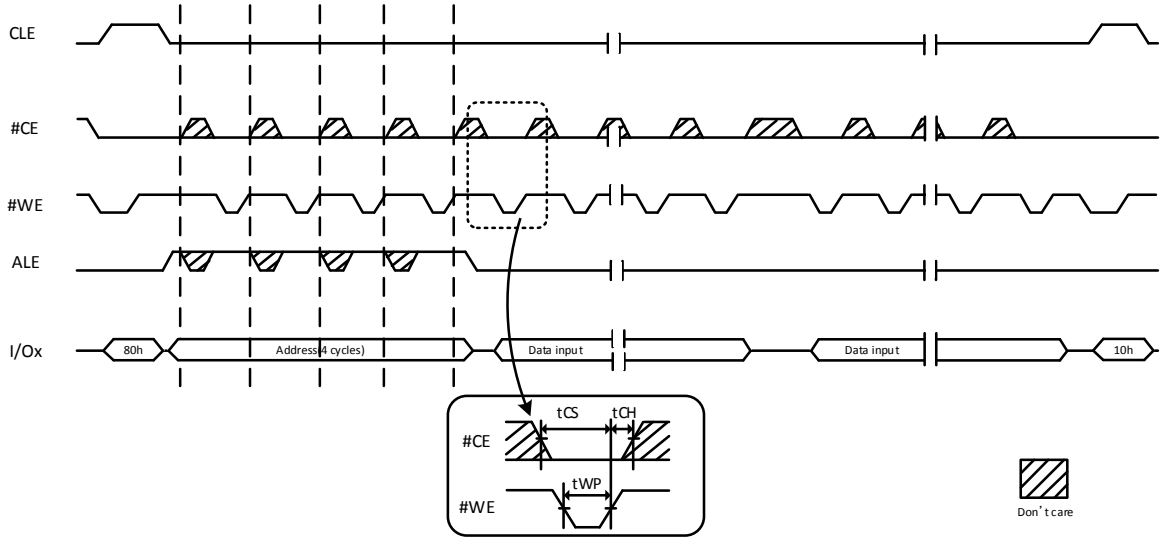

Figure 11-12 #CE Don't Care Page Program Operation

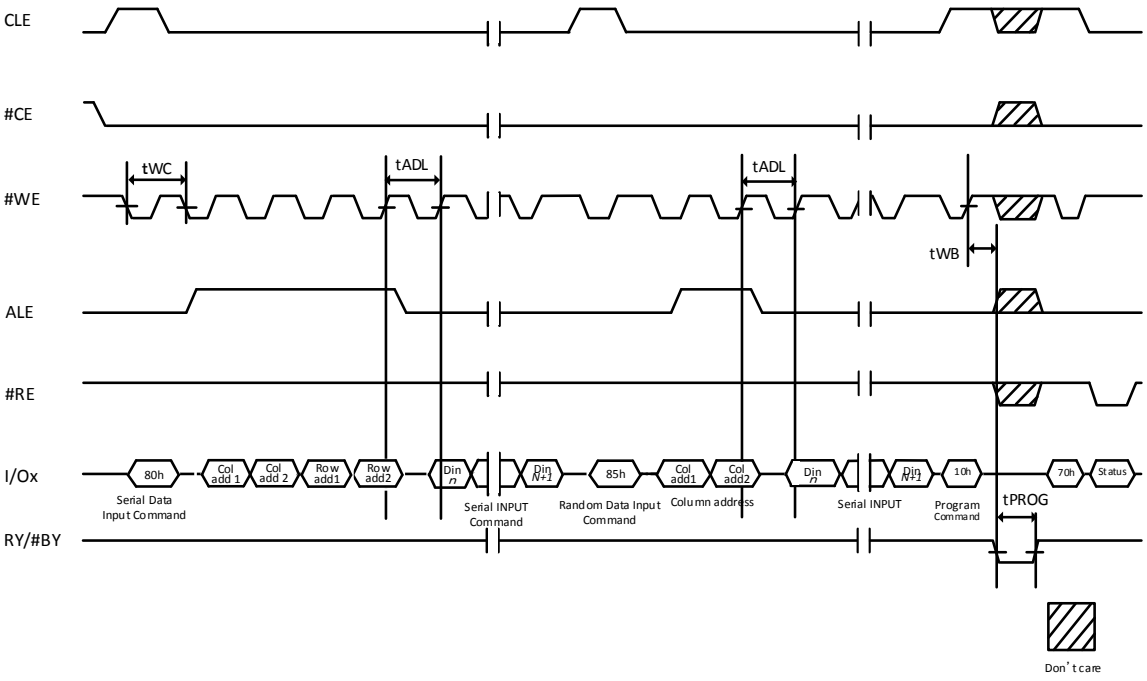

Figure 11-13 Page Program with Random Data Input

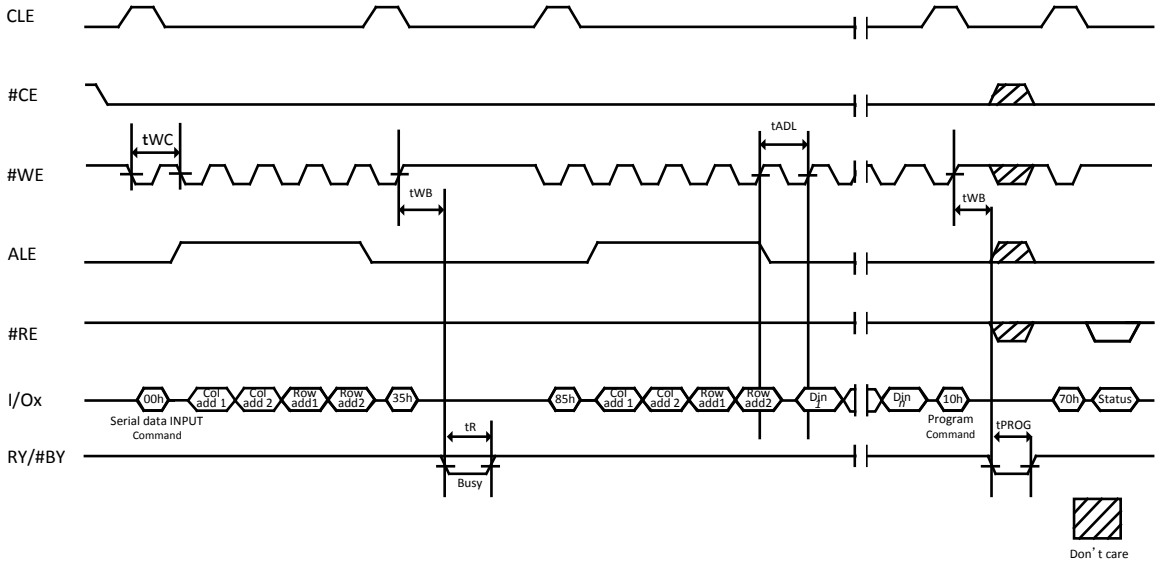

Figure 11-14 Copy Back

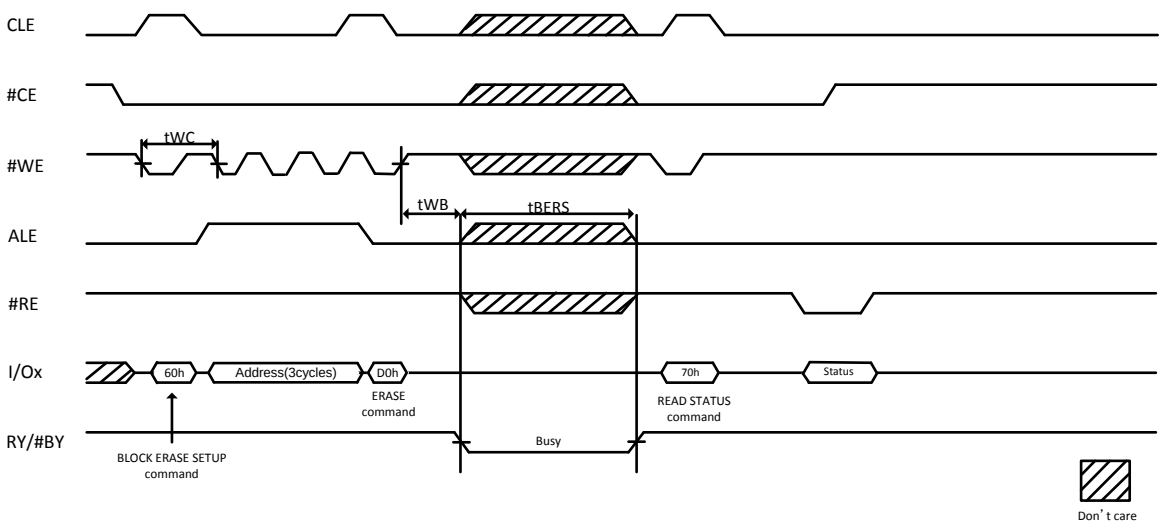

Figure 11-15 Block Erase

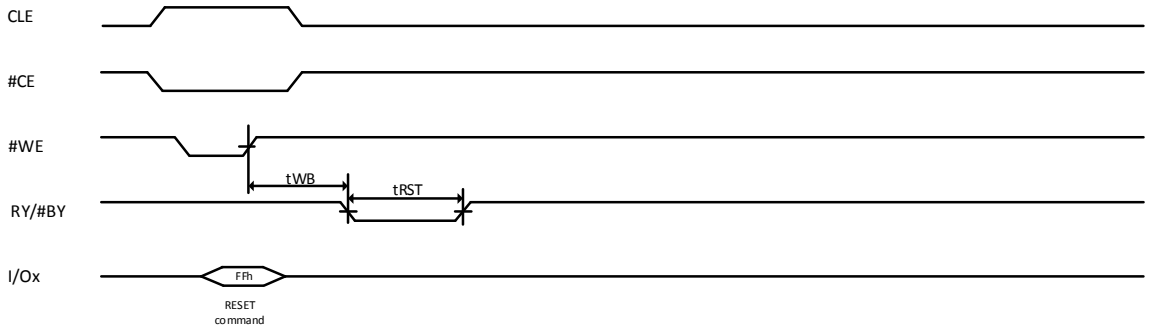

Figure 11-16 Reset

12. INVALID BLOCK MANAGEMENT

12.1 Invalid blocks

The W29N02GW/Z may have initial invalid blocks when it ships from factory. Also, additional invalid blocks may develop during the use of the device. Nvb represents the minimum number of valid blocks in the total number of available blocks (See Table 12.1). An invalid block is defined as blocks that contain one or more bad bits. Block 0, block address 00h is guaranteed to be a valid block at the time of shipment.

Parameter	Symbol	Min	Max	Unit
Valid block number	Nvb	2008	2048	blocks

Table 12-1 Valid Block Number

12.2 Initial invalid blocks

Initial invalid blocks are defined as blocks that contain one or more invalid bits when shipped from factory.

Although the device contains initial invalid blocks, a valid block of the device is of the same quality and reliability as all valid blocks in the device with reference to AC and DC specifications. The W29N02GW/Z has internal circuits to isolate each block from other blocks and therefore, the invalid blocks will not affect the performance of the entire device.

Before the device is shipped from the factory, it will be erased and invalid blocks are marked. All initial invalid blocks are marked with non-FFh at the first byte of spare area on the 1st or 2nd page. The initial invalid block information cannot be recovered if inadvertently erased. Therefore, software should be created to initially check for invalid blocks by reading the marked locations before performing any program or erase operation, and create a table of initial invalid blocks as following flow chart

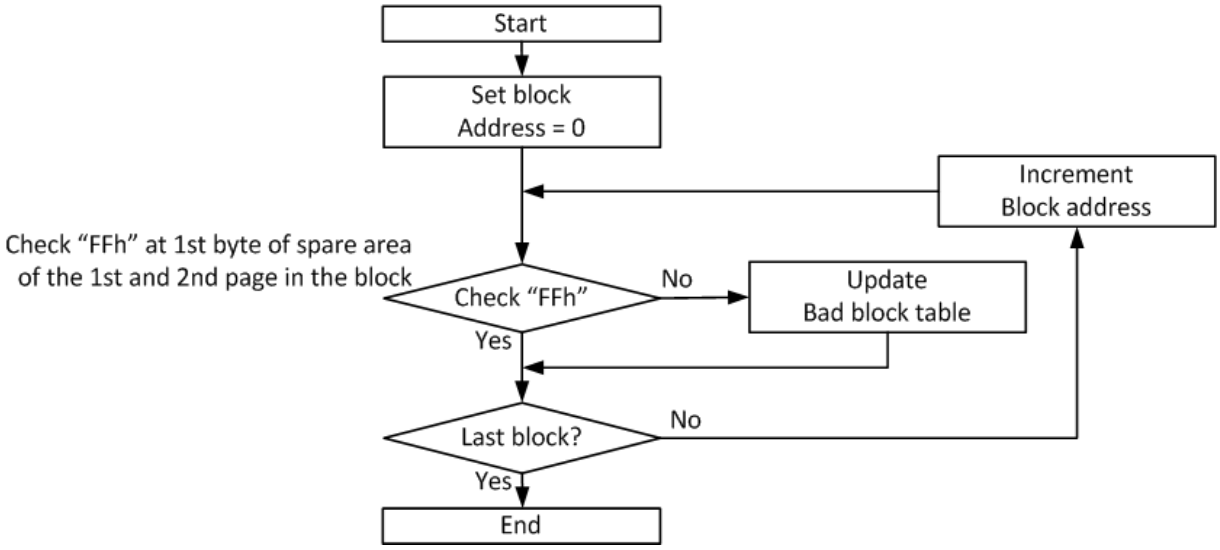

Figure 12-1 Flow chart of create initial invalid block table

12.3 Error in operation

Additional invalid blocks may develop in the device during its life cycle. Following the procedures herein is required to guarantee reliable data in the device.

After each program and erase operation, check the status read to determine if the operation failed. In case of failure, a block replacement should be done with a bad-block management algorithm. The system has to use a minimum 1-bit ECC per 528 bytes of data to ensure data recovery.

Operation	Detection and recommended procedure
Erase	Status read after erase → Block Replacement
Program	Status read after program → Block Replacement
Read	Verify ECC → ECC correction

Table 12-2 Block failure

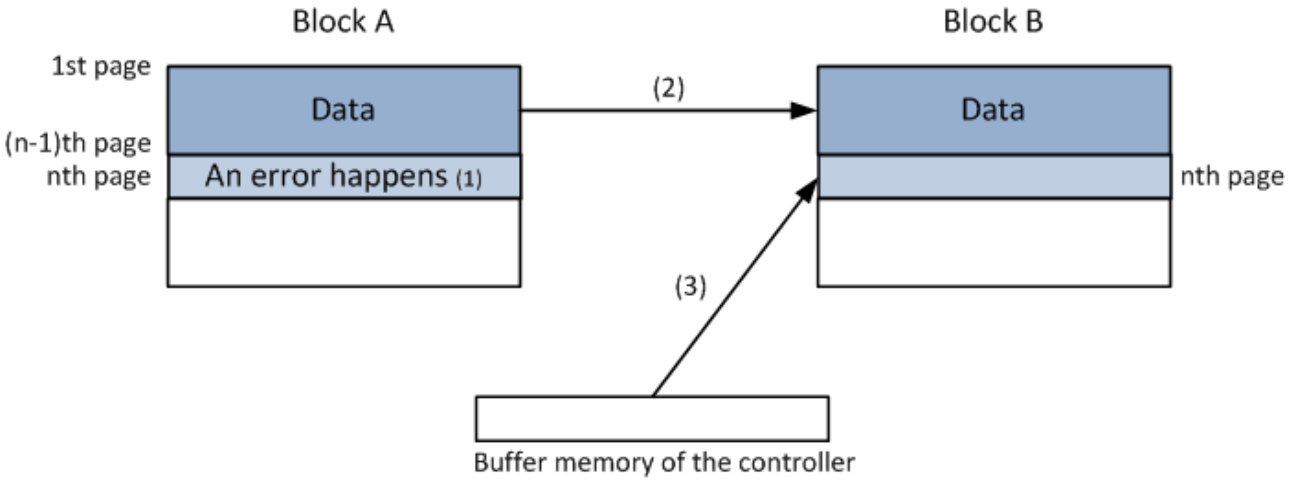

Figure 12-2 Bad block Replacement

Note:

1. **An error happens in the nth page of block A during program or erase operation.**
2. **Copy the data in block A to the same location of block B which is valid block.**
3. **Copy the nth page data of block A in the buffer memory to the nth page of block B**
4. **Creating or updating bad block table for preventing further program or erase to block A**

.

12.4 Addressing in program operation

The pages within the block have to be programmed sequentially from LSB (least significant bit) page to the MSB (most significant bit) within the block. The LSB is defined as the start page to program, does not need to be page 0 in the block. Random page programming is prohibited.

13. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
0.1	8/22/14		New Create as preliminary
0.2	10/23/14	77 79	Update POD Correct Valid Part Numbers
0.3	05/19/15		Remove Cache operation mode
	06/08/2015		Modified for MCP Datasheet.

Table 16-1 History Table

Preliminary Designation

The “Preliminary” designation on a *Winbond* datasheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *Winbond* or an authorized sales representative should be consulted for current information before using this product.

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winbond

LPDDR2 S-4B 1Gb

1. GENERAL DESCRIPTION

LPDDR2 is a high-speed SDRAM device internally configured as a 8-Bank memory.These devices contain 1 Gb has 1,073,741,824 bits.

All LPDDR2 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

For LPDDR2 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

2. FEATURES

- VDD1 = 1.7~1.95V
- VDD2/VDDCA/VDDQ = 1.14V ~ 1.30V
- Data width: x32
- Clock rate: up to 533MHz
- Four-bit prefetch DDR architecture
- Eight internal banks for concurrent operation
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- Per Bank Refresh
- Partial Array Self-Refresh(PASR)
- Deep Power Down Mode (DPD Mode)
- Programmable output buffer driver strength
- Data mask (DM) for write data
- Clock Stop capability during idle periods
- Double data rate for data output
- Differential clock inputs
- Bidirectional differential data strobe
- Interface: HSUL_12
- JEDEC LPDDR2-S4B compliance
- Support KGD (Known Good Die) form
- Operating Temperature Range

  Tj :

  -25 ~ 85 °C

  -40 ~ 85 °C

TABLE OF CONTENTS

4. PIN DESCRIPTION

4.1 Signal Description

Name	Type	Description
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions.CKE is considered part of the command code. CKE is sampled at the positive Clock edge.
CS_n	Input	Chip Select: CS_n is considered part of the command code and CS_n is sampled at the positive Clock edge.
CA[n:0]	Input	DDR Command/Address Inputs: Uni-directional command/address bus inputs. CA is considered part of the command code.
DQ[n:0]	I/O	Data Inputs/Output: Bi-directional data bus. n=15 for 16 bits DQ; n=31 for 32 bits DQ.
DQSn_t, DQSn_c	I/O	Data Strobe (Bi-directional, Differential): The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x32 DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31.
DMn	Input	Input Data Mask: DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS_c). DM0 is the input data mask signal for the data on DQ0-7. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
V_{DD1}	Supply	Core Power Supply 1: Power supply for core.
V_{DD2}	Supply	Core Power Supply 2: Power supply for core.
V_{DDCA}	Supply	Input Receiver Power Supply: Power supply for CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers.
V_{DDQ}	Supply	I/O Power Supply: Power supply for Data input/output buffers.
$V_{REF(CA)}$	Supply	Reference Voltage for CA Command and Control Input Receiver: Reference voltage for all CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers.
$V_{REF(DQ)}$	Supply	Reference Voltage for DQ Input Receiver: Reference voltage for all DQ input buffers: Reference voltage for all Data input buffers.
V_{SS}	Supply	Ground
V_{SSCA}	Supply	Ground for CA Input Receivers
V_{SSQ}	Supply	I/O Ground
ZQ	I/O	Reference Pin for Output Drive Strength Calibration
TQ (option)	Output	Temperature sensor output: Asynchronous, HSUL_12 level output. It is logic-HIGH when device temperature equals or exceeds 85°C. It is logic-LOW when device temperature is less than 85°C.The drive strength is same as DQ (40 ohm).
GOHIZ (option)	Input	Asynchronous, HSUL_12 level input. When logic High, all outputs of device are in Hi-Z state, when Low, device is in normal operation. When GOHIZ pad transitions from Low to High, all outputs will enter Hi-z within tgo-hiz. When GOHIZ pad transitions from High to Low, all outputs will return to normal function within texit-hiz. The tgo-hiz and texit-hiz are to be defined. Internal pulldown is implemented. E-fuse option is provided to change GOHIZ's polarity(from active HIGH to active Low).

Note : Data includes DQ and DM.

4.2 Addressing Table

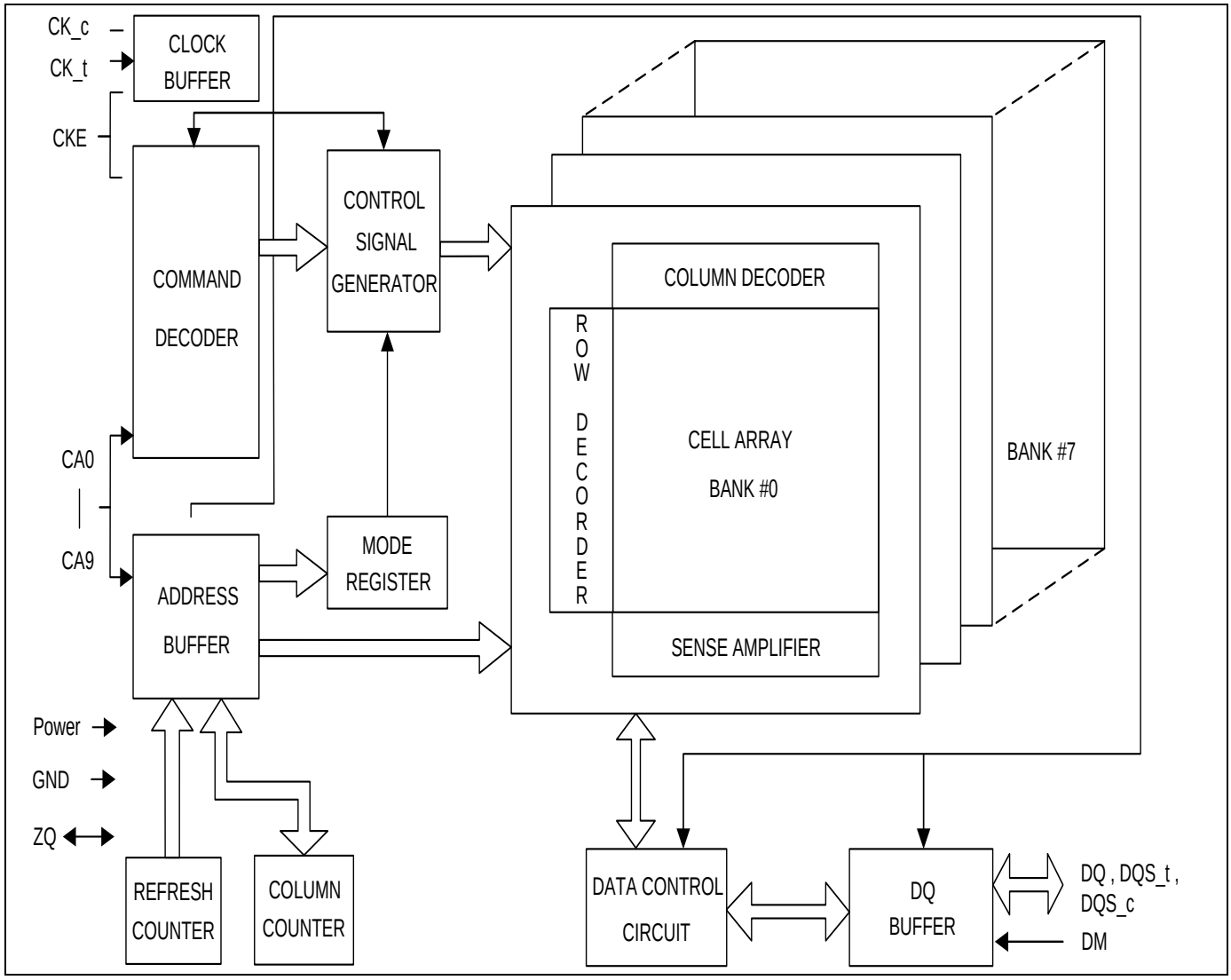
Density		1Gb
Number of Banks		8
Bank Addresses		BA0-BA2
tREFI(us) (*2)		7.8
X32	Row Addresses	R0-R12
	Column Addresses*1	C0-C8

Note 1.The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.

2. tREFI values for all bank refresh is Tj = -40~85°C.

3. Row and Column Address values on the CA bus that are not used are “don’t care.”

5. BLOCK DIAGRAM



6. FUNCTIONAL DESCRIPTION

LPDDR2-S4 devices use a double data rate architecture on the DQ pins to achieve highspeed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

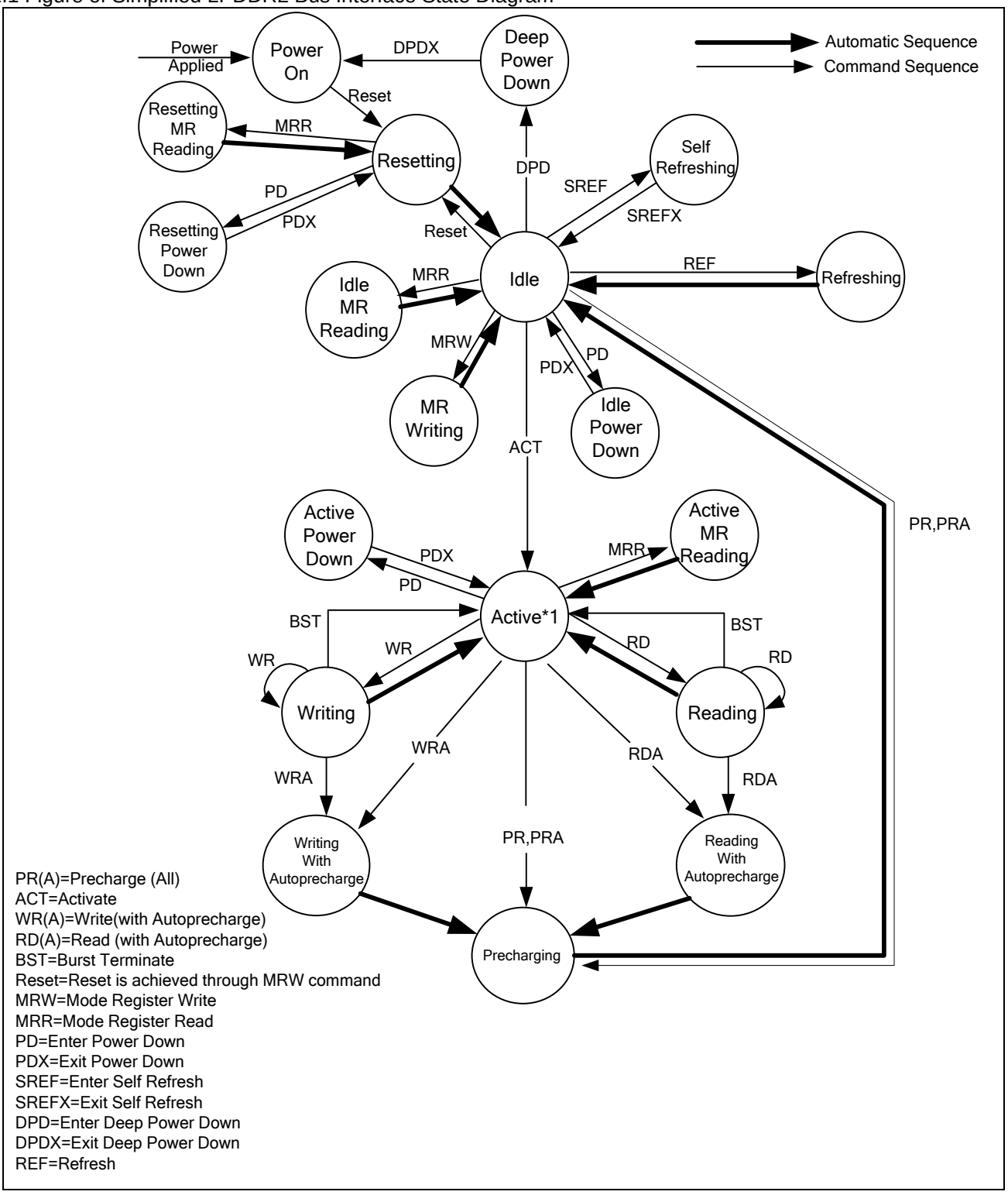
Prior to normal operation, the LPDDR2 device must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

6.1 Simplified LPDDR2 State Diagram

LPDDR2-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

6.1.1 Figure of Simplified LPDDR2 Bus Interface State Diagram



Note : For LPDDR2-SDRAM in the Idle state, all banks are precharged

6.2 Power-up, Initialization, and Power-Off

The LPDDR2 Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

6.2.1 Power Ramp and Device Initialization

The following sequence shall be used to power up an LPDDR2 device. Unless specified otherwise, these steps are mandatory.

1. Power Ramp

While applying power (after Ta), CKE shall be held at a logic low level (=<0.2xVDDCA), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

On or before the completion of the power ramp (Tb) CKE must be held low.

DQ, DM, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latchup. CK_t, CK_c, CS_n, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up.

The following conditions apply:

Ta is the point where any power supply first reaches 300mV.

After Ta is reached, VDD1 must be greater than VDD2 - 200mV.

After Ta is reached, VDD1 and VDD2 must be greater than VDDCA - 200mV.

After Ta is reached, VDD1 and VDD2 must be greater than VDDQ - 200mV.

After Ta is reached, VREF must always be less than all other supply voltages.

The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100mV.

The above conditions apply between Ta and power-off (controlled or uncontrolled).

Tb is the point when all supply voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.

Power ramp duration tINIT0 (Tb - Ta) must be no greater than 20 ms.

2. CKE and clock

Beginning at Tb, CKE must remain low for at least tINIT1 = 100 ns, after which it may be asserted high. Clock must be stable at least tINIT2 = 5 x tCK prior to the first low to high transition of CKE (Tc). CKE, CS_n and CA inputs must observe setup and hold time (tIS, tIH) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

The clock period shall be within the range defined for tCKb (18 ns to 100 ns), if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met. Furthermore, some AC parameters (e.g. tDQSCK) may have relaxed timings (e.g. tDQSCKb) before the system is appropriately configured.

While keeping CKE high, issue NOP commands for at least tINIT3 = 200 us. (Td).

3. Reset command

After tINIT3 is satisfied, a MRW(Reset) command shall be issued (Td). The memory controller may optionally issue a Precharge-All command prior to the MRW Reset command. Wait for at least tINIT4 = 1 µs while keeping CKE asserted and issuing NOP commands.

4. Mode Registers Reads and Device Auto-Initialization (DAI) polling:

After tINIT4 is satisfied (Te) only MRR commands and power-down entry/exit commands are allowed. Therefore, after Te, CKE may go low in accordance to Power-Down entry and exit specification.

The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of tINIT5 before proceeding.

As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.

After the DAI-bit (MR#0, “DAI”) is set to zero “DAI complete“ by the memory device, the device is in idle state (Tf). The state of the DAI status bit can be determined by an MRR command to MR#0.

The LPDDR2 SDRAM device will set the DAI-bit no later than tINIT5 (10 us) after the Reset command. The memory controller shall wait a minimum of tINIT5 or until the DAI-bit is set before proceeding.

After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 “Device Information” etc.).

5. ZQ Calibration:

After tINIT5 (Tf), an MRW ZQ Initialization Calibration command may be issued to the memory. This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature variations. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after tZQINIT.

6. Normal Operation:

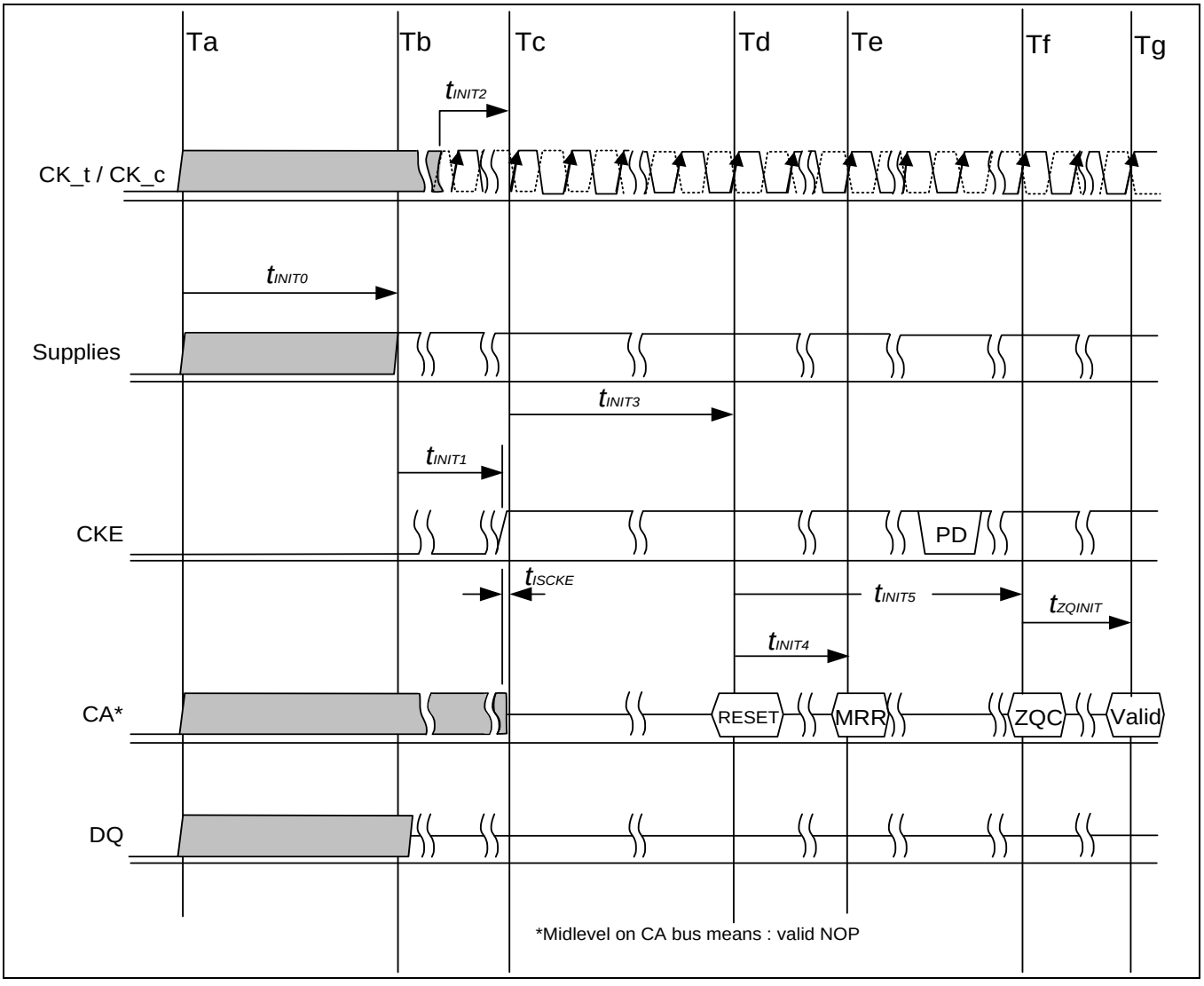
After tZQINIT (Tg), MRW commands may be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration. The LPDDR2 device will now be in IDLE state and ready for any valid command.

After Tg, the clock frequency may be changed according to the clock frequency change procedure.

6.2.2 Timing Parameters for initialization

Symbol	Value		Unit	Comment
	min	max		
tINIT0		20	ms	Maximum Power Ramp Time
tINIT1	100		ns	Minimum CKE low time after completion of power ramp
tINIT2	5		tCK	Minimum stable clock before first CKE high
tINIT3	200		µs	Minimum Idle time after first CKE assertion
tINIT4	1		µs	Minimum Idle time after Reset command
tINIT5		10	µs	Maximum duration of Device Auto-Initialization
tZQINIT	1		µs	ZQ Initial Calibration for LPDDR2-S4
tCKb	18	100	ns	Clock cycle time during boot

6.2.3 Figure of Power Ramp and Initialization Sequence



6.2.4 Initialization after Reset (without Power ramp)

If the RESET command is issued outside the power up initialization sequence, the reinitialization procedure shall begin with step 3 (Td).

6.2.5 Power-off Sequence

The following sequence shall be used to power off the LPDDR2 device.

While removing power, CKE shall be held at a logic low level (=< 0.2 x VDDCA), all other inputs shall be between VILmin and VIHmax. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

DQ, DM, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during power off sequence to avoid latch-up. CK_t, CK_c, CS_n and CA input levels must be between VSSCA and VDDCA during power off sequence to avoid latch-up.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table.

Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.

The time between Tx and Tz (tPOFF) shall be less than 2s.

The following conditions apply:

Between Tx and Tz, VDD1 must be greater than VDD2 - 200 mV.

Between Tx and Tz, VDD1 and VDD2 must be greater than VDDCA - 200 mV.

Between Tx and Tz, VDD1 and VDD2 must be greater than VDDQ - 200 mV.

Between Tx and Tz, VREF must always be less than all other supply voltages.

The voltage difference between any of VSS, VSSQ, and VSSCA pins may not exceed 100 mV.

6.2.6 Timing Parameters Power-Off

Symbol	Value		Unit	Comment
	min	max		
tPOFF		2	s	Maximum Power-Off Ramp Time

6.2.7 Uncontrolled Power-Off Sequence

The following sequence shall be used to power off the LPDDR2 device under uncontrolled condition.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.

Tz is the point where all power supply first reaches 300 mV. After Tz, the device is powered off.

The time between Tx and Tz shall be less than 2s. The relative level between supply voltages are uncontrolled during this period.

VDD1 and VDD2 shall decrease with a slope lower than 0.5 V/us between Tx and Tz.

Uncontrolled power off sequence can be applied only up to 400 times in the life of the device.

6.3 Mode Register Definition

6.3.1 Mode Register Assignment and Definition

Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written.

Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

6.3.1.1 Table of Mode Register Assignment

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0	Link
0	00_H	Device Info.	R	(RFU)			RZQI		DNVI	DI	DAI	go to MR0
1	01_H	Device Feature 1	W	nWR (for AP)			WC	BT	BL			go to MR1
2	02_H	Device Feature 2	W	(RFU)				RL & WL				go to MR2
3	03_H	I/O Config-1	W	(RFU)				DS				go to MR3
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate			go to MR4
5	05_H	Basic Config-1	R	LPDDR2 Manufacturer ID								go to MR5
6	06_H	Basic Config-2	R	Revision ID1								go to MR6
7	07_H	Basic Config-3	R	Revision ID2								go to MR7
8	08_H	Basic Config-4	R	I/O width		Density				Type		go to MR8
9	09_H	Test Mode	W	Vendor-Specific Test Mode								go to MR9
10	$0A_H$	I/O Calibration	W	Calibration Code								go to MR10
11-15	$0B_H$~$0F_H$	(reserved)	-	(RFU)								
16	10_H	PASR_Bank	W	Bank Mask								go to MR16
17	11_H	PASR_Seg	W	Segment Mask								go to MR17
18-19	12_H~13_H	(Reserved)	-	(RFU)								
20-31	14h – 1Fh	Reserved for NVM										
32	20H	DQ Calibration Pattern A	R	See “DQ Calibration”								go to MR32
33-39	21_H~27_H	(Do Not Use)	-									
40	28H	DQ Calibration Pattern B	R	See “DQ Calibration”								go to MR40
41-47	29_H~$2F_H$	(Do Not Use)	-									
48-62	30_H~$3E_H$	(Reserved)	-	(RFU)								
63	3FH	Reset	W	X								go to MR63
64-126	40_H~$7E_H$	(Reserved)	-	(RFU)								
127	7FH	(Do Not Use)	-									
128-190	80H~BE_H	(Reserved for Vendor Use)	-	(RFU)								
191	BFH	(Do Not Use)	-									
192-254	$C0_H$~FE_H	(Reserved for Vendor Use)	-	(RFU)								
255	FFH	(Do Not Use)	-									

Note 1. RFU bits shall be set to ‘0’ during Mode Register writes.
2. RFU bits shall be read as ‘0’ during Mode Register reads.
3. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impact on the functionality of the device.

6.3.2 MR0_Device Information (MA[7:0] = 00H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)			RZQI		DNVI	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	0_b: DAI complete 1_b: DAI still in progress
DI (Device Information)	Read-only	OP1	0_b: SDRAM 1_b: NVM
DNVI (Data Not Valid Information)	Read-only	OP2	LPDDR2 SDRAM will not implement DNV functionalit
RZQI (Built in Self Test for RZQ Information)	Read-only	OP[4:3]	00b: RZQ self test not executed. 01b: ZQ-pin may connect to VDDCA or float 10b: ZQ-pin may short to GND 11b: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)

Note 1. RZQI will be set upon completion of the MRW ZQ Initialization Calibration command.
2.If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 4), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240-ohm +/-1%).

6.3.3 MR1_Device Feature 1 (MA[7:0] = 01H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write-only	OP[2:0]	010_b: BL4 (default) 011_b: BL8 100_b: BL16 All others: reserved	
BT	Write-only	OP3	0_b: Sequential (default) 1_b: Interleaved	
WC	Write-only	OP4	0_b: Wrap (default) 1 $_b$: No wrap (allowed for SDRAM BL4 only)	
nWR	Write-only	OP[7:5]	001_b nWR=3 (default) 010_b: nWR=4 011b: nWR=5 100_b: nWR=6 101_b: nWR=7 110_b: nWR=8 All others: reserved	1

Note 1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

6.3.3.1 1 Table of Burst Sequence by Burst Length (BL), Burst Type (BT), and Warp Control (WC)

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	0_b	0_b	wrap	any	4	0	1	2	3												
X	X	1_b	0_b				2	3	0	1												
X	X	X	0_b	nw	any		y	y+1	y+2	y+3												
X	0_b	0_b	0_b	wrap	seq	8	0	1	2	3	4	5	6	7								
X	0_b	1_b	0_b				2	3	4	5	6	7	0	1								
X	1_b	0_b	0_b				4	5	6	7	0	1	2	3								
X	1_b	1_b	0_b				6	7	0	1	2	3	4	5								
X	0_b	0_b	0_b		int		0	1	2	3	4	5	6	7								
X	0_b	1_b	0_b				2	3	0	1	6	7	4	5								
X	1_b	0_b	0_b				4	5	6	7	0	1	2	3								
X	1_b	1_b	0_b				6	7	4	5	2	3	0	1								
X	X	X	0_b	nw	any		illegal (not allowed)															
0_b	0_b	0_b	0_b	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0_b	0_b	1_b	0_b				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0_b	1_b	0_b	0_b				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0_b	1_b	1_b	0_b				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1_b	0_b	0_b	0_b				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1_b	0_b	1_b	0_b				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1_b	1_b	0_b	0_b				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1_b	1_b	1_b	0_b				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
X	X	X	0_b		int		illegal (not allowed)															
X	X	X	0_b	nw	any		illegal (not allowed)															

Note:1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C[1: 0].
3. For BL=8, the burst address represents C[2:0].
4. For BL=16, the burst address represents C[3:0].
5. For no-wrap (nw), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary. The variable y may start at any address with C0 equal to 0 and may not start at any address in table below for the respective density and bus width combinations.

6.3.3.2 Table of Non Wrap Restrictions

Bus Width	1Gb
Not across full page boundary	
x32	1FE, 1FF, 000, 001
Not across sub page boundary	
X32	None

Note : Non-wrap BL=4 data-orders shown above are prohibited.

6.3.4 MR2_Device Feature 2 (MA[7:0] = 02H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

RL & WL	Write-only	OP[3:0]	0001b: RL = 3 / WL = 1 (default) 0010b: RL = 4 / WL = 2 0011b: RL = 5 / WL = 2 0100b: RL = 6 / WL = 3 0101b: RL = 7 / WL = 4 0110b: RL = 8 / WL = 4 All others: reserved

.

6.3.5 MR3_I/O Configuration 1 (MA[7:0] = 03H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP[3:0]	0000_b: reserved 0001_b: 34.3-ohm typical 0010_b: 40-ohm typical (default) 0011_b: 48-ohm typical 0100_b: 60-ohm typical 0101_b: reserved for 68.6-ohm typical 0110_b: 80-ohm typical 0111_b: 120-ohm typical All others: reserved

6.3.6 MR4_Device Temperature (MA[7:0] = 04H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		

SDRAM Refresh Rate	Read-only	OP[2:0]	000_b: SDRAM Low temperature operating limit exceeded 001b: 4x tREFI, 4x tREFIpb, 4x tREFW 010_b: 2x tREFI, 2x tREFIpb, 2x tREFW 011_b: 1x tREFI, 1x tREFIpb, 1x tREFW (<=85°C) 100_b: Reserved 101_b: 0.25x tREFI, 0.25x tREFIpb, 0.25x tREFW, do not de-rate SDRAM AC timing 110_b: 0.25x tREFI, 0.25x tREFIpb, 0.25x tREFW, de-rate SDRAM AC timing 111_b: SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP7	0_b: OP[2:0] value has not changed since last read of MR4 . 1_b: OP[2:0] value has changed since last read of MR4.

Note 1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up
3. If OP2 equals '1', the device temperature is greater than 85'C
4. OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
5. LPDDR2 might not operate properly when OP[2:0] = 000b or 111b.
6. LPDDR2 devices must be derated by adding 1.875ns to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating value in AC timing table. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
7. The recommended frequency for reading MR4 is provided in Temperature Sensor

6.3.7 MR5_Basic Configuration 1 (MA[7:0] = 05H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							

LPDDR2 Manufacturer ID	Read-only	OP[7:0]	0000 1000b : Winbond

6.3.8 MR6_Basic Configuration 2 (MA[7:0] = 06H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP[7:0]	00000000b: A-version

6.3.9 MR7_Basic Configuration 3 (MA[7:0] = 07H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP[7:0]	00000000b: A-version

6.3.10 MR8_Basic Configuration 4 (MA[7:0] = 08H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP[1:0]	00_b: S4 SDRAM
Density	Read-only	OP[5:2]	0100_b: 1Gb
I/O width	Read-only	OP[7:6]	00_b: x32

6.3.11 MR9_Test Mode (MA[7:0] = 09H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

6.3.12 MR10_Calibration (MA[7:0] = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write-only	OP[7:0]	0xFF: Calibration command after initialization 0xAB: Long calibration 0x56: Short calibration 0xC3: ZQ Reset others: Reserved

Note: 1. Host processor shall not write MR10 with “Reserved” values
2. LPDDR2 devices shall ignore calibration command when a “Reserved” value is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function or default calibration (through the ZQreset command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
5. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connec-tion.

6.3.13 MR16_PASR_Bank Mask (MA[7:0] = 10H)

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
S4 SDRAM	Bank Mask (8-bank)							

Bank [7:0] Mask	Write-only	OP[7:0]	0b: refresh enable to the bank (=unmasked, default) 1b: refresh blocked (=masked)

OP	Bank Mask	8-Bank S4 SDRAM
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3
4	XXX1XXXX	Bank 4
5	XX1XXXXX	Bank 5
6	X1XXXXXX	Bank 6
7	1XXXXXXX	Bank 7

6.3.14 MR17_PASR_Segment Mask (MA[7:0] = 11H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

Segment [7:0] Mask	Write-only	OP[7:0]	0b: refresh enable to the segment (=unmasked, default) 1b: refresh blocked (=masked)

Segment	OP	Segment Mask	R[12:10]
0	0	XXXXXXX1	000b
1	1	XXXXXX1X	001b
2	2	XXXXX1XX	010b
3	3	XXXX1XXX	011b
4	4	XXX1XXXX	100b
5	5	XX1XXXXX	101b
6	6	X1XXXXXX	110b
7	7	1XXXXXXX	111b

6.3.15 MR32_DQ Calibration Pattern A (MA[7:0] = 20H)
Reads to MR32 return DQ Calibration Pattern “A”. See “DQ Calibration”.

6.3.16 MR40_DQ Calibration Pattern B (MA[7:0] = 28H)
Reads to MR40 return DQ Calibration Pattern “B”. See “DQ Calibration”.

6.3.17 MR63_Reset (MA[7:0] = 3FH): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

For additonal information on MRW RESET see “Mode Register Write Command”.

6.4 Command Definitions and Timing Diagram

6.4.1 LPDDR2-S4: Activate Command .

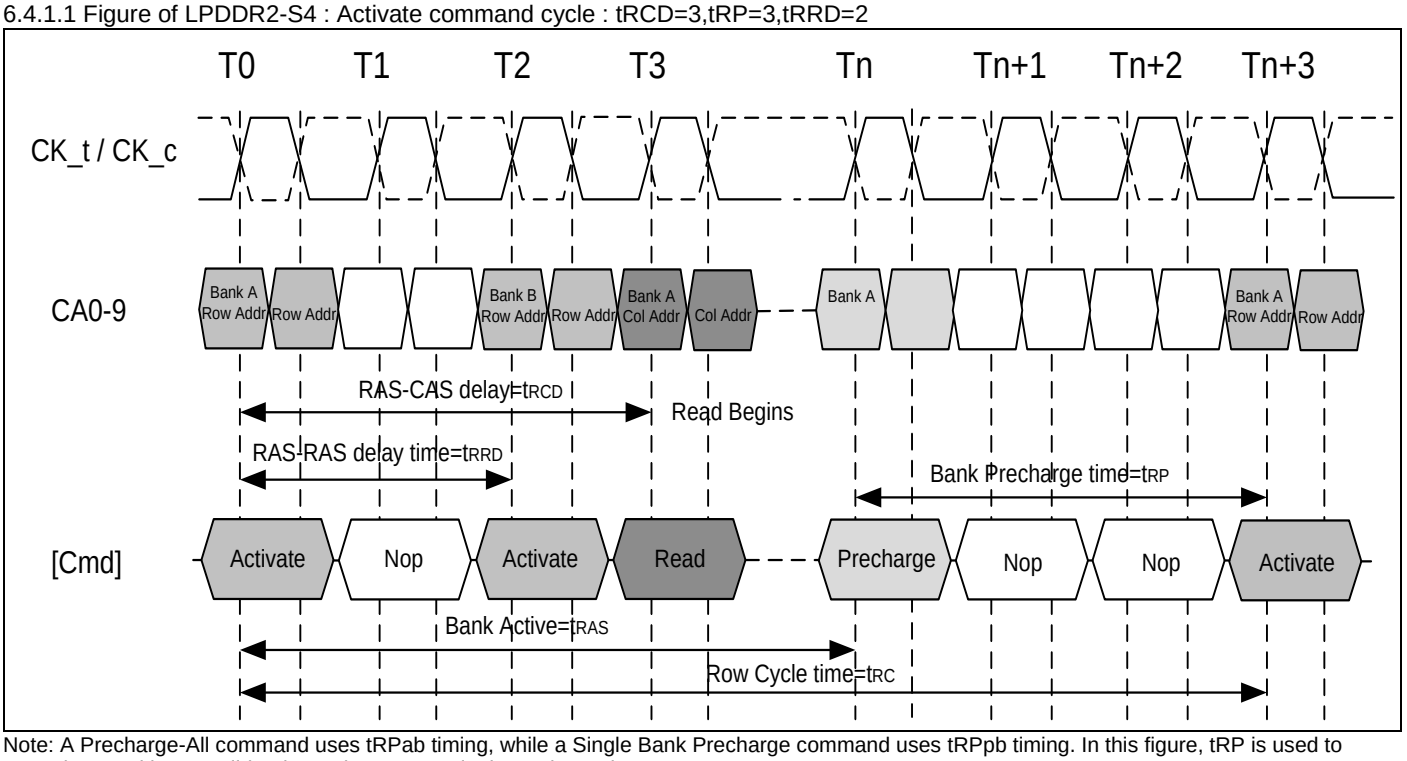
The SDRAM Activate command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses are used to select the desired bank. The row addresses are used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The LPDDR2 SDRAM can accept a read or write command at time tRCD after the activate command is sent. Once a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between Activate commands to different banks is tRRD.

Certain restrictions on operation of the 8-bank devices must be observed. There are two rules. One for restricting the number of sequential Activate commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

8-bank device Sequential Bank Activation Restriction : No more than 4 banks may be activated (or refreshed, in the case of REFpb) in a rolling tFAW window. Converting to clocks is done by dividing tFAW[ns] by tCK[ns], and rounding up to next integer value. As an example of the rolling window, if RU{ (tFAW / tCK) } is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9. REFpb also counts as bank-activation for the purposes of tFAW.

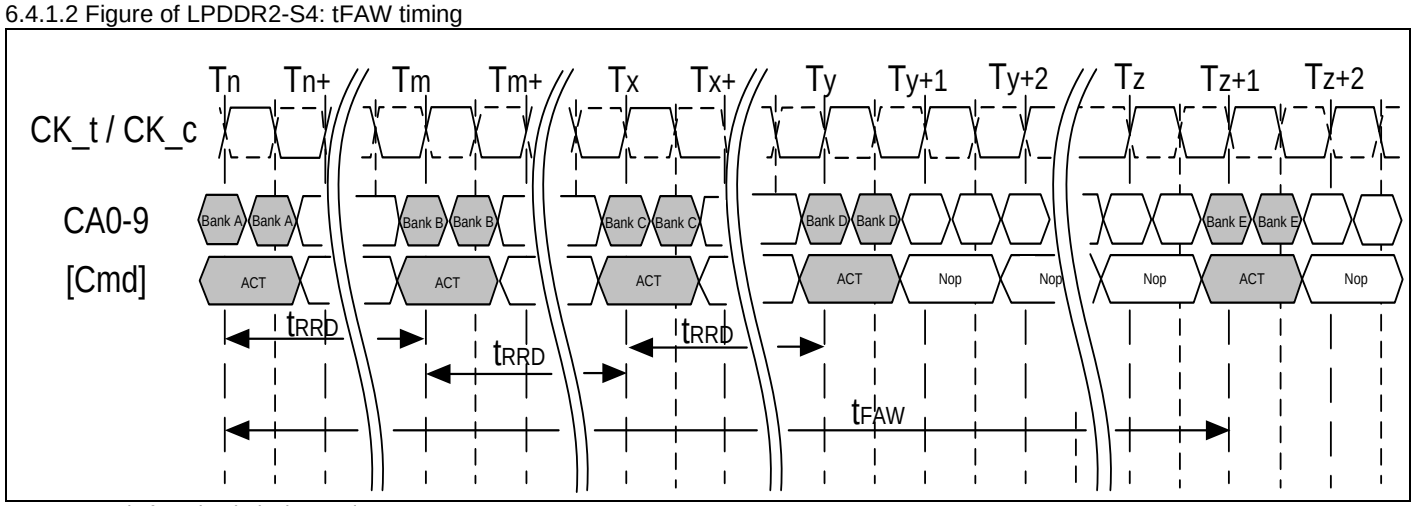
8-bank device Precharge All Allowance : tRP for a Precharge All command for an 8-bank device shall equal tRPab, which is greater than tRPpb.

6.4.1.1 Figure of LPDDR2-S4 : Activate command cycle : tRCD=3,tRP=3,tRRD=2



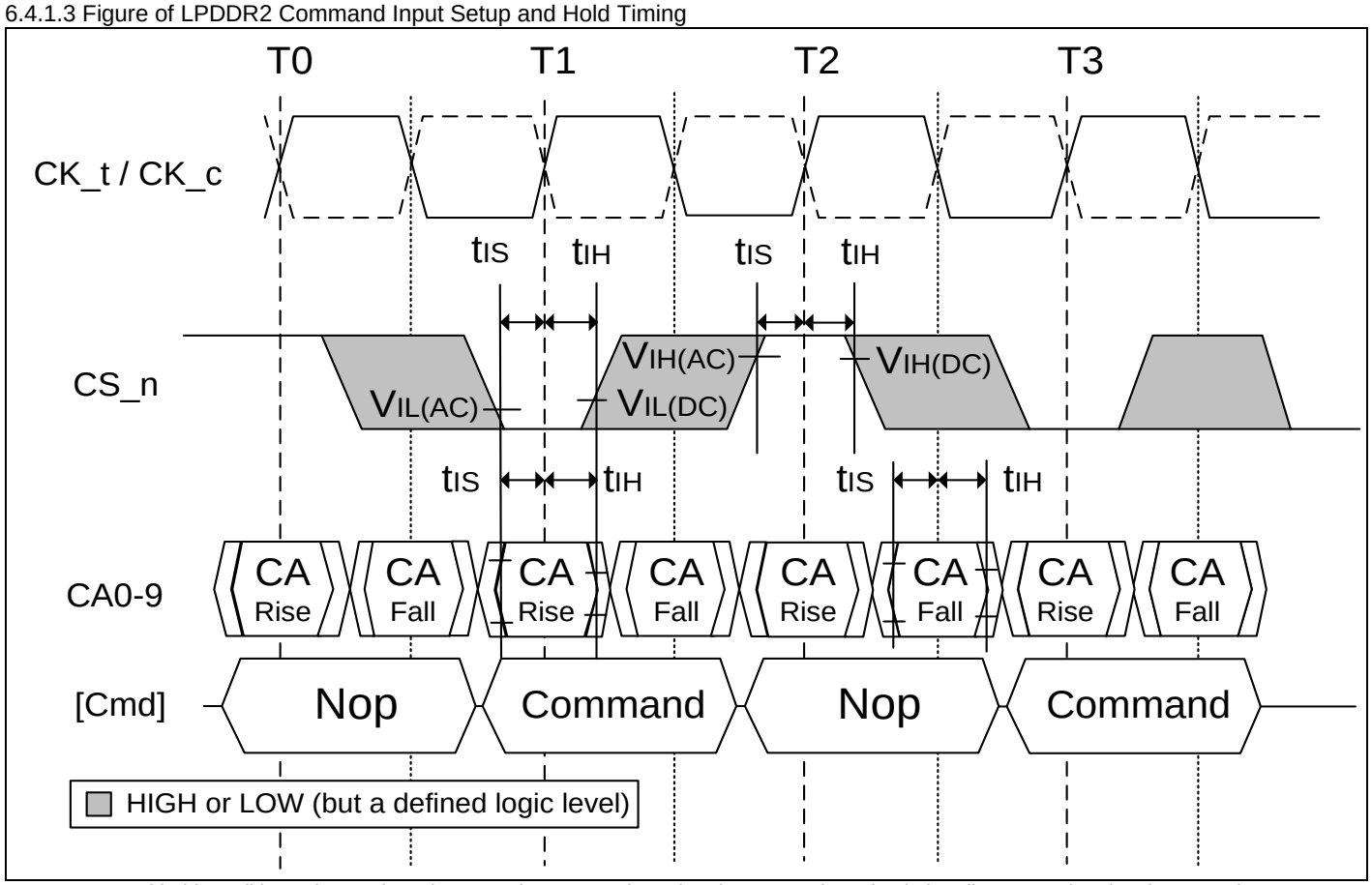
Note: A Precharge-All command uses tRPab timing, while a Single Bank Precharge command uses tRPpb timing. In this figure, tRP is used to denote either an All-bank Precharge or a Single Bank Precharge

6.4.1.2 Figure of LPDDR2-S4: tFAW timing



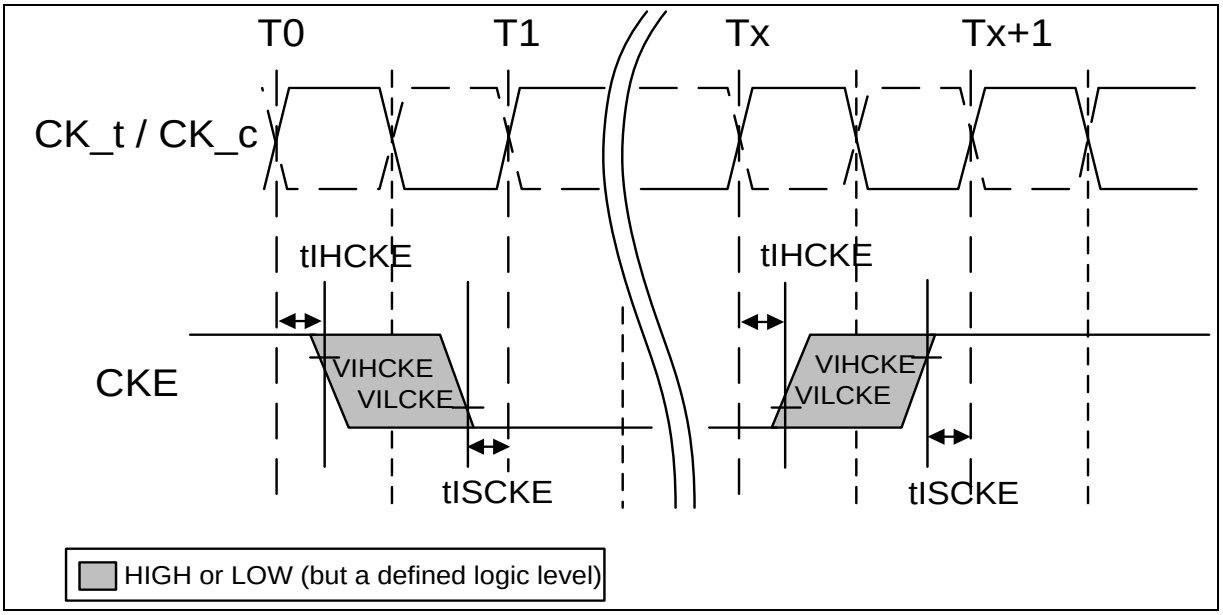
Note : tFAW is for 8-bank devices only.

6.4.1.3 Figure of LPDDR2 Command Input Setup and Hold Timing



Note: Setup and hold conditions also apply to the CKE pin. See section related to power down for timing diagrams related to the CKE pin.

6.4.1.4 Figure of LPDDR2 CKE Input Setup and Hold Timing



Note: 1.After CKE is registered LOW, CKE signal level shall be maintained below VILCKE for tCKE specification (LOW pulse width).
2.After CKE is registered HIGH, CKE signal level shall be maintained above VIHCKE for tCKE specification (HIGH pulse width)

6.4.2 LPDDR2-S4: Read and Write access modes

After a bank has been activated, a read or write cycle can be executed. This is accomplished by setting CS_n LOW, CA0 HIGH, and CA1 LOW at the rising edge of the clock. CA2 must also be defined at this time to determine whether the access cycle is a READ operation (CA2 HIGH) or a WRITE operation (CA2 LOW).

The LPDDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a burst read or write operation on successive clock cycles.

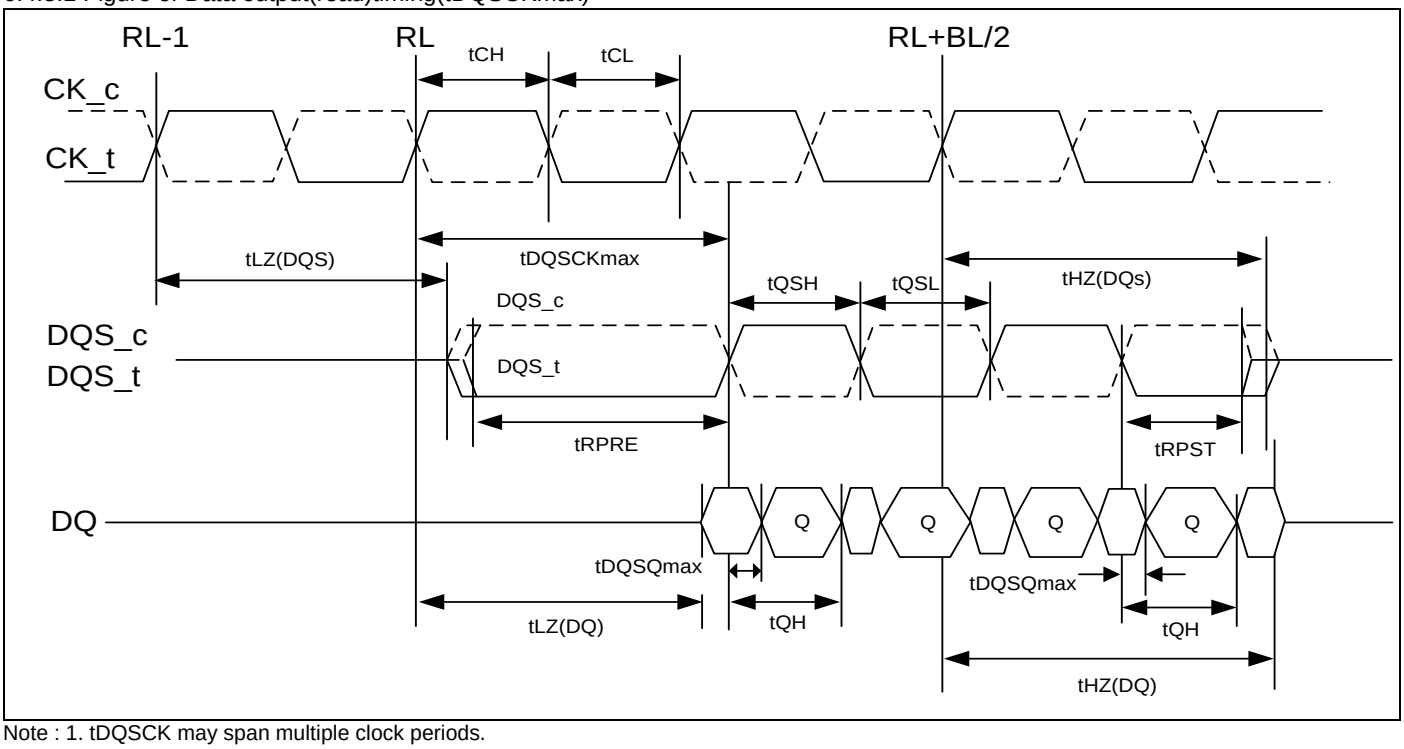
For LPDDR2-S4 devices, a new burst access must not interrupt the previous 4-bit burst operation in case of BL = 4 setting. In case of BL = 8 and BL = 16 settings, Reads may be interrupted by Reads and Writes may be interrupted by Writes provided that this occurs on even clock cycles after the Read or Write command and tCCD is met.

6.4.3 Burst Read command

The Burst Read command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 HIGH at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Read Latency (RL) is defined from the rising edge of the clock on which the Read Command is issued to the rising edge of the clock from which the tDQSCK delay is measured. The first valid datum is available RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Read Command is issued. The data strobe output is driven LOW tRPRE before the first rising valid strobe edge. The first bit of the burst is synchronized with the first rising edge of the data strobe. Each subsequent data-out appears on each DQ pin edge aligned with the data strobe. The RL is programmed in the mode registers.

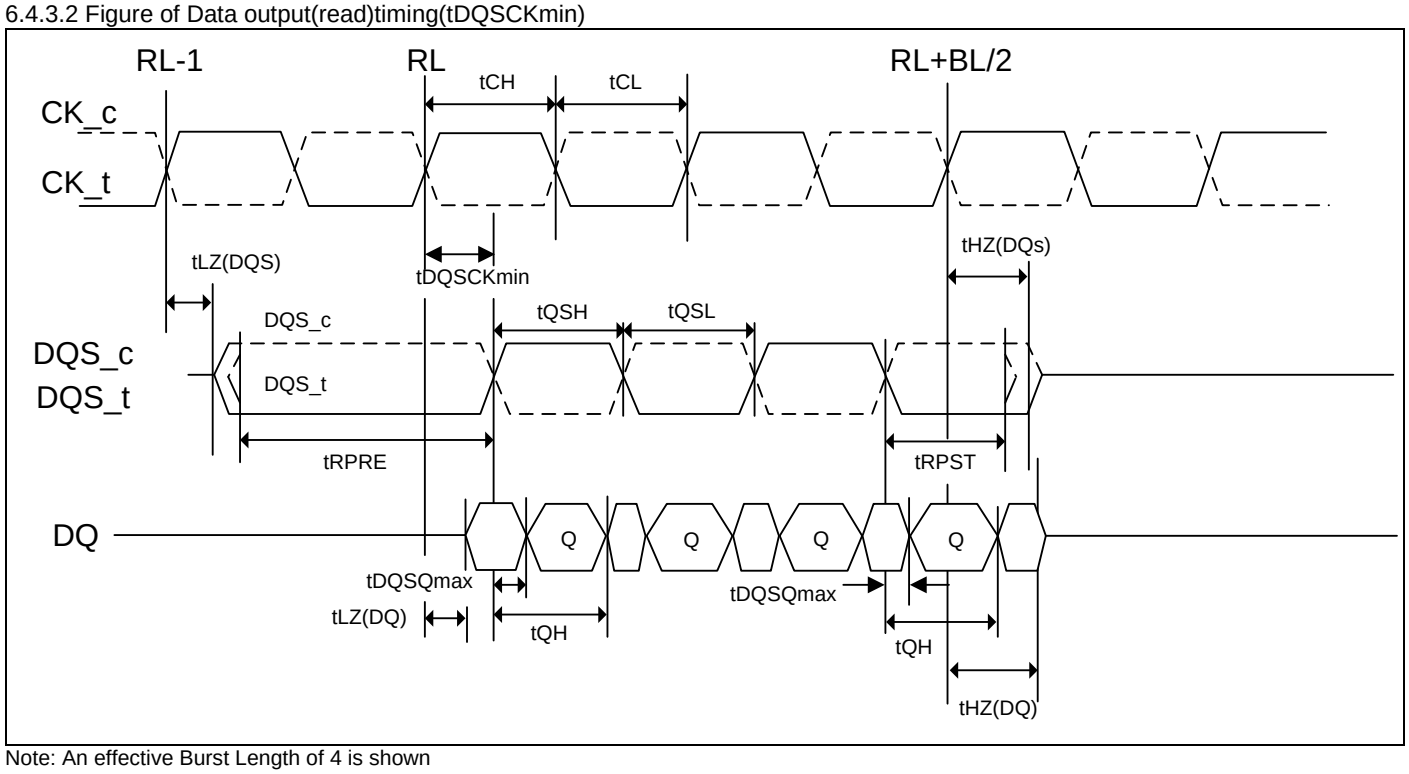
Timings for the data strobe are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

6.4.3.1 Figure of Data output(read)timing(tDQSCKmax)



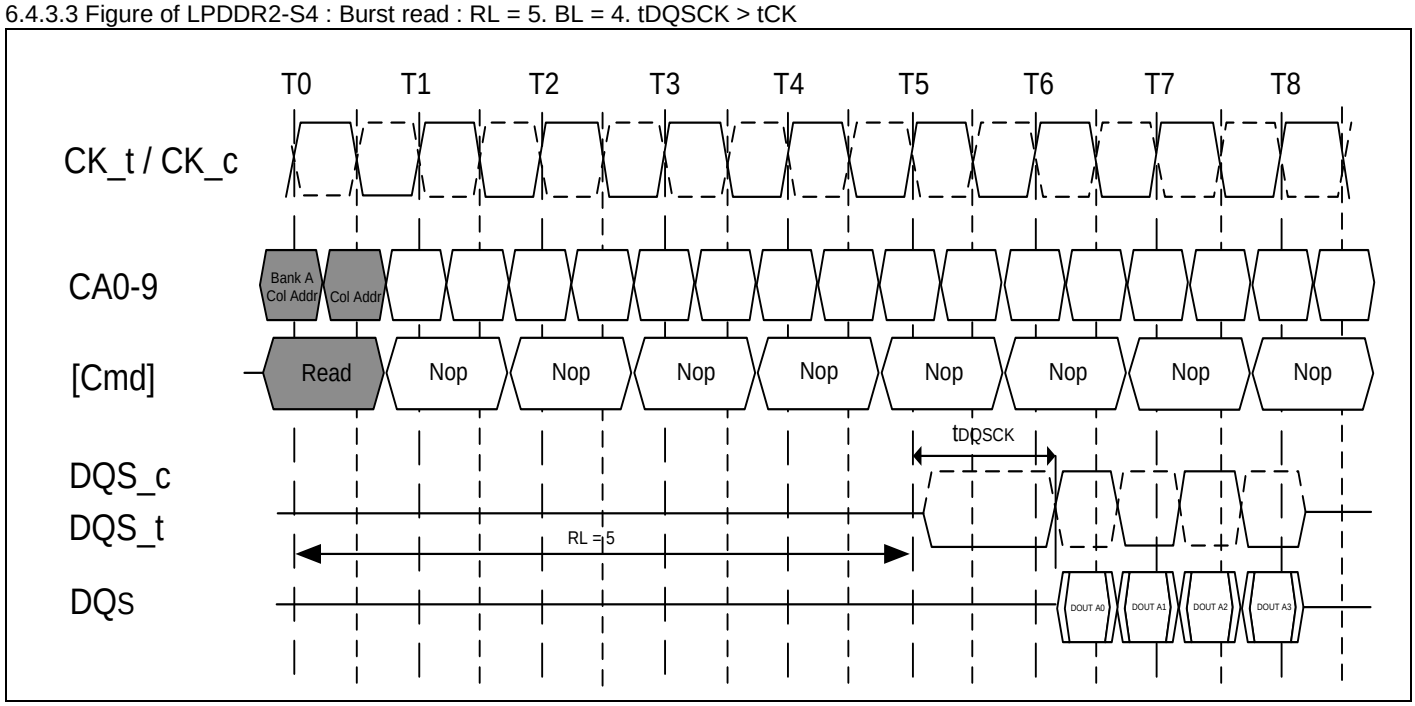
Note : 1. tDQSCK may span multiple clock periods.
2. An effective Burst Length of 4 is shown

6.4.3.2 Figure of Data output(read)timing(tDQSCKmin)

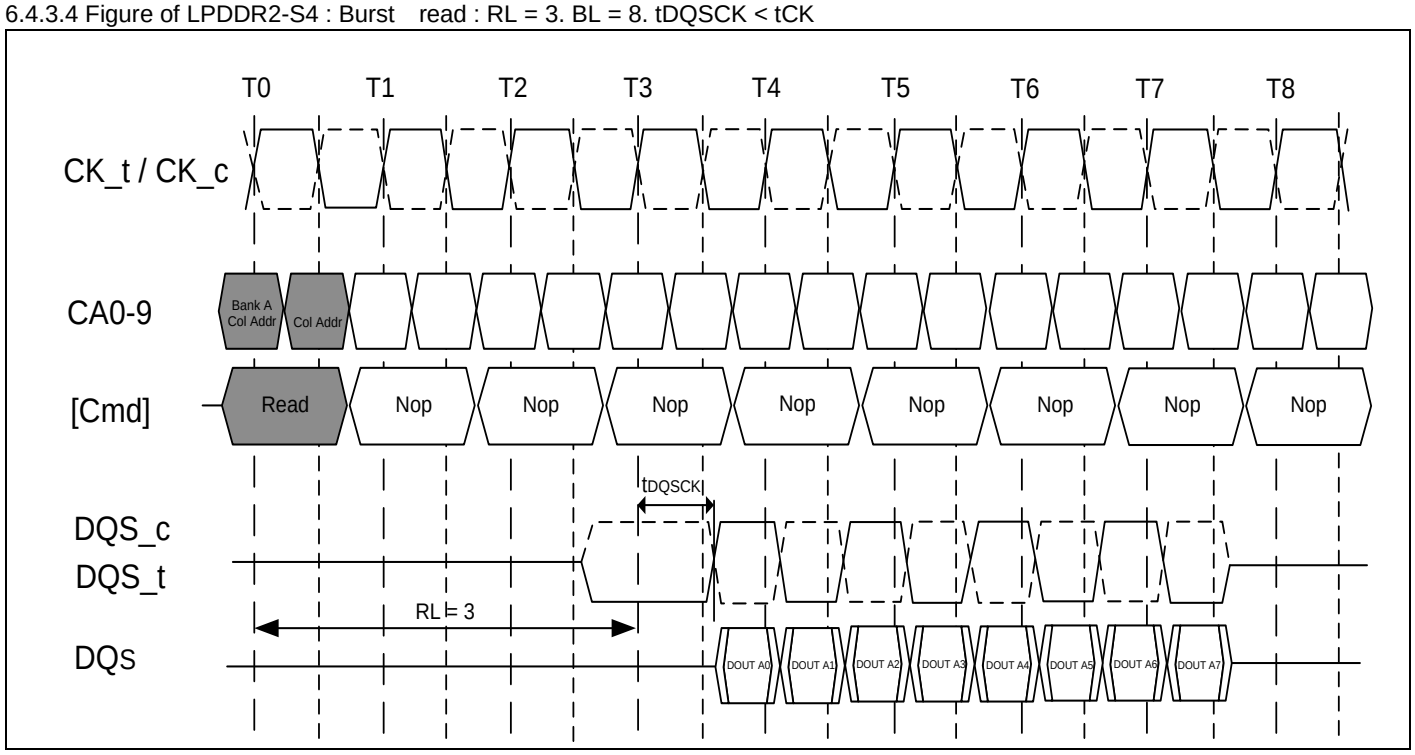


Note: An effective Burst Length of 4 is shown

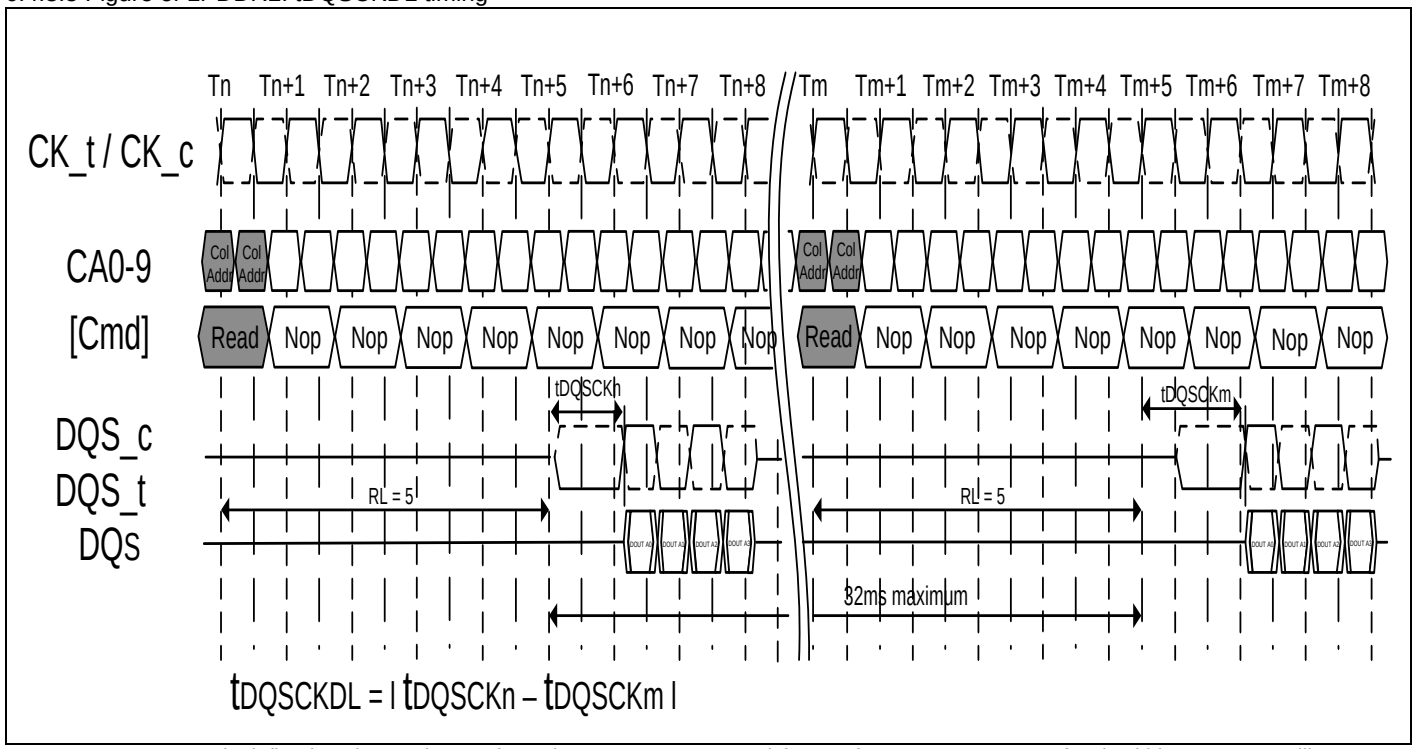
6.4.3.3 Figure of LPDDR2-S4 : Burst read : RL = 5. BL = 4. tDQSCK > tCK



6.4.3.4 Figure of LPDDR2-S4 : Burst read : RL = 3. BL = 8. tDQSCK < tCK

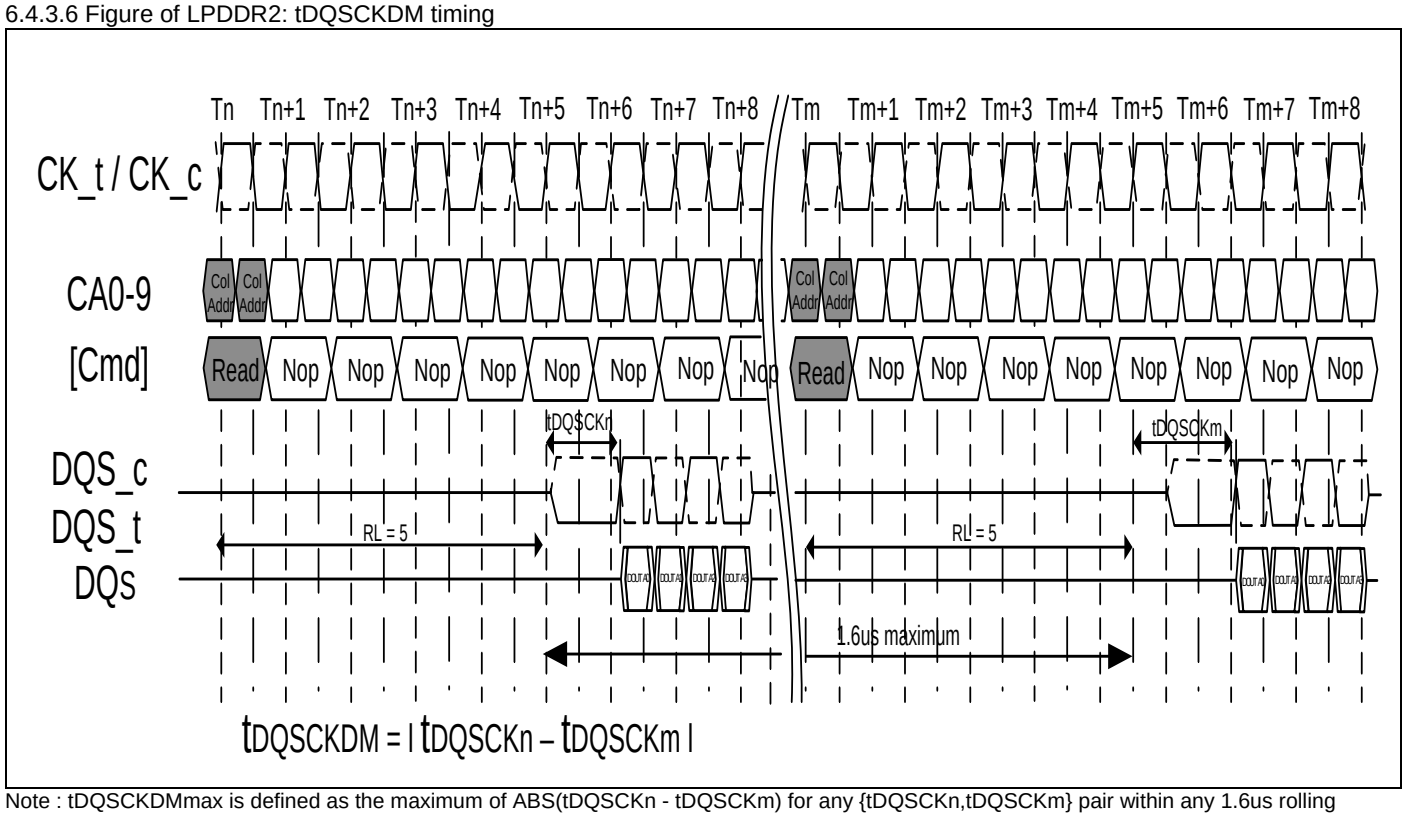


6.4.3.5 Figure of LPDDR2: tDQSCKDL timing



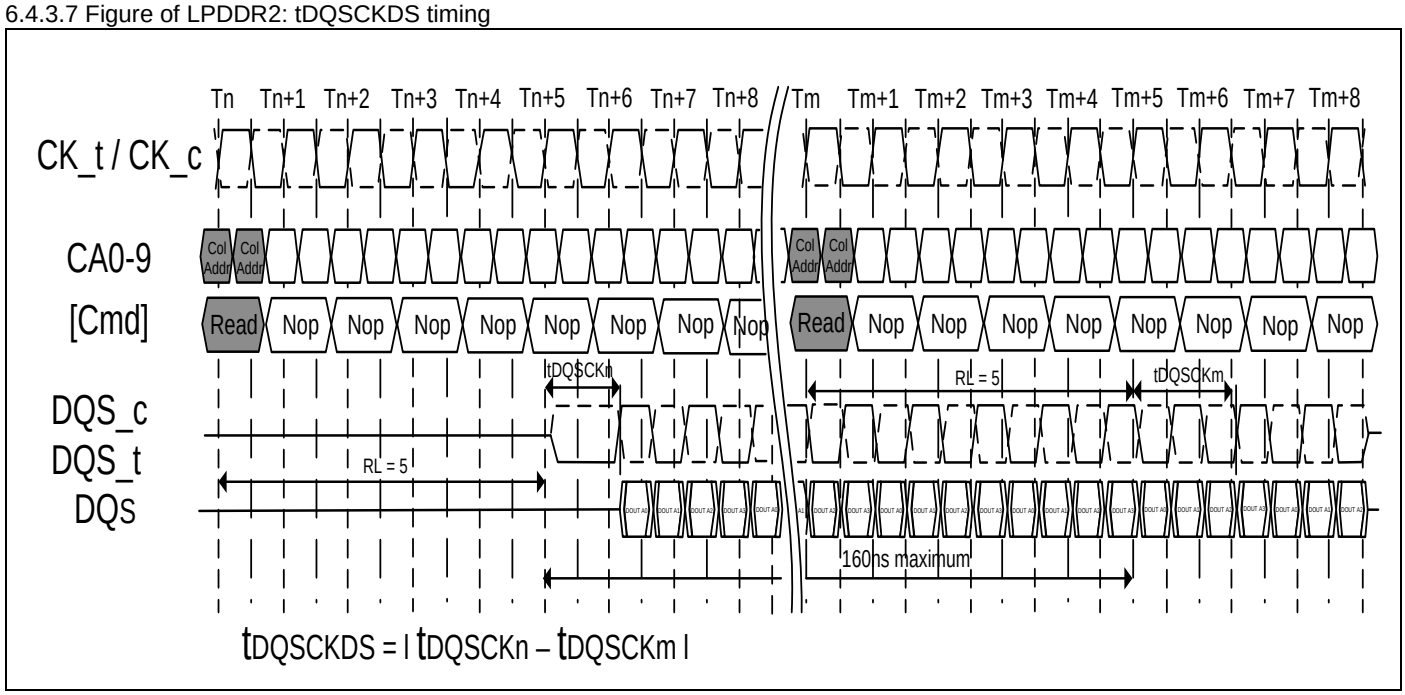
Note : tDQSCKDLmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn ,tDQSCKm} pair within any 32ms rolling window.

6.4.3.6 Figure of LPDDR2: tDQSCKDM timing



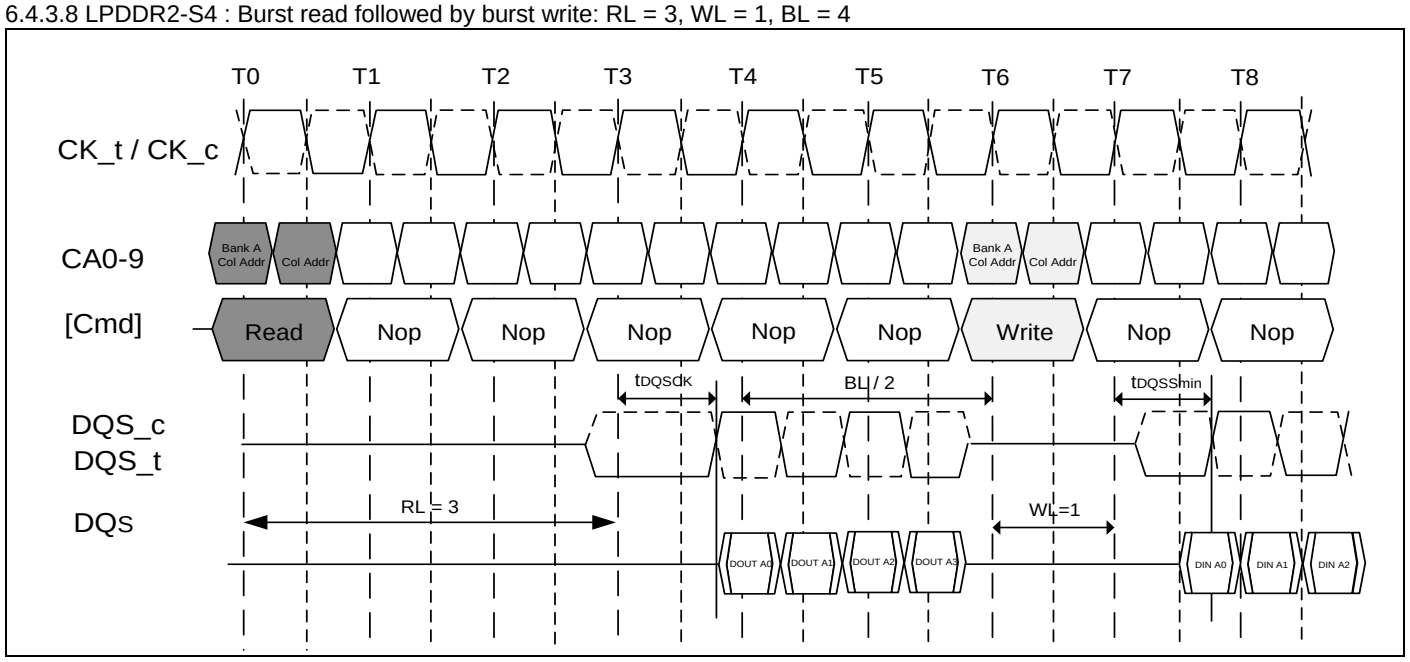
Note : tDQSCKDMmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn,tDQSCKm} pair within any 1.6us rolling window.

6.4.3.7 Figure of LPDDR2: tDQSCKDS timing



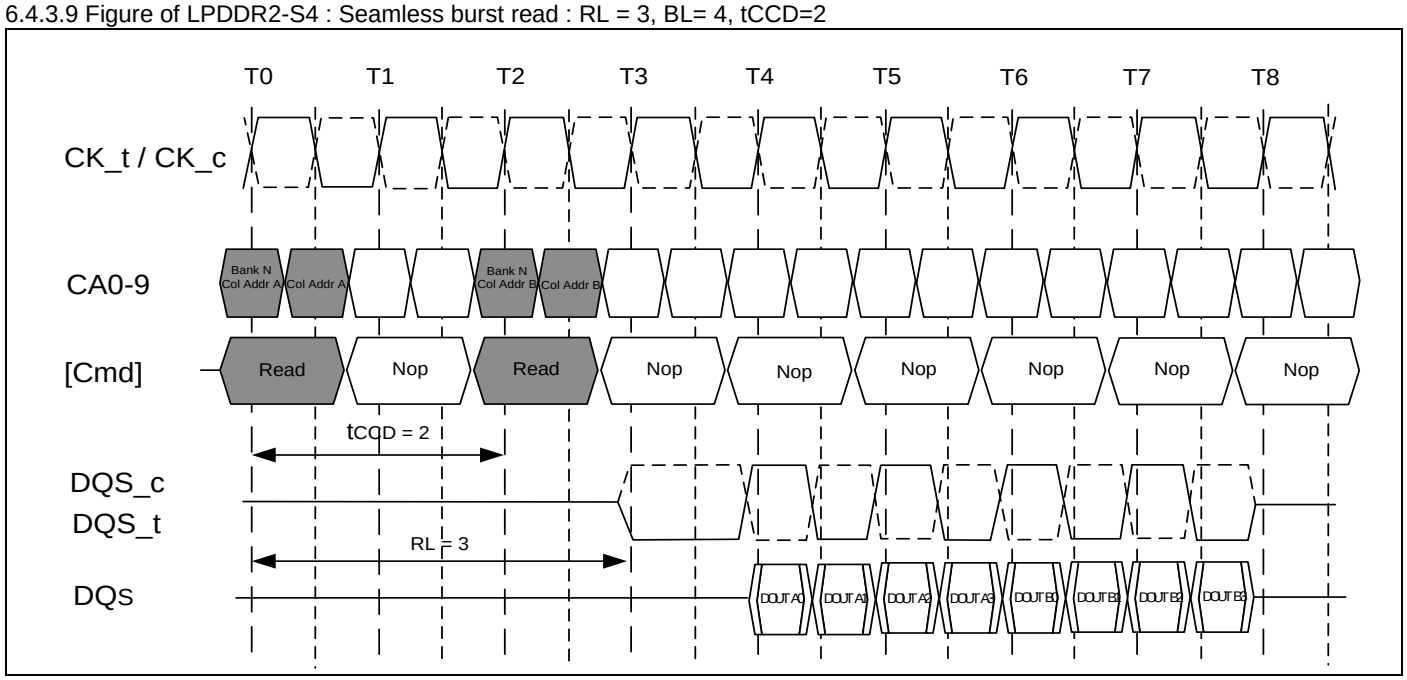
Note : tDQSCKDSmax is defined as the maximum of ABS(tDQSCKn - tDQSCKm) for any {tDQSCKn ,tDQSCKm} pair for reads within a consecutive burst within any 160ns rolling window.

6.4.3.8 LPDDR2-S4 : Burst read followed by burst write: RL = 3, WL = 1, BL = 4



The minimum time from the burst read command to the burst write command is defined by the Read Latency (RL) and the Burst Length (BL). Minimum read to write latency is RL + RU(tDQSCKmax/tCK) + BL/2 + 1 - WL clock cycles. Note that if a read burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated read burst should be used as “BL” to calculate the minimum read to write delay.

6.4.3.9 Figure of LPDDR2-S4 : Seamless burst read : RL = 3, BL= 4, tCCD=2



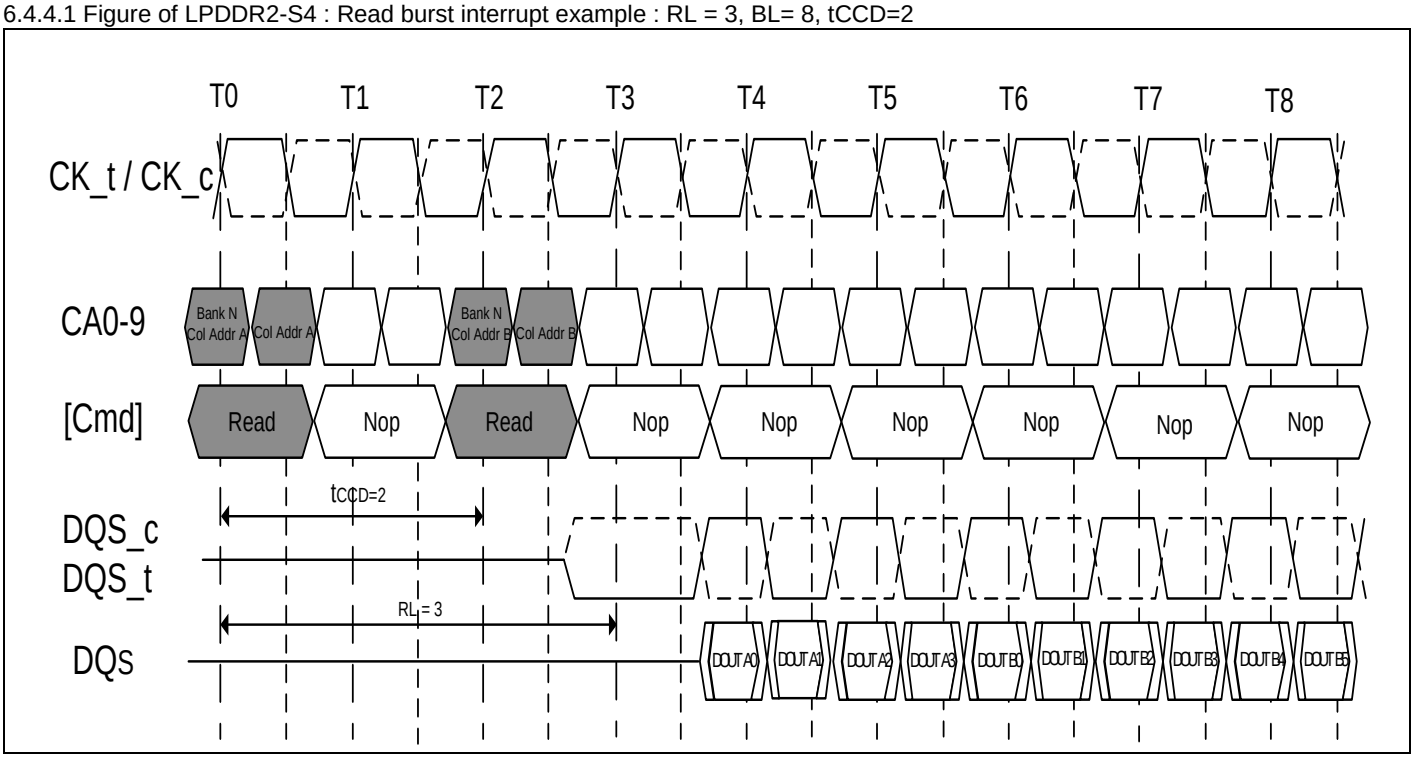
The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, every 4 clocks for BL = 8 operation, and every 8 clocks for BL=16 operation.

For LPDDR2-SDRAM, this operation is allowed regardless of whether the accesses read the same or different banks as long as the banks are activated.

6.4.4 Reads interrupted by a read

For LPDDR2-S4 device, burst read can be interrupted by another read on even clock cycles after the Read command, provided that tCCD is met.

6.4.4.1 Figure of LPDDR2-S4 : Read burst interrupt example : RL = 3, BL= 8, tCCD=2



Note : 1. For LPDDR2-S4 devices, read burst interrupt function is only allowed on burst of 8 and burst of 16.
2. For LPDDR2-S4 devices, read burst interrupt may only occur on even clock cycles after the previous commands, provided that tCCD is met.
3. Reads can only be interrupted by other reads or the BST command.
4. Read burst interruption is allowed to any bank inside DRAM.
5. Read burst with Auto-Precharge is not allowed to be interrupted.
6.The effective burst length of the first read equals two times the number of clock cycles between the first read and the interrupting read.

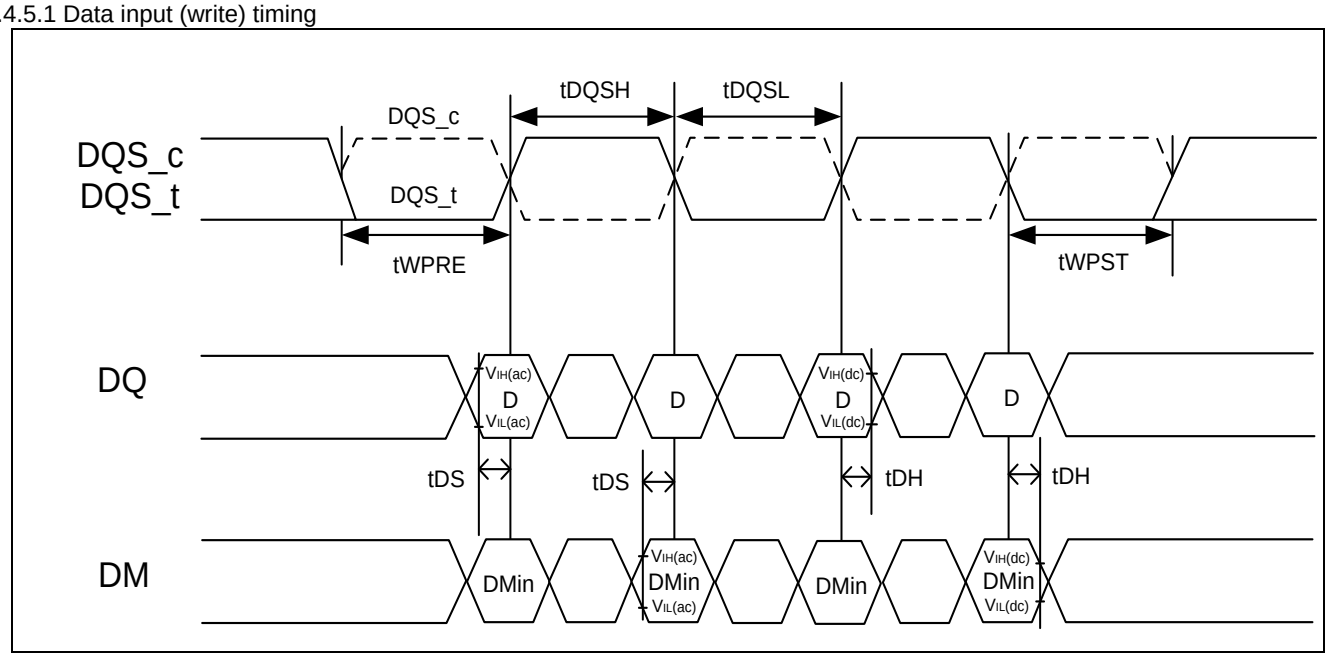
6.4.5 Burst Write operation

The Burst Write command is initiated by having CS_n LOW, CA0 HIGH, CA1 LOW and CA2 LOW at the rising edge of the clock. The command address bus inputs, CA5r-CA6r and CA1f-CA9f, determine the starting column address for the burst. The Write Latency (WL) is defined from the rising edge of the clock on which the Write Command is issued to the rising edge of the clock from which the tDQSS delay is measured. The first valid data must be driven WL * tCK + tDQSS from the rising edge of the clock from which the Write command is issued. The data strobe signal (DQS) should be driven LOW tWPRE prior to the data input. The data bits of the burst cycle must be applied to the DQ pins tDS prior to the respective edge of the DQS and held valid until tDH after that edge. The burst data are sampled on successive edges of the DQS until the burst length is completed, which is 4, 8, or 16 bit burst.

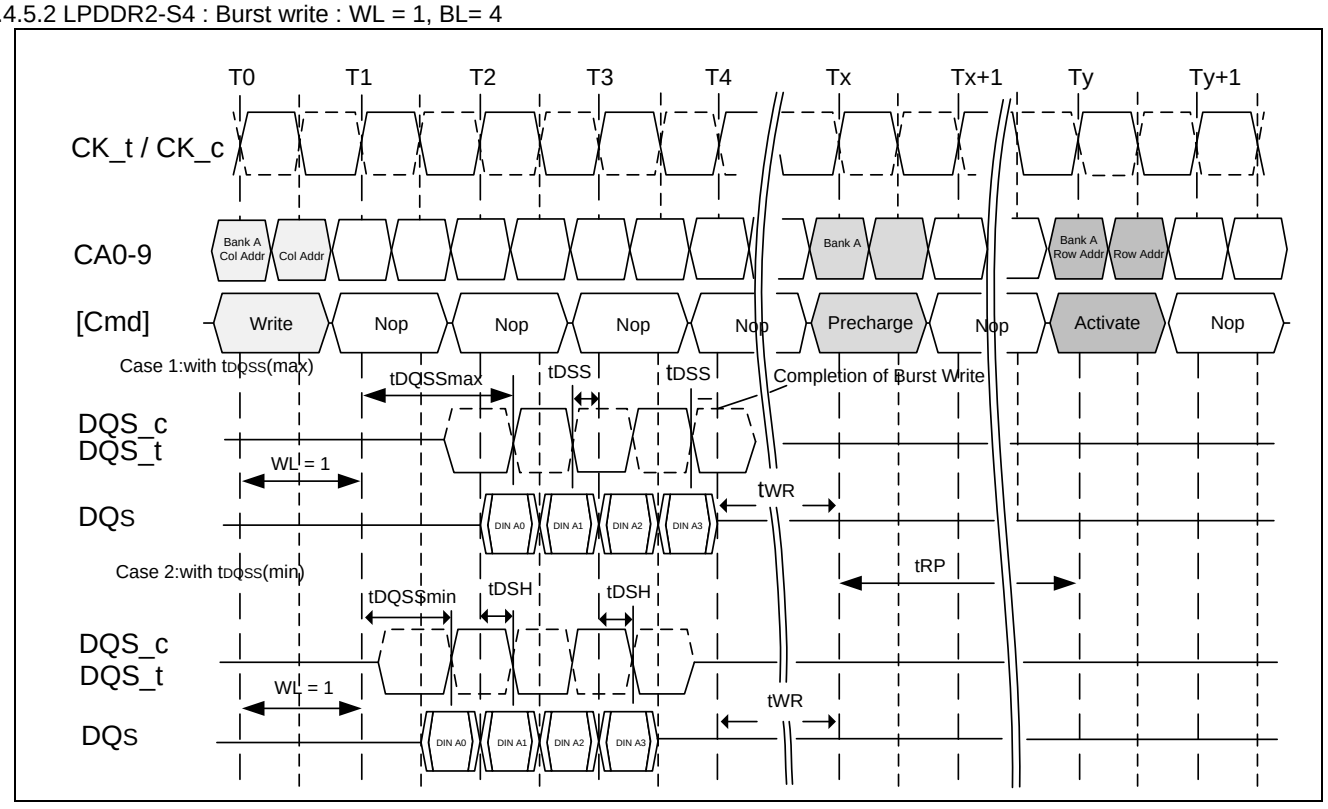
For LPDDR2-SDRAM devices, tWR must be satisfied before a precharge command to the same bank may be issued after a burst write operation.

Input timings are measured relative to the crosspoint of DQS_t and its complement, DQS_c.

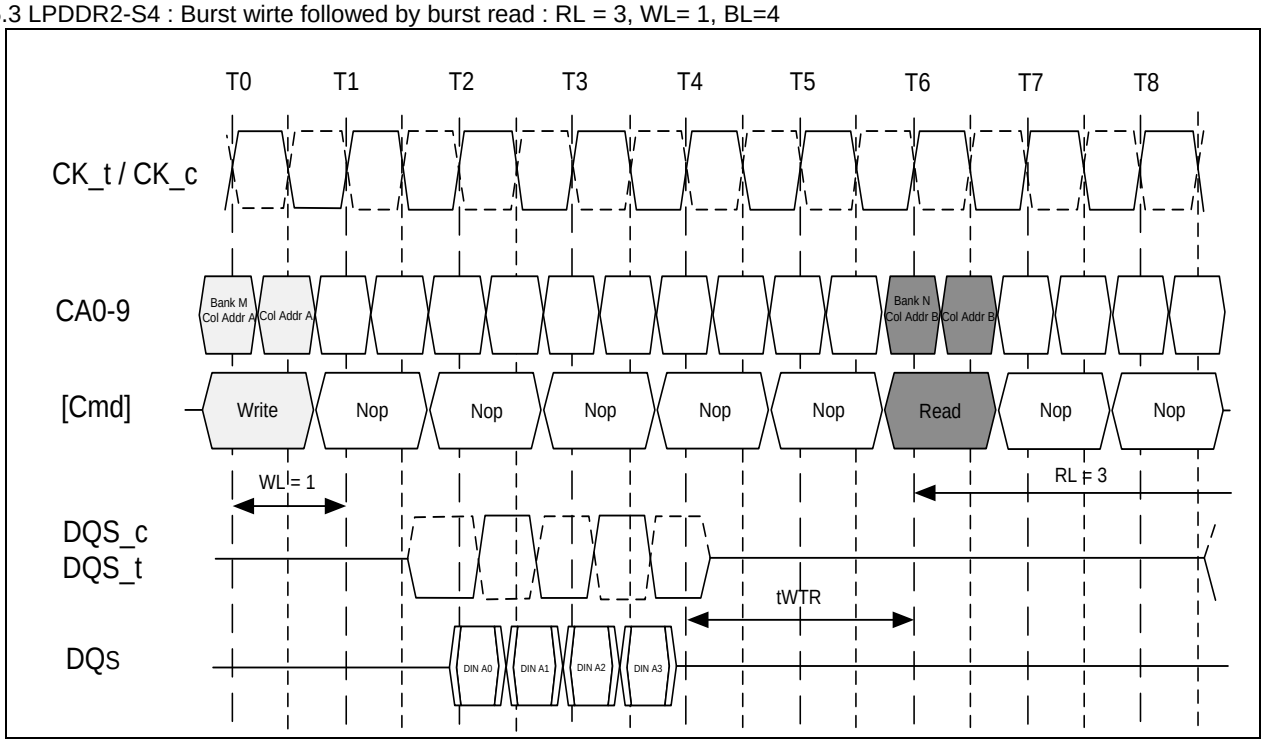
6.4.5.1 Data input (write) timing



6.4.5.2 LPDDR2-S4 : Burst write : WL = 1, BL= 4



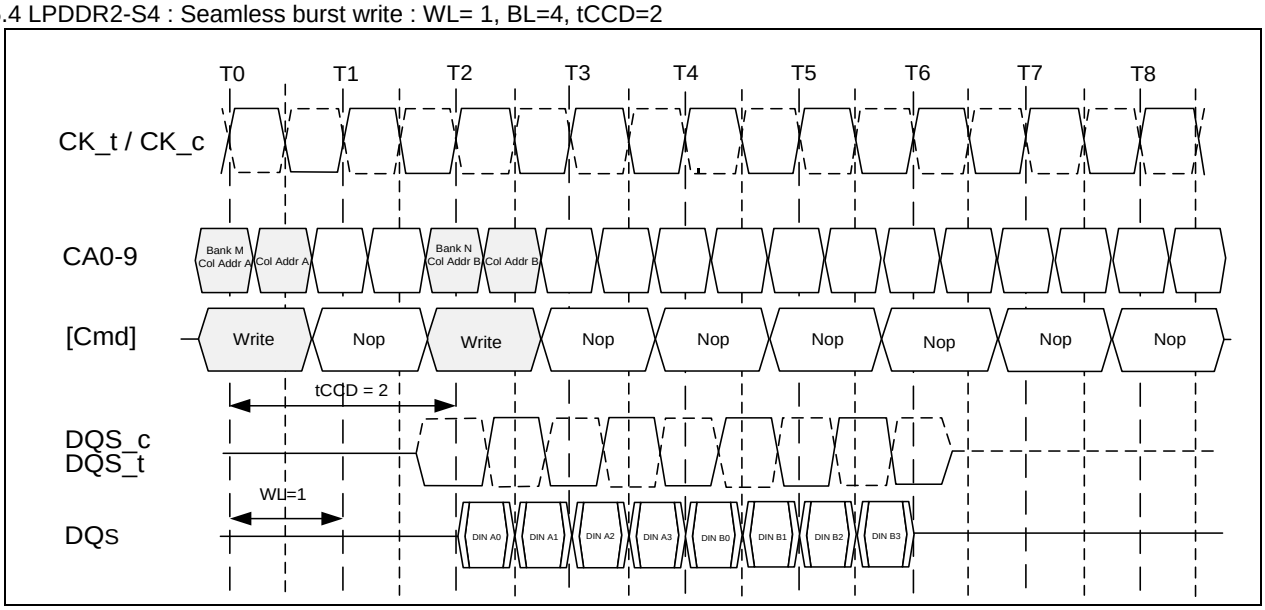
6.4.5.3 LPDDR2-S4 : Burst wirte followed by burst read : RL = 3, WL= 1, BL=4



Note :1.The minimum number of clock cycles from the burst write command to the burst read command for any bank is [WL + 1 + BL/2 + RU(tWTR/tCK)].

2. tWTR starts at the rising edge of the clock after the last valid input datum.
3. If a write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated write burst should be used as “BL” to calculate the minimum write to read delay.

6.4.5.4 LPDDR2-S4 : Seamless burst write : WL= 1, BL=4, tCCD=2

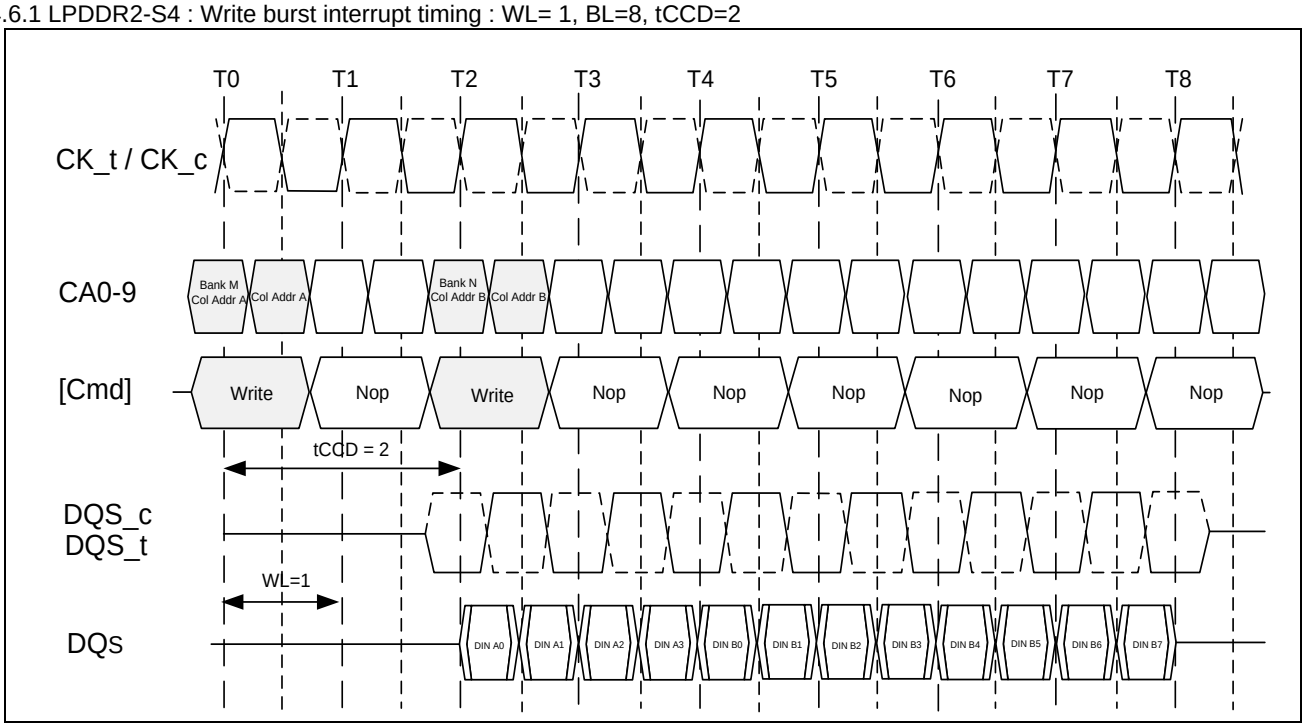


Note: The seamless burst write operation is supported by enabling a write command every other clock for BL = 4 operation, every four clocks for BL = 8 operation, or every eight clocks for BL=16 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

6.4.6 Writes interrupted by a write

For LPDDR2-S4 devices, burst writes can only be interrupted by another write on even clock cycles after the write command, provided that tCCD(min) is met.

6.4.6.1 LPDDR2-S4 : Write burst interrupt timing : WL= 1, BL=8, tCCD=2



Note : 1. For LPDDR2-S4 devices, write burst interrupt function is only allowed on burst of 8 and burst of 16.
2. For LPDDR2-S4 devices, write burst interrupt may only occur on even clock cycles after the previous write commands, provided that tCCD(min) is met.
3. Writes can only be interrupted by other writes or the BST command.
4. Write burst interruption is allowed to any bank inside DRAM.
5. Write burst with Auto-Precharge is not allowed to be interrupted.
6. The effective burst length of the first write equals two times the number of clock cycles between the first write and the interrupting write.

6.4.7 Burst Terminate

The Burst Terminate (BST) command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 LOW at the rising edge of clock. A Burst Teminate command may only be issued to terminate an active Read or Write burst. Therefore, a Burst Terminate command may only be issued up to and including BL/2 - 1 clock cycles after a Read or Write command. The effective burst length of a Read or Write command truncated by a BST command is as follows:

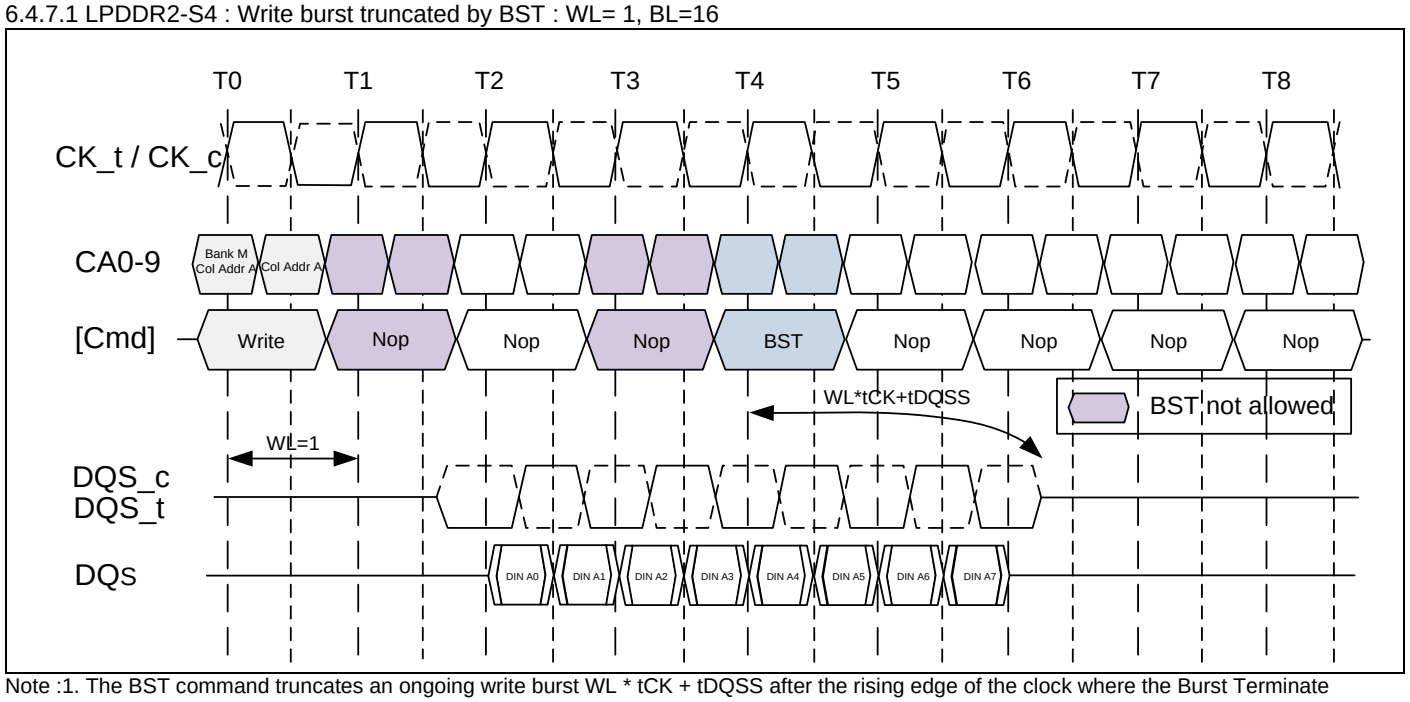
Effective burst length = 2 x {Number of clock cycles from the Read or Write Command to the BST command}

Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL” to calculate the minimum read to write or write to read delay.

The BST command only affects the most recent read or write command. The BST command truncates an ongoing read burst RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Burst Terminate command is issued. The BST command truncates an on going write burst WL * tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.

For LPDDR2-S4 devices, the 4-bit prefetch architecture allows the BST command to be issued on an even number of clock cycles after a Write or Read command. Therefore, the effective burst length of a Read or Write command truncated by a BST command is an integer multiple of 4.

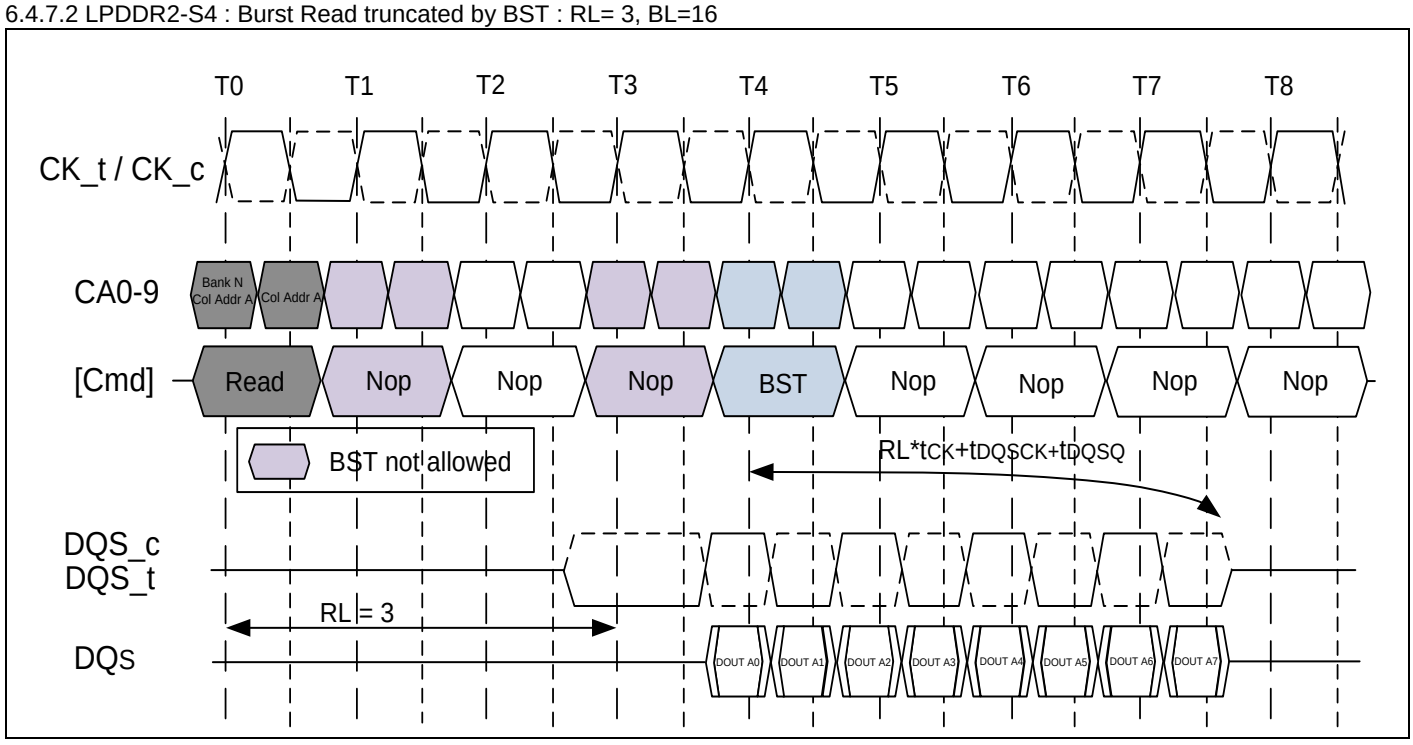
6.4.7.1 LPDDR2-S4 : Write burst truncated by BST : WL= 1, BL=16



Note :1. The BST command truncates an ongoing write burst WL * tCK + tDQSS after the rising edge of the clock where the Burst Terminate command is issued.

2. Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

6.4.7.2 LPDDR2-S4 : Burst Read truncated by BST : RL= 3, BL=16



Note :1. The BST command truncates an ongoing read burst RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Burst Terminate command is issued.

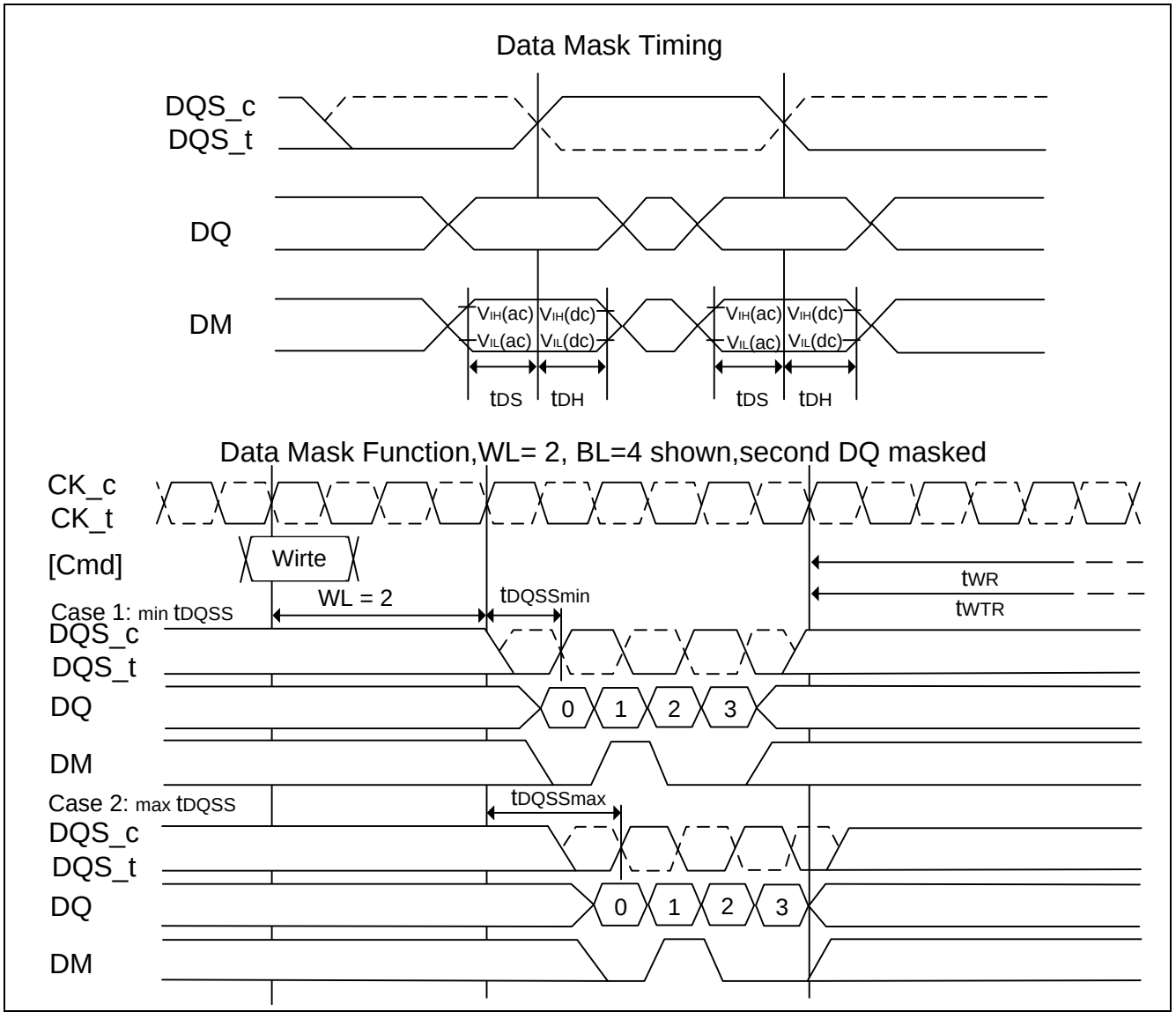
2. For LPDDR2-S4 devices, BST can only be issued at even number of clock cycles after the Write command.

3. Additional BST commands are not allowed after T4 and may not be issued until after the next Read or Write command.

6.4.8 Write data mask

One write data mask (DM) pin for each data byte (DQ) will be supported on LPDDR2 devices, consistent with the implementation on LPDDR SDRAMs. Each data mask (DM) may mask its respective data byte (DQ) for any given cycle of the burst. Data mask has identical timings on write operations as the data bits, though used as input only, is internally loaded identically to data bits to insure matched system timing.

6.4.8.1 LPDDR2-S4 : Write data mask



6.4.9 LPDDR2-S4: Precharge operation

The Precharge command is used to precharge or close a bank that has been activated. The Precharge command is initiated by having CS_n LOW, CA0 HIGH, CA1 HIGH, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The Precharge Command can be used to precharge each bank independently or all banks simultaneously. For 8-bank devices, the AB flag, and the bank address bits, BA0, BA1, and BA2, are used to determine which bank(s) to precharge. The bank(s) will be available for a subsequent row access tRPab after an All-Bank Precharge command is issued and tRPpb after a Single-Bank Precharge command is issued.

In order to ensure that 8-bank devices do not exceed the instantaneous current supplying capability of 4-bank devices, the Row Precharge time (tRP) for an All-Bank Precharge for 8-bank devices (tRPab) will be longer than the Row Precharge time for a Single-Bank Precharge (tRPpb).

6.4.9.1 Table of Bank selection for Precharge by address bits

AB (CA4r)	BA2 (CA9r)	BA1 (CA8r)	BA0 (CA7r)	Precharged Bank(s) 8-bank device
0	0	0	0	Bank 0 only
0	0	0	1	Bank 1 only
0	0	1	0	Bank 2 only
0	0	1	1	Bank 3 only
0	1	0	0	Bank 4 only
0	1	0	1	Bank 5 only
0	1	1	0	Bank 6 only
0	1	1	1	Bank 7 only
1	DON'T CARE	DON'T CARE	DON'T CARE	All Banks

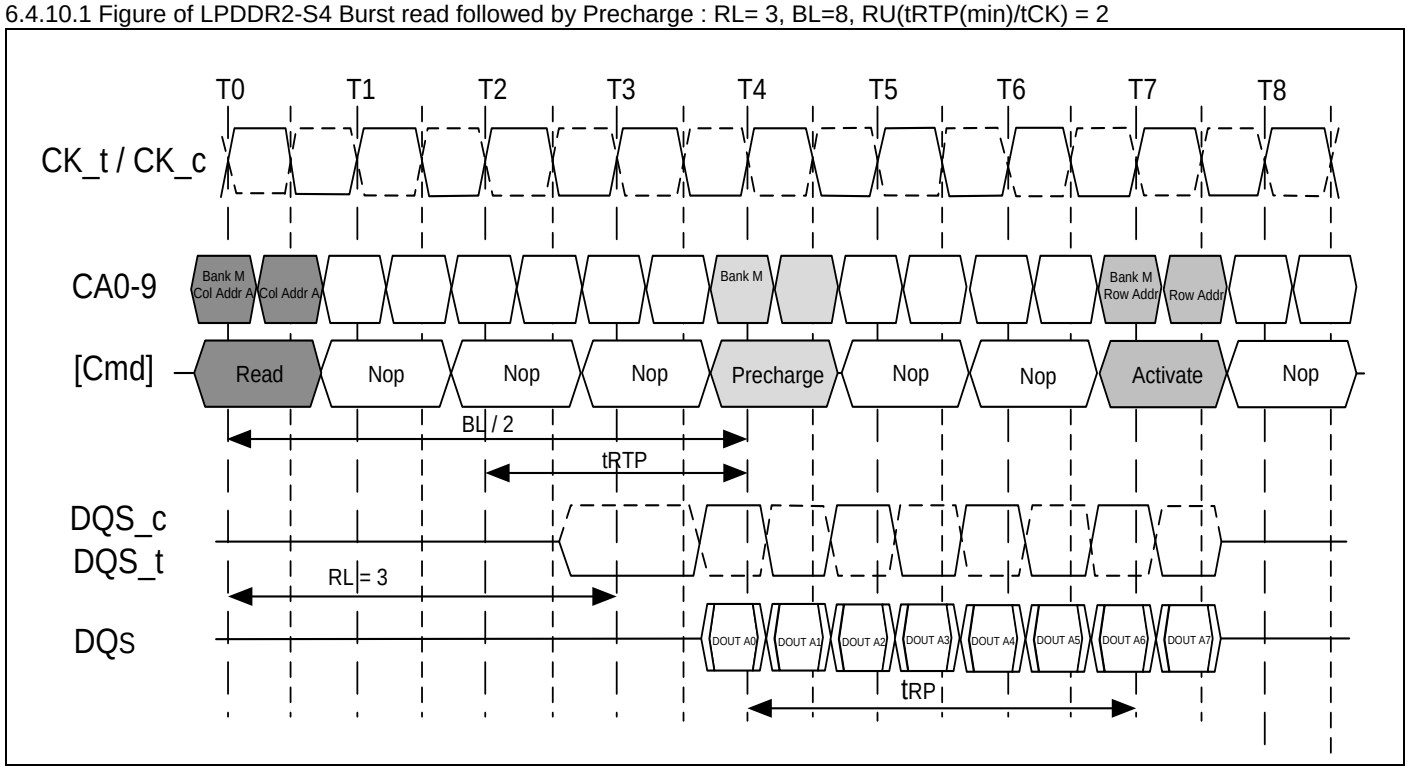
6.4.10 LPDDR2-S4: Burst Read operation followed by Precharge

For the earliest possible precharge, the precharge command may be issued BL/2 clock cycles after a Read command. For an untruncated burst, BL is the value from the Mode Register. For a truncated burst, BL is the effective burst length. A new bank active (command) may be issued to the same bank after the Row Precharge time (tRP). A precharge command cannot be issued until after tRAS is satisfied.

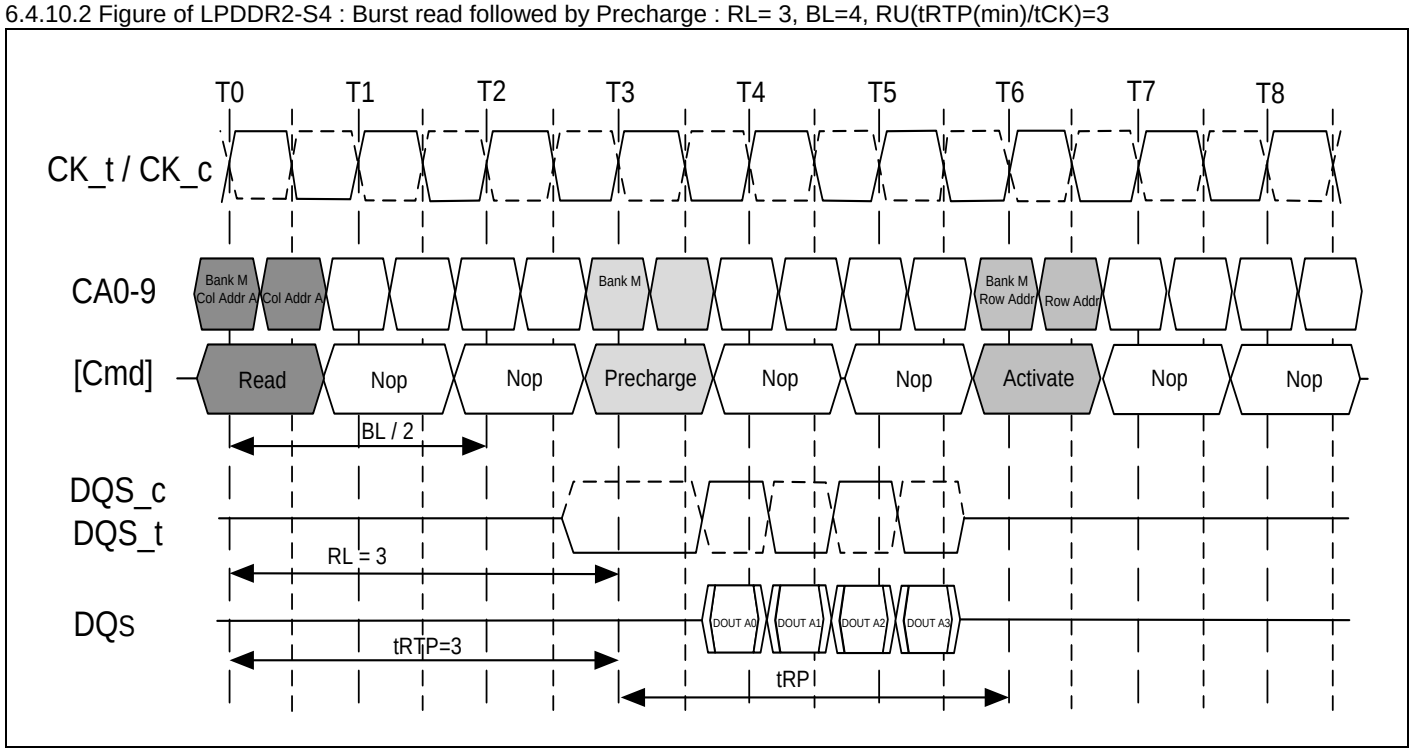
For LPDDR2-S4 devices, the minimum Read to Precharge spacing has also to satisfy a minimum analog time from the rising clock edge that initiates the last 4-bit prefetch of a Read command.This time is called tRTP (Read to Precharge).

For LPDDR2-S4 devices, tRTP begins BL/2 - 2 clock cycles after the Read command. If the burst is truncated by a BST command or a Read command to a different bank, , the effective "BL" shall be used to calculate when tRTP begins.

6.4.10.1 Figure of LPDDR2-S4 Burst read followed by Precharge : RL= 3, BL=8, RU(tRTP(min)/tCK) = 2



6.4.10.2 Figure of LPDDR2-S4 : Burst read followed by Precharge : RL= 3, BL=4, RU(tRTP(min)/tCK)=3



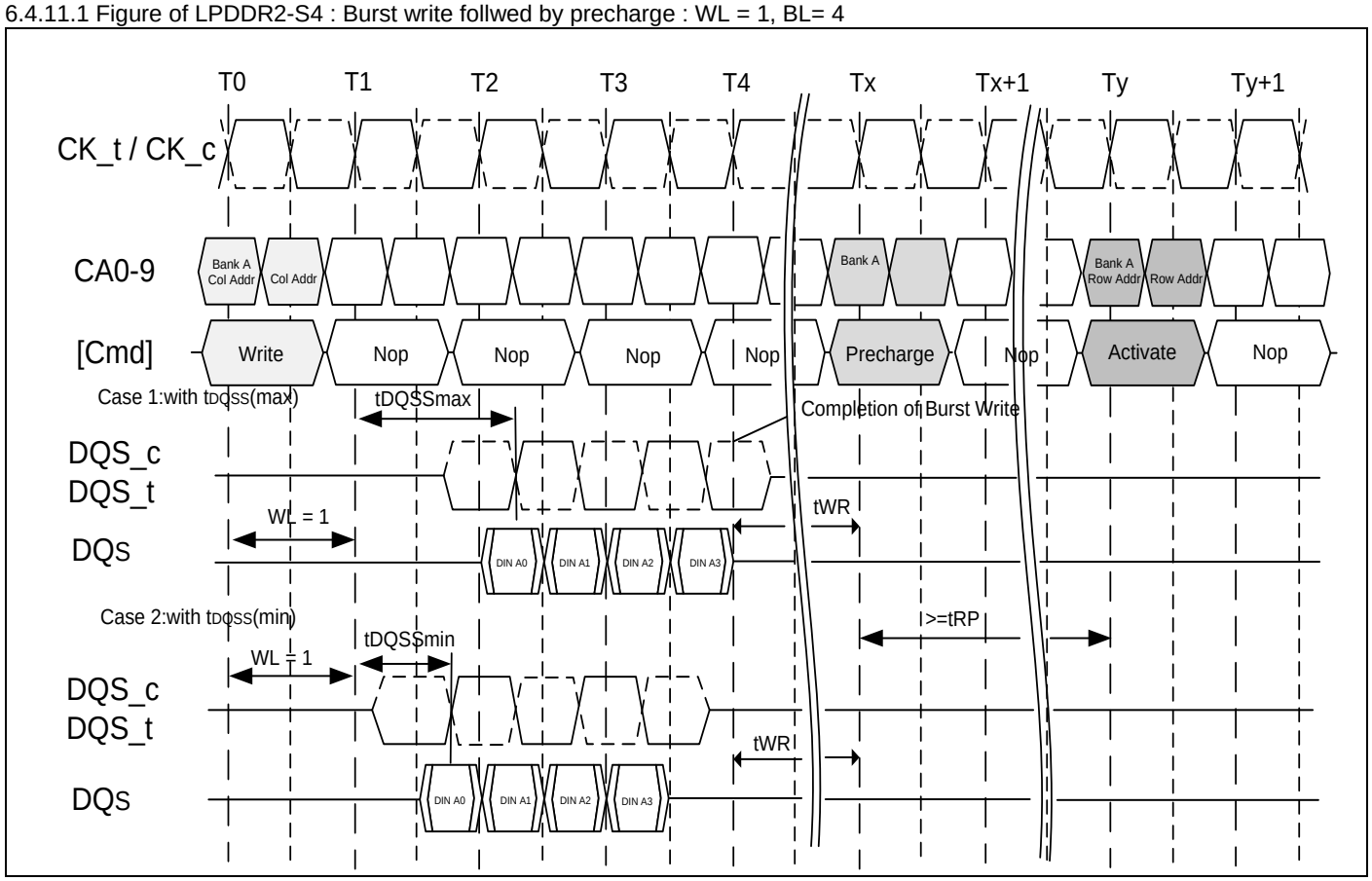
6.4.11 LPDDR2-S4: Burst Write followed by Precharge

For write cycles, a delay must be satisfied from the time of the last valid burst input data until the Precharge command may be issued. This delay is known as the write recovery time (tWR) referenced from the completion of the burst write to the precharge command. No Precharge command should be issued prior to the tWR delay.

These devices write data to the array in prefetch quadruples (prefetch = 4). The beginning of an internal write operation may only begin after a prefetch group has been latched completely.

The minimum Write to Precharge command spacing to the same bank is WL + BL/2 + 1 + RU(tWR/tCK) clock cycles. For an untruncated burst, BL is the value from the Mode Register. For an truncated burst, BL is the effective burst length.

6.4.11.1 Figure of LPDDR2-S4 : Burst write follwed by precharge : WL = 1, BL= 4



6.4.12 LPDDR2-S4: Auto Precharge operation

Before a new row in an active bank can be opened, the active bank must be precharged using either the Precharge command or the auto-precharge function. When a Read or a Write command is given to the LPDDR2 SDRAM, the AP bit (CA0f) may be set to allow the active bank to automatically begin precharge at the earliest possible moment during the burst read or write cycle.

If AP is LOW when the Read or Write command is issued, then normal Read or Write burst operation is executed and the bank remains active at the completion of the burst.

If AP is HIGH when the Read or Write command is issued, then the auto-precharge function is engaged. This feature allows the precharge operation to be partially or completely hidden during burst read cycles (dependent upon Read or Write latency) thus improving system performance for random data access.

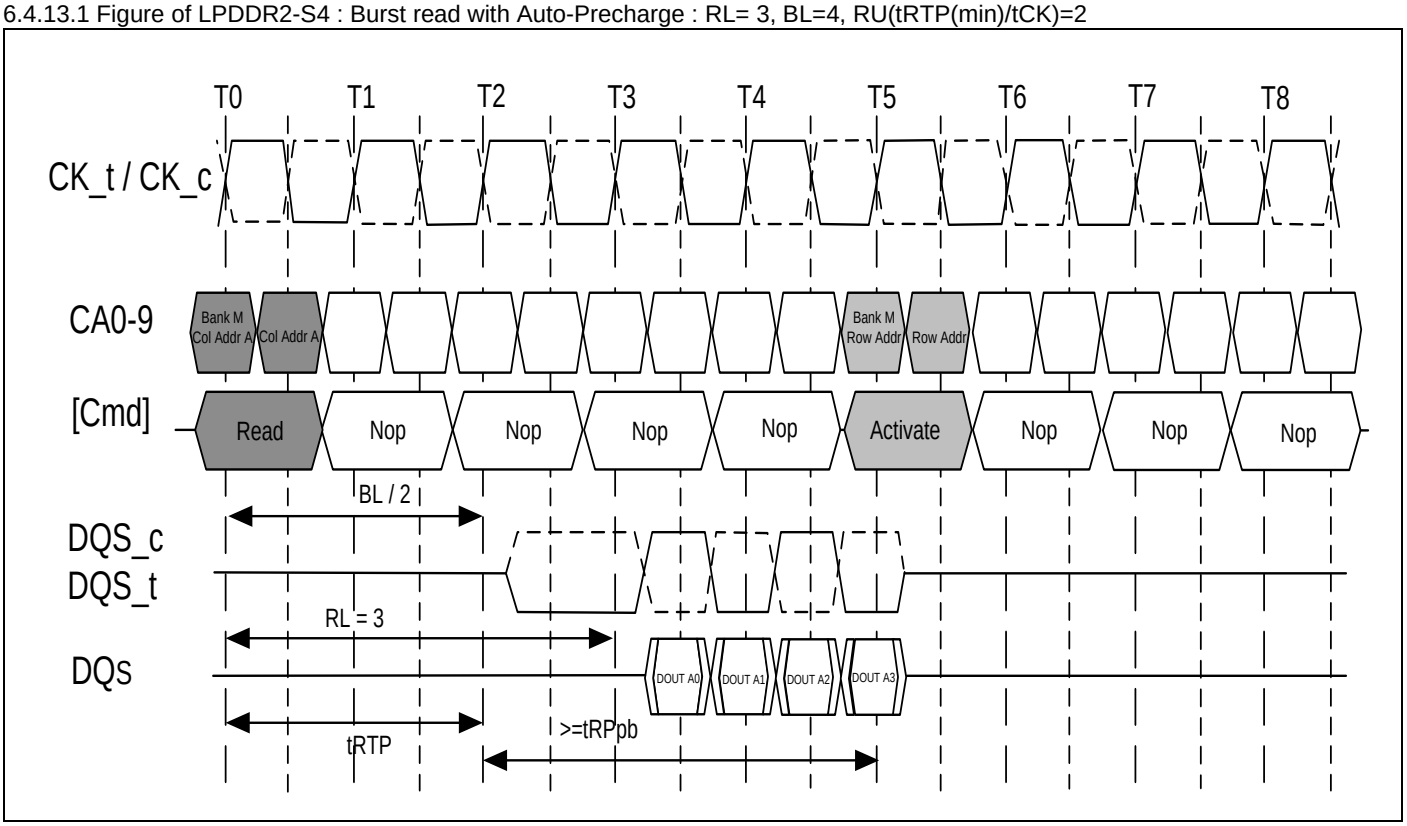
6.4.13 LPDDR2-S4: Burst Read with Auto-Precharge

If AP (CA0f) is HIGH when a Read Command is issued, the Read with Auto-Precharge function is engaged. LPDDR2-S4 devices start an Auto-Precharge operation on the rising edge of the clock BL/2 or BL/2 - 2 + RU(tRTP/tCK) clock cycles later than the Read with AP command.

A new bank Activate command may be issued to the same bank if both of the following two conditions are satisfied simultaneously.

- The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
- The RAS cycle time (tRC) from the previous bank activation has been satisfied

6.4.13.1 Figure of LPDDR2-S4 : Burst read with Auto-Precharge : RL= 3, BL=4, RU(tRTP(min)/tCK)=2



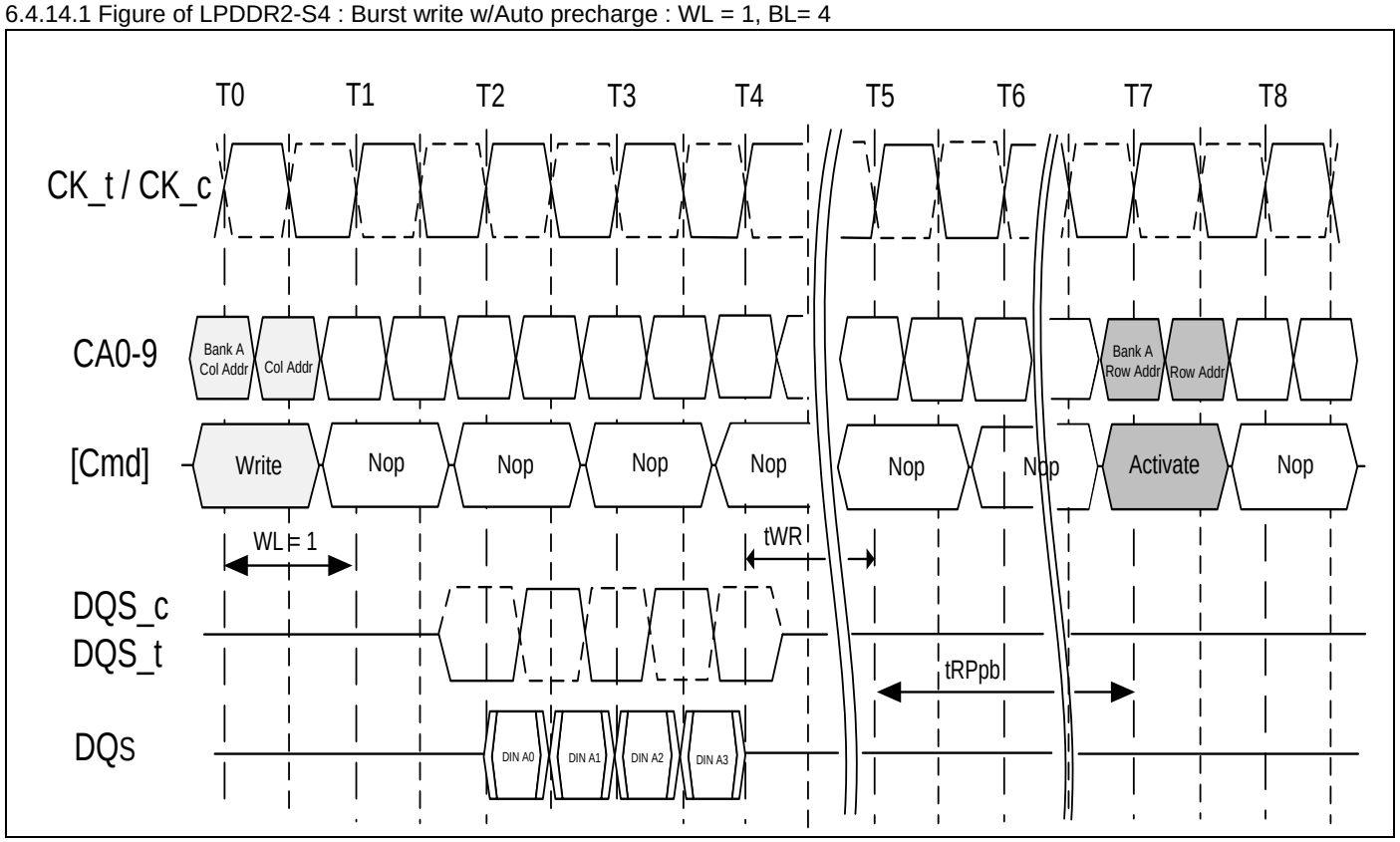
6.4.14 LPDDR2-S4: Burst write with Auto-Precharge

If AP (CA0f) is HIGH when a Write Command is issued, the Write with Auto-Precharge function is engaged. The LPDDR2 SDRAM starts an Auto Precharge operation on the rising edge which is tWR cycles after the completion of the burst write.

A new bank activate (command) may be issued to the same bank if both of the following two conditions are satisfied.

- The RAS precharge time (tRP) has been satisfied from the clock at which the auto precharge begins.
- RAS cycle time (tRC) from the previous bank activation has been satisfied.

6.4.14.1 Figure of LPDDR2-S4 : Burst write w/Auto precharge : WL = 1, BL= 4



6.4.14.2 Table of LPDDR2-S4 Precharge & Auto Precharge Clarification

From Command	To Command	Minimum Delay between "From Command" to "To Command"	Unit	Note
Read	Precharge (to same Bank as Read)	BL/2 + max(2, RU(tRTP/tCK)) - 2	CLK	1
	Precharge ALL	BL/2 + max(2, RU(tRTP/tCK)) - 2	CLK	1
BST (for Reads)	Precharge (to same Bank as Read)	1	CLK	1
	Precharge ALL	1	CLK	1
Read w/AP	Precharge (to same Bank as Read w/AP)	BL/2 + max(2, RU(tRTP/tCK)) - 2	CLK	1,2
	Precharge ALL	BL/2 + max(2, RU(tRTP/tCK)) - 2	CLK	1
	Activate (to same Bank as Read w/AP)	BL/2 + max(2, RU(tRTP/tCK)) - 2 + RU(tRPpb/tCK)	CLK	1
	Write or Write w/AP (same bank)	Illegal	CLK	3
	Write or Write w/AP (different bank)	RL + BL/2 + RU(tDQSCKmax/tCK) - WL + 1	CLK	3
	Read or Read w/AP (same bank)	Illegal	CLK	3
	Read or Read w/AP (different bank)	BL/2	CLK	3
Write	Precharge (to same Bank as Write)	WL + BL/2 + RU(tWR/tCK) + 1	CLK	1
	Precharge ALL	WL + BL/2 + RU(tWR/tCK) + 1	CLK	1
BST (for Writes)	Precharge (to same Bank as Write)	WL + RU(tWR/tCK) + 1	CLK	1
	Precharge ALL	WL + RU(tWR/tCK) + 1	CLK	1
Write w/AP	Precharge (to same Bank as Write w/AP)	WL + BL/2+ RU(tWR/tCK) + 1	CLK	1
	Precharge ALL	WL + BL/2 + RU(tWR/tCK) + 1	CLK	1
	Activate (to same Bank as Write w/AP)	WL + BL/2 + RU(tWR/tCK) + 1 + RU(tRPpb/tCK)	CLK	1
	Write or Write w/AP (same bank)	Illegal	CLK	3
	Write or Write w/AP (different bank)	BL/2	CLK	3
	Read or Read w/AP (same bank)	Illegal	CLK	3
	Read or Read w/AP (different bank)	WL + BL/2 + RU(tWTR/tCK) + 1	CLK	3
Precharge	Precharge (to same Bank as Precharge)	1	CLK	1
	Precharge ALL	1	CLK	1
Precharge All	Precharge	1	CLK	1
	Precharge ALL	1	CLK	1

Note :1. For a given bank, the precharge period should be counted from the latest precharge command, either one bank precharge or precharge all, issued to that bank. The precharge period is satisfied after tRP depending on the latest precharge command issued to that bank.
2. Any command issued during the minimum delay time is illegal.
3. After Read with AP, seamless read operations to different banks are supported. After Write with AP, seamless write operations to different banks are supported. Read w/AP and Write w/AP may not be interrupted or truncated.

6.4.15 LPDDR2-S4: Refresh command

The Refresh command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of clock. Per Bank Refresh is initiated by having CA3 LOW at the rising edge of clock and All Bank Refresh is initiated by having CA3 HIGH at the rising edge of clock. Per Bank Refresh is only allowed in devices with 8 banks.

A Per Bank Refresh command, REFpb performs a refresh operation to the bank which is scheduled by the bank counter in the memory device. The bank sequence of Per Bank Refresh is fixed to be a sequential round-robin: "0-1-2-3-4-5-6-7-0-1-...". The bank count is synchronized between the controller and the SDRAM upon issuing a RESET command or at every exit from self refresh, by resetting bank count to zero. The bank addressing for the Per Bank Refresh count is the same as established in the single-bank Precharge command. A bank must be idle before it can be refreshed. It is the responsibility of the controller to track the bank being refreshed by the Per Bank Refresh command.

The REFpb command may not be issued to the memory until the following conditions are met:

a) tRFCab has been satisified after the prior REFab command
b) tRFCpb has been satisfied after the prior REFpb command
c) tRP has been satisified after the prior Precharge command to that given bank

tRRD has been satisfied after the prior ACTIVATE command (if applicable, for example after activating a row in a different bank than affected by the REFpb command).

The target bank is inaccessable during the Per Bank Refresh cycle time (tRFCpb), however other banks within the device are accessable and may be addressed during the Per Bank Refresh cycle. During the REFpb operation, any of the banks other than the one being refreshed can be maintained in active state or accessed by a read or a write command.

When the Per Bank refresh cycle has completed, the affected bank will be in the Idle state.after issuing REFpb:

a) tRFCpb must be satisified before issuing a REFab command
b) tRFCpb must be satisfied before issuing an ACTIVATE command to the same bank
c) tRRD must be satisified before issuing an ACTIVATE command to a different bank
d) tRFCpb must be satisified before issuing another REFpb command

An All Bank Refresh command, REFab performs a refresh operation to all banks. All banks have to be in Idle state when REFab is issued (for instance, by Precharge all-bank command). REFab also synchronizes the bank count between the controller and the SDRAM to zero. the REFab command may not be issued to the memory until the following conditions have been met:

a) tRFCab has been satisified after the prior REFab command
b) tRFCpb has been satisified after the prior REFpb command
c) tRP has been satisified after prior PRECHARGE commands

When the All Bank refresh cycle has completed, all banks will be in the Idle state. after issuing REFab:

a) the tRFCab latency must be satisfied before issuing an ACTIVATE command
b) the tRFCab latency must be satisfied before issuing a REFab or REFpb command

6.4.15.1 Table of Command Scheduling Separations related to Refresh

Symbol	minimum delay from	to	Note
tRFCab	REFab	REFab	
		Activate cmd to any bank	
		REFpb	
tRFCpb	REFpb	REFab	
		Activate cmd to same bank as REFpb	
		REFpb	
tRRD	REFpb	Activate cmd to different bank than REFpb	
	Activate	REFpb affecting an idle bank (different bank than Activate)	1
		Activate cmd to different bank than prior Activate	
Note : A bank must be in the Idle state before it is refreshed. Therefore, after Activate,REFab is not allowed and REFpb is allowed only if it affects a bank which is in the Idle state..			

6.4.16 LPDDR2 SDRAM Refresh Requirements

(1) Minimum number of Refresh commands:

The LPDDR2 SDRAM requires a minimum number of R Refresh (REFab) commands within any rolling Refresh Window (tREFW = 32 ms @ MR4[2:0] = “011” or Tj ≤85 °C). The minimum number R depends on density. The resulting average refresh interval (tREFI) also depends on density.

See Mode Register 4 for tREFW and tREFI refresh multipliers at different MR4 settings.

(2) Burst Refresh limitation:

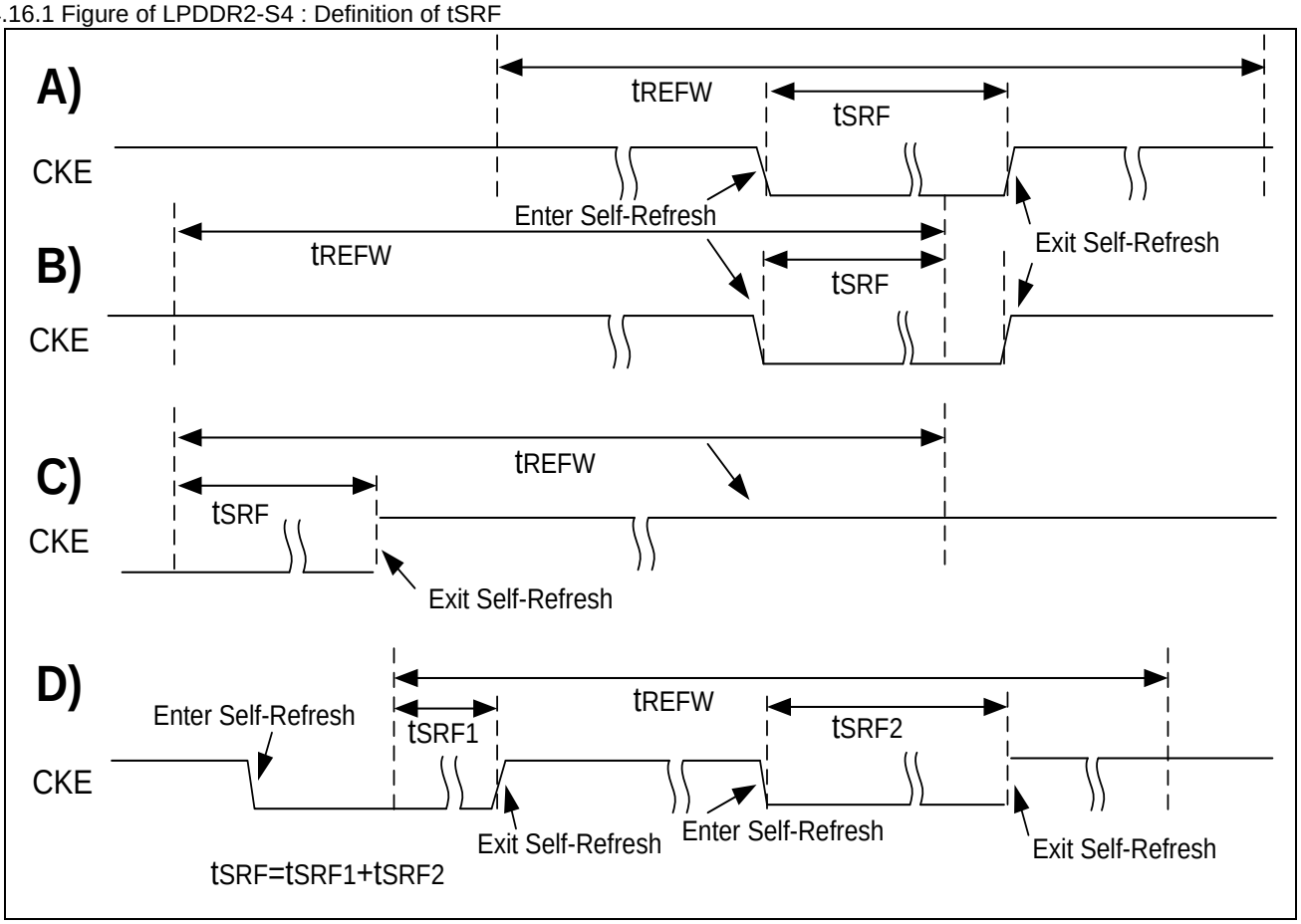
To limit maximum current consumption, a maximum of 8 REFab commands may be issued in any rolling tREFBW (tREFBW = 4 x 8 x tRFCab).

(3) Refresh Requirements and Self-Refresh:

If any time within a refresh window is spent in Self-Refresh Mode, the number of required Refresh commands in this particular window is reduced to:

R* = R - RU{tSRF / tREFI} = R - RU{R * tSRF / tREFW}; where RU stands for the round-up function

6.4.16.1 Figure of LPDDR2-S4 : Definition of tSRF



Several examples on how tSRF is caclulated:
A: with the time spent in Self-Refresh Mode fully enclosed in the Refresh Window (tREFW),
B: at Self-Refresh entry
C: at Self-Refresh exit
D: with several different invervals spent in Self Refresh during one tREFW interval

In contrast to JESD79 and JESD79-2 and JESD79-3 compliant SDRAM devices, LPDDR2-S4 devices allow significant flexibiliy in scheduling REFRESH commands, as long as the boundary conditions above are met.
In the most straight forward case a REFRESH command should be scheduled every tREFI. In this case Self-Refresh may be entered at any time.

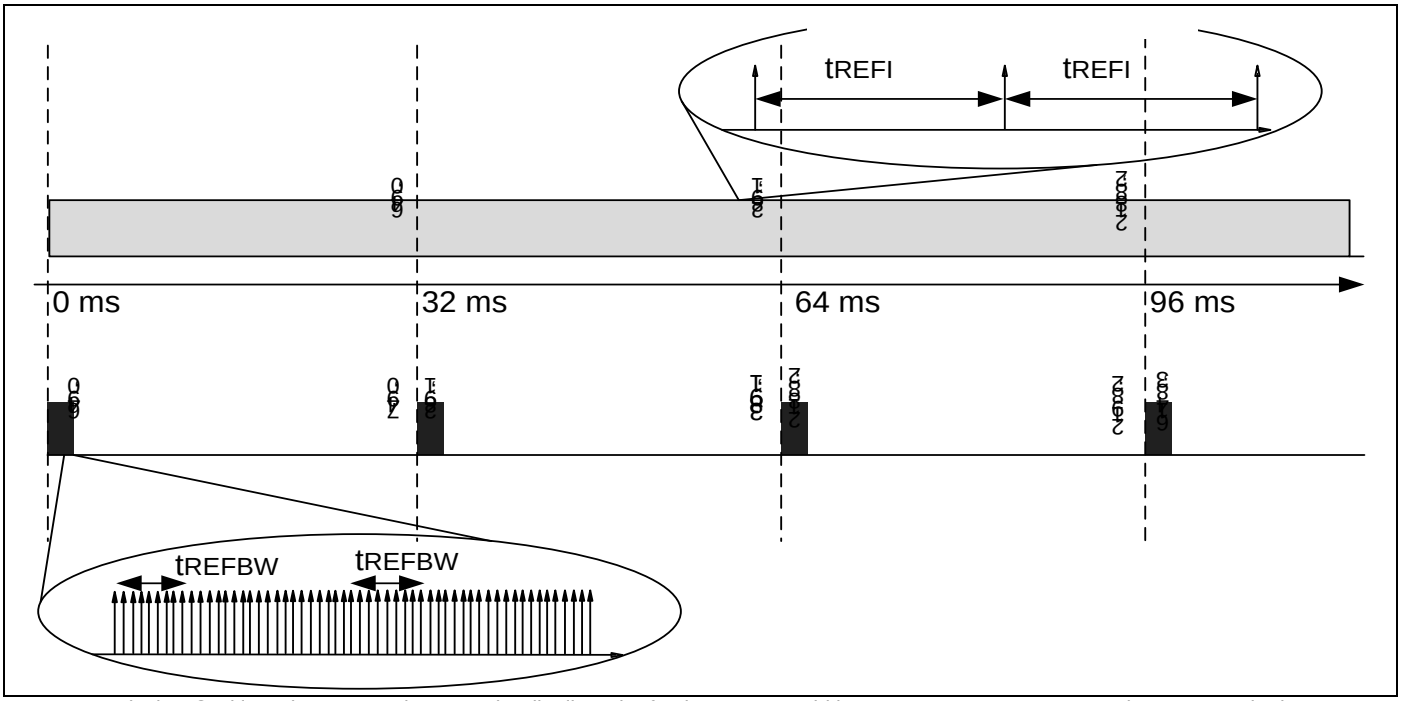
The users may choose to deviate from this regular refresh pattern e.g., to enable a period where no refreshes are required. In the extreme the user may choose to issue a refresh burst of 4096 REFRESH commands with the maximum allowable rate (limited by tREFBW) followed by a long time without any REFRESH commands, until the refresh window is complete, then repeating this sequence. The achieveable time without REFRESH commands is given by tREFW - (R / 8) * tREFBW = tREFW - R * 4 * tRFCab.@ Tj <= 85℃ this can be up to 32 ms - 4096 * 4 * 130 ns ~ 30 ms.

While both - the regular and the burst/pause - patterns can satisfy the refresh requirements per rolling refresh interval, if they are repeated in every subsequent 32 ms window, extreme care must be taken when transitioning from one pattern to another to satisfy the refresh requirement in every rolling refresh window during the transition. If this transition happens directly after the burst refresh phase, all rolling tREFW intervalls will have at least the required number of refreshes.

As an example of a non-allowable transition, the regular refresh pattern starts after the completion of the pause-phase of the burst/pause refresh pattern. For several rolling tREFW intervals the minimmun number of REFRESH commands is not satisfied.

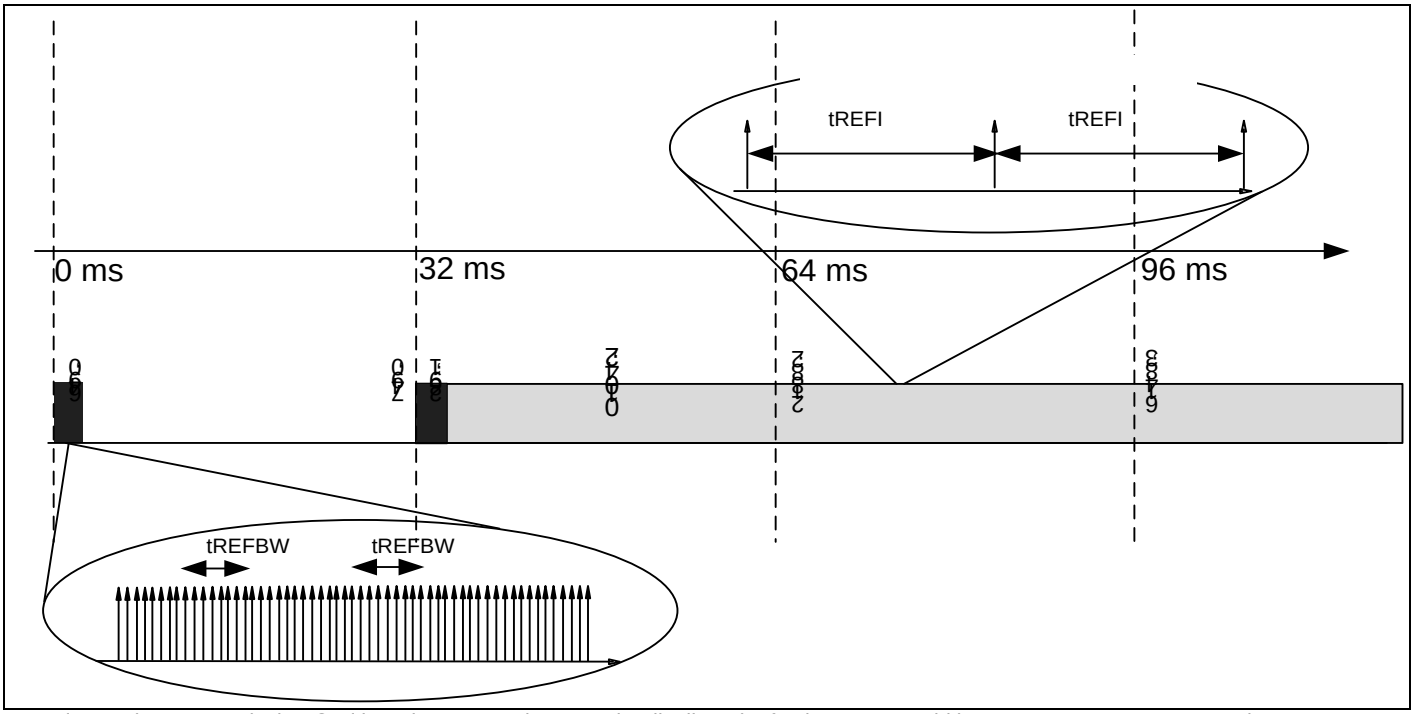
The understanding of the pattern transition is extremly relevant (even if in normal operation only one pattern is employed), as in Self-Refresh-Mode a regular, distributed refresh pattern has to be assumed, which is reflected in the equation for R* above. Therefore it is recommended to enter Self-Refresh-Mode ONLY directly after the burst-phase of a burst/pause refresh pattern and begin with the burst phase upon exit from Self-Refresh.

6.4.16.2 Figure of LPDDR2-S4 Regular, Distributed Refresh Pattern vs. Repetitive Burst Refresh with Subsequent Refresh Pause



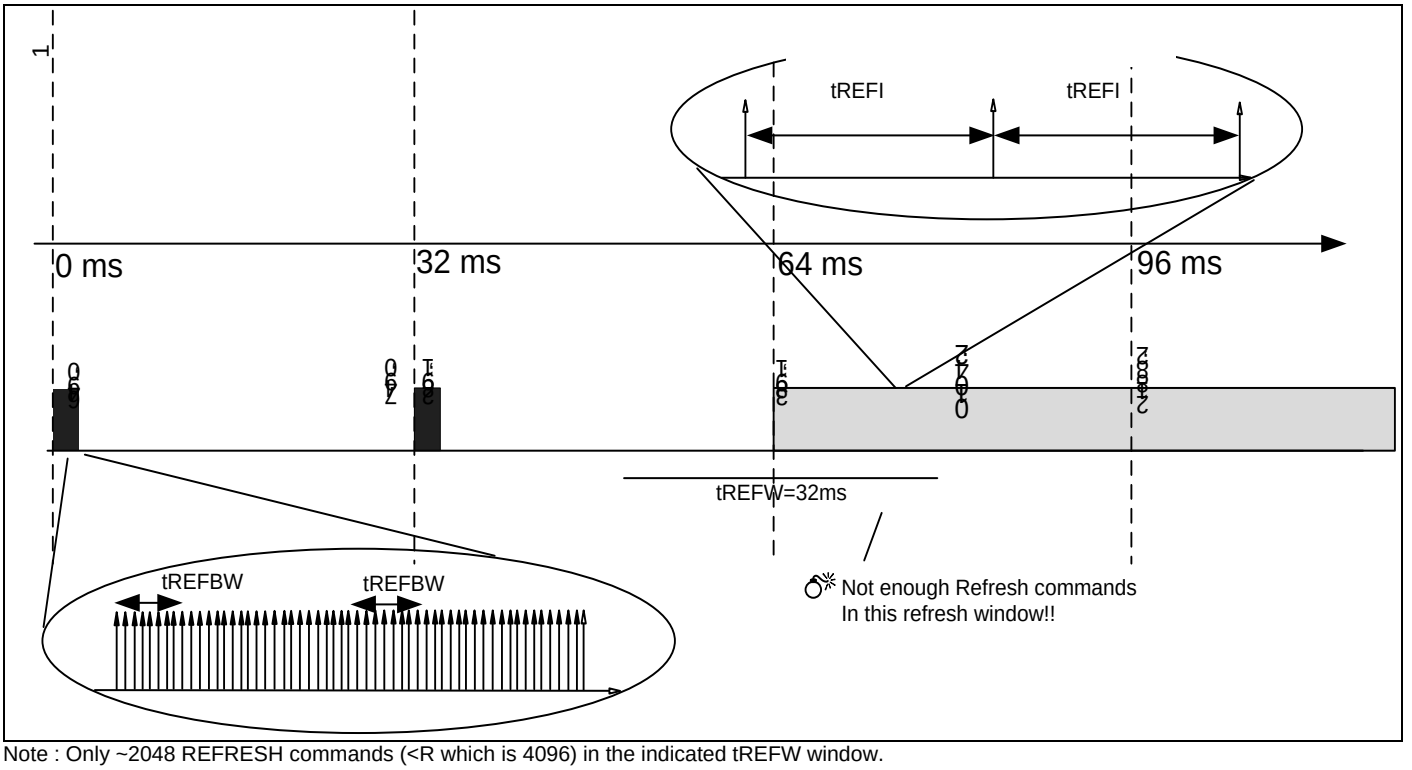
Note : For a device @ Tj less than or equal to 85 C the distributed refresh pattern would have one REFRESH command per 7.8 us; the burst refresh pattern would have one refresh command per 0.52 us followed by ~30 ms without any REFRESH command.

6.4.16.3 Figure of LPDDR2-S4: Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern



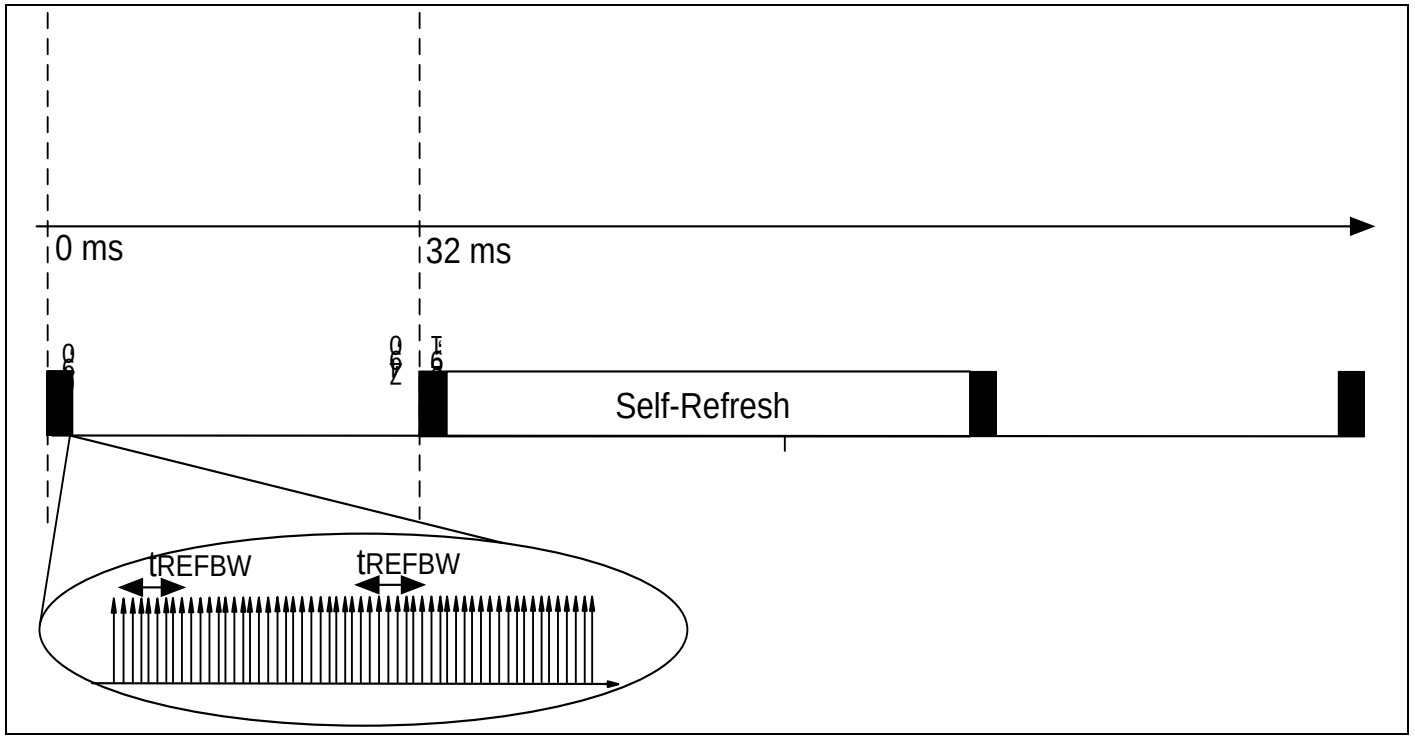
Note : in a 1Gb LPDDR2 device @ Tj less than or equal to 85 C the distributed refresh pattern would have one REFRESH command per 7.8 us; the burst refresh pattern would have one refresh command per 0.52us followed by ~30 ms without any REFRESH command.

6.4.16.4 Figure of LPDDR2-S4: NOT-Allowable Transition from Repetitive Burst Refresh with Subsequent Refresh Pause to Regular, Distributed Refresh Pattern

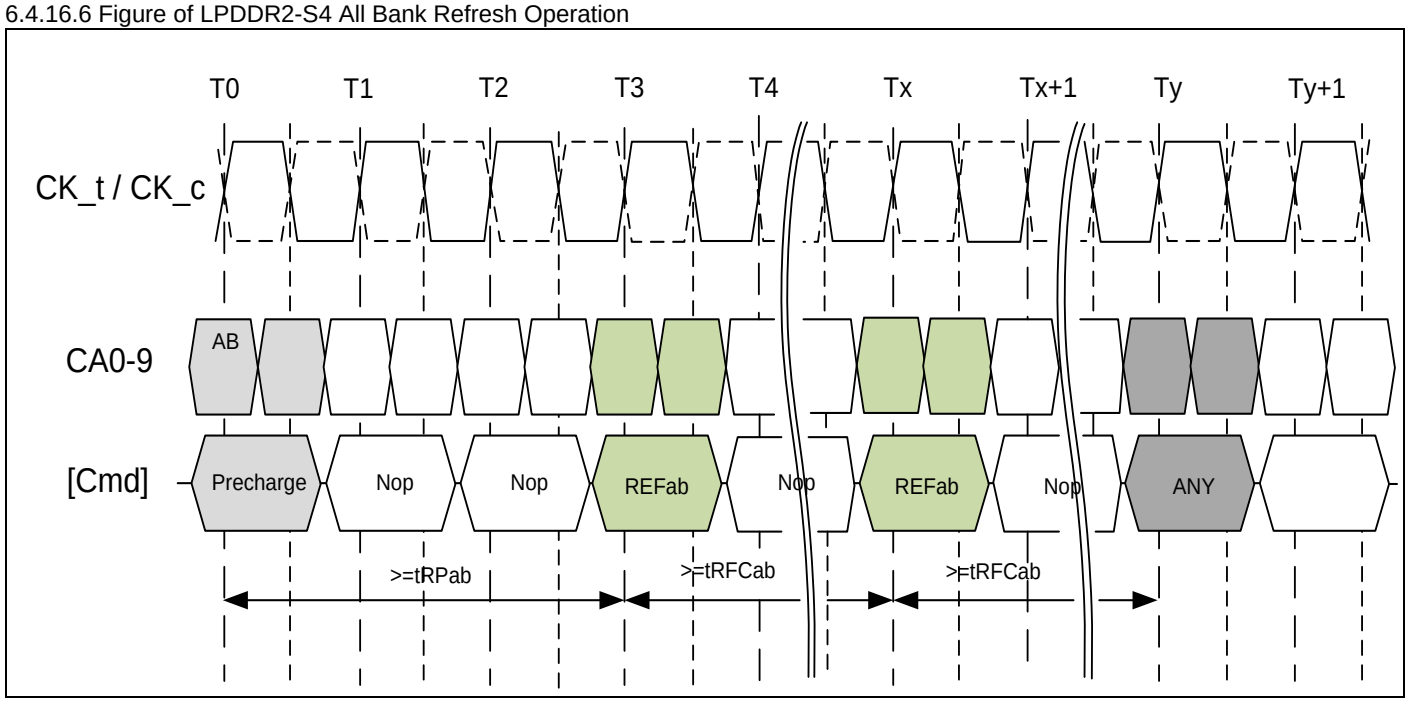


Note : Only ~2048 REFRESH commands (<R which is 4096) in the indicated tREFW window.

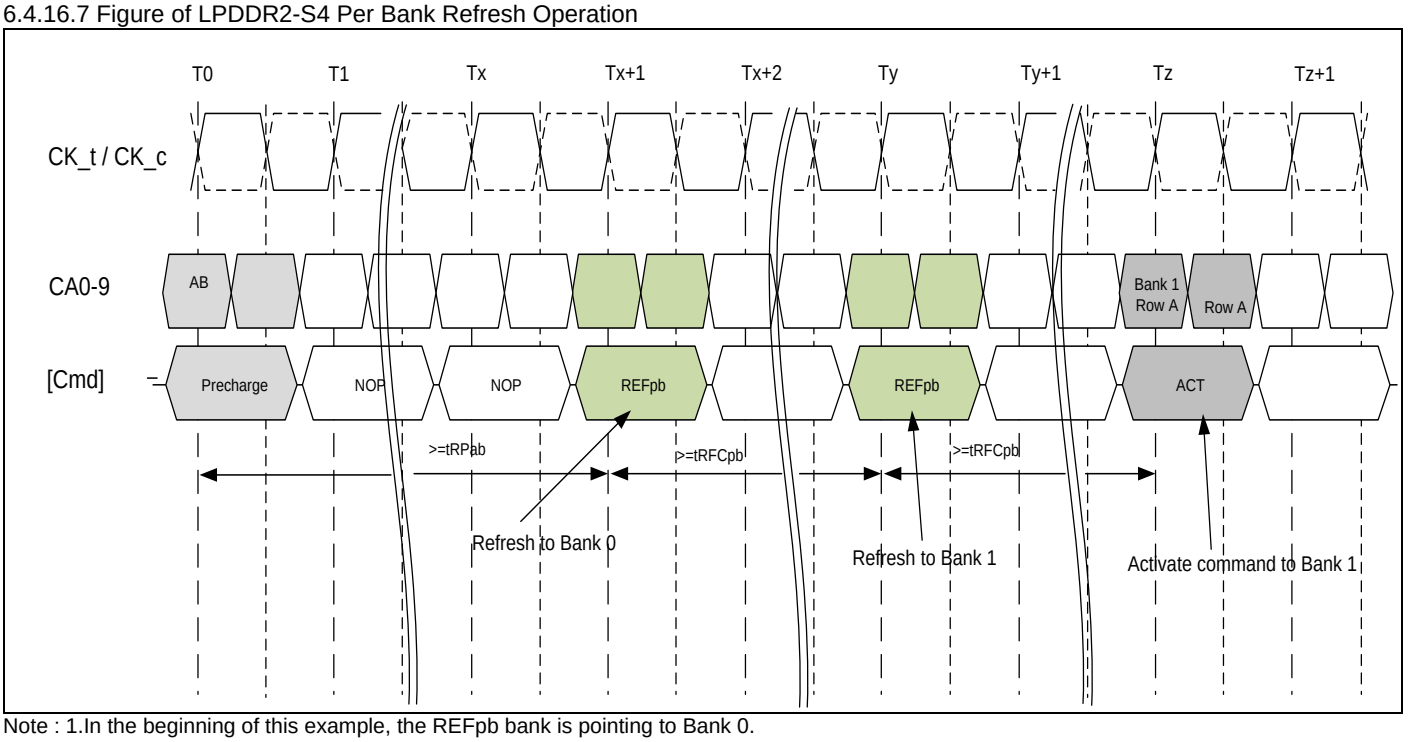
6.4.16.5 Figure of LPDDR2-S4: Recommended Self-refresh entry and exit in conjunction with a Burst/Pause Refresh patterns.



6.4.16.6 Figure of LPDDR2-S4 All Bank Refresh Operation



6.4.16.7 Figure of LPDDR2-S4 Per Bank Refresh Operation



Note : 1.In the beginning of this example, the REFpb bank is pointing to Bank 0.

2.Operations to other banks than the bank being refreshed are allowed during the tRFCpb period.

6.4.17 LPDDR2-S4: Self Refresh operation

The Self Refresh command can be used to retain data in the LPDDR2 SDRAM, even if the rest of the system is powered down. When in the Self Refresh mode, the LPDDR2 SDRAM retains data without external clocking. The LPDDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. The Self Refresh Command is defined by having CKE LOW, CS_n LOW, CA0 LOW, CA1 LOW, and CA2 HIGH at the rising edge of the clock. CKE must be HIGH during the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode.

LPDDR2-S4 devices can operate in Self Refresh in both the Standard or Extended Temperature Ranges. LPDDR2-S4 devices will also manage Self Refresh power consumption when the operating temperature changes, lower at low temperatures and higher temperatures.

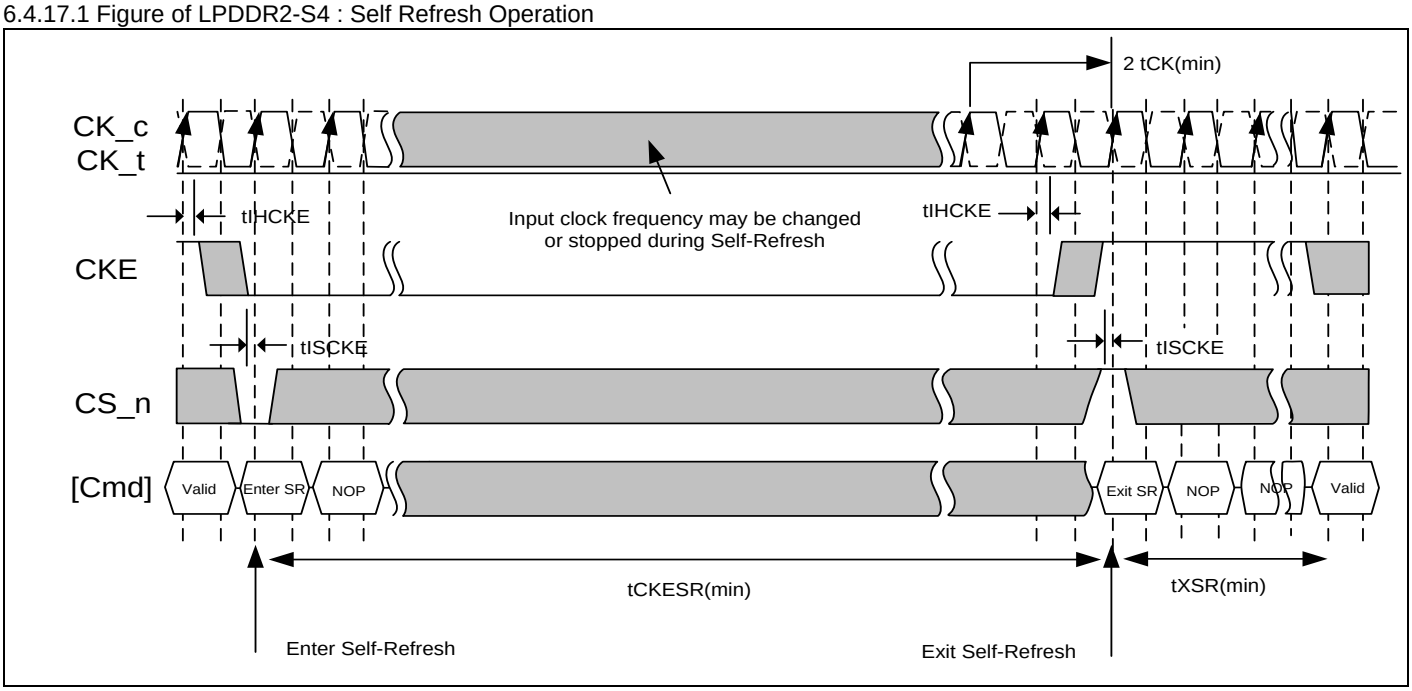
Once the LPDDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are “don’t care”. For proper self refresh operation, power supply pins (VDD1, VDD2, and VDDCA) must be at valid levels.
VDDQ may be turned off during Self-Refresh. Prior to exiting Self-Refresh, VDDQ must be within specified limits.
VrefDQ and VrefCA may be at any level within minimum and maximum levels. However prior to exit Self-Refresh, VrefDQ and VrefCA must be within specified limits. The SDRAM initiates a minimum of one all-bank refresh command internally within tCKESR period once it enters Self Refresh mode. The clock is internally disabled during Self Refresh Operation to save power. The minimum time that the LPDDR2 SDRAM must remain in Self Refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit Self Refresh operation.

The procedure for exiting Self Refresh requires a sequence of commands.First, the clock shall be stable and within specified limits for a minmum of 2 clock cycles prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least tXSR must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period tXSR for proper operation except for self refresh re-entry. NOP commands must be registered on each positive clock edge during the Self Refresh exit interval tXSR.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, it is required that at least one Refresh command (8 per-bank or 1 all-bank) is issued before entry into a subsequent Self Refresh.

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements outlined in section “LPDDR2 SDRAM Refresh Requirements”, since no refresh operations are performed in power-down mode.

6.4.17.1 Figure of LPDDR2-S4 : Self Refresh Operation



Note :1. Input clock frequency may be changed or stopped during self-refresh, provided that upon exiting self-refresh, a minimum of 5 clocks (tINIT2) of stable clock are provided and the clock frequency is between the minimum and maximum frequency for the particular speed grade.

2. Device must be in the “All banks idle” state prior to entering Self Refresh mode.
3. tXSR begins at the rising edge of the clock after CKE is driven HIGH.
4. A valid command may be issued only after tXSR is satisfied. NOPs shall be issued during tXSR.

6.4.18 LPDDR2-S4: Partial Array Self-Refresh: Bank Masking

Each bank of LPDDR2 SDRAM can be independently configured whether a self refresh operation is taking place. One mode register unit of 8 bits accessible via MRW command is assigned to program the bank masking status of each bank up to 8 banks. For bank masking bit assignments, see Mode Register 16

The mask bit to the bank controls a refresh operation of entire memory within the bank. If a bank is masked via MRW, a refresh operation to the entire bank is blocked and data retention by a bank is not guaranteed in self refresh mode. To enable a refresh operation to a bank, a coupled mask bit has to be programmed, “unmasked”. When a bank mask bit is unmasked, a refresh to a bank is determined by the programmed status of segment mask bits, which is decribed in the following chapter.

6.4.19 LPDDR2-S4: Partial Array Self-Refresh: Segment Masking

Segment masking scheme may be used in place of or in combination with bank masking scheme in LPDDR2-S4 SDRAM. The number of segments differ by the density and the setting of each segment mask bit is applied across all the banks. For segment masking bit assignments, see Mode Register 17.

For those refresh-enabled banks, a refresh operation to the address range which is represented by a segment is blocked when the mask bit to this segment is programmed, “masked”. Programming of segment mask bits is similar to the one of bank mask bits.

Example of Bank and Segment Masking use in LPDDR2-S4 devices

	Segment Mask (MR17)	Bank 0	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6	Bank 7
Segment Mask (MR16)		0	1	0	0	0	0	0	1
Segment 0	0	-	M	-	-	-	-	-	M
Segment 1	0	-	M	-	-	-	-	-	M
Segment 2	1	M	M	M	M	M	M	M	M
Segment 3	0	-	M	-	-	-	-	-	M
Segment 4	0	-	M	-	-	-	-	-	M
Segment 5	0	-	M	-	-	-	-	-	M
Segment 6	0	-	M	-	-	-	-	-	M
Segment 7	1	M	M	M	M	M	M	M	M

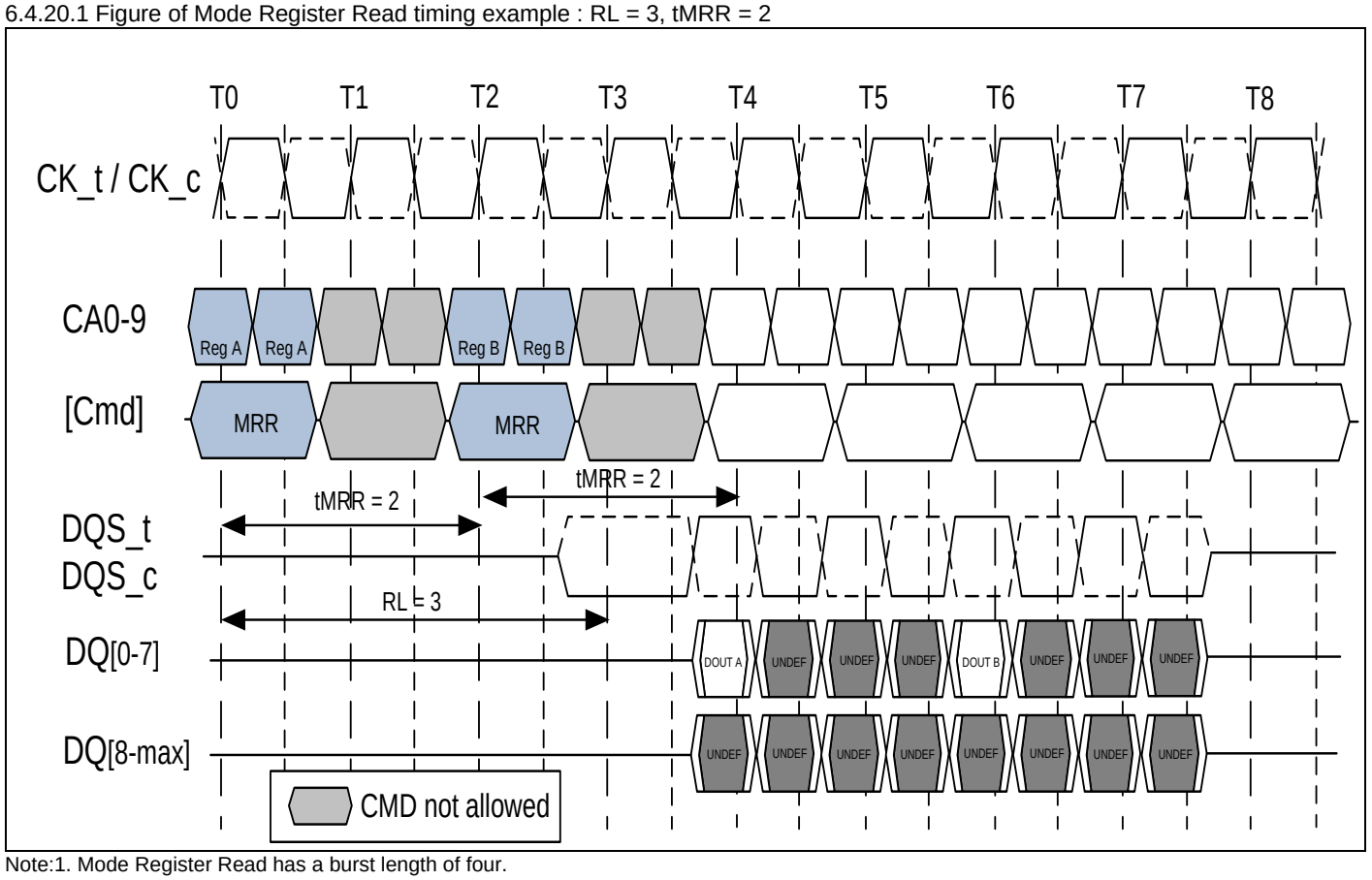
Note : This table illustrates an example of an 8-bank LPDDR2-S4 device, when a refresh operation to bank 1 and bank 7, as well as segment 2 and segment 7 are masked.

6.4.20 Mode Register Read Command

The Mode Register Read command is used to read configuration and status data from mode registers. The Mode Register Read (MRR) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 HIGH at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r- CA4r}. The mode register contents are available on the first data beat of DQ[0:7], RL * tCK + tDQSCK + tDQSQ after the rising edge of the clock where the Mode Register Read Command is issued. Subsequent data beats contain valid, but undefined content.

The MRR command has a burst length of four. The Mode Register Read operation (consisting of the MRR command and the corresponding data traffic) shall not be interrupted. The MRR command period (tMRR) is 2 clock cycles. Mode Register Reads to reserved and write-only registers shall return valid, but undefined content on all data beats and DQS shall be toggled.

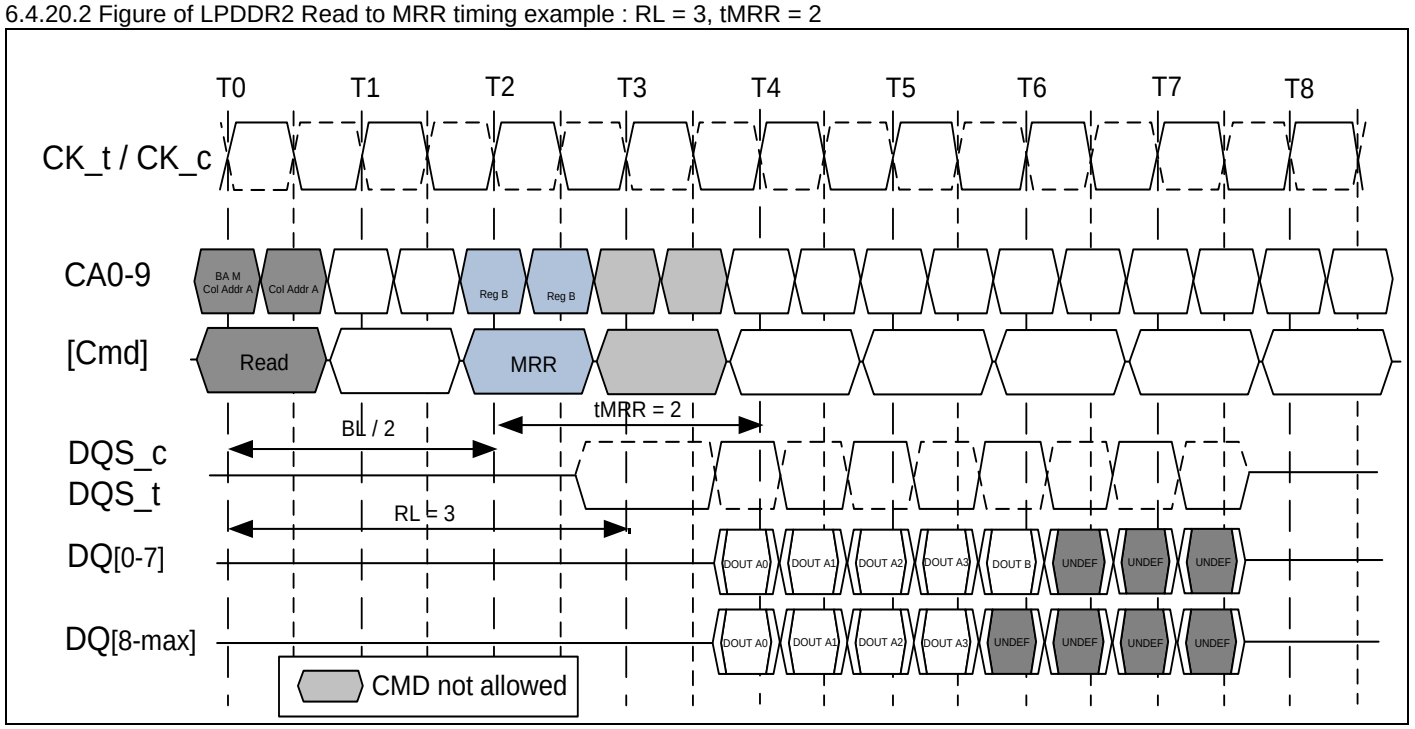
6.4.20.1 Figure of Mode Register Read timing example : RL = 3, tMRR = 2



Note:1. Mode Register Read has a burst length of four.
2. Mode Register Read operation shall not be interrupted.
3. Mode Register data is valid only on DQ[0-7] on the first beat. Subsequent beats contain valid, but undefined data. DQ[8-max] contain valid, but undefined data for the duration of the MRR burst.
4. The Mode Register Command period is tMRR. No command (other than Nop) is allowed during this period.
5. Mode Register Reads to DQ Calibration registers MR32 and MR40 are described in the section on DQ Calibration.
6. Minimum Mode Register Read to write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 - WL clock cycles.
7. Minimum Mode Register Read to Mode Register Write latency is RL + RU(tDQSCKmax/tCK) + 4/2 + 1 clock cycles.

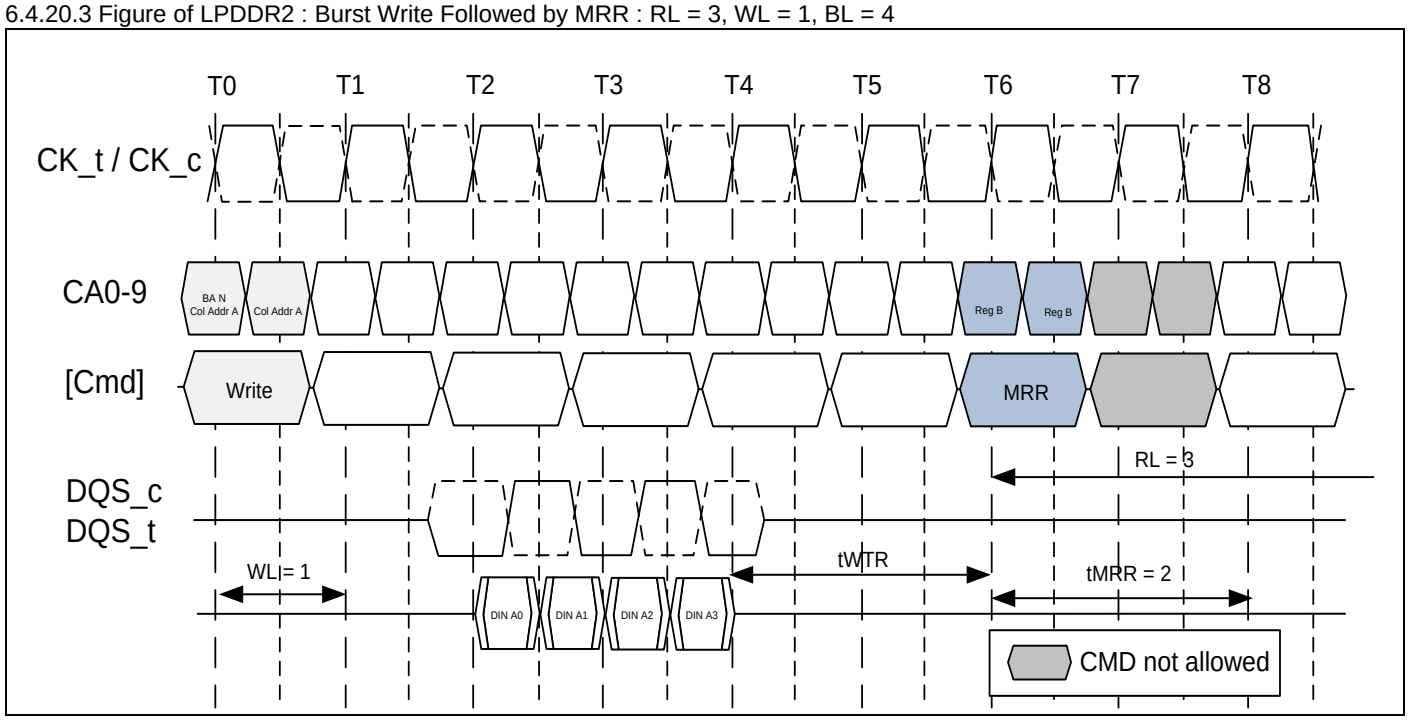
The MRR command shall not be issued earlier than BL/2 clock cycles after a prior Read command and WL + 1 + BL/2 + RU(tWTR/tCK) clock cycles after a prior Write command, because read-bursts and write-bursts shall not be truncated by MRR. Note that if a read or write burst is truncated with a Burst Terminate (BST) command, the effective burst length of the truncated burst should be used as “BL.”

6.4.20.2 Figure of LPDDR2 Read to MRR timing example : RL = 3, tMRR = 2



Note :1.The minimum number of clocks from the burst read command to the Mode Register Read command is BL/2.
2.The Mode Register Read Command period is tMRR. No command (other than Nop) is allowed during this period

6.4.20.3 Figure of LPDDR2 : Burst Write Followed by MRR : RL = 3, WL = 1, BL = 4



Note :1.The minimum number of clock cycles from the burst write command to the Mode Register Read command is [WL + 1 + BL/2 + RU(tWTR/tCK)].
2.The Mode Register Read Command period is tMRR. No command (other than No) is allowed during this period

6.4.21 Temperature Sensor

LPDDR2 SDRAM features a temperature sensor whose status can be read from MR4. This sensor can be used to determine an appropriate refresh rate (SDRAM), determine whether AC timing derating is required in the Extended Temperature Range and/or monitor the operating temperature. Either the temperature sensor or the device TOPER (See “Operating Temperature Conditions”) may be used to determine whether operating temperature requirements are being met.

LPDDR2 devices shall monitor device temperature and update MR4 according to tTSI. Upon exiting self-refresh or power-down, the device temperature status bits shall be no older than tTSI.

When using the temperature sensor, the actual device temperature may be higher than the TOPER specification (See “Operating Temperature Conditions” that applies for the Standard or Extended Temperature Ranges. For example, Tj may be above 85 ºC when MR4[2:0] equals 011b.

To assure proper operation using the temperature sensor, applications should consider the following factors:

TempGradient is the maximum temperature gradient experienced by the memory device at the temperature of interest over a range of 2ºC.

ReadInterval is the time period between MR4 reads from the system.

TempSensorInterval (tTSI) is maximum delay between internal updates of MR4.

SysRespDelay is the maximum time between a read of MR4 and the response by the system.

TempMargin: LPDDR2 devices shall allow for a 2ºC temperature margin between the point at which the device temperature enters the Extended Temperature Range and point at which the controller re-configures the system accordingly.

Symbol	Parameter	Max/Min	Value	Unit
TempGradient	System Temperature Gradient	Max	System Dependent	ºC/s
ReadInterval	MR4 Read Interval	Max	System Dependent	ms
tTSI	Temperature Sensor Interval	Max	32	ms
SysRespDelay	System Response Delay	Max	System Dependent	ms
TempMargin	Device Temperature Margin	Max	2	ºC

In order to determine the required frequency of polling MR4, the system shall use the maximum TempGradient and the maximum response time of the system using the following equation:

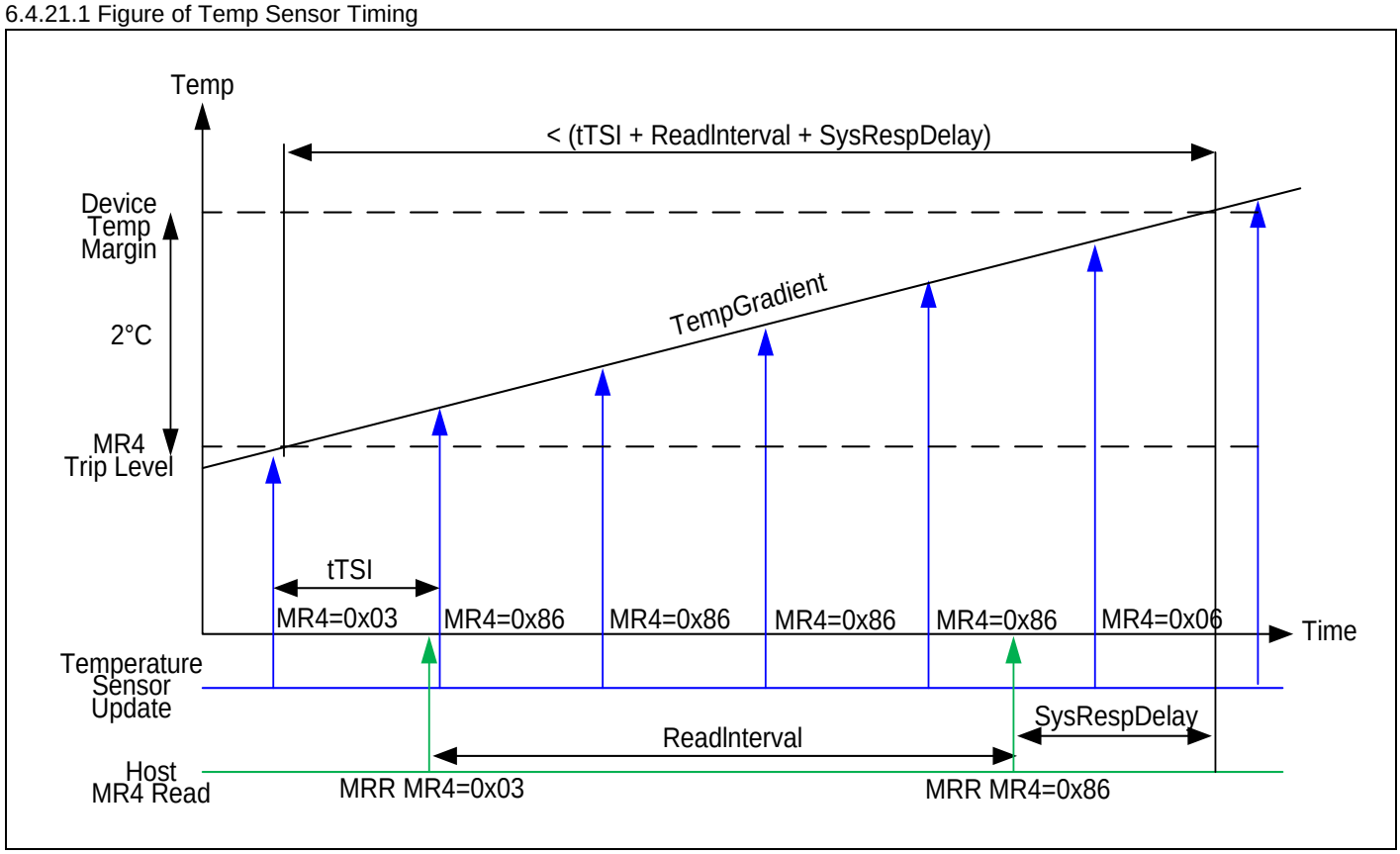
TempGradient x (ReadInterval + tTSI + SysRespDelay) ≤2C

For example, if TempGradient is 10ºC/s and the SysRespDelay is 1 ms:

10ºC/s * (ReadInterval+32ms+1ms) ≤2C

In this case, ReadInterval shall be no greater than 167ms.

6.4.21.1 Figure of Temp Sensor Timing



6.4.21.2 DQ Calibration

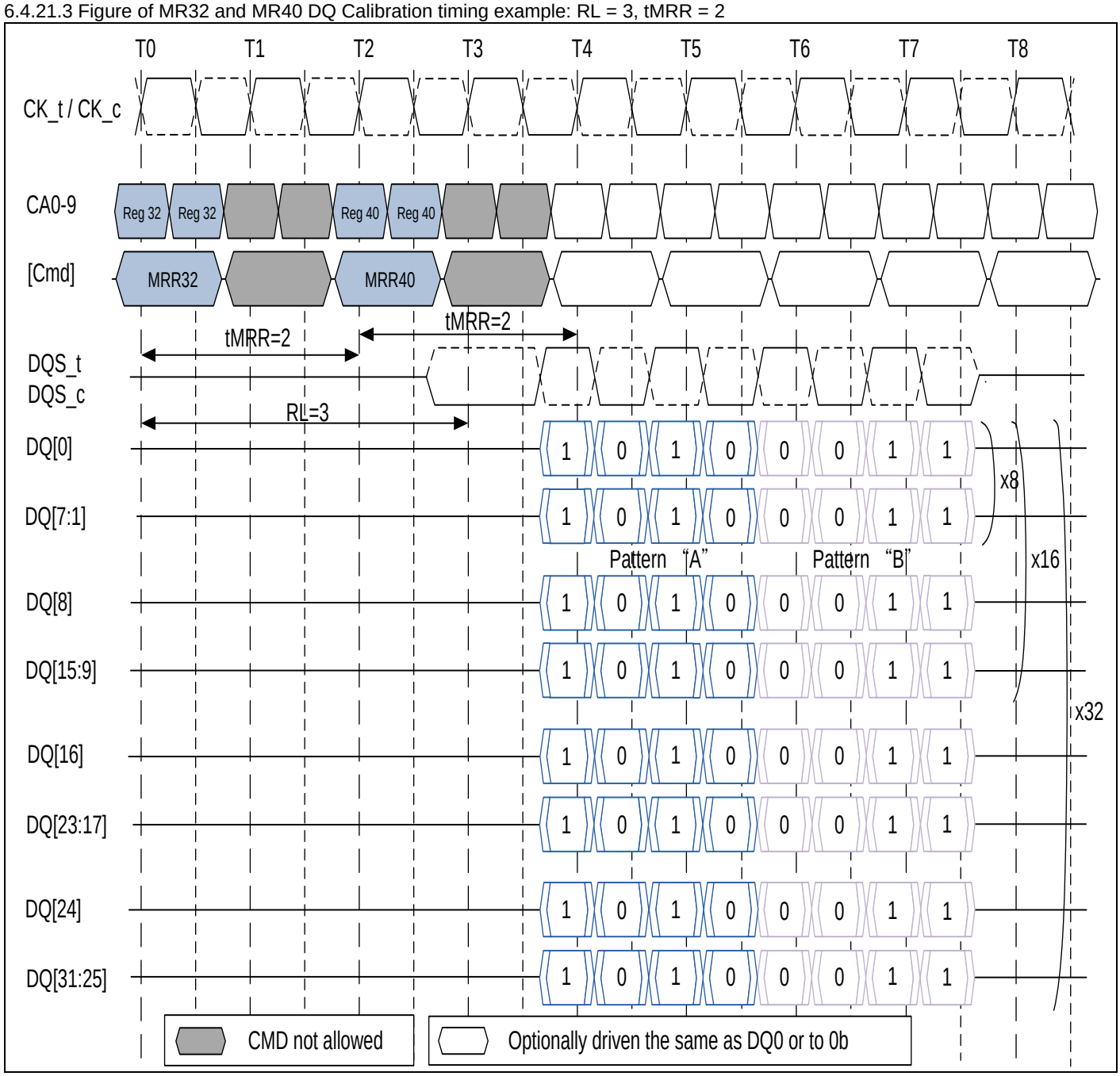
LPDDR2-S4 device features a DQ Calibration function that outputs one of two predefined system timing calibration patterns. A Mode Register Read to MR32 (Pattern “A”) or MR40 (Pattern “B”) will return the specified pattern on DQ[0], DQ[8], DQ[16], and DQ[24] for x32 devices.

For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or may drive 0b during the MRR burst.

For LPDDR2-S4 devices, MRR DQ Calibration commands may only occur in the Idle state.

Pattern	MR#	Bit Time 0	Bit Time 1	Bit Time 2	Bit Time 3	Description
Pattern A	MR32	1	0	1	0	Read to MR32 return DQ calibration pattern A
Pattern B	MR40	0	0	1	1	Read to MR32 return DQ calibration pattern B

6.4.21.3 Figure of MR32 and MR40 DQ Calibration timing example: RL = 3, tMRR = 2



NOTE : 1. Mode Register Read has a burst length of four.

2. Mode Register Read operation shall not be interrupted.

3. Mode Register Reads to MR32 and MR40 drive valid data on DQ[0] during the entire burst. For x32 devices, DQ[8], DQ[16], and DQ[24] shall drive the same information as DQ[0] during the burst.

4. ~~For x8 devices, DQ[7:1] may optionally drive the same information as DQ[0] or they may drive 0b during the burst.~~ For x32 devices, DQ[7:1], DQ[15:9], DQ[23:17], and DQ[31:25] may optionally drive the same information as DQ[0] or they may drive 0b during the burst.

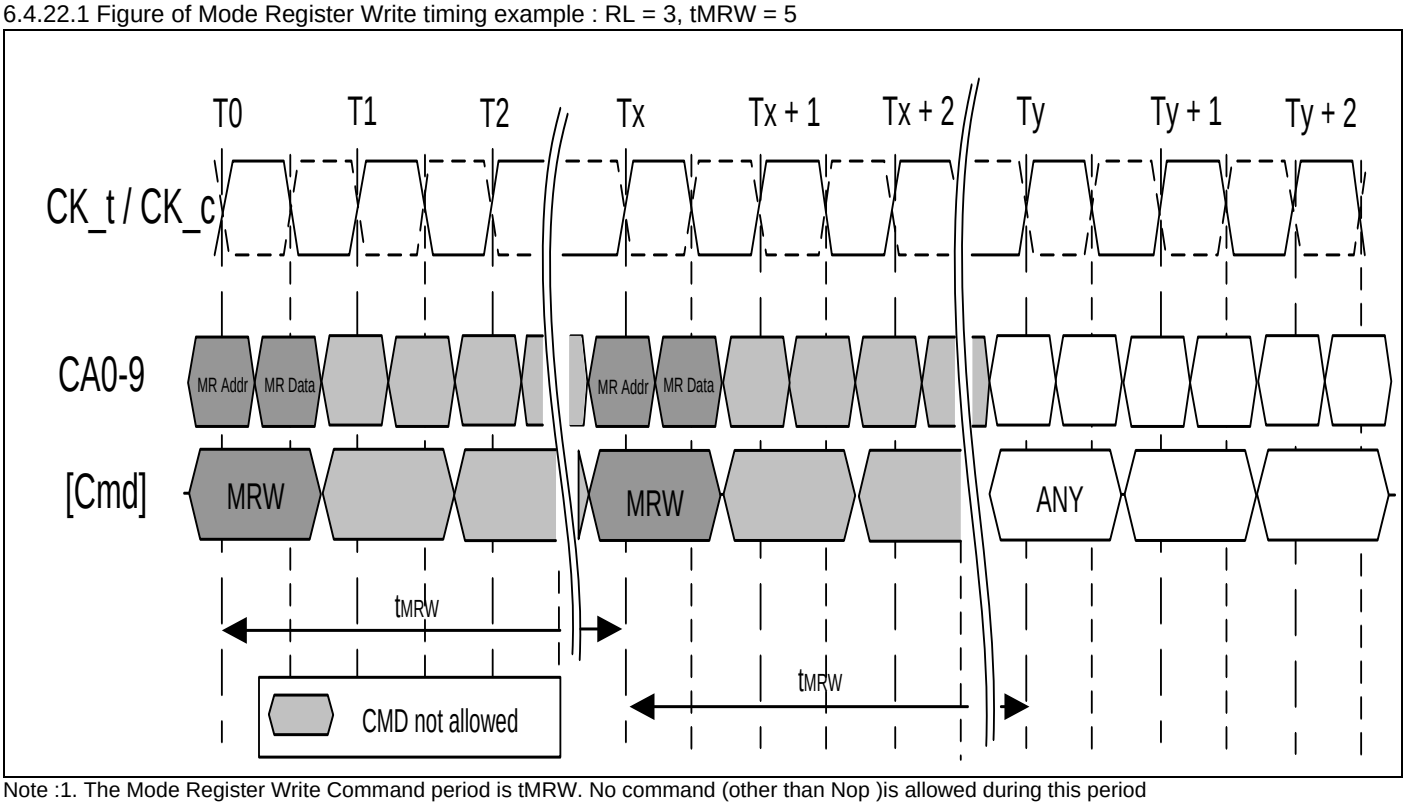
5. The Mode Register Command period is tMRR. No command (other than Nop) is allowed during this period.

6.4.22 Mode Register Write Command

The Mode Register Write command is used to write configuration data to mode registers. The Mode Register Write (MRW) command is initiated by having CS_n LOW, CA0 LOW, CA1 LOW, CA2 LOW, and CA3 LOW at the rising edge of the clock. The mode register is selected by {CA1f-CA0f, CA9r-CA4r}. The data to be written to the mode register is contained in CA9f-CA2f. The MRW command period is defined by tMRW. Mode Register Writes to read-only registers shall have no impact on the functionality of the device.

For LPDDR2-S4 devices, the MRW may only be issued when all banks are in the idle precharge state. One method of ensuring that the banks are in the idle precharge state is to issue a Precharge-All command

6.4.22.1 Figure of Mode Register Write timing example : RL = 3, tMRW = 5



Note :1. The Mode Register Write Command period is tMRW. No command (other than Nop)is allowed during this period
2. At time Ty, the device is in the idle state

6.4.22.2 Truth Table for Mode Register Read (MRR) and Mode Register Write (MRW)

Current State	Command	Intermediate State	Next State
All Banks Idle	MRR	Mode Register Reading (All Banks Idle)	All Banks Idle
	MRW	Mode Register Writing (All Banks Idle)	All Banks Idle
	MRW (RESET)	Resetting (Device Auto-Init)	All Banks Idle
Bank(s) Active	MRR	Mode Register Reading (Bank(s) Active)	Bank(s) Active
	MRW	Not Allowed	Not Allowed
	MRW (RESET)	Not Allowed	Not Allowed

6.4.23 Mode Register Write Reset (MRW Reset)

Any MRW command issued to MRW63 initiates an MRW Reset. The MRW Reset command brings the device to the Device Auto-Initialization (Resetting) State in the Power-On Initialization sequence. The MRW Reset command may be issued from the Idle state for LPDDR2-S4 devices. This command resets all Mode Registers to their default values. No commands other than NOP may be issued to the LPDDR2 device during the MRW Reset period (tINIT4). After MRW Reset, boot timings must be observed until the device initialization sequence is complete and the device is in the Idle state. Array data for LPDDR2-S4 devices are undefined after the MRW Reset command.

6.4.24 Mode Register Write ZQ Calibration Command

The MRW command is also used to initiate the ZQ Calibration command. The ZQ Calibration command is used to calibrate the LPDDR2 ouput drivers (RON) over process, temperature, and voltage. LPDDR2-S4 devices support ZQ Calibration.

There are four ZQ Calibration commands and related timings times, tZQINIT, tZQRESET, tZQCL, and tZQCS. tZQINIT corresponds to the initialization calibration, tZQRESET for resetting ZQ setting to default, tZQCL is for long calibration, and tZQCS is for short calibration.

The Initialization ZQ Calibration (ZQINIT) shall be performed for LPDDR2-S4 devices. This Initialization Calibration achieves a RON accuracy of +/-15%. After initialization, the ZQ Long Calibration may be used to re-calibrate the system to a RON accuracy of +/-15%. A ZQ Short Calibration may be used periodically to compensate for temperature and voltage drift in the system.

The ZQReset Command resets the RON calibration to a default accuracy of +/-30% across process, voltage, and temperature. This command is used to ensure RON accuracy to +/-30% when ZQCS and ZQCL are not used.

One ZQCS command can effectively correct a minimum of 1.5% (ZQCorrection) of RON impedance error within tZQCS for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity'. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.

One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the LPDDR2 is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where TSens = max(dRONdT) and VSens = max(dRONdV) define the LPDDR2 temperature and voltage sensitivities.

For example, if TSens = 0.75% / oC, VSens = 0.20% / mV, Tdriftrate = 1 oC / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

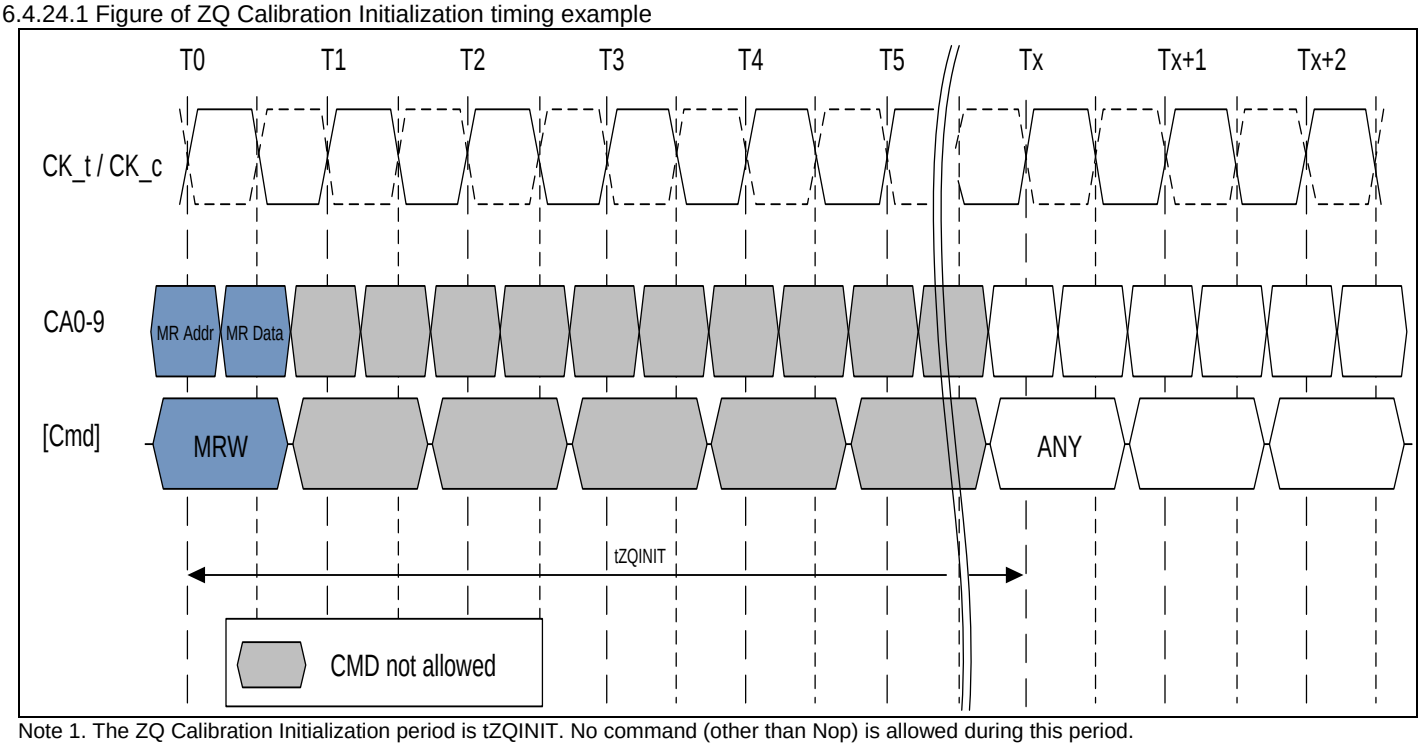
$$\frac{1.5}{(0.75 \times 1) + (0.20 \times 15)} = 0.4s$$

For LPDDR2-S4 devices, a ZQ Calibration command may only be issued when the device is in Idle state with all banks precharged.

No other activities can be performed on the LPDDR2 data bus during the calibration period (tZQINIT, tZQCL, tZQCS). The quiet time on the LPDDR2 data bus helps to accurately calibrate RON. There is no required quiet time after the ZQ Reset command. If multiple devices share a single ZQ Resistor, only one device may be calibrating at any given time. After calibration is achieved, the LPDDR2 device shall disable the ZQ ball's current consumption path to reduce power.

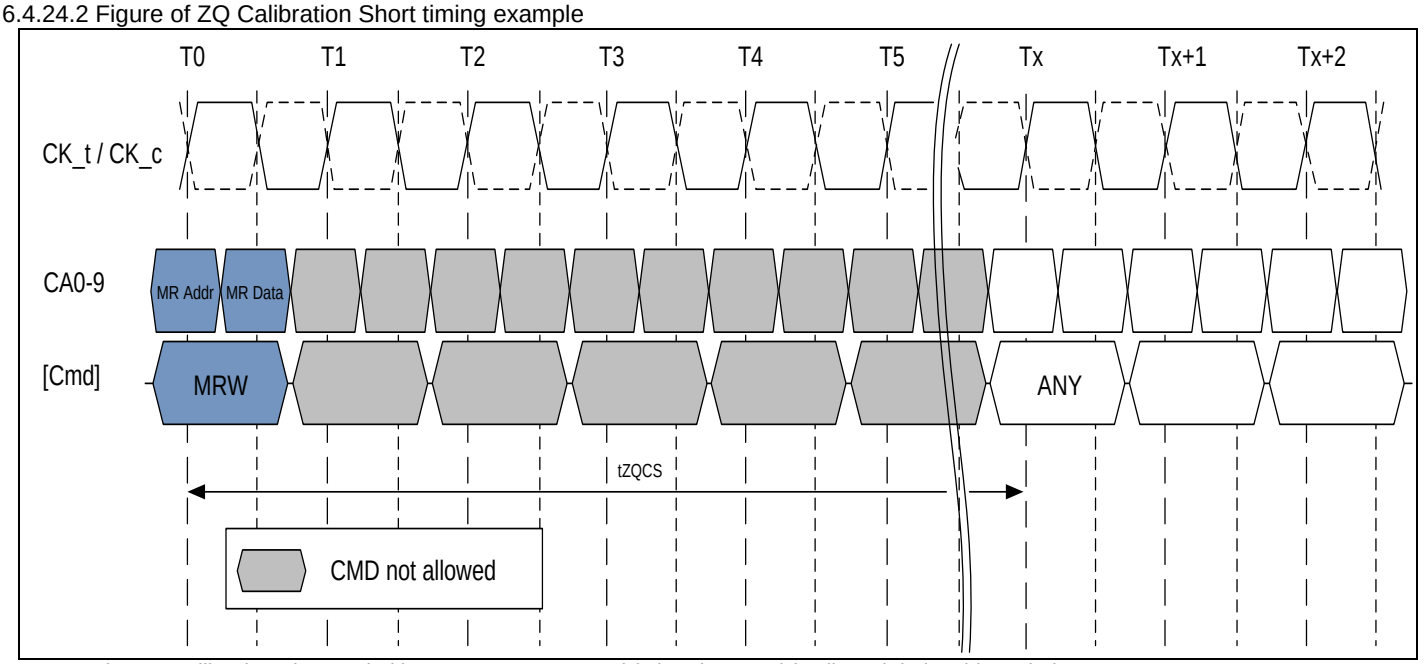
In systems that share the ZQ resistor between devices, the controller must not allow overlap of tZQINIT, tZQCS, or tZQCL between the devices. ZQ Reset overlap is allowed. If the ZQ resistor is absent from the system, ZQ shall be connected to VDDCA. In this case, the LPDDR2 device shall ignore ZQ calibration commands and the device will use the default calibration settings.

6.4.24.1 Figure of ZQ Calibration Initialization timing example



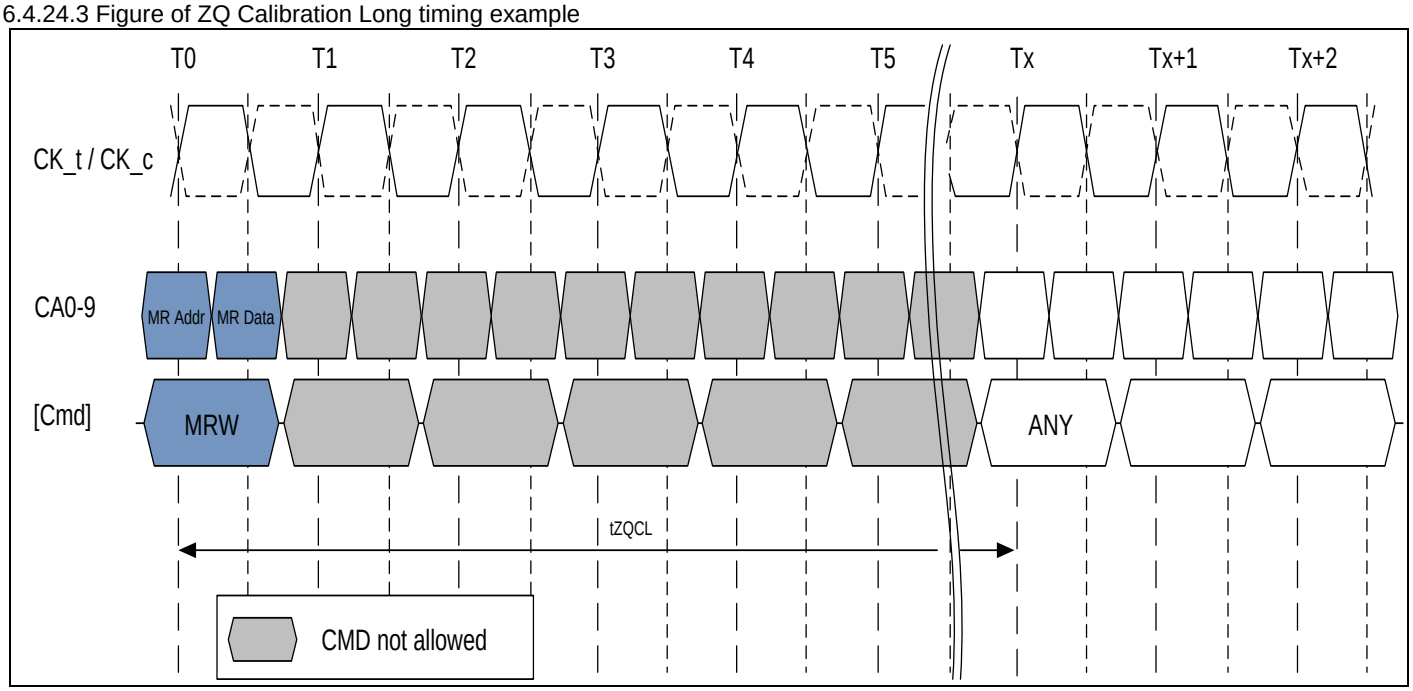
Note 1. The ZQ Calibration Initialization period is tZQINIT. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

6.4.24.2 Figure of ZQ Calibration Short timing example



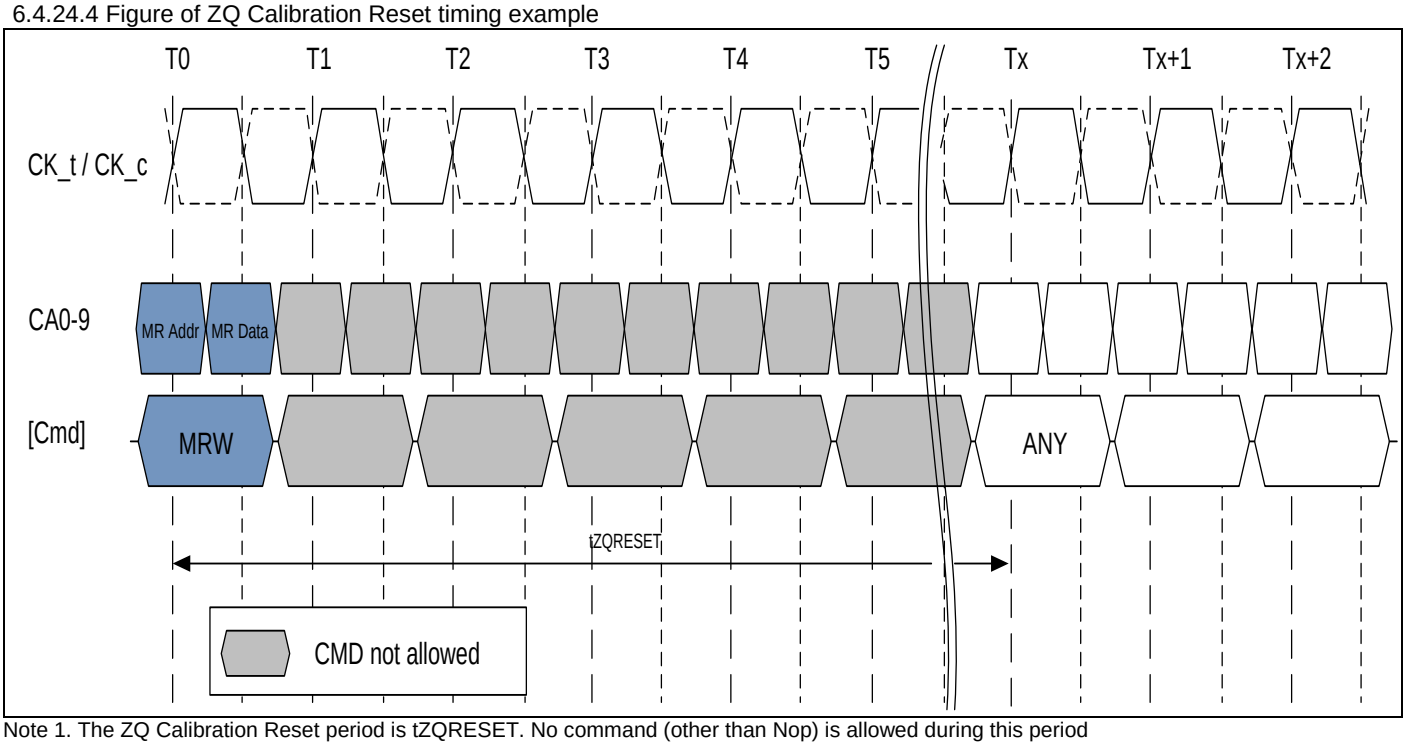
Note 1. The ZQ Calibration Short period is tZQCS. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

6.4.24.3 Figure of ZQ Calibration Long timing example



Note 1. The ZQ Calibration Long period is tZQCL. No command (other than Nop) is allowed during this period.
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

6.4.24.4 Figure of ZQ Calibration Reset timing example



Note 1. The ZQ Calibration Reset period is tZQRESET. No command (other than Nop) is allowed during this period
2. CKE must be continuously registered HIGH during the calibration period.
3. All devices connected to the DQ bus should be high impedance during the calibration process.

6.4.25 ZQ External Resistor Value, Tolerance, and Capacitive Loading

To use the ZQ Calibration function, a 240 Ohm +/- 1% tolerance external resistor must be connected between the ZQ pin and ground. A single resistor can be used for each LPDDR2 device or one resistor can be shared between multiple LPDDR2 devices if the ZQ calibration timings for each LPDDR2 device do not overlap. The total capacitive loading on the ZQ pin must be limited.

6.4.26 Power-down

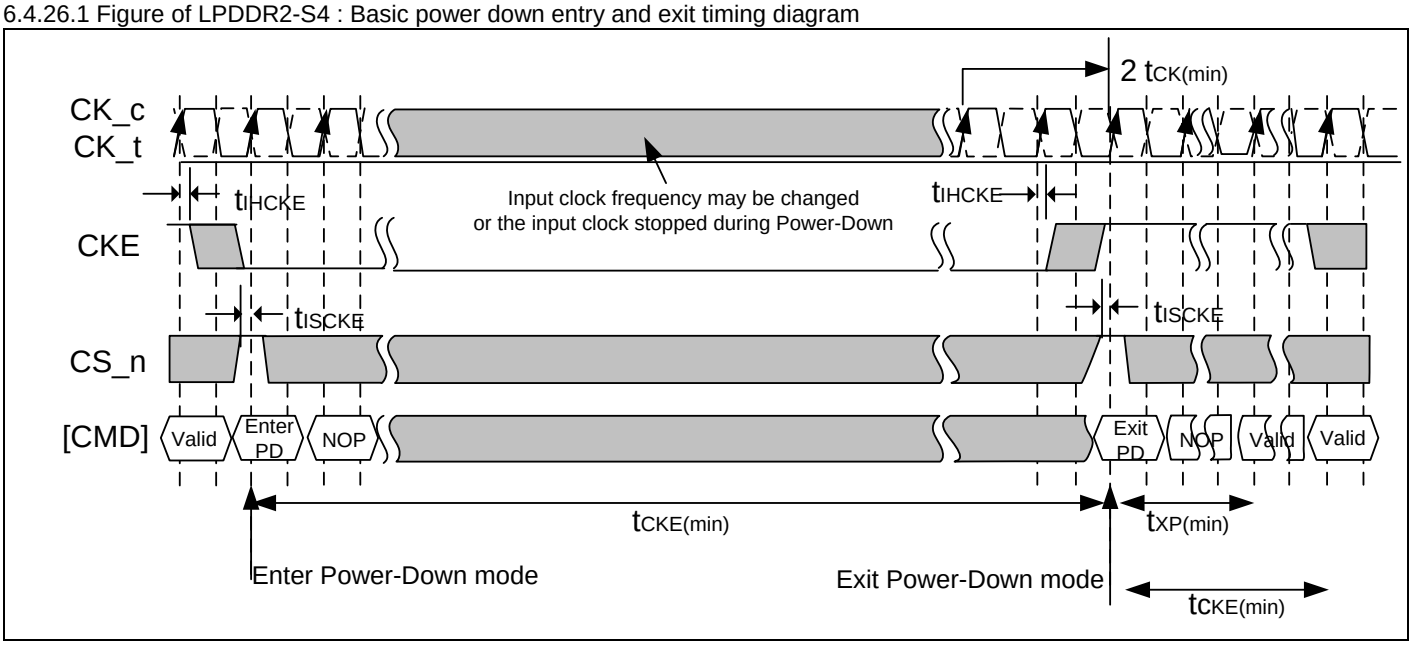
For LPDDR2 SDRAM, power-down is synchronously entered when CKE is registered LOW and CS_n HIGH at the rising edge of clock. CKE must be registered HIGH in the previous clock cycle. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress. CKE is allowed to go LOW while any of other operations such as row activation, precharge, autoprecharge, or refresh is in progress, but power-down IDD spec will not be applied until finishing those operations.

For LPDDR2 SDRAM, if power-down occurs when all banks are idle, this mode is referred to as idle power- down; if power-down occurs when there is a row active in any bank, this mode is referred to as active power-down.
Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, and CKE. In power-down mode, CKE must be maintained LOW while all other input signals are “Don’t Care”. CKE LOW must be maintained until tCKE has been satisfied. VREF must be maintained at a valid level during power down.,
VDDQ may be turned off during power down. If VDDQ is turned off, then VREFDQ must also be turned off. Prior to exiting power down, both VDDQ and VREFDQ must be within their respective min/max operating ranges.

For LPDDR2 SDRAM, the maximum duration in power-down mode is only limited by the refresh requirements, as no refresh operations are performed in power-down mode.

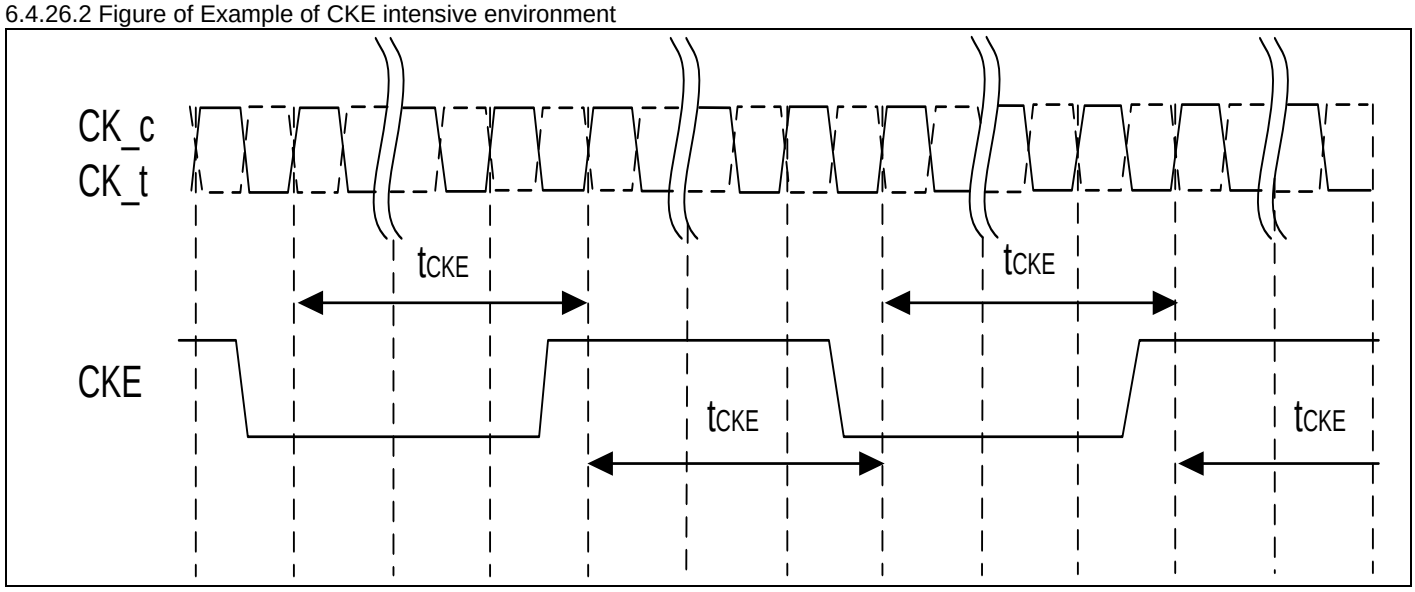
The power-down state is exited when CKE is registered HIGH. The controller shall drive CS_n HIGH in conjunction with CKE HIGH when exiting the power-down state. CKE HIGH must be maintained until tCKE has been satisfied. A valid, executable command can be applied with power-down exit latency, tXP after CKE goes HIGH.

6.4.26.1 Figure of LPDDR2-S4 : Basic power down entry and exit timing diagram

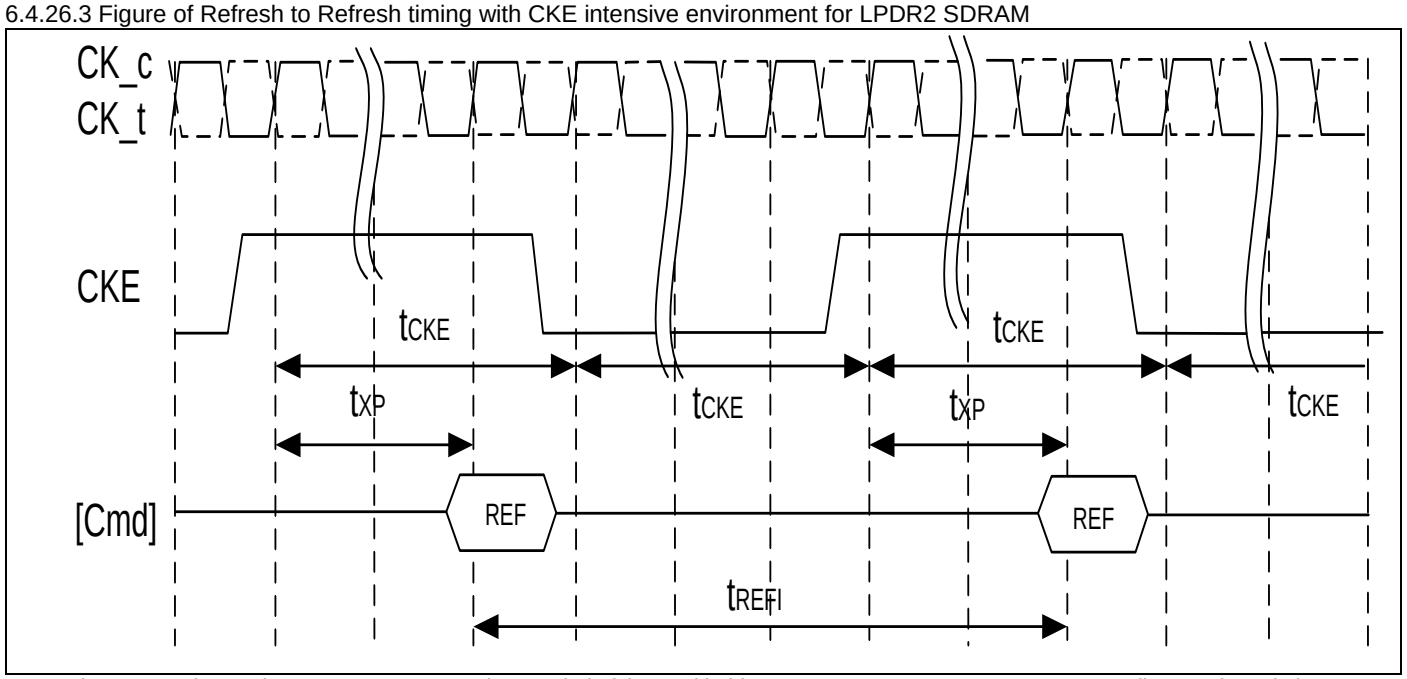


Note :1. Input clock frequency may be changed or the input clock stopped during power-down, provided that upon exiting power-down, the clock is stable and within specified limits for a minmum of 2 clock cycles prior to power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade

6.4.26.2 Figure of Example of CKE intensive environment

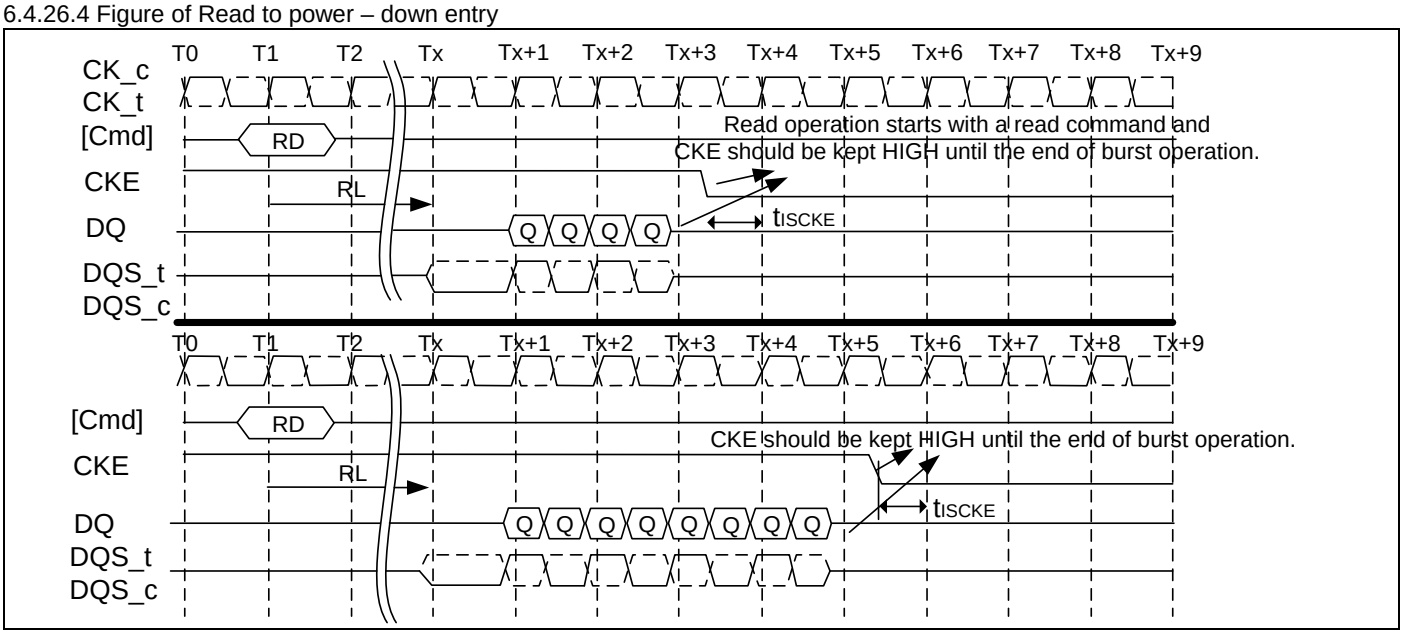


6.4.26.3 Figure of Refresh to Refresh timing with CKE intensive environment for LPDR2 SDRAM



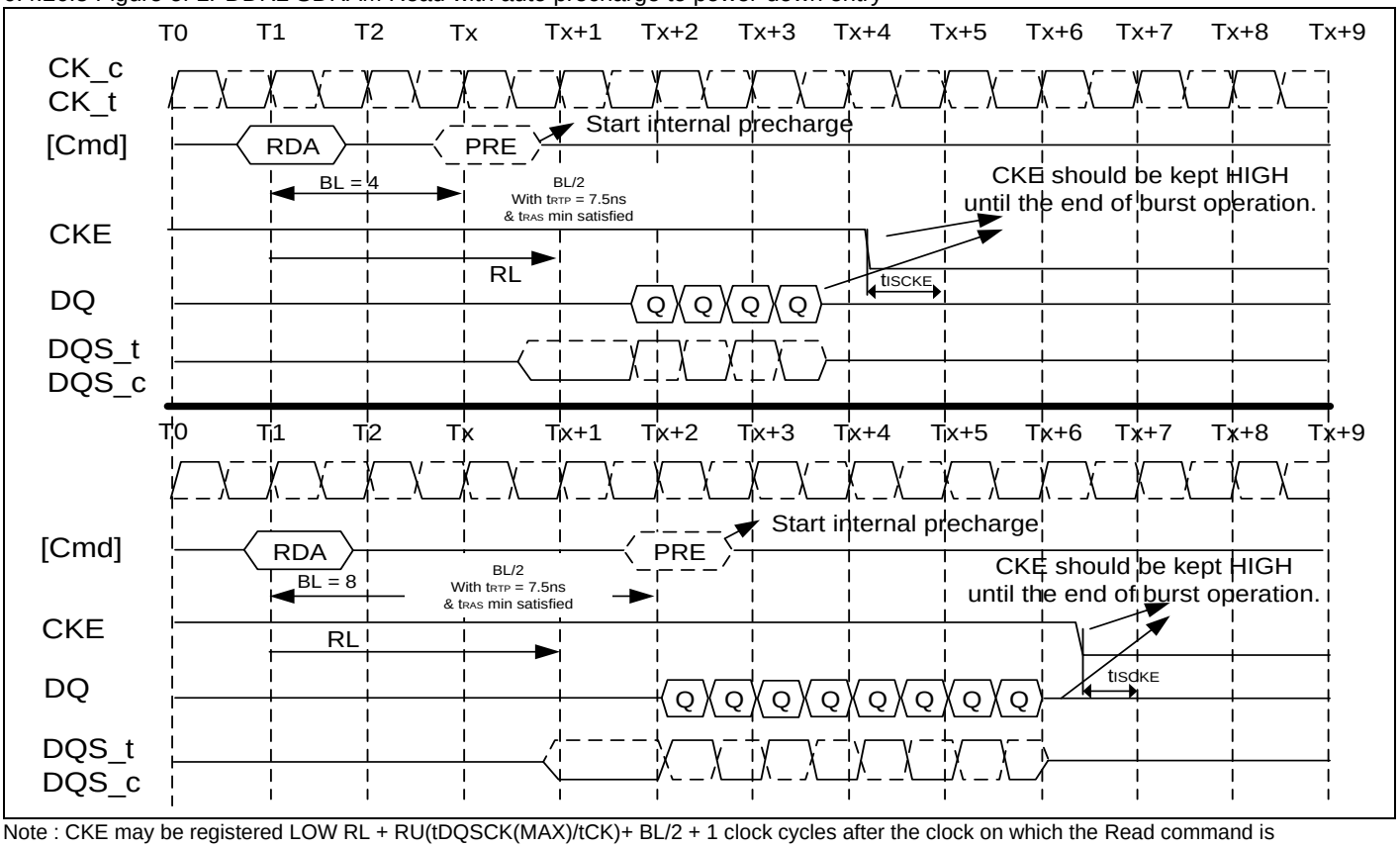
Note : The pattern shown above can repeat over a long period of time. With this pattern, LPDDR2 SDRAM guarantees all AC and DC timing & voltage specifications with temperature and voltage drift

6.4.26.4 Figure of Read to power – down entry



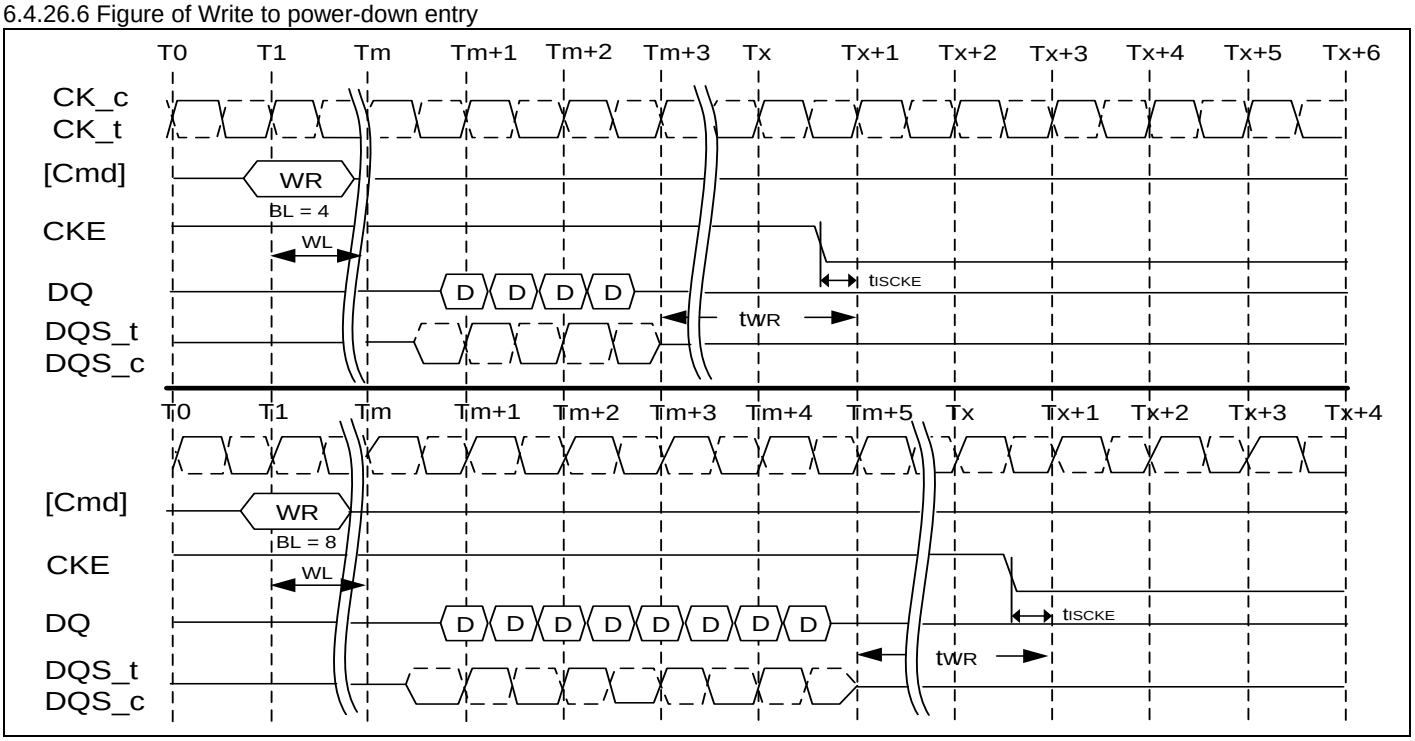
Note : CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK) + BL/2 + 1 clock cycles after the clock on which the Read command is registered

6.4.26.5 Figure of LPDDR2 SDRAM Read with auto precharge to power-down entry



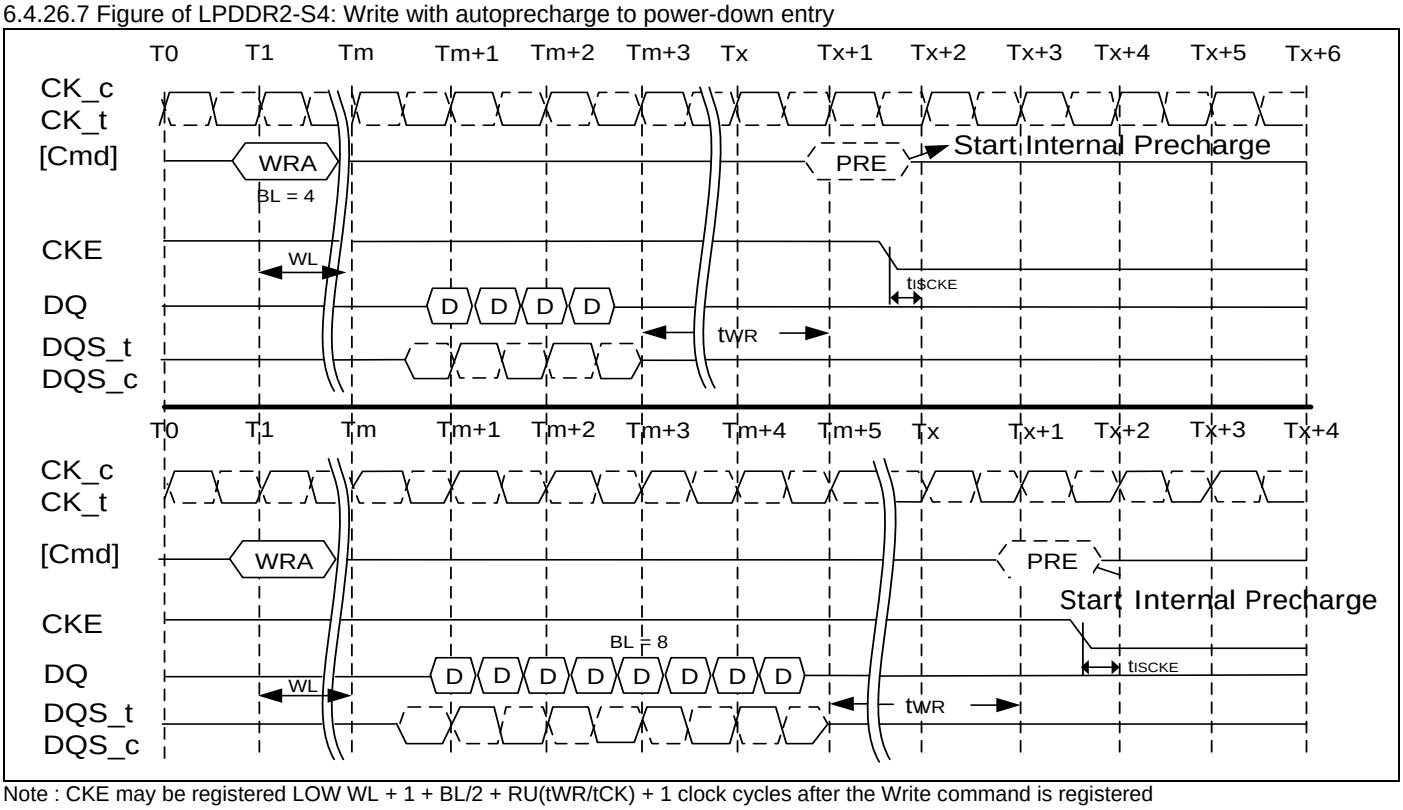
Note : CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK)+ BL/2 + 1 clock cycles after the clock on which the Read command is registered

6.4.26.6 Figure of Write to power-down entry



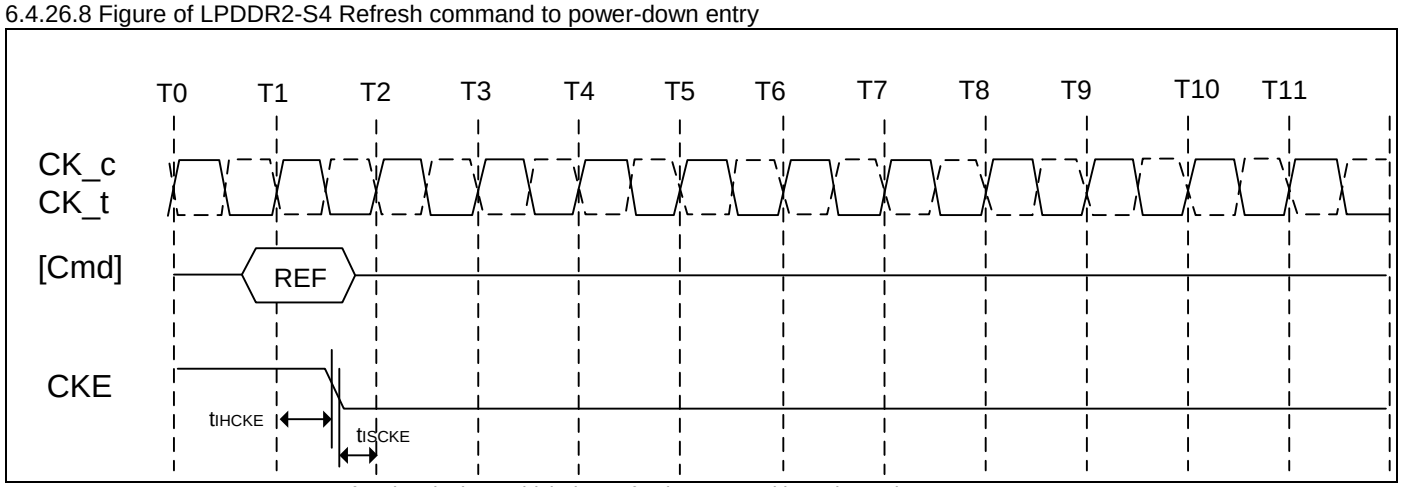
Note : CKE may be registered LOW WL + 1 + BL/2 + RU(tWR/tCK)clock cycles after the clock on which the Write command is registered

6.4.26.7 Figure of LPDDR2-S4: Write with autoprecharge to power-down entry



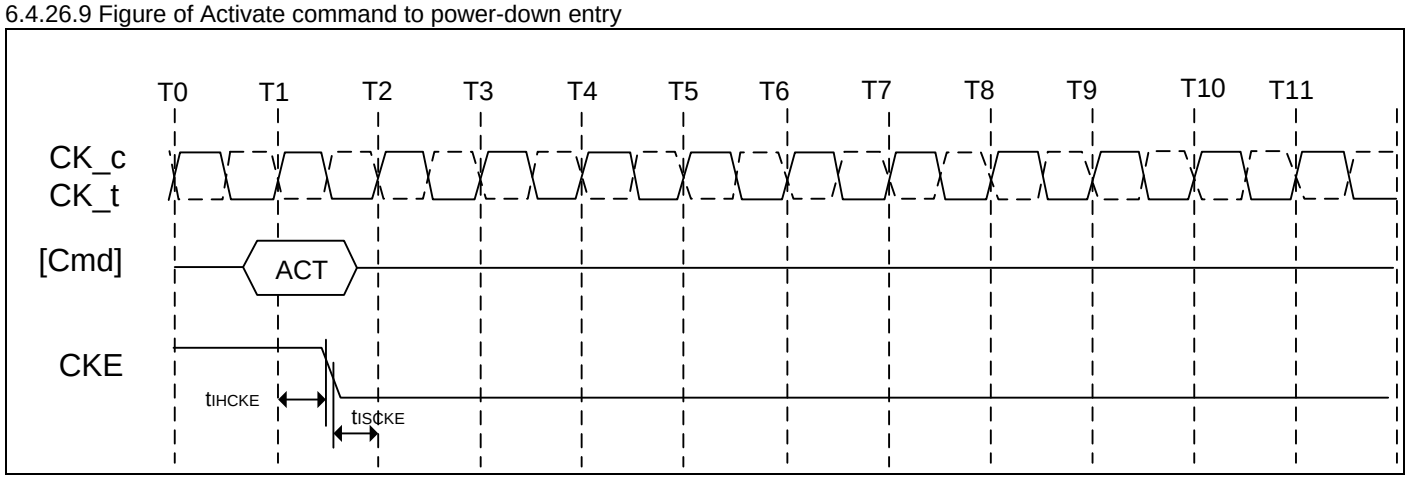
Note : CKE may be registered LOW WL + 1 + BL/2 + RU(tWR/tCK) + 1 clock cycles after the Write command is registered

6.4.26.8 Figure of LPDDR2-S4 Refresh command to power-down entry



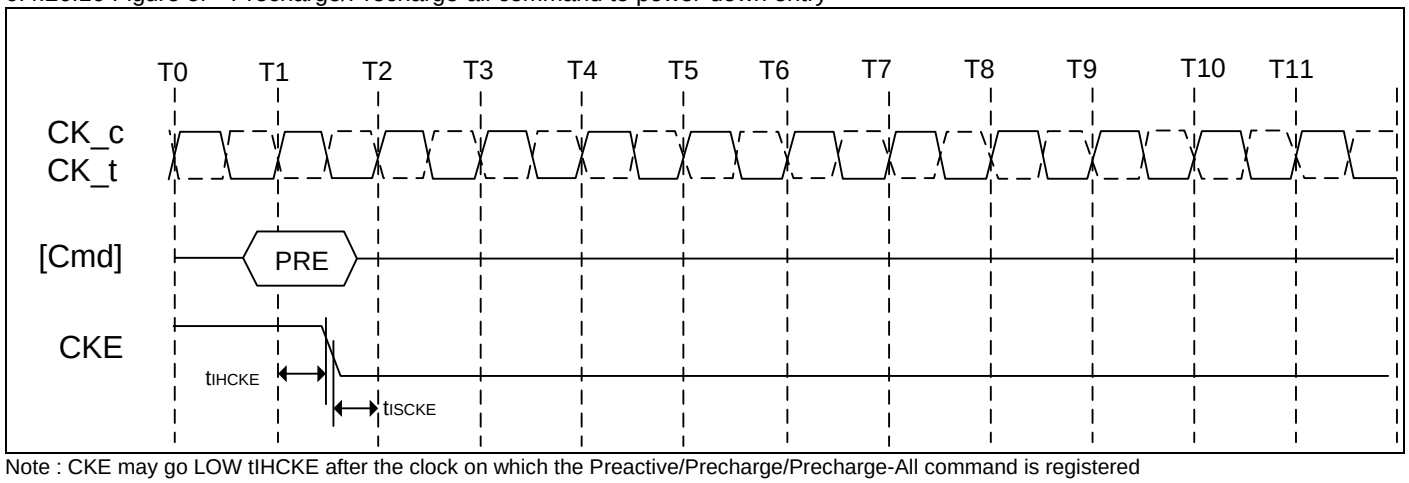
Note : CKE may go LOW tIHCKE after the clock on which the Refresh command is registered

6.4.26.9 Figure of Activate command to power-down entry



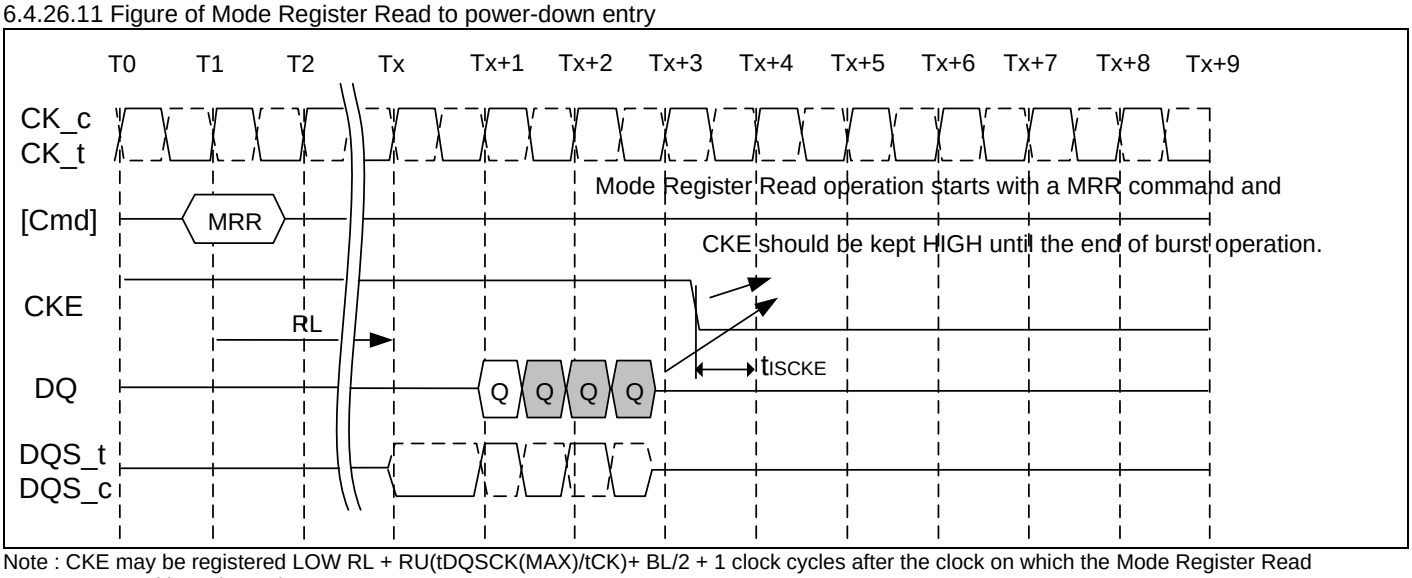
Note : CKE may go LOW tIHCKE after the clock on which the Activate command is registered

6.4.26.10 Figure of Precharge/Precharge-all command to power-down entry



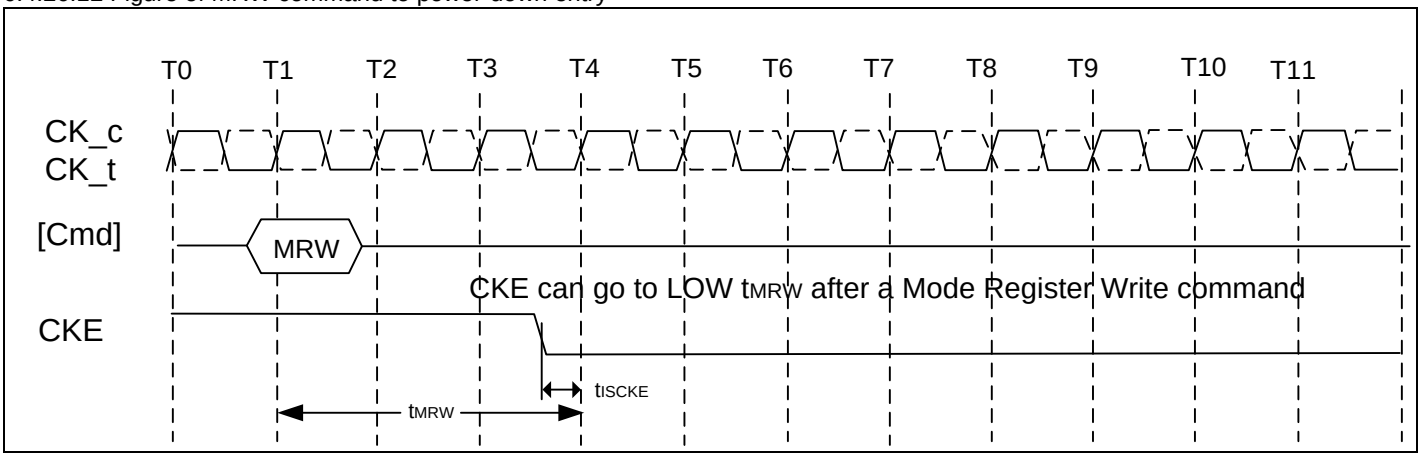
Note : CKE may go LOW tIHCKE after the clock on which the Preactive/Precharge/Precharge-All command is registered

6.4.26.11 Figure of Mode Register Read to power-down entry



Note : CKE may be registered LOW RL + RU(tDQSCK(MAX)/tCK)+ BL/2 + 1 clock cycles after the clock on which the Mode Register Read command is registered

6.4.26.12 Figure of MRW command to power-down entry



Note : CKE may be registered LOW tMRW after the clock on which the Mode Register Write command is registered

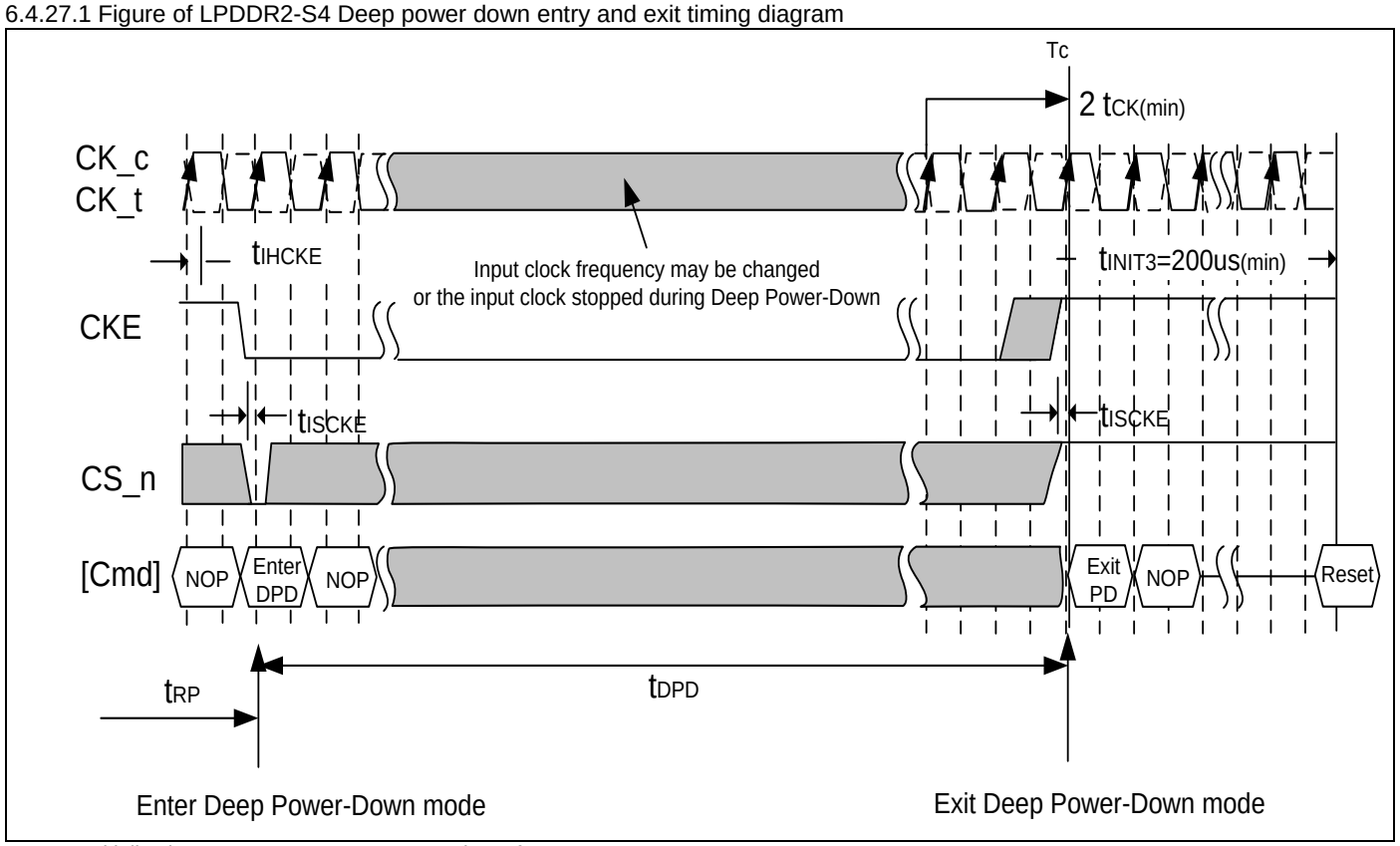
6.4.27 LPDDR2-S4: Deep Power-Down

Deep Power-Down is entered when CKE is registered LOW with CS_n LOW, CA0 HIGH, CA1 HIGH, and CA2 LOW at the rising edge of clock. A NOP command must be driven in the clock cycle following the power-down command. CKE is not allowed to go LOW while mode register, read, or write operations are in progress.All banks must be in idle state with no activity on the data bus prior to entering the Deep Power Down mode. During Deep Power-Down, CKE must be held LOW.

In Deep Power-Down mode, all input buffers except CKE, all output buffers, and the power supply to internal circuitry may be disabled within the SDRAM. All power supplies must be within specified limits prior to exiting Deep Power-Down. VrefDQ and VrefCA may be at any level within minimum and maximum levels (See "Absolute Maximum DC Ratings"). However prior to exiting Deep Power-Down, Vref must be within specified limits (See "Recommended DC Operating Conditions").

The contents of the SDRAM may be lost upon entry into Deep Power-Down mode.
The Deep Power-Down state is exited when CKE is registered HIGH, while meeting tISCKE with a stable clock input. The SDRAM must be fully re-initialized by controller as described in the Power up initialization Sequence. The SDRAM is ready for normal operation after the initialization sequence.

6.4.27.1 Figure of LPDDR2-S4 Deep power down entry and exit timing diagram



Note :1. Initialization sequence may start at any time after Tc.
2. tINIT2, tINIT3, and Tc refer to timings in the LPDDR2 initialization sequence. For more detail, see “Power- up, Initialization, and Power-down”.
3. Input clock frequency may be changed or the input clock stopped during deep power-down, provided that upon exiting deep power-down, the clock is stable and within specified limits for a minmum of 2 clock cycles prior to deep power-down exit and the clock frequency is between the minimum and maximum frequency for the particular speed grade

6.4.28 Input clock stop and frequency change

LPDDR2 devices support input clock frequency change during CKE LOW under the following conditions:

- tCK(MIN) and tCK(MAX) are met for each clock cycle;
- Refresh Requirements apply during clock frequency change;
- During clock frequency change, only REFab or REFpb commands may be executing;
- Any Activate, or Precharge commands have executed to completion prior to changing the frequency;
- The related timing conditions (tRCD, tRP) have been met prior to changing the frequency;
- The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
- The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.

After the input clock frequency is changed and CKE is held HIGH, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE LOW under the following conditions:
• CK_t is held LOW and CK_c is held HIGH during clock stop;
• Refresh Requirements apply during clock stop;
• During clock stop, only REFab or REFpb commands may be executing;
• Any Activate, or Precharge commands have executed to completion prior to stopping the clock;
• The related timing conditions (tRCD, tRP) have been met prior to stopping the clock;
• The initial clock frequency shall be maintained for a minimum of 2 clock cycles after CKE goes LOW;
• The clock satisfies tCH(abs) and tCL(abs) for a minimum of 2 clock cycles prior to CKE going HIGH.

LPDDR2 devices support input clock frequency change during CKE HIGH under the following conditions:
• tCK(MIN) and tCK(MAX) are met for each clock cycle;
• Refresh Requirements apply during clock frequency change;
• Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to changing the frequency;
• The related timing conditions (tRCD, tWR, tWRA, tRP, tMRW, tMRR, etc.) have been met prior to changing the frequency;
• CS_n shall be held HIGH during clock frequency change;
• During clock frequency change, only REFab or REFpb commands may be executing;
• The LPDDR2 device is ready for normal operation after the clock satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK + tXP.
After the input clock frequency is changed, additional MRW commands may be required to set the WR, RL etc. These settings may need to be adjusted to meet minimum timing requirements at the target clock frequency.

LPDDR2 devices support clock stop during CKE HIGH under the following conditions:
• CK_t is held LOW and CK_c is held HIGH during clock stop;
• CS_n shall be held HIGH during clock clock stop;
• Refresh Requirements apply during clock stop;
• During clock stop, only REFab or REFpb commands may be executing;
• Any Activate, Read, Write, Precharge, Mode Register Write, or Mode Register Read commands must have executed to completion, including any associated data bursts prior to stopping the clock;
• The related timing conditions (tRCD, tWR, tWRA, tRP, tMRW, tMRR, etc.) have been met prior to stopping the clock;
• The LPDDR2 device is ready for normal operation after the clock is restarted and satisfies tCH(abs) and tCL(abs) for a minimum of 2tCK + tXP.

6.4.29 No Operation command

The purpose of the No Operation command (NOP) is to prevent the LPDDR2 device from registering any unwanted command between operations. Only when the CKE level is constant for clock cycle N-1 and clock cycle N, a NOP command may be issued at clock cycle N. A NOP command has two possible encodings:
1. CS_n HIGH at the clock rising edge N.
2. CS_n LOW and CA0, CA1, CA2 HIGH at the clock rising edge N.
The No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

6.4.30 Truth tables

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

6.4.31 Command truth table

Command	Command Pins			DDR CA pins (10)										CK EDGE
	CKE		CS_N	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	
	CK_t(n-1)	CK_t(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
			X	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
			X	MA6	MA7	X								↓
Refresh (per bank)11	H	H	L	L	L	H	L	X						↑
			X	X										↓
Refresh (all bank)	H	H	L	L	L	H	H	X						↑
			X	X										↓
Enter Self Refresh	H	L	L	L	L	H	X							↑
	X		X	X										↓
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
			X	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	↓
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
			X	AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
			X	AP[3,4]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Precharge (per bank, all bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	↑
			X	X										↓
BST	H	H	L	H	H	L	L	X						↑
			X	X										↓
Enter Deep Power Down	H	L	L	H	H	L	X							↑
	X		X	X										↓
NOP	H	H	L	H	H	H	X							↑
			X	X										↓
Maintain PD, SREF,DPD(NOP)	L	L	L	H	H	H	X							↑
			X	X										↓
NOP	H	H	H	X										↑
			X	X										↓
Maintain PD, SREF,DPD(NOP)	L	L	H	X										↑
			X	X										↓
Enter Power Down	H	L	H	X										↑
	X		X	X										↓
Exit PD, SREF,DPD	L	H	H	X										↑
	X		X	X										↓

Note :1. All LPDDR2 commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock.
2. For LPDDR2 SDRAM, Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
3. AP is significant only to SDRAM.
4. AP “high” during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
5. “X” means “H or L (but a defined logic level)”
6. Self refresh exit and Deep Power Down exit are asynchronous.
7. VREF must be between 0 and VDDQ during Self Refresh and Deep Power Down operation.
8. CAxr refers to command/address bit “x” on the rising edge of clock.
9. CAxf refers to command/address bit “x” on the falling edge of clock.
10. CS_n and CKE are sampled at the rising edge of clock.
11. Per Bank Refresh is only allowed in devices with 8 banks.
12. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
13. AB “high”during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

6.4.32 LPDDR2-SDRAM Truth Tables

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the Banks.

6.4.32.1 Table of LPDDR2-S4 : CKE Table

Device Current State *3	CKEn-1 *1	CKEn *1	CS_n *2	Command n *4	Operation n *4	Device Next State	Note
Active Power Down	L	L	X	X	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6, 9
Idle Power Down	L	L	X	X	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6, 9
Resetting Power Down	L	L	X	X	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6, 9, 12
Deep Power Down (DPD)	L	L	X	X	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	X	X	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7, 10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Dow	
	H	L	L	Self-Refresh	Enter Self Refresh	Self Refresh	
	H	L	L	DPD	Enter Deep Power Down	Deep Power Down	
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
Others states	H	H	Refer to the Command Truth Table				

Note :1. “CKEn” is the logic state of CKE at clock rising edge n; “CKEn-1” was the state of CKE at the previous clock edge.

2. “CS_n” is the logic state of CS_n at the clock rising edge n;
3. “Current state” is the state of the LPDDR2 device immediately prior to clock edge n.
4. “Command n” is the command registered at clock edge N, and “Operation n” is a result of “Command n”.
5. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6. Power Down exit time (tXP) should elapse before a command other than NOP is issued.
7. Self-Refresh exit time (tXSR) should elapse before a command other than NOP is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Func tional Description.
9. The clock must toggle at least once during the tXP period.
10. The clock must toggle at least once during the tXSR time.
11. X’ means ‘Don’t care’.
12. Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.

6.4.32.2 Table of Current State Bank n - Command to Bank n

Current State	Command	Operation	Next State	Note
Any	NOP	Continue previous operation	Current State	
Idle	ACTIVATE	Select and activate row	Active	
	Refresh (Per Bank)	Begin to refresh	Refreshing (Per Bank)	6
	Refresh (All Bank)	Begin to refresh	Refreshing(All Bank)	7
	MRW	Load value to Mode Register	MR Writing	7
	MRR	Read value from Mode Register	Idle MR Reading	
	Reset	Begin Device Auto-Initialization	Resetting	7, 8
	Precharge	Deactivate row in bank or banks	Precharging	9, 15
Row Active	Read	Select column, and start read burst	Reading	
	Write	Select column, and start write burst	Writing	
	MRR	Read value from Mode Register	Active MR Reading	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading	Read	Select column, and start new read burst	Reading	10, 11
	Write	Select column, and start write burst	Writing	10, 11, 12
	BST	Read burst terminate	Active	13
Writing	Write	Select column, and start new write burst	Writing	10, 11
	Read	Select column, and start read burst	Reading	10, 11, 14
	BST	Write burst terminate	Active	13
Power On	Reset	Begin Device Auto-Initialization	Resetting	7, 9
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note : 1. The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Power Down.

2. All states and sequences not shown are illegal or reserved.

3. Current State Definitions:
   Idle: The bank or banks have been precharged, and tRP has been met.
   Active: A row in the bank has been activated, and tRCD has been met. No data bursts / accesses and no register accessesare in progress.
   Reading: A Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Writing: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4. The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state, and according to Table of Current State Bank n - Command to Bank m.
   Precharging: starts with the registration of a Precharge command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
   Row Activating: starts with registration of an Activate command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'Active' state.
   Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
   Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.
   Refreshing (Per Bank): starts with registration of an Refresh (Per Bank) command and ends when tRFCpb is met. Once tRFCpb is met, the bank will be in an 'idle' state.
   Refreshing (All Bank): starts with registration of an Refresh (All Bank) command and ends when tRFCab is met. Once tRFCab is met, the device will be in an 'all banks idle' state.
   Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
   Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
   Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
   MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
   Precharging All: starts with the registration of a Precharge-All command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
6. Bank-specific; requires that the bank is idle and no bursts are in progress.
7. Not bank-specific; requires that all banks are idle and no bursts are in progress.
8. Not bank-specific reset command is achieved through Mode Register Write command.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for pre- charging.
10. A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
11. The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
12. A Write command may be applied after the completion of the Read burst; otherwise, a BST must be used to end the Read prior to asserting a Write command.
13. Not bank-specific. Burst Terminate (BST) command affects the most recent read/write burst started by the most recent Read/Write command, regardless of bank. A Read command may be applied after the completion of the Write burst; other- wise, a BST must be used to end the Write prior to asserting a Read command.
14. A Read command may be applied after the completion of the Write burst; otherwise, a BST must be used to end the Write prior to asserting a Read command.
15. If a Precharge command is issued to a bank in the Idle state, tRP shall still apply.

6.4.32.3 Tableof Current State Bank n - Command to Bank m

Current State of Bank n	Command for Bank m	Operation	Next State for NOTES Bank m	Note
Any	NOP	Continue previous operation	Current State of Bank m	
Idle	Any	Any command allowed to Bank m	-	18
Row Activating, Active, or Precharging	Activate	Select and activate row in Bank m	Active	7
	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8
	Precharge	Deactivate row in bank or banks	Precharging	9
	MRR	Read value from Mode Register	Idle MR Reading or Active MR Readin	10, 11, 13
	BST	Read or Write burst terminate an ongoing Read/Write from/to Bank m	Active	18
Reading (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8
	Write	Select column, and start write burst to Bank m	Writing	8, 14
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing (Autoprecharge disabled)	Read	Select column, and start read burst from Bank m	Reading	8, 16
	Write	Select column, and start write burst to Bank m	Writing	8
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Reading with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15
	Write	Select column, and start write burst to Bank m	Writing	8, 14, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Writing with Autoprecharge	Read	Select column, and start read burst from Bank m	Reading	8, 15, 16
	Write	Select column, and start write burst to Bank m	Writing	8, 15
	Activate	Select and activate row in Bank m	Active	
	Precharge	Deactivate row in bank or banks	Precharging	9
Power On	Reset	Begin Device Auto-Initialization	Resetting	12, 17
Resetting	MRR	Read value from Mode Register	Resetting MR Reading	

Note : 1.The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.

2. All states and sequences not shown are illegal or reserved.

3. Current State Definitions:

Idle: the bank has been precharged, and tRP has been met.

Active: a row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.

Reading: a Read burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

Writing: a Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.

4. Refresh, Self-Refresh, and Mode Register Write commands may only be issued when all bank are idle.
5. A Burst Terminate (BST) command cannot be issued to another bank; it applies to the bank represented by the current state only.
6. The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
   Idle MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Idle state.
   Resetting MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Resetting state.
   Active MR Reading: starts with the registration of a MRR command and ends when tMRR has been met. Once tMRR has been met, the bank will be in the Active state.
   MR Writing: starts with the registration of a MRW command and ends when tMRW has been met. Once tMRW has been met, the bank will be in the Idle state.
7. tRRD must be met between Activate command to Bank n and a subsequent Activate command to Bank m.
8. Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
9. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for pre- charging.
10. MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when tRCD is met.)
11. MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when tRP is met.
12. Not bank-specific; requires that all banks are idle and no bursts are in progress.
13. The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon tRCD and tRP respectively.
14. A Write command may be applied after the completion of the Read burst, otherwise a BST must be issued to end the Read prior to asserting a Write command.
15. Read with auto precharge enabled or a Write with auto precharge enabled may be followed by any valid command to other banks provided that the timing restrictions of auto precharge are followed.
16. A Read command may be applied after the completion of the Write burst; otherwise, a BST must be issued to end the Write prior to asserting a Read command.
17. Reset command is achieved through Mode Register Write command.
18. BST is allowed only if a Read or Write burst is ongoing.

6.4.33 Data mask truth table

Table below provides the data mask truth table.

Name (Functional)	DM	DQs	Note
Write enable	L	Valid	1
Write inhibit	H	X	1

Note : Used to mask write data, provided coincident with the corresponding data

7. ELECTRICAL CHARACTERISTIC

7.1 Absolute Maximum DC Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Parameter	Symbol	Min	Max	Units	Notes
VDD1 supply voltage relative to VSS	VDD1	-0.4	+2.3	V	2
VDD2 supply voltage relative to VSS	VDD2	-0.4	+1.6	V	2
VDDCA supply voltage relative to VSSCA	VDDCA	-0.4	+1.6	V	2,4
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	+1.6	V	2,3
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	+1.6	V	
Storage Temperature	TSTG	-55	+125	°C	5

Note :1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

2. See “Power-Ramp” section in “Power-up, Initialization, and Power-Off” for relationships between power supplies.

3. VREFDQ ≦ 0.6 x VDDQ; however, VREFDQ may be ≧VDDQ provided that VREFDQ ≦300mV.

4. VREFCA ≦ 0.6 x VDDCA; however, VREFCA may be ≧VDDCA provided that VREFCA ≦ 300mV.

5.Storage Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.

7.2 AC & DC operating conditions

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR2 Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

7.2.1 Recommended DC Operating Conditions

7.2.1.1 Recommended DC Operating Conditions

Symbol	LPDDR2-S4B			DRAM	Unit
	Min	Typ	Max		
VDD1	1.70	1.80	1.95	Core Power1	V
VDD2	1.14	1.20	1.30	Core Power2	V
VDDCA	1.14	1.20	1.30	Input Buffer Power	V
VDDQ	1.14	1.20	1.30	I/O Buffer Power	V

Note :1. When VDD2 is used, VDD1 uses significantly less current than VDD2;

7.2.2 Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input Leakage current For CA, CKE, CS_n, CK_t, CK_c Any input 0V≦ VIN ≦ VDDCA (All other pins not under test = 0V)	IL	-2	2	uA	2
VREF supply leakage current VREFDQ = VDDQ/2 or VREFCA = VDDCA/2 (All other pins not under test = 0V)	IVREF	-1	1	uA	1

Note :1. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.
2. Although DM is for input only, the DM leakage shall match the DQ and DQS_t/DQS_c output leakage specification.

7.2.3 Operating Temperature Conditions

Parameter/Condition	Symbol	Min	Max	Unit
Standard	TOPER	-40	85	℃
Extended		85	105	℃

Note :1. Operating Temperature is the case surface temperature on the center/top side of the LPDDR2 device. For the measurement conditions, please refer to JESD51-2 standard.
2. Some applications require operation of LPDDR2 in the maximum temperature conditons in the Extended Temperature Range between 85℃ and 105℃ temperature. For LPDDR2 devices, some derating is neccessary to operate in this range. (see the MR4 Device Temperature (MA[7:0] = 04h) table).
3. Either the device temperature rating or the temperature sensor (See “Temperature Sensor”) may be used to set an appropriate refresh rate (SDRAM), determine the need for AC timing derating (SDRAM) and/or monitor the operating temperature (SDRAM). When using the temperature sensor, the actual device temperature may be higher than the TOPER rating that applies for the Standard or Extended Temperature Ranges. For example, Tj may be above 85ºC when the temperature sensor indicates a temperature of less than 85ºC.

7.2.4 AC and DC Input Measurement Levels

7.2.4.1 AC and DC Logic Input Levels for Single-Ended Signals

7.2.4.1.1 Table of Single-Ended AC and DC Input Levels for CA and CS_n Inputs

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Note
		Min	Max	Min	Max		
VIHCA(AC)	AC input logic high	Vref + 0.220	Note 2	Vref + 0.300	Note 2	V	1, 2
VILCA(AC)	AC input logic low	Note 2	Vref - 0.220	Note 2	Vref - 0.300	V	1, 2
VIHCA(DC)	DC input logic high	Vref + 0.130	VDDCA	Vref + 0.200	VDDCA	V	1
VILCA(DC)	DC input logic low	VSSCA	Vref - 0.130	VSSCA	Vref - 0.200	V	1
VRefCA(DC)	Reference Voltage for CA and CS_n inputs	0.49 * VDDCA	0.51 * VDDCA	0.49 * VDDCA	0.51 * VDDCA	V	3, 4

Note 1. For CA and CS_n input only pins. Vref = VrefCA(DC).
2. See “Overshoot and Undershoot Specifications”
3. The ac peak noise on VRefCA may not allow VRefCA to deviate from VRefCA(DC) by more than +/-1% VDDCA (for reference: approx. +/- 12 mV)
4. For reference: approx. VDDCA/2 +/- 12 mV

7.2.4.1.2 Table of Single-Ended AC and DC Input Levels for CKE

Symbol	Parameter	Min	Max	Unit	Note
V_{IHCKE}	CKE Input High Level	0.8 * VDDCA	Note 1	V	1
V_{ILCKE}	CKE Input Low Level	Note 1	0.2 * VDDCA	V	1
Note : See “Overshoot and Undershoot Specifications”					

7.2.4.1.3 Table of Single-Ended AC and DC Input Levels for DQ and DM

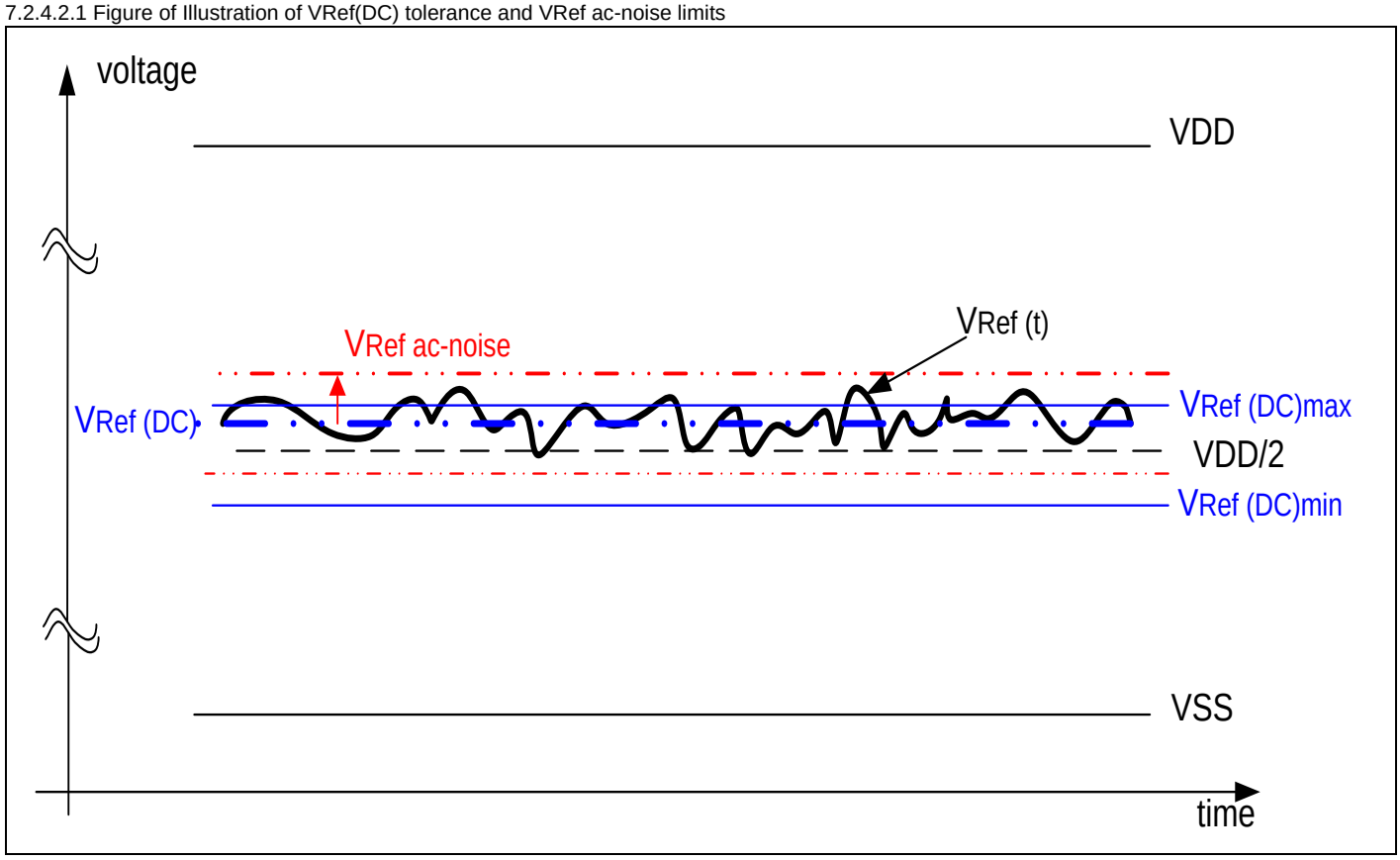
Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Note
		Min	Max	Min	Max		
V_{IHDQ}(AC)	AC input logic high	Vref + 0.220	Note 2	Vref + 0.300	Note 2	V	1,2
V_{ILDQ}(AC)	AC input logic low	Note 2	Vref - 0.220	Note 2	Vref - 0.300	V	1,2
V_{IHDQ}(DC)	DC input logic high	Vref + 0.130	VDDQ	Vref + 0.200	VDDQ	V	1
V_{ILDQ}(DC)	DC input logic low	VSSQ	Vref - 0.130	VSSQ	Vref - 0.200	V	1
V_{RefDQ}(DC)	Reference Voltage for DQ, DM inputs	0.49 * VDDQ	0.51 * VDDQ	0.49 * VDDQ	0.51 * VDDQ	V	3, 4

Note 1. For DQ input only pins. Vref = VrefDQ(DC)
2. See “Overshoot and Undershoot Specifications”
3. The ac peak noise on VRefDQ may not allow VRefDQ to deviate from VRefDQ(DC) by more than +/-1% VDDQ (for reference: approx. +/- 12 mV)
4. For reference: approx. VDDQ/2 +/- 12 mV

7.2.4.2 Vref Tolerances

The DC tolerance limits and ac-noise limits for the reference voltages VRefCA and VRefDQ are illustrated in.the Figure below. It shows a valid reference voltage VRef(t) as a function of time. (VRef stands for VRefCA and VRefDQ likewise). VDD stands for VDDCA for VRefCA and VDDQ for VRefDQ. VRef(DC) is the linear average of VRef(t) over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VDDQ or VDDCA also over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table of Single-Ended AC and DC Input Levels for CA and CS_n Inputs. Furthermore VRef(t) may temporarily deviate from VRef(DC) by no more than +/- 1% VDD. Vref(t) cannot track noise on VDDQ or VDDCA if this would send Vref outside these specifications.

7.2.4.2.1 Figure of Illustration of VRef(DC) tolerance and VRef ac-noise limits



The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VRef.

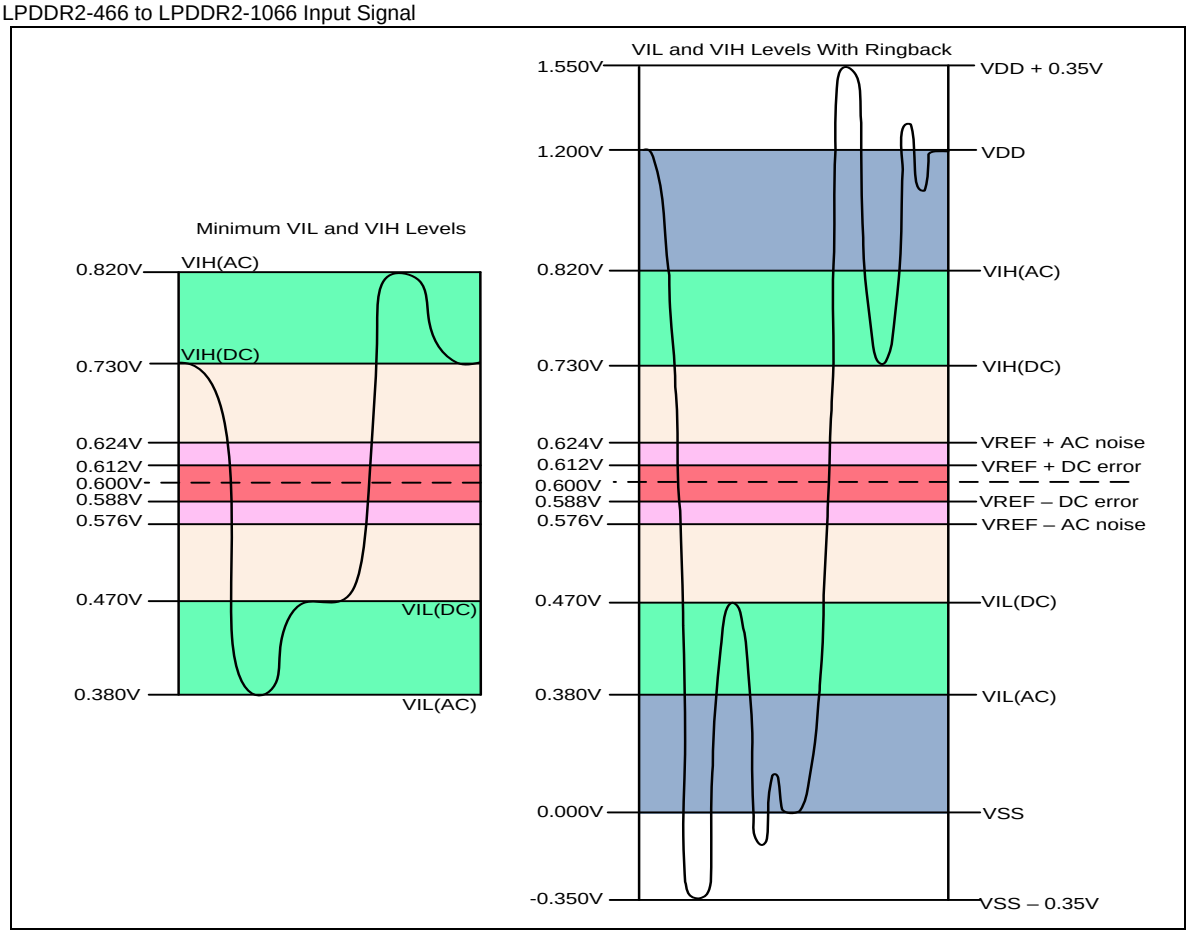
“VRef “ shall be understood as VRef(DC), as defined in Figure above.
This clarifies that dc-variations of VRef affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. Devices will function correctly with appropriate timing deratings with VREF outside these specified levels so long as:

VREF is maintained between 0.44 x VDDQ (or VDDCA) and 0.56 x VDDQ (or VDDCA) and so long as the controller achieves the required single-ended AC and DC input levels from instantaneous VREF (see the Single-Ended AC and DC Input Levels for CA and CS_n Inputs Table and Single-Ended AC and DC Input Levels for DQ and DM) Therefore, system timing and voltage budgets need to account for VRef deviations outside of this range.

This also clarifies that the LPDDR2 setup/hold specification and derating values need to include time and voltage associated with VRef ac-noise. Timing and voltage effects due to ac-noise on VRef up to the specified limit (+/-1% of VDD) are included in LPDDR2 timings and their associated deratings.

7.2.4.3 Input Signal

7.2.4.3.1 LPDDR2-466 to LPDDR2-1066 Input Signal

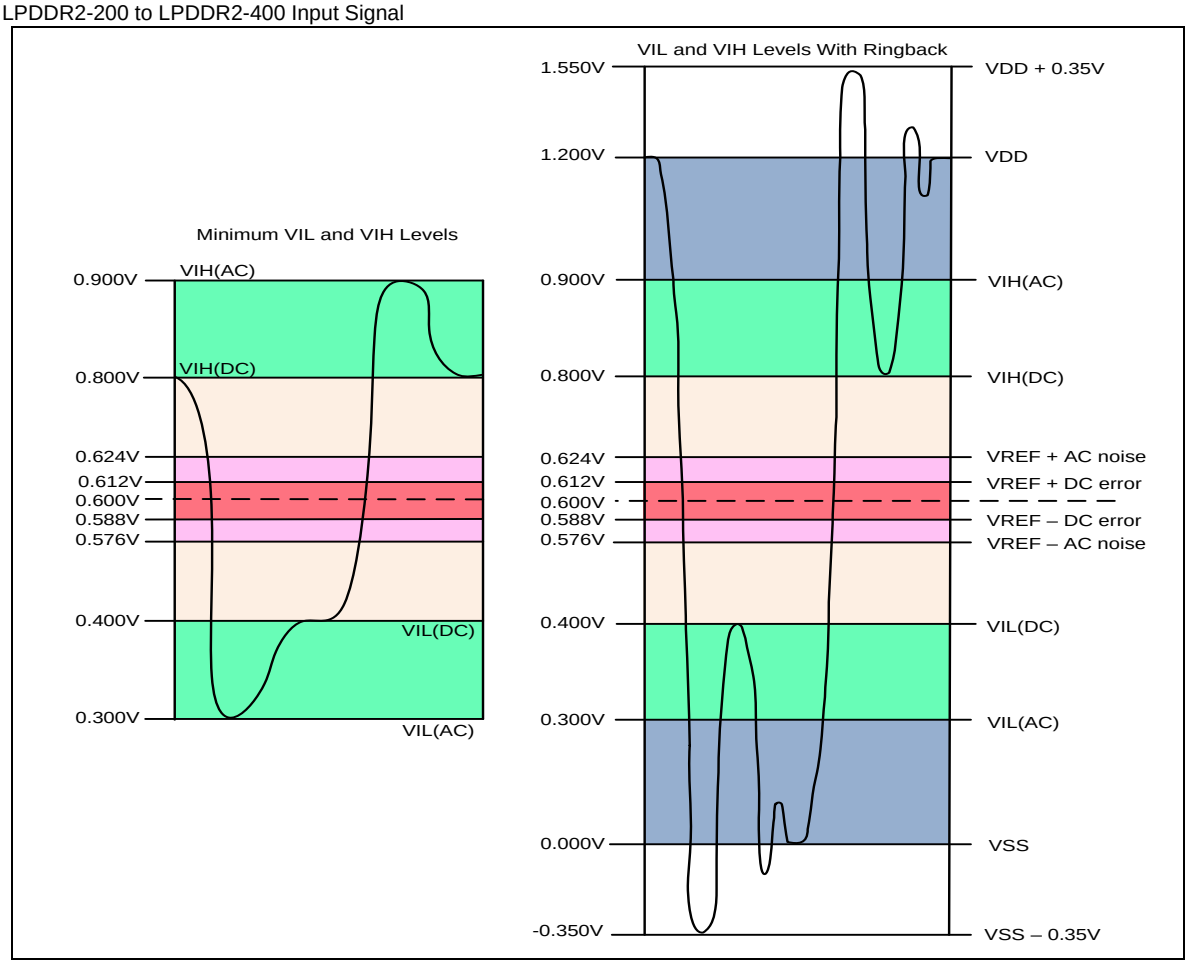


Note :1. Numbers reflect nominal values.

2.For CA0-9, CK_t, CK_c, and CS_n, VDD stands for VDDCA. For DQ, DM, DQS_t, and DQS_c, VDD stands for VDDQ.

3. For CA0-9, CK_t, CK_c, and CS_n, VSS stands for VSSCA. For DQ, DM, DQS_t, and DQS_c, VSS stands for VSSQ.

7.2.4.3.2 LPDDR2-200 to LPDDR2-400 Input Signal



Note :1. Numbers reflect nominal values.

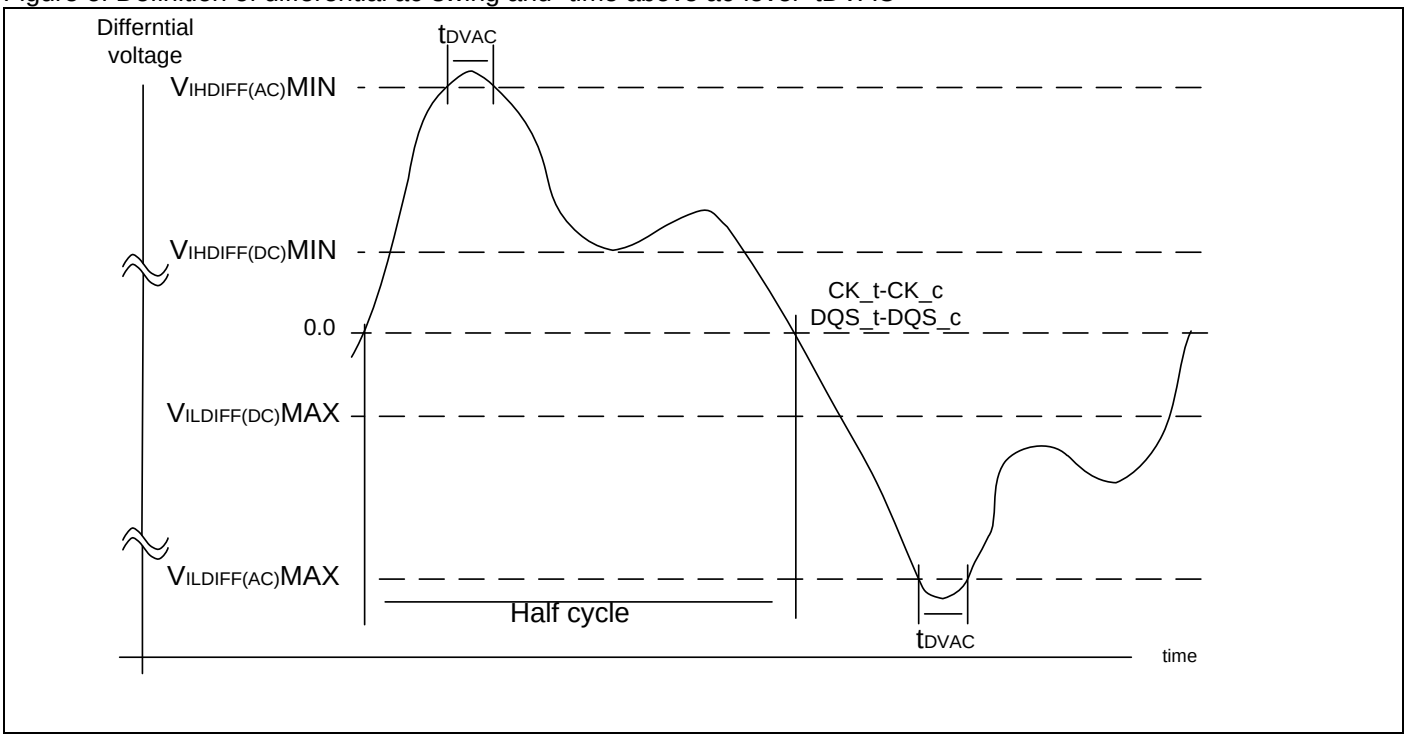
2. For CA0-9, CK_t, CK_c, and CS_n, VDD stands for VDDCA. For DQ, DM, DQS_t, and DQS_c, VDD stands for VDDQ.

3. For CA0-9, CK_t, CK_c, and CS_n, VSS stands for VSSCA. For DQ, DM, DQS_t, and DQS_c, VSS stands for VSSQ.

7.2.4.4 AC and DC Logic Input Levels for Differential Signals

7.2.4.4.1 Differential signal definition

Figure of Definition of differential ac-swing and “time above ac-level” tDVAC



7.2.4.4.2 Differential swing requirements for clock and strobe

Table of Differential AC and DC Input Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Note
		Min	Max	Min	Max		
VIHdiff(dc)	Differential input high	2 x (VIH(dc) - Vref)	Note 3	2 x (VIH(dc) - Vref)	Note 3	V	1
VILdiff(dc)	Differential input logic low	Note 3	2 x (Vref - VIL(dc))	Note 3	2 x (Vref - VIL(dc))	V	1
VIHdiff(ac)	Differential input high ac	2 x (VIH(ac) - Vref)	Note 3	2 x (VIH(ac) - Vref)	Note 3	V	2
VILdiff(ac)	Differential input low ac	Note 3	2 x (Vref - VIL(ac))	Note 3	2 x (Vref - VIL(ac))	V	2

Note 1. Used to define a differential signal slew-rate.

2.For CK_t - CK_c use VIH/VIL(ac) of CA and VREFCA; for DQS_t - DQS_c, use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to “Overshoot and Undershoot Specifications” .

4. For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC).

Table of Allowed time before ringback (tDVAC) for CK_t - CK_c and DQS_t - DQS_c

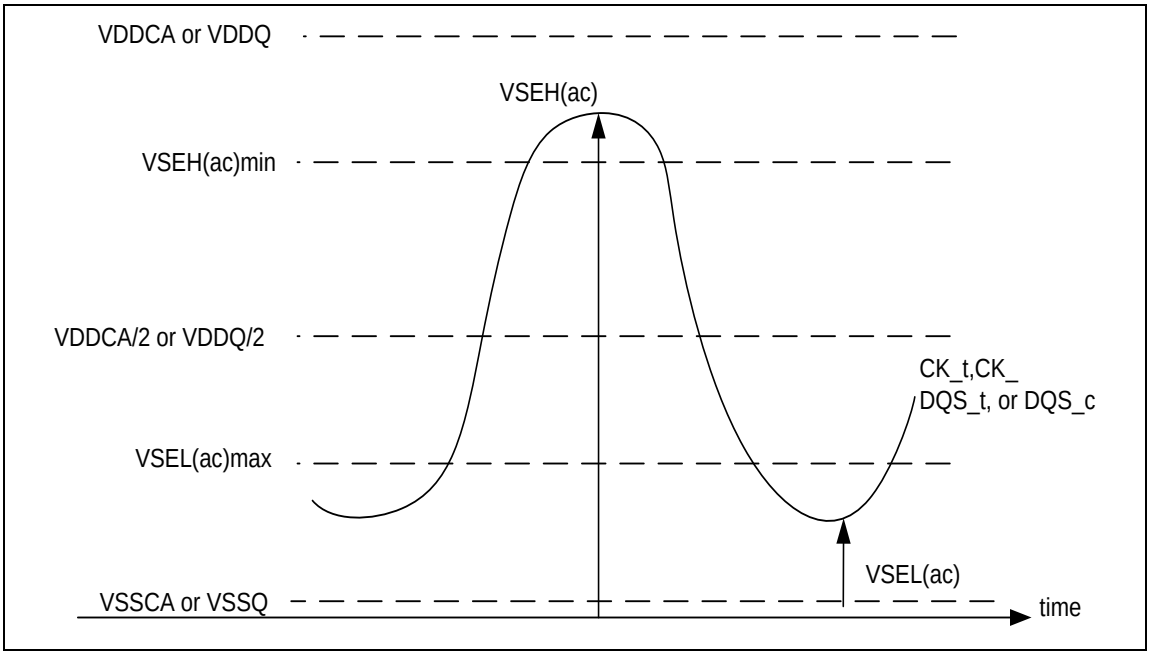
Slew Rate [V/ns]	tDVAC [ps] @ |VIHdiff(ac) or VILdiff(ac)| = 440mV	tDVAC [ps] @ |VIHdiff(ac) or VILdiff(ac)| = 600mV
> 4.0	175	75
4.0	170	57
3.0	167	50
2.0	163	38
1.8	162	34
1.6	161	29
1.4	159	22
1.2	155	13
1.0	150	0
< 1.0	150	0

7.2.4.5 Single-ended requirements for differential signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle.
DQS_t, DQS_c shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle preceeding and following a valid transition.

Note that the applicable ac-levels for CA and DQ's are different per speed-bin.
Figure of Single-ended requirement for differential signals



Note that while CA and DQ signal requirements are with respect to Vref, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS and VDDCA/2 for CK; this is nominally the same.

The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL(ac)max, VSEH(ac)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.
The signal ended requirements for CK and DQS are found in tables of Single-Ended AC and DC Input Levels for CA and CS_n Inputs and table of Single-Ended AC and DC Input Levels for DQ and DM respectively.

Table of Single-ended levels for CK_t, DQS_t, CK_c, DQS_c

Symbol	Parameter	LPDDR2-1066 to LPDDR2-466		LPDDR2-400 to LPDDR2-200		Unit	Note
		Min	Max	Min	Max		
VSEH (AC)	Single-ended high-level for strobes	(VDDQ / 2) + 0.220	Note 3	(VDDQ / 2) + 0.300	Note 3	V	1, 2
	Single-ended high-level for CK_t, CK_c	(VDDCA / 2) + 0.220	Note 3	(VDDCA / 2) + 0.300	Note 3	V	1, 2
VSEL (AC)	Single-ended low-level for strobes	Note 3	(VDDDQ / 2) - 0.220	Note 3	(VDDQ / 2) - 0.300	V	1, 2
	Single-ended low-level for CK_t, CK_c	Note 3	(VDDCA / 2) - 0.220	Note 3	(VDDCA / 2) - 0.300	V	1, 2

Note :
1. For CK_t, CK_c use VSEH/VSEL(ac) of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use VIH/VIL(ac) of DQs.
2. VIH(ac)/VIL(ac) for DQs is based on VREFDQ; VSEH(ac)/VSEL(ac) for CA is based on VREFCA; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to “Overshoot and Undershoot Specifications”.

7.2.4.6 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements of Single-ended levels for CK_t, DQS_t, CK_c, DQS_c. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.
Figure of Vix Definition

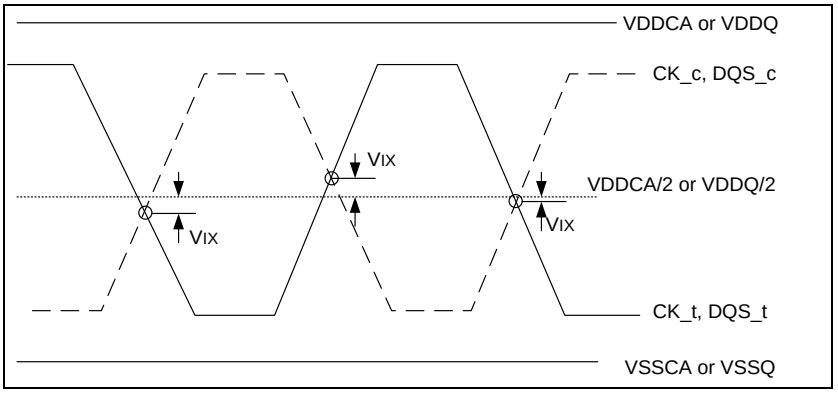


Table of Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200		Unit	Note
		Min	Max		
VIXCA	Differential Input Cross Point Voltage relative to VDDCA/2 for CK_t, CK_c	- 120	120	mV	1,2
VIXDQ	Differential Input Cross Point Voltage relative to VDDQ/2 for DQS_t, DQS_c	- 120	120	mV	1,2

Note :1. The typical value of VIX(AC) is expected to be about 0.5 × VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
2. For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC).

7.2.4.7 Slew Rate Definitions for Single-Ended Input Signals

See “Address / Command CA and CS_n Setup, Hold and Derating” for single-ended slew rate definitions for address and command signals.

See “Data Setup, Hold and Slew Rate Derating” for single-ended slew rate definitions for data signals.

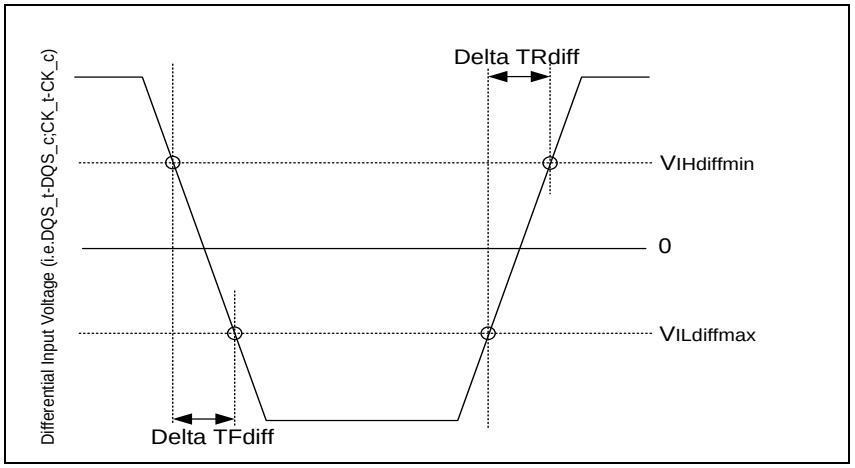
7.2.4.8 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in Table and Figure below.

Table of Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK_t - CK_c and DQS_t - DQS_c).	VILdiffmax	VIHdiffmin	[VIHdiffmin - VILdiffmax] / DeltaTRdiff
Differential input slew rate for falling edge (CK_t - CK_c and DQS_t - DQS_c).	VIHdiffmin	VILdiffmax	[VIHdiffmin - VILdiffmax] / DeltaTFdiff
Note : The differential signal (i.e. CK_t - CK_c and DQS_t - DQS_c) must be linear between these thresholds			

Figure of Differential Input Slew Rate Definition for DQS_t, DQS_c and CK_t, CK_c



7.2.5 AC and DC Output Measurement Levels

7.2.5.1 Single Ended AC and DC Output Levels

Table of Single-ended AC and DC Output Levels

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200		Unit	Note
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.9 x VDDQ		V	1
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.1 x VDDQ		V	2
VOH(AC)	AC output high measurement level (for output slew rate)	VREFDQ + 0.12		V	
VOL(AC)	AC output low measurement level (for output slew rate)	VREFDQ - 0.12		V	
I_{OZ}	Output Leakage current (DQ, DM, DQS_t, DQS_c) (DQ, DQS_t, DQS_c are disabled;0V≦Vout≦VDDQ)	Min:	-5	uA	
		Max:	+5		
MM_{PUPD}	Delta RON between pull-up and pull-down for DQ/DM	Miin:	-15	%	
		Max:	+15		

Note 1. IOH = -0.1mA
2. IOL = 0.1mA

7.2.5.2 Differential AC and DC Output Levels

Table of Differential AC and DC Output Levels of (DQS_t, DQS_c)

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200	Unit	Note
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	+ 0.20 x V_{DDQ}	V	
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	- 0.20 x V_{DDQ}	V	

7.2.5.3 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in Table and Figure below.

Table of Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC) - VOL(AC)] / DeltaTRse
Single-ended output slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC) - VOL(AC)] / DeltaTFse
Note:Output slew rate is verified by design and characterization, and may not be subject to production test.			

Figure of Single Ended Output Slew Rate Definiton

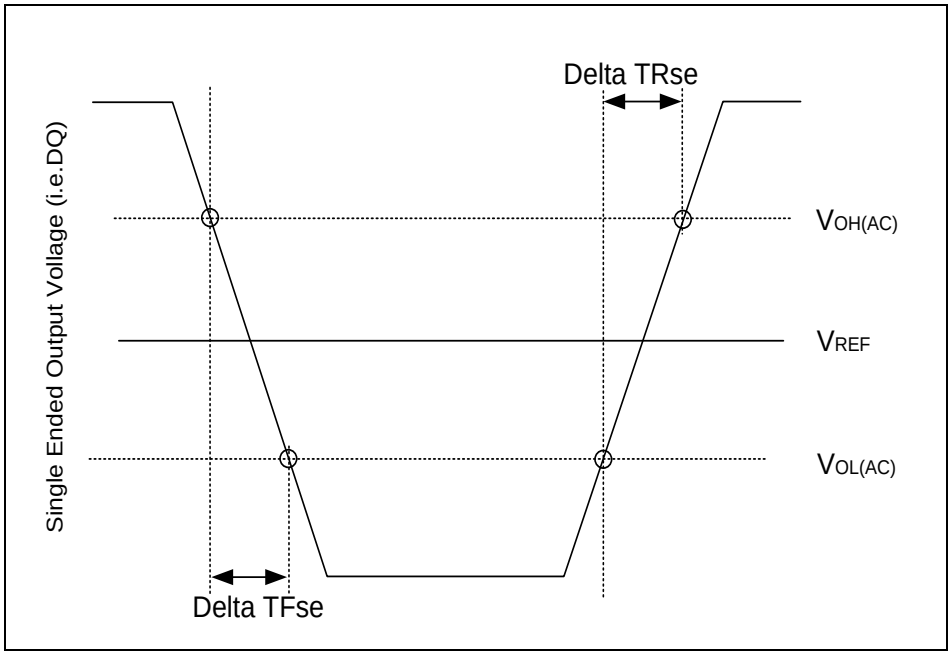


Table of Output Slew Rate (single-ended)

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200		Unit
		Min	Max	
SRQse	Single-ended Output Slew Rate (RON = 40Ω +/- 30%)	1.5	3.5	V/ns
SRQse	Single-ended Output Slew Rate (RON = 60Ω +/- 30%)	1.0	2.5	V/ns
	Output slew-rate matching Ratio (Pull-up to Pull-down)	0.7	1.4	

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals

Note : 1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pulldown drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
4. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic high and 1/2 of DQ signals per data byte driving logic low.

7.2.5.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table and Figure below.

Table of Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	[VOHdiff(AC) - VOLdiff(AC)] / DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	[VOHdiff(AC) - VOLdiff(AC)] / DeltaTFdiff
Note: Output slew rate is verified by design and characterization, and may not be subject to production test.			

Figure of Differential Output Slew Rate Definition

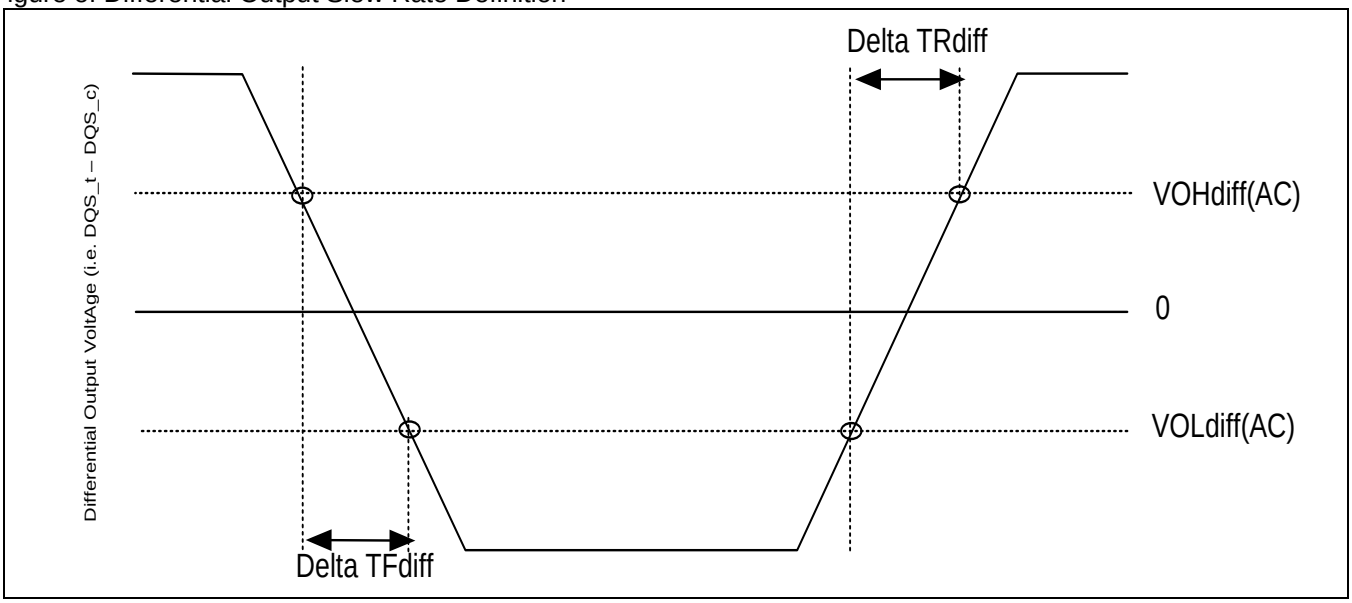


Table of Differential Output Slew Rate

Symbol	Parameter	LPDDR2-1066 to LPDDR2-200		Unit
		Min	Max	
SRQdiff	Differential Output Slew Rate (RON = 40Ω +/- 30%)	3.0	7.0	V/ns
SRQdiff	Differential Output Slew Rate (RON = 60Ω +/- 30%)	2.0	5.0	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: differential Signals

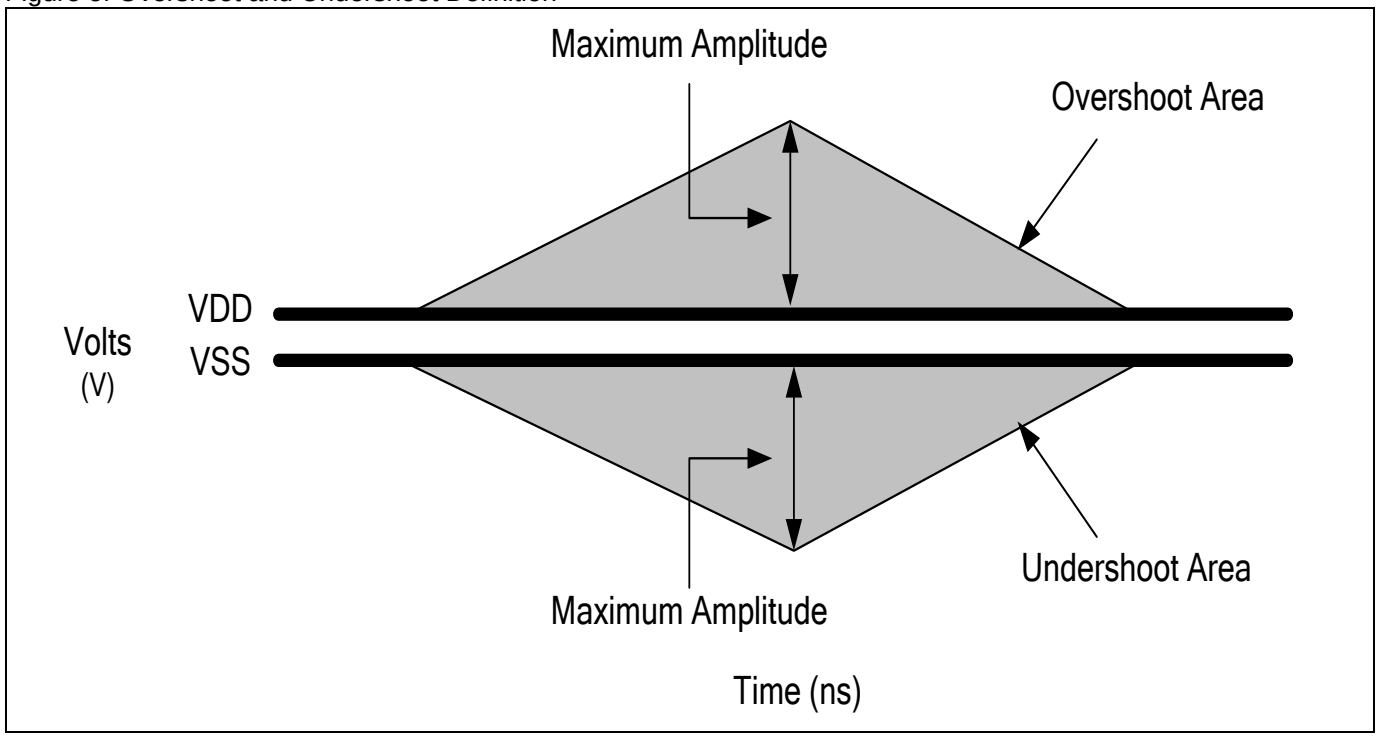
Note :1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC).
3. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic-high and 1/2 of DQ signals per data byte driving logic-low.

7.2.5.5 Overshoot and Undershoot Specifications

Table of AC Overshoot/Undershoot Specification

Parameter		LPDDR2							Unit
		1066	933	800	667	533	400	333	
Maximum peak amplitude allowed for overshoot area. (See Figure below)	Max	0.35							V
Maximum peak amplitude allowed for undershoot area. (See Figure below)	Max	0.35							V
Maximum area above VDD. (See Figure below)	Max	0.15	0.17	0.20	0.24	0.30	0.40	0.48	V-ns
Maximum area below VSS. (See Figure below)	Max	0.15	0.17	0.20	0.24	0.30	0.40	0.48	V-ns
CA0-9, CS_n, CKE, CK_t, CK_c, DQ, DQS_t, DQS_c, DM Note : 1. For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDDCA. For DQ, DM, DQS_t, and DQS_c, VDD stands for VDDQ. 2. For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSSCA. For DQ, DM, DQS_t, and DQS_c, VSS stands for VSSQ. 3. Values are referenced from actual VDDQ, VDDCA, VSSQ, and VSSCA levels.									

Figure of Overshoot and Undershoot Definition



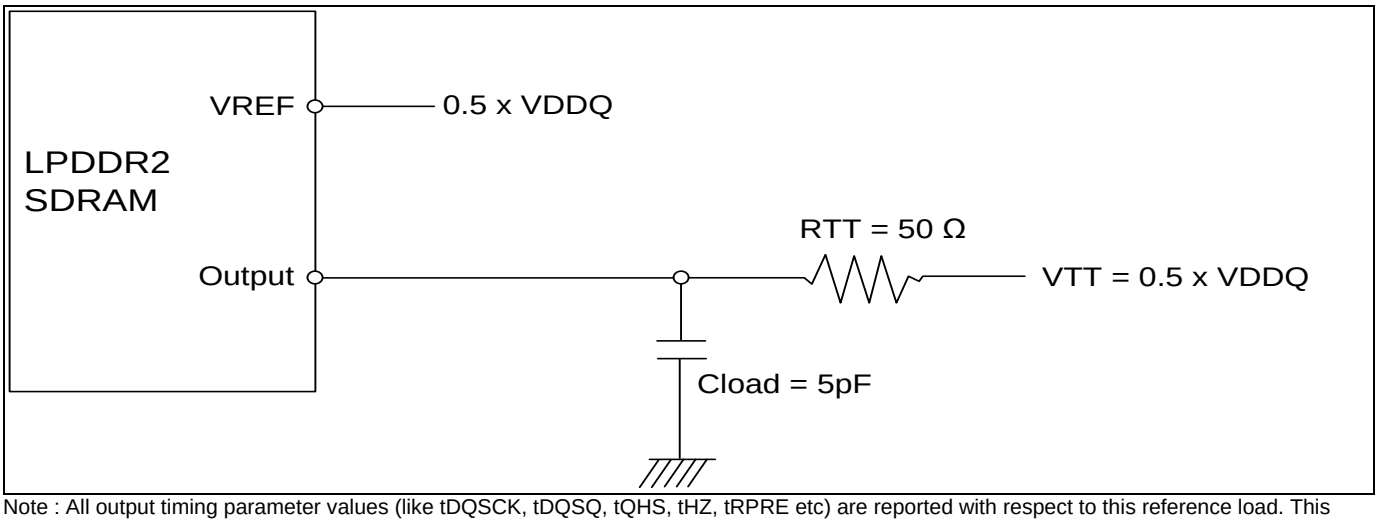
Note : 1. For CA0-9, CK_t, CK_c, CS_n, and CKE, VDD stands for VDDCA. For DQ, DM, DQS_t, and DQS_c, VDD stands for VDDQ.
2. For CA0-9, CK_t, CK_c, CS_n, and CKE, VSS stands for VSSCA. For DQ, DM, DQS_t, and DQS_c, VSS stands for VSSQ.

7.2.6 Output buffer characteristics

7.2.6.1 HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure of HSUL_12 Driver Output Reference Load for Timing and Slew Rate



Note : All output timing parameter values (like tDQSCK, tDQSQ, tQHS, tHZ, tRPRE etc) are reported with respect to this reference load. This reference load is also used to report slew rate.

7.2.6.2 RONPU and RONPD Resistor Definition

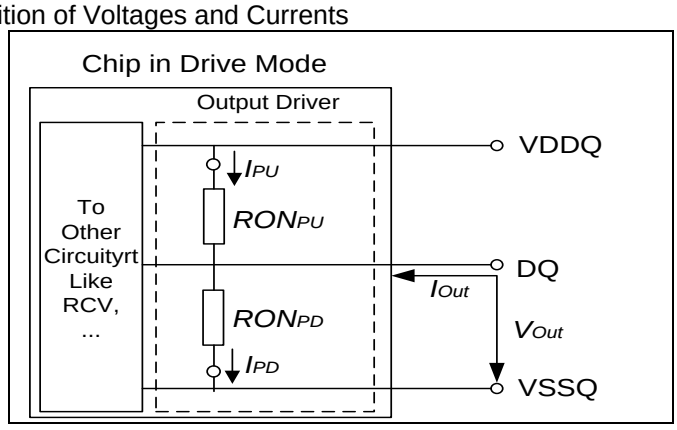
$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

Note : This is under the condition that RONPD is turned off

$$RONPD = \frac{Vout}{ABS(Iout)}$$

Note : This is under the condition that RONPU is turned off

Figure of Output Driver Definition of Voltages and Currents



7.2.6.3 RONPU and RONPD Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω.

Table — Output Driver DC Electrical Characteristics with ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Note
34.3Ω	RON34PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
	RON34PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/7	1,2,3,4
40.0Ω	RON40PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
	RON40PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/6	1,2,3,4
48.0Ω	RON48PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
	RON48PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/5	1,2,3,4
60.0Ω	RON60PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
	RON60PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/4	1,2,3,4
80.0Ω	RON80PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
	RON80PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/3	1,2,3,4
120.0Ω	RON120PD	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1,2,3,4
	RON120PU	0.5 x VDDQ	0.85	1.00	1.15	RZQ/2	1,2,3,4
Mismatch between pull-up and pull-down	MMPUPD		-15.00		+15.00	%	1,2,3,4,5

Note 1. Across entire operating temperature range, after calibration.

2. RZQ = 240Ω.

3.The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

4. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 x VDDQ.

5. Mesaurement definition for mismatch between pull-up and pull-down: MMPUPD: Measure RONPU and RONPD, both at 0.5 x VDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

For example, with MMPUPD(max) = 15% and RONPD = 0.85, RONPU must be less than 1.0.

7.2.6.3.1 Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown Below

Table of Output Driver Sensitivity Definition

Resistor	Vout	Min	Max	Unit	Note
RONPD	0.5 x VDDQ	85 – (dR ONdT ×|ΔT|) – (dRON d V × |ΔV|)	115 + (dRONdT ×| ΔT|)+(dRONdV × |ΔV|)	%	1,2
RONPU					

Note 1. ΔT = T–T (@calibration), ΔV=V–V(@ calibration)

2. dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Table of Output Driver Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit	Note
dRONdT	RON Temperature Sensitivity	0.00	0.75	% / C	
dRONdV	RON Voltage Sensitivity	0.00	0.20	% / mV	

7.2.6.4 RONPU and RONPD Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

Table of Output Driver DC Electrical Characteristics without ZQ Calibration

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	Note
34.3Ω	RON34PD	0.5 x VDDQ	24	34.3	44.6	Ω	1
	RON34PU	0.5 x VDDQ	24	34.3	44.6	Ω	1
40.0Ω	RON40PD	0.5 x VDDQ	28	40	52	Ω	1
	RON40PU	0.5 x VDDQ	28	40	52	Ω	1
48.0Ω	RON48PD	0.5 x VDDQ	33.6	48	62.4	Ω	1
	RON48PU	0.5 x VDDQ	33.6	48	62.4	Ω	1
60.0Ω	RON60PD	0.5 x VDDQ	42	60	78	Ω	1
	RON60PU	0.5 x VDDQ	42	60	78	Ω	1
80.0Ω	RON80PD	0.5 x VDDQ	56	80	104	Ω	1
	RON80PU	0.5 x VDDQ	56	80	104	Ω	1
120.0Ω	RON120PD	0.5 x VDDQ	84	120	156	Ω	1
	RON120PU	0.5 x VDDQ	84	120	156	Ω	1

Note : Across entire operating temperature range, without calibration.

7.2.6.5 RZQ I-V Curve

Table of RZQ I-V Curve

Voltage[V]	RON = 240Ω (RZQ)							
	Pull-Down				Pull-Up			
	Current [mA] / RON [Ohms]				Current [mA] / RON [Ohms]			
	default value after ZQReset		With Calibration		default value after ZQReset		With Calibration	
	Min	Max	Min	Max	Min	Max	Min	Max
	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]	[mA]
0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
0.05	0.19	0.32	0.21	0.26	-0.19	-0.32	-0.21	-0.26
0.10	0.38	0.64	0.40	0.53	-0.38	-0.64	-0.40	-0.53
0.15	0.56	0.94	0.60	0.78	-0.56	-0.94	-0.60	-0.78
0.20	0.74	1.26	0.79	1.04	-0.74	-1.26	-0.79	-1.04
0.25	0.92	1.57	0.98	1.29	-0.92	-1.57	-0.98	-1.29
0.30	1.08	1.86	1.17	1.53	-1.08	-1.86	-1.17	-1.53
0.35	1.25	2.17	1.35	1.79	-1.25	-2.17	-1.35	-1.79
0.40	1.40	2.46	1.52	2.03	-1.40	-2.46	-1.52	-2.03
0.45	1.54	2.74	1.69	2.26	-1.54	-2.74	-1.69	-2.26
0.50	1.68	3.02	1.86	2.49	-1.68	-3.02	-1.86	-2.49
0.55	1.81	3.30	2.02	2.72	-1.81	-3.30	-2.02	-2.72
0.60	1.92	3.57	2.17	2.94	-1.92	-3.57	-2.17	-2.94
0.65	2.02	3.83	2.32	3.15	-2.02	-3.83	-2.32	-3.15
0.70	2.11	4.08	2.46	3.36	-2.11	-4.08	-2.46	-3.36
0.75	2.19	4.31	2.58	3.55	-2.19	-4.31	-2.58	-3.55
0.80	2.25	4.54	2.70	3.74	-2.25	-4.54	-2.70	-3.74
0.85	2.30	4.74	2.81	3.91	-2.30	-4.74	-2.81	-3.91
0.90	2.34	4.92	2.89	4.05	-2.34	-4.92	-2.89	-4.05
0.95	2.37	5.08	2.97	4.23	-2.37	-5.08	-2.97	-4.23
1.00	2.41	5.20	3.04	4.33	-2.41	-5.20	-3.04	-4.33
1.05	2.43	5.31	3.09	4.44	-2.43	-5.31	-3.09	-4.44
1.10	2.46	5.41	3.14	4.52	-2.46	-5.41	-3.14	-4.52
1.15	2.48	5.48	3.19	4.59	-2.48	-5.48	-3.19	-4.59
1.20	2.50	5.55	3.23	4.65	-2.50	-5.55	-3.23	-4.65

Figure of RON = 240 Ohms IV Curve after ZQReset

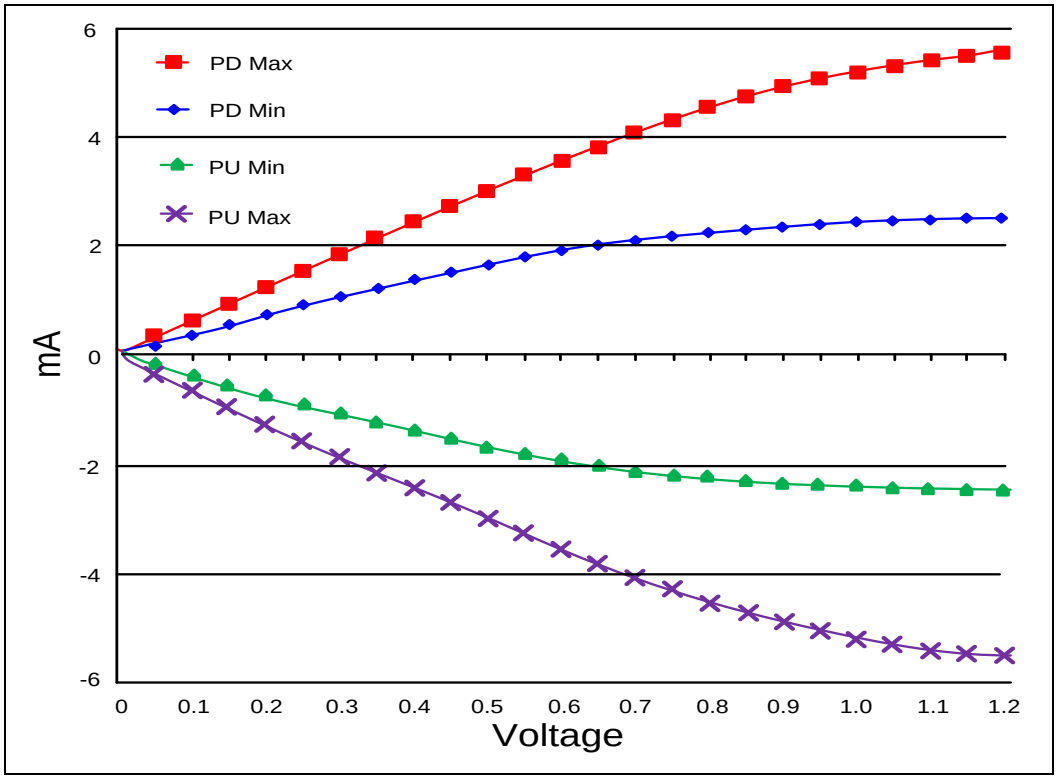
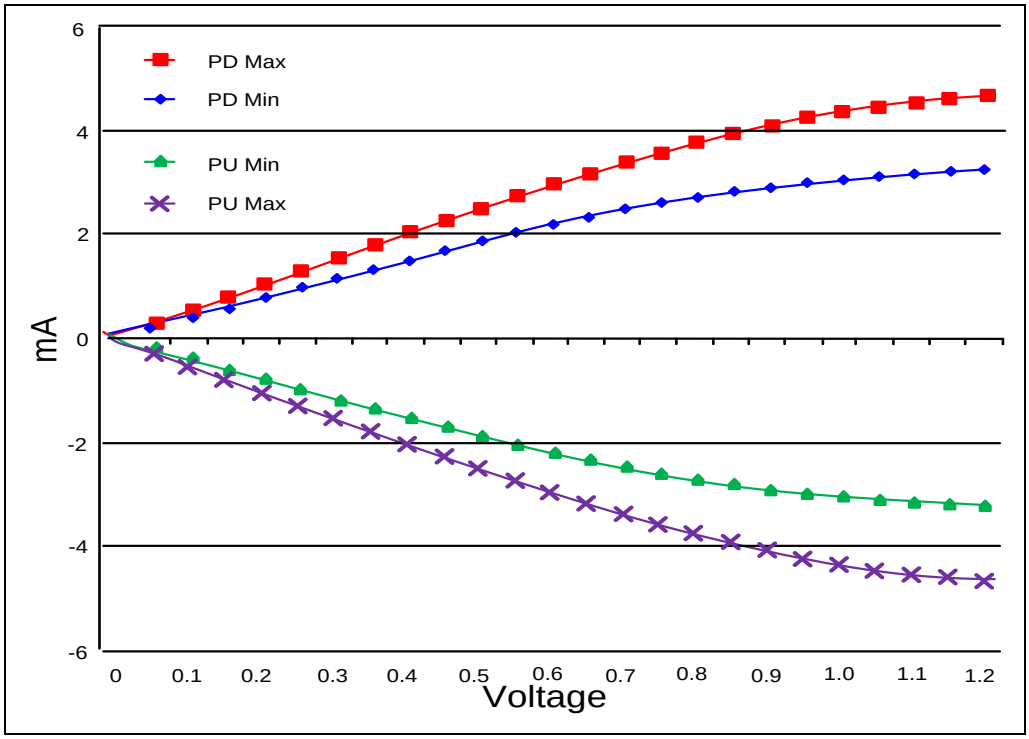


Figure of RON = 240 Ohms IV Curve after calibration



7.2.7 Input/Ouput Capacitance

Table — Input/output capacitance

Parameter	Symbol		LPDDR2 1066-466	LPDDR2 400-200	Units	Note
Input capacitance, CK_t and CK_c	CCK	Min	1.0		pF	1,2
		Max	2.0		pF	1,2
Input capacitance delta, CK_t and CK_c	CDCK	Min	0		pF	1,2,3
		Max	0.20	0.25	pF	1,2,3
Input capacitance, all other input-only pins	CI	Min	1.0		pF	1,2,4
		Max	2.0		pF	1,2,4
Input capacitance delta, all other input-only pins	CDI	Min	-0.40	-0.50	pF	1,2,5
		Max	0.40	0.50	pF	1,2,5
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	Min	1.25		pF	1,2,6,7
		Max	2.5		pF	1,2,6,7
Input/output capacitance delta, DQS_t, DQS_c	CDDQS	Min	0		pF	1,2,7,8
		Max	0.25	0.30	pF	1,2,7,8
Input/output capacitance delta, DQ, DM	CDIO	Min	-0.5	-0.6	pF	1,2,7,9
		Max	0.5	0.6	pF	1,2,7,9
Input/output capacitance ZQ Pin	CZQ	Min	0		pF	1,2
		Max	2.5		pF	1,2

(T_{OPER}; V_{DDQ} = 1.14- 1.3V; V_{DDCA} = 1.14-1.3V; V_{DD1} = 1.7-1.95V, LPDDR2-S4 V_{DD2} = 1.14-1.3V)

Note 1. This parameter applies to die device only (does not include package capacitance).

2.This parameter is not subject to production test. It is verified by design.

3. Absolute value of CCK_t - CCK_c.

4. CI applies to CS_n, CKE, CA0-CA9.

5. CDI = CI - 0.5 * (CCK_t + CCK_c)

6. DM loading matches DQ and DQS.

7. MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ohm typical)

8. Absolute value of CDQS_t and CDQS_c.

9. CDIO = CIO - 0.5 * (CDQS_t + CDQS_c) in byte-lane.

7.3 IDD Specification Parameters and Test Conditions

7.3.1 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:

LOW: VIN ≦VIL(DC) MAX

HIGH: VIN ≧VIH(DC) MIN

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See tables below.

7.3.1.1 Table of Definition of Switching for CA Input Signals

Switching for CA								
	CK_t (RISING) / Ck_C (FALLING)	CK_t (FALLING) / Ck_C (RISING)	CK_t (RISING) / Ck_C (FALLING)	CK_t (FALLING) / Ck_C (RISING)	CK_t (RISING) / Ck_C (FALLING)	CK_t (FALLING) / Ck_C (RISING)	CK_t (RISING) / Ck_C (FALLING)	CK_t (FALLING) / Ck_C (RISING)
Cycle	N		N+1		N+2		N+3	
CS_n	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Note 1. CS_n must always be driven HIGH.

2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.

3. The above pattern (N, N+1, N+2, N+3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.

7.3.1.2 Table of Definition of Switching for IDD4R

Clock	CKE	CS_n	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Read_Rising	HLH	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Read_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

Note 1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4R.

7.3.1.3 Table of Definition of Switching for IDD4W

Clock	CKE	CS_n	Clock Cycle Number	Command	CA0-CA2	CA3-CA9	All DQ
Rising	HIGH	LOW	N	Write_Rising	HLL	LHLHLHL	L
Falling	HIGH	LOW	N	Write_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 2	Write_Rising	HLL	HLHLLHL	H
Falling	HIGH	LOW	N + 2	Write_Falling	LLL	HHHHHHH	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	HHHHHHH	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	LHLHLHL	L

Note 1.Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2.Data masking (DM) must always be driven LOW.
3.The above pattern (N, N+1...) is used continuously during IDD measurement for IDD4W.

7.3.2 IDD Specifications

7.3.2.1 Table of LPDDR2 IDD Specification Parameters and Operating Conditions (x32)

Parameter/Condition	Symbol	Power Supply	533 MHz	400 MHz	Units	Note
Operating one bank active-precharge current: tCK = tCKmin; tRC = tRCmin; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD01	VDD1	TBD	8	mA	1
	IDD02	VDD2	TBD	25	mA	1
	IDD0IN	VDDCA VDDQ	TBD	3.5 1	mA	1,2
Idle power-down standby current: tCK = tCKmin; CKE is LOW;CS_n is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD2P1	VDD1	TBD	0.9	mA	1
	IDD2P2	VDD2	TBD	0.9	mA	1
	IDD2PIN	VDDCA VDDQ	TBD	0.015	mA	1,2
Idle power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is LOW;CS_n is HIGH; All banks/RBs idle; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD2PS1	VDD1	TBD	0.9	mA	1
	IDD2PS2	VDD2	TBD	0.9	mA	1
	IDD2PSIN	VDDCA VDDQ	TBD	0.015	mA	1,2
Idle non power-down standby current: tCK = tCKmin; CKE is HIGH;CS_n is HIGH; All banks/RBs idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD2N1	VDD1	TBD	1.2	mA	1
	IDD2N2	VDD2	TBD	10	mA	1
	IDD2NIN	VDDCA VDDQ	TBD	3.5 0.05	mA	1,2
Idle non power-down standby current with clock stop: CK_t =LOW, CK_c =HIGH; CKE is HIGH;CS_n is HIGH; All banks/RBs idle; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD2NS1	VDD1	TBD	1.2	mA	1
	IDD2NS2	VDD2	TBD	10	mA	1
	IDD2NSIN	VDDCA VDDQ	TBD	3.5 0.05	mA	1,2
Active power-down standby current tCK = tCKmin; CKE is LOW;CS_n is HIGH; One bank/RDB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD3P1	VDD1	TBD	2.3	mA	1
	IDD3P2	VDD2	TBD	1.4	mA	1
	IDD3PIN	VDDCA VDDQ	TBD	0.015	mA	1,2
Active power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is LOW;CS_n is HIGH; One bank/RDB active; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD3PS1	VDD1	TBD	2.3	mA	1
	IDD3PS2	VDD2	TBD	1.4	mA	1
	IDD3PSIN	VDDCA VDDQ	TBD	0.015	mA	1,2
Active non power-down standby current: tCK = tCKmin; CKE is HIGH;CS_n is HIGH; One bank/RDB active; CA bus inputs are SWITCHING; Data bus inputs are STABLE	IDD3N1	VDD1	TBD	2	mA	1
	IDD3N2	VDD2	TBD	14	mA	1
	IDD3NIN	VDDCA VDDQ	TBD	3.5 0.05	mA	1,2
Active non power-down standby current with clock stop: CK_t=LOW, CK_c=HIGH; CKE is HIGH;CS_n is HIGH; One bank/RDB active; CA bus inputs are STABLE; Data bus inputs are STABLE	IDD3NS1	VDD1	TBD	2	mA	1
	IDD3NS2	VDD2	TBD	14	mA	1
	IDD3NSIN	VDDCA VDDQ	TBD	3.5 0.05	mA	1,2

Parameter/Condition	Symbol	Power Supply	533 MHz	400 MHz	Units	Note
Operating burst read current: $t_{CK} = t_{CKmin}$; CS_n is HIGH; One bank/RDB active; BL = 4; RL = RLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4R_1$	VDD1	TBD	2	mA	1
	$IDD4R_2$	VDD2	TBD	160	mA	1
	$IDD4R_{IN}$	VDDCA	TBD	3.5	mA	1
Operating burst write current: $t_{CK} = t_{CKmin}$; CS_n is HIGH; One bank/RDB active; BL = 4; WL = WLmin; CA bus inputs are SWITCHING; 50% data change each burst transfer	$IDD4W_1$	VDD1	TBD	3	mA	1
	$IDD4W_2$	VDD2	TBD	200	mA	1
	$IDD4W_{IN}$	VDDCA VDDQ	TBD	3.5 12	mA	1,2
All Bank Refresh Burst current: $t_{CK} = t_{CKmin}$; CKE is HIGH; $t_{RC} = t_{RFCabmin}$; Burst refresh; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5_1$	VDD1	TBD	50	mA	1
	$IDD5_2$	VDD2	TBD	120	mA	1
	$IDD5_{IN}$	VDDCA VDDQ	TBD	3.5 0.05	mA	1,2
All Bank Refresh Average current: $t_{CK} = t_{CKmin}$; CKE is HIGH; $t_{RC} = t_{REFI}$; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5AB_1$	VDD1	TBD	8	mA	1
	$IDD5AB_2$	VDD2	TBD	15	mA	1
	$IDD5AB_{IN}$	VDDCA VDDQ	TBD	3.5 0.05	mA	1,2
Per Bank Refresh Average current: $t_{CK} = t_{CKmin}$; CKE is HIGH; $t_{RC} = t_{REFI}/8$; CA bus inputs are SWITCHING; Data bus inputs are STABLE;	$IDD5PB_1$	VDD1	TBD	3	mA	1
	$IDD5PB_2$	VDD2	TBD	16	mA	1
	$IDD5PB_{IN}$	VDDCA VDDQ	TBD	3.5 0.05	mA	1,2
Deep Power-Down current: CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;	$IDD8_1$	VDD1	TBD	15	uA	1
	$IDD8_2$	VDD2	TBD	15	uA	1
	$IDD8_{IN}$	VDDCA VDDQ	TBD	15	uA	1,2

Note :1. IDD values published are the typical of the distribution of the arithmetic mean.
2. Measured currents are the summation of VDDQ and VDDCA.
3. Guaranteed by design with output reference load of 5pfFand RON = 40Ohm.
4. IDD current specifications are tested after the device is properly initialized.

7.3.2.2 Table of IDD6 Partial Array Self-Refresh Current

Parameter		Symbol	Power Supply	533 MHz	400 MHz	Condition	Unit
IDD6 Partial Array Self-Refresh Current	Full Array	$IDD6_1$	VDD1	TBD	900	Self refresh current CK_t=LOW, CK_c=HIGH; CKE is LOW; CA bus inputs are STABLE; Data bus inputs are STABLE;	uA
		$IDD6_2$	VDD2	TBD	1900		
		$IDD6_{IN}$	VDDCA VDDQ	TBD	15		
	1/2 Array	$IDD6_1$	VDD1	TBD	750		uA
		$IDD6_2$	VDD2	TBD	1100		
		$IDD6_{IN}$	VDDCA VDDQ	TBD	15		
	1/4 Array	$IDD6_1$	VDD1	TBD	650		uA
		$IDD6_2$	VDD2	TBD	900		
		$IDD6_{IN}$	VDDCA VDDQ	TBD	15		
	1/8 Array	$IDD6_1$	VDD1	TBD	600		uA
		$IDD6_2$	VDD2	TBD	750		
		$IDD6_{IN}$	VDDCA VDDQ	TBD	15		

Note :1. LPDDR2-S4 SDRAM uses the same PASR scheme & IDD6 current value categorization as LPDDR (JESD209).
2. IDD values published are the typical of the distribution of the arithmetic mean.

7.4 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR2 device.

7.4.1 Definition for tCK(avg) and nCK

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^{N} tCK_j \right) / N$$

$$where \qquad N = 200$$

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

7.4.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

tCK(abs) is not subject to production test.

7.4.3 Definition for tCH(avg) and tCL(avg)
tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses

$$tCH(avg) = \left(\sum_{j=1}^{N} tCH_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^{N} tCL_j \right) / (N \times tCK(avg))$$

$$where \qquad N = 200$$

7.4.4 Definition for tJIT(per)
tJIT(per) is defined as the largest deviation of any signal tCK from tCK(avg).
tJIT(per) = Min/max of {tCKi - tCK(avg) where i = 1 to 200}.
tJIT(per) defines the single period jitter when the DLL is already locked.
tJIT(per) is not subject to production test.

7.4.5 Definition for tJIT(cc)
tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.
tJIT(cc) = Max of |{tCKi +1 - tCKi}|.
tJIT(cc) defines the cycle to cycle jitter.
tJIT(cc) is not subject to production test.

7.4.6 Definition for tERR(nper)
tERR is defined as the cumulative error across n multiple consecutive cycles from tCK(avg).
tERR(nper),act is the actual clock jitter over n cycles for a given system.
tERR(nper),allowed is the specified allowed clock period jitter over n cycles.
tERR(nper) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

tERR(nper),min can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68LN(n)) \times tJIT(per), min$$

tERR(nper),max can be calculated by the formula shown below:

$$tERR(nper), max = (1 + 0.68LN(n)) \times tJIT(per), max$$

Using these equations, tERR(nper) tables can be generated for each tJIT(per),act value.

7.4.7 Definition for duty cycle jitter tJIT(duty)

tJIT(duty) is defined with absolute and average specification of tCH / tCL.

tJIT(duty),min=MIN((tCH(abs),min–tCH(avg),min),tCL(abs),min–tCL(avg),min)) x tCK(avg)

tJIT(duty),max=MAX((tCH(abs),max–tCH(avg),max),tCL(abs),max–tCL(avg),max)) x tCK(avg)

7.4.8 Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

Table 100 — Definition for tCK(abs), tCH(abs), and tCL(abs)

Parameter	Symbol	Min	Unit
Absolute Clock Period	tCK(abs)	tCK(avg),min + tJIT(per),min	PS
Absolute Clock HIGH Pulse Width	tCH(abs)	tCH(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)
Absolute Clock LOW Pulse Width	tCL(abs)	tCL(avg),min + tJIT(duty),min / tCK(avg)min	tCK(avg)

Note 1. tCK(avg),min is expressed is ps for this table.
2 .tJIT(duty),min is a negative value.

7.4.9 Period Clock Jitter

LPDDR2 devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in Table of AC timing and how to determine cycle time de-rating and clock cycle de-rating.

7.4.9.1 Clock period jitter effects on core timing parameters (tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR2 device is characterized and verified to support tnPARAM = RU{tPARAM / tCK(avg)}.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

7.4.9.2 Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter (tCORE).

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

7.4.9.3 Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)).

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter (tCORE).

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM),act - tERR(tnPARAM),allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

7.4.9.4 Clock jitter effects on C/A timing (tIS,tIH,tISCKE,tIHCKE,tISb, tIHb, tISCKEb, tIHCKEb)

These parameters are measured from a command/address signal (CKE, CS, CA0 - CA9) transition edge to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

Clock jitter effects on Read timing parameters

7.4.9.5 Clock jitter effects on Read timing tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per),act,max - tJIT(per),allowed,max}{tCK(avg)}\right)$$

For example,

if the measured jitter into a LPDDR2-800 device has tCK(avg) = 2500 ps, tJIT(per),act,min = -172 ps and tJIT(per),act,max = + 193 ps, then

tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 0.9 - (193 - 100)/2500= .8628 tCK(avg)

7.4.9.6 Clock jitter effects on Read timing tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0–31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per).

7.4.9.7 Clock jitter effects on Read timing parameters tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min. Therefore tQSH(abs)min and tQSL(abs)min can be specified with tCH(abs)min and tCL(abs)min.

tQSH(abs)min = tCH(abs)min – 0.05

tQSL(abs)min = tCL(abs)min – 0.05

These parameters determine absolute Data-Valid window at the LPDDR2 device pin.

Absolute min data-valid window @ LPDDR2 device pin =

min { (tQSH(abs)min * tCK(avg)min – tDQSQmax – tQHSmax) , (tQSL(abs)min * tCK(avg)min – tDQSQmax – tQHSmax) }

This minimum data-valid window shall be met at the target frequency regardless of clock jitter.

7.4.9.8 Clock jitter effects on Read timing parameters tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.

tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

Clock jitter effects on Write timing parameters

7.4.9.9 Clock jitter effects on Write timing parameters tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQSn_t, DQSn_c : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

7.4.9.10 Clock jitter effects on Write timing parameters tDSS, tDSH

These parameters are measured from a data strobe signal (DQSx_t, DQSx_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), as the setup and hold are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values shall be met.

7.4.9.11 Clock jitter effects on Write timing parameters tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS(min, derated) = 0.75 - \frac{tJIT(per), act,min - tJIT(per),allowed,min}{tCK(avg)}$$

$$tDQSS(max, derated) = 1.25 - \frac{tJIT(per), act,max - tJIT(per),allowed,max}{tCK(avg)}$$

For example,

if the measured jitter into a LPDDR2-800 device has tCK(avg)= 2500 ps, tJIT(per),act,min= -172 ps and tJIT(per),act,max= + 193 ps, then

tDQSS,(min,derated) = 0.75 +(tJIT(per),act,min - tJIT(per),allowed,min)/tCK(avg) = 0.75 - (-172 + 100)/2500 = .7788 tCK(avg) and tDQSS,(max,derated) = 1.25 + (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 1.25 - (193 - 100)/2500 = 1.2128 tCK(avg)

7.5 Refresh Requirements

7.5.1 LPDDR2-S4 Refresh Requirement Parameters

Parameter		Symbol	1 Gb	Unit
Number of Banks			8	
Refresh WindowTj ≤ 85°C		tREFW	32	ms
Refresh Window85°C < Tj ≤ 105°C ms		tREFW	8	ms
Required number of REFRESH commands (min)		R	4,096	
Average time between REFRESH commands (for reference only) Tj ≤ 85°C	REFab	tREFI	7.8	us
	REFpb	tREFIpb	0.975	us
Refresh Cycle time		tRFCab	130	ns
Per Bank Refresh Cycle time		tRFCpb	60	ns
Burst Refresh Window= 4 x 8 x tRFCab		tREFBW	4.16	us

7.6 AC Timings

7.6.1 Table of LPDDR2 AC Timing

Parameter	Symbol	min / max	min tCK	1066	933	800	667	533	400	333	Unit
Max. Frequency*4		~		533	466	400	333	266	200	166	MHz
Clock Timing											
Average Clock Period	tCK(avg)	min		1.875	2.15	2.5	3	3.75	5	6	ns
		max		100							
Average high pulse width	tCH(avg)	min		0.45							tCK(avg)
		max		0.55							
Average low pulse width	tCL(avg)	min		0.45							tCK(avg)
		max		0.55							
Absolute Clock Period	tCK(abs)	min		tCK(avg)min + tJIT(per)min							ps
Absolute clock HIGH pulse width (with allowed jitter)	tCH(abs) allowed	min		0.43							tCK(avg)
		max		0.57							
Absolute clock LOW pulse width (with allowed jitter)	tCL(abs) (allowed)	min		0.43							tCK(avg)
		max		0.57							
Clock Period Jitter (with allowed jitter)	tJIT(per) (allowed)	min		-90	-95	-100	-110	-120	-140	-150	ps
		max		90	95	100	110	120	140	150	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	tJIT(cc) allowed	max		180	190	200	220	240	280	300	ps
Duty cycle Jitter (with allowed jitter)	tJIT(duty), allowed	min		min((tCH(abs),min - tCH(avg),min), (tCL(abs),min - tCL(avg),min)) * tCK(avg)							ps
		max		max((tCH(abs),max - tCH(avg),max), (tCL(abs),max - tCL(avg),max)) * tCK(avg)							ps
Cumulative error across 2 cycles	tERR(2per) (allowed)	min		-132	-140	-147	-162	-177	-206	-221	ps
		max		132	140	147	162	177	206	221	
Cumulative error across 3 cycles	tERR(3per) (allowed)	min		-157	-166	-175	-192	-210	-245	-262	ps
		max		157	166	175	192	210	245	262	
Cumulative error across 4 cycles	tERR(4per) (allowed)	min		-175	-185	-194	-214	-233	-272	-291	ps
		max		175	185	194	214	233	272	291	
Cumulative error across 5 cycles	tERR(5per) (allowed)	min		-188	-199	-209	-230	-251	-293	-314	ps
		max		188	199	209	230	251	293	314	
Cumulative error	tERR(6per)	min		-200	-211	-222	-244	-266	-311	-333	ps

across 6 cycles	(allowed)	max		200	211	222	244	266	311	333	
Cumulative error across 7 cycles	tERR(7per) (allowed)	min		-209	-221	-232	-256	-279	-325	-348	ps
		max		209	221	232	256	279	325	348	
Cumulative error across 8 cycles	tERR(8per) (allowed)	min		-217	-229	-241	-266	-290	-338	-362	ps
		max		217	229	241	266	290	338	362	
Cumulative error across 9 cycles	tERR(9per) (allowed)	min		-224	-237	-249	-274	-299	-349	-374	ps
		max		224	237	249	274	299	349	374	
Cumulative error across 10 cycles	tERR(10per) (allowed)	min		-231	-244	-257	-282	-308	-359	-385	ps
		max		231	244	257	282	308	359	385	
Cumulative error across 11 cycles	tERR(11per) (allowed)	min		-237	-250	-263	-289	-316	-368	-395	ps
		max		237	250	263	289	316	368	395	
Cumulative error across 12 cycles	tERR(12per) (allowed)	min		-242	-256	-269	-296	-323	-377	-403	ps
		max		242	256	269	296	323	377	403	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper) (allowed)	min		tERR(nper),allowed,min = (1 + 0.68ln(n)) * tJIT(per),allowed,min							ps
		max		tERR(nper),allowed,max = (1 + 0.68ln(n)) * tJIT(per),allowed,max							

Parameter	Symbol	min / max	min tCK	1066	933	800	667	533	400	333	Unit
ZQ Calibration Parameters											
Initialization Calibration Time*14	tZQINIT	min		1							us
Full Calibration Time*14	tZQCL	min	6	360							ns
Short Calibration Time*14	tZQCS	min	6	90							ns
Calbration Reset Time*14	tZQRESET	min	3	50							ns
Read Parameters*11											
DQS output access time from CK_t/CK_c	tDQSCK	min		2500							ps
		max		5500							
DQSCK Delta Short*15	tDQSCKDS	max		330	380	450	540	670	900	1080	ps
DQSCK Delta Medium*16	tDQSCKDM	max		680	780	900	1050	1350	1800	1900	ps
DQSCK Delta Long*17	tDQSCKDL	max		920	1050	1200	1400	1800	2400	-	ps
DQS - DQ skew	tDQSQ	max		200	220	240	280	340	400	500	ps
Data hold skew factor	tQHS	max		230	260	280	340	400	480	600	ps
DQS Output High Pulse Width	tQSH	min		tCH(abs) - 0.05							tCK(avg)
DQS Output Low Pulse Width	tQSL	min		tCL(abs) - 0.05							tCK(avg)
Data Half Period	tQHP	min		min(tQSH, tQSL)							tCK(avg)
DQ / DQS output hold time from DQS	tQH	min		tQHP - tQHS							ps
Read preamble*11,*12	tRPRE	min		0.9							tCK(avg)
Read postamble*11,*13	tRPST	min		tCL(abs) - 0.05							tCK(avg)
DQS low-Z from clock*11	tLZ(DQS)	min		tDQSCK(MIN) - 300							ps
DQ low-Z from clock*11	tLZ(DQ)	min		tDQSCK(MIN) - (1.4 * tQHS(MAX))							ps
DQS high-Z from clock*11	tHZ(DQS)	max		tDQSCK(MAX) - 100							ps
DQ high-Z from clock*11	tHZ(DQ)	max		tDQSCK(MAX) + (1.4 * tDQSQ(MAX))							ps

Parameter	Symbol	min / max	min tCK	1066	933	800	667	533	400	333	Unit
Write Parameters*11											
DQ and DM input hold time (Vref based)	tDH	min		210	235	270	350	430	480	600	ps
DQ and DM input setup time (Vref based)	tDS	min		210	235	270	350	430	480	600	ps
DQ and DM input pulse width	tDIPW	min		0.35							tCK(avg)
Write command to 1st DQS latching transition	tDQSS	min		0.75							tCK(avg)
		max		1.25							
DQS input high-level width	tDQSH	min		0.4							tCK(avg)
DQS input low-level width	tDQSL	min		0.4							tCK(avg)
DQS falling edge to CK setup time	tDSS	min		0.2							tCK(avg)
DQS falling edge hold time from CK	tDSH	min		0.2							tCK(avg)
Write postamble	tWPST	min		0.4							tCK(avg)
Write preamble	tWPRE	min		0.35							tCK(avg)
CKE Input Parameters											
CKE min. pulse width (high and low pulse width)	tCKE	min	3	3							tCK(avg)
CKE input setup time	tISCKE*2	min		0.25							tCK(avg)
CKE input hold time	tIHCKE*3	min		0.25							tCK(avg)
Command Address Input Parameters*11											
Address and control input setup time (Vref based)	tIS*1	min		220	250	290	370	460	600	740	ps
Address and control input hold time (Vref based)	tIH*1	min		220	250	290	370	460	600	740	ps
Address and control input pulse width	tIPW	min		0.40							tCK(avg)

Parameter	Symbol	min / max	min tCK	LPDDR2							Unit
				1066	933	800	667	533	400	333	
Boot Parameters (10 MHz - 55 MHz) *5,7											
Clock Cycle Time	tCKb	max		100							ns
		min		18							
CKE Input Setup Time	tISCKEb	min		2.5							ns
CKE Input Hold Time	tIHCKEb	min		2.5							ns
Address & Control Input Setup Time	tISb	min		1150							ps
Address & Control Input Hold Time	tIHb	min		1150							ps
DQS Output Data Access Time from CK_t/CK_c	tDQSCKb	min		2.0							ns
		max		10.0							
Data Strobe Edge to Ouput Data Edge tDQSQb - 1.2	tDQSQb	max		1.2							ns
Data Hold Skew Factor	tQHSb	max		1.2							ns

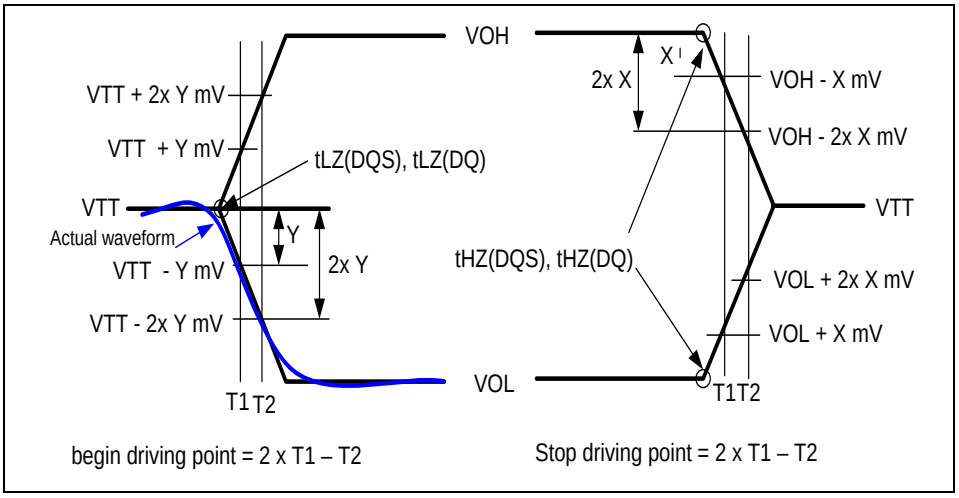
Parameter	Symbol	min / max	min tCK	LPDDR2							Unit
				1066	933	800	667	533	400	333	
Mode Register Parameters											ns
MODE REGISTER Write command period	tMRW	min	5	5							tCK(avg)
Mode Register Read command period	tMRR	min	2	2							tCK(avg)
LPDDR2 SDRAM Core Parameters*9											
Read Latency	RL	min	3	8	7	6	5	4	3	3	tCK(avg)
Write Latency	WL	min	1	4	4	3	2	2	1	1	tCK(avg)
ACTIVE to ACTIVE command period	tRC	min		tRAS + tRPab (with all-bank Precharge) tRAS + tRPpb (with per-bank Precharge)							ns
CKE min. pulse width during Self-Refresh (low pulse width during Self-Refresh)	tCKESR	min	3	15							ns
Self refresh exit to next valid command delay	tXSR	min	2	tRFCab + 10							ns
Exit power down to next valid command delay	tXP	min	2	7.5							ns
LPDDR2-S4 CAS to CAS delay	tCCD	min	2	2							tCK(avg)
Internal Read to Precharge command delay	tRTP	min	2	7.5							ns
RAS to CAS Delay	tRCD	Fast	3	15							ns
Row Precharge Time (single bank)	tRPpb	Fast	3	15							ns
Row Precharge Time (all banks)	tRPab 8-bank	Fast	3	18							ns
Row Active Time	tRAS	min	3	42							ns
		max		70							us
Write Recovery Time	tWR	min	3	15							ns
Internal Write to Read Command Delay	tWTR	min	2	7.5					10		ns
Active bank A to Active bank B	tRRD	min	2	10							ns
Four Bank Activate Window	tFAW	min	8	50						60	ns
Minimum Deep Power Down Time	tDPD	min		500							us

Parameter	Symbol	min / max	min tCK	LPDDR2							Unit
				1066	933	800	667	533	400	333	
LPDDR2 Temperature De-Rating											
tDQSCK De-Rating	tDQSCK (Derated)	max		5620	6000						ps
Core Timings Temperature De-Rating	tRCD (Derated)	min		tRCD + 1.875							ns
	tRC (Derated)	min		tRC + 1.875							ns
	tRAS (Derated)	min		tRAS + 1.875							ns
	tRP (Derated)	min		tRP + 1.875							ns
	tRRD (Derated)	min		tRRD + 1.875							ns

Note :1. Input set-up/hold time for signal(CA[0:n], CS_n)

2. CKE input setup time is measured from CKE reaching high/low voltage level to CK_t/CK_c crossing.
3. CKE input hold time is measured from CK_t/CK_c crossing to CKE reaching high/low voltage level
4. Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.
5. To guarantee device operation before the LPDDR2 device is configured a number of AC boot timing parameters are defined in this Table. Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.
6. Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.
7. The SDRAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in “Mode Register Definition”.
8. The output skew parameters are measured with Ron default settings into the reference load.
9. The min tCK column applies only when tCK is greater than 6ns for LPDDR2-S4 devices .
10. All AC timings assume an input slew rate of 1V/ns.
11. Read, Write, and Input Setup and Hold values are referenced to Vref.
12. For low-to-high and high-to-low transitions, the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure below shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.

Figure of HSUL_12 Driver Output Reference Load for Timing and Slew Rate



The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS_t-DQS_c.

13. Measured from the start driving of DQS_t - DQS_c to the start driving the first rising strobe edge.
14. Measured from the from start driving the last falling strobe edge to the stop driving DQS_t , DQS_c.
15. tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a contiguous sequence of bursts within a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.
16. tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 1.6us rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.
17. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10C/s. Values do not include clock jitter.

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7.6.2 CA and CS_n Setup, Hold and Derating

For all input signals (CA and CS_n) the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value to the ∆tIS and ∆tIH derating value respectively. Example: tIS (total setup time) = tIS(base) + ∆tIS.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in Tablebelow, the derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization.

7.6.2.1 Table of CA and CS_n Setup and Hold Base-Values for 1V/ns

unit [ps]	LPDDR2					reference
	1066	933	800	667	533	
tIS(base)	0	30	70	150	240	$V_{IH/L(ac)=VREF(dc)+-220mV}$
tIH(base)	90	120	160	240	330	$V_{IH/L(dc)=VREF(dc)+-130mV}$

unit [ps]	LPDDR2		reference
	400	333	
tIS(base)	300	440	$V_{IH/L(ac)=VREF(dc)+-300mV}$
tIH(base)	400	540	VIH/L(dc)VREF(dc)+-200mV

Note : ac/dc referenced for 1V/ns CA and CS_n slew rate and 2V/ns differential CK_t-CK_c slew rate.

7.6.2.2 Table of Derating values LPDDR2 tIS/tIH - ac/dc based AC220

ΔtIS, ΔtIH derating in [ps] AC/DC based
AC220 Threshold -> VIH(ac)=VREF(dc)+220mV, VIL(ac)=VREF(dc)-220mV
DC100 Threshold -> VIH(dc)=VREF(dc)+130mV, VIL(dc)=VREF(dc)-130mV

		CK_t,CK_c Differential Slew Ratee															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA , CS_n Slew Rate V/ns	2.0	110	65	110	65	110	65										
	1.5	74	43	73	43	73	43	89	59								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-3	-5	-3	-5	13	11	29	27	45	43				
	0.8					-8	-13	8	3	24	19	40	35	56	55		
	0.7							2	-6	18	10	34	26	50	46	66	78
	0.6									10	-3	26	13	42	33	58	65
	0.5											4	-4	20	16	36	48
	0.4													-7	2	17	34

Note: Cell contents shaded in red are defined as 'not supported'.

7.6.2.3 Table of Derating values LPDDR2 tIS/tIH - ac/dc based AC300

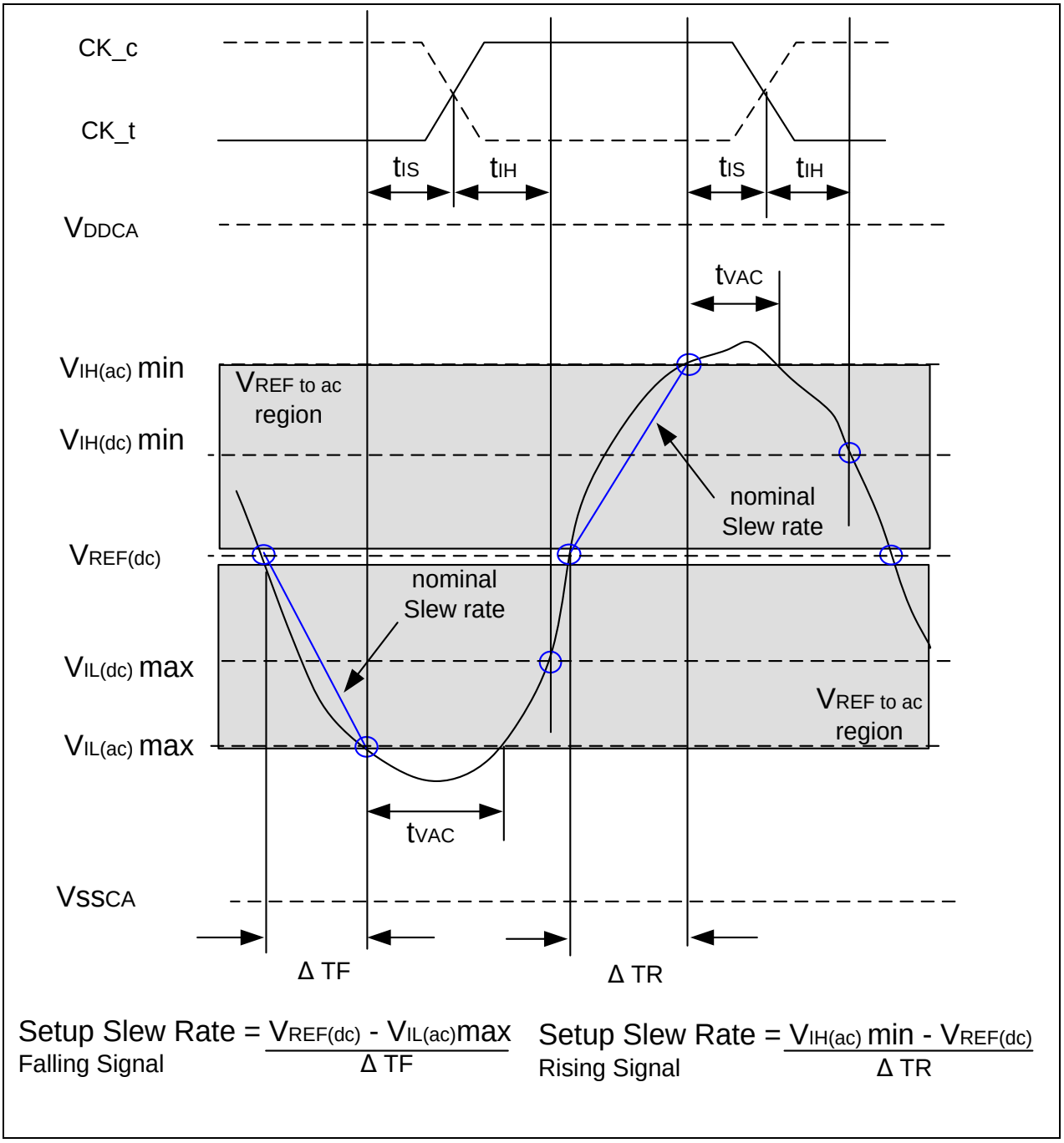
ΔtIS, ΔtIH derating in [ps] AC/DC based AC300 Threshold -> VIH(ac)=VREF(dc)+300mV, VIL(ac)=VREF(dc)-300mV DC200 Threshold -> VIH(dc)=VREF(dc)+200mV, VIL(dc)=VREF(dc)-200mV																	
		CK_t,CK_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CA, CS_n Slew Rate V/ns	2.0	150	100	150	100	150	100										
	1.5	100	67	100	67	100	67	116	83								
	1.0	0	0	0	0	0	0	16	16	32	32						
	0.9			-4	-8	-4	-8	12	8	28	24	44	40				
	0.8					-12	-20	4	-4	20	12	36	28	52	48		
	0.7							-3	-18	13	-2	29	14	45	34	61	66
	0.6									2	-21	18	-5	34	15	50	47
	0.5											-12	-32	4	-12	20	20
	0.4													-35	-40	-11	-8

Note: Cell contents shaded in red are defined as 'not supported'.

7.6.2.4 Table of Required time tVAC above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate [V/ns]	tVAC @ 300mV [ps]		tVAC @ 220mV [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
<0.5	0	-	150	-

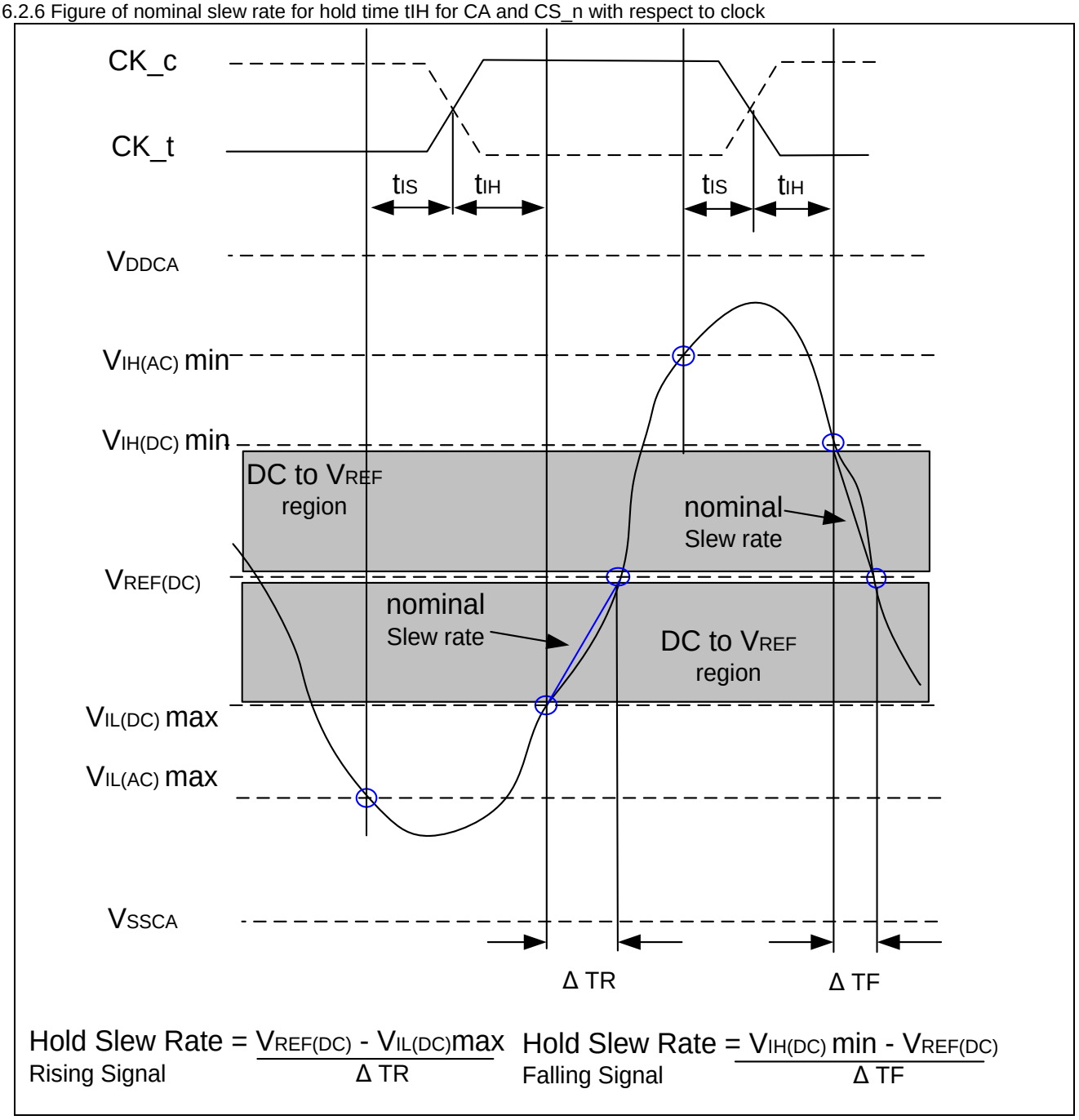
7.6.2.5 Figure of nominal slew rate and tVAC for tIS for CA and CS_n with respect to clock.



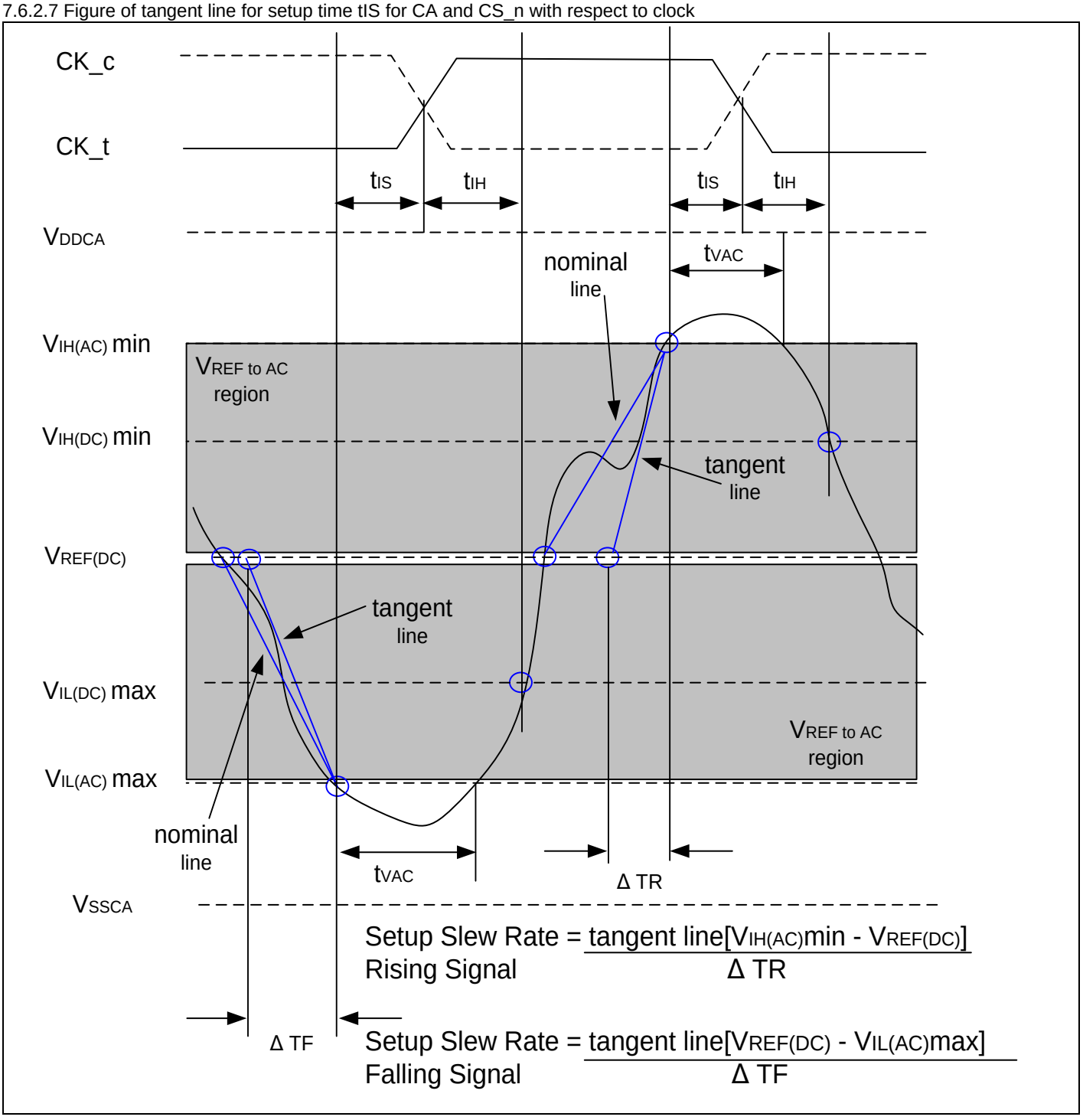
Setup Slew Rate = $\frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF}$ Falling Signal

Setup Slew Rate = $\frac{V_{IH(ac)}\,min - V_{REF(dc)}}{\Delta TR}$ Rising Signal

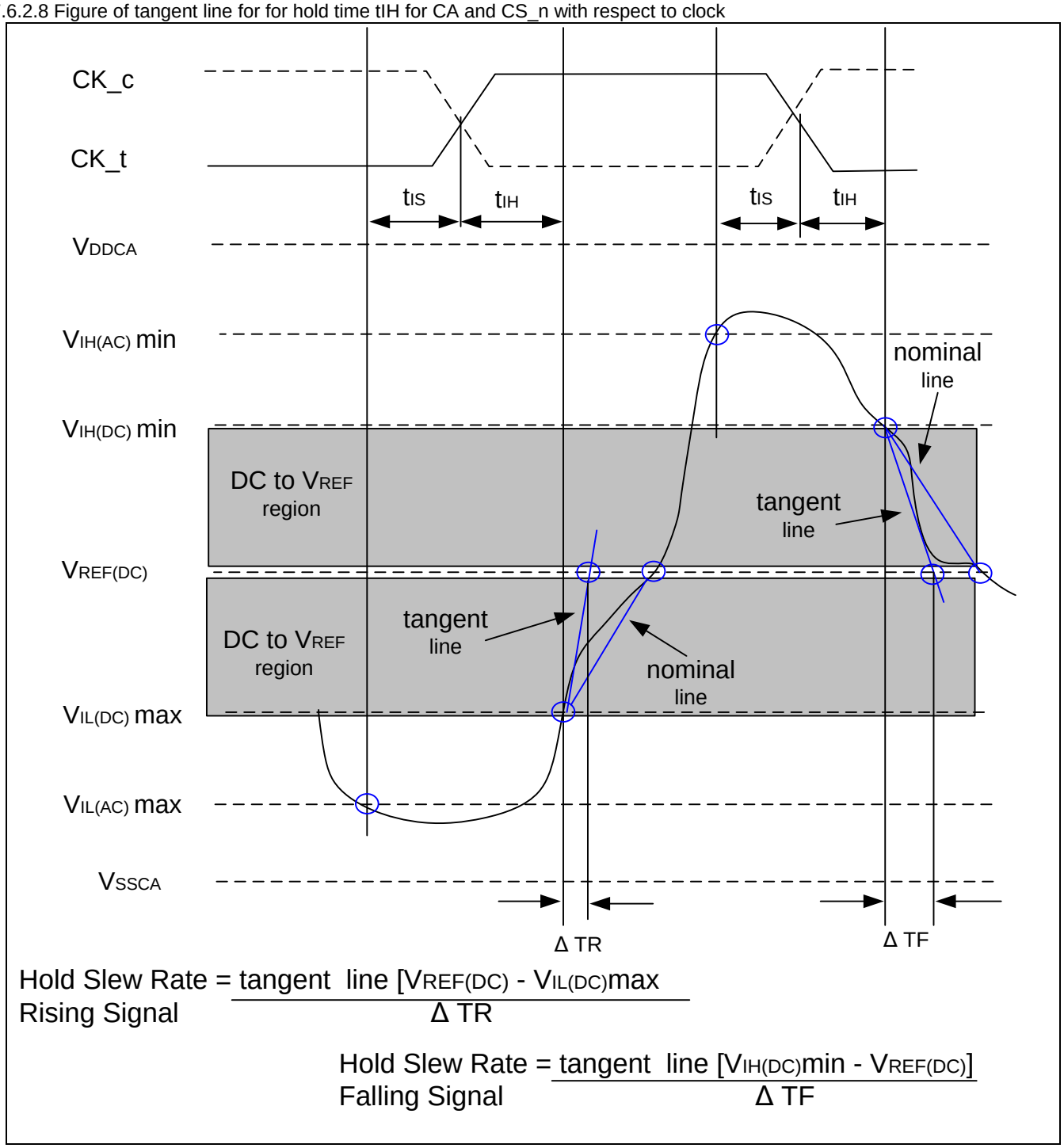
7.6.2.6 Figure of nominal slew rate for hold time tIH for CA and CS_n with respect to clock



7.6.2.7 Figure of tangent line for setup time tIS for CA and CS_n with respect to clock



7.6.2.8 Figure of tangent line for for hold time tIH for CA and CS_n with respect to clock



$$\text{Hold Slew Rate}_{\text{Rising Signal}} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)}\text{max}}{\Delta \text{ TR}}$$

$$\text{Hold Slew Rate}_{\text{Falling Signal}} = \frac{\text{tangent line } [V_{IH(DC)}\text{min} - V_{REF(DC)}]}{\Delta \text{ TF}}$$

7.6.3 Data Setup, Hold and Slew Rate Derating

For all input signals (DQ, DM) the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS(base) and tDH(base) value to the ∆tDS and ∆tDH derating value respectively. Example: tDS (total setup time) = tDS(base) + ∆tDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIL(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tDH) nominal slew rate for a falling sig5nal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to VREF(dc) region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC.

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization

7.6.3.1 Table of Data Setup and Hold Base-Values

[ps]	LPDDR2					reference
	1066	933	800	667	533	
tDS(base)	-10	15	50	130	210	$V_{IH/L(ac)=VREF(dc)+-220mV}$
tDH(base)	80	105	140	220	300	$V_{IH/L(dc)=VREF(dc)+-130mV}$

unit [ps]	LPDDR2		reference
	400	333	
tDS(base)	180	300	$V_{IH/L(ac)=VREF(dc)+-300mV}$
tDH(base)	280	400	$V_{IH/L(dc)VREF(dc)+-200mV}$

Note : ac/dc referenced for 1V/ns DQ,DM slew rate and 2V/ns differential DQS_t-DQS_c slew rate

7.6.3.2 Table of Derating values LPDDR2 tDS/tDH - ac/dc based AC220

ΔtDS, ΔDH derating in [ps] AC/DC based a AC220 Threshold -> VIH(ac)=VREF(dc)+220mV, VIL(ac)=VREF(dc)-220mV DC130 Threshold -> VIH(dc)=VREF(dc)+130mV, VIL(dc)=VREF(dc)-130mV																	
		DQS_t, DQS_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ, DM Slew Rate V/ns	2.0	110	65	110	65	110	65	-	-	-	-	-	-	-	-	-	-
	1.5	74	43	73	43	73	43	89	59	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-3	-5	-3	-5	13	11	29	27	45	43	-	-	-	-
	0.8	-	-	-	-	-8	-13	8	3	24	19	40	35	56	55	-	-
	0.7	-	-	-	-	-	-	2	-6	18	10	34	26	50	46	66	78
	0.6	-	-	-	-	-	-	-	-	10	-3	26	13	42	33	58	65
	0.5	-	-	-	-	-	-	-	-	-	-	4	-4	20	16	36	48
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-7	2	17	34

Note: Cell contents shaded in red are defined as 'not supported'.

7.6.3.3 Table of Derating values LPDDR2 tDS/tDH - ac/dc based AC300

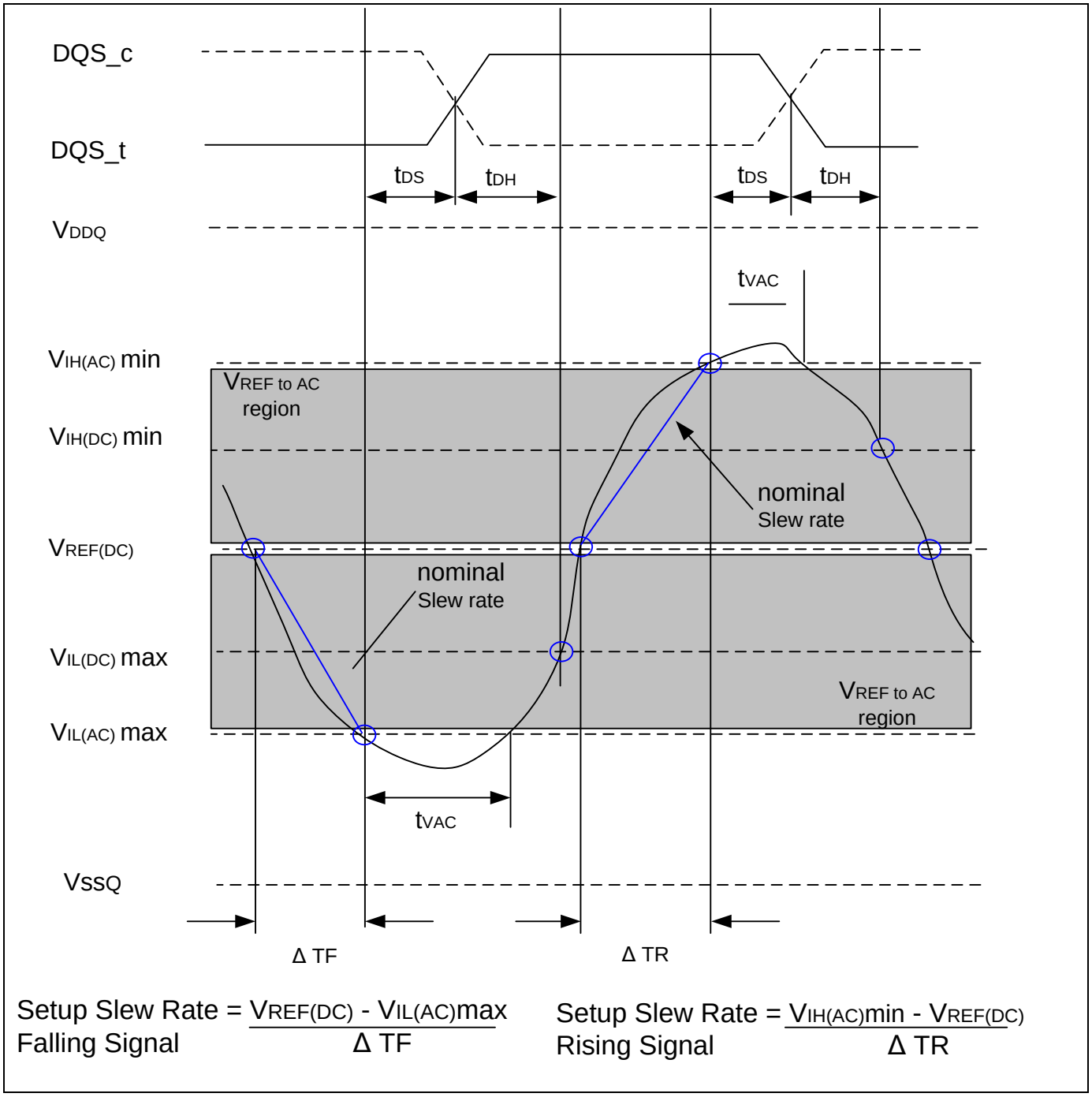
ΔtDS, ΔDH derating in [ps] AC/DC based a AC300 Threshold -> VIH(ac)=VREF(dc)+300mV, VIL(ac)=VREF(dc)-300mV DC200 Threshold -> VIH(dc)=VREF(dc)+200mV, VIL(dc)=VREF(dc)-200mV																	
		DQS_t, DQS_c Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ, DM Slew Rate V/ns	2.0	150	100	150	100	150	100	-	-	-	-	-	-	-	-	-	-
	1.5	100	67	100	67	100	67	116	83	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	16	16	32	32	-	-	-	-	-	-
	0.9	-	-	-4	-8	-4	-8	12	8	28	24	44	40	-	-	-	-
	0.8	-	-	-	-	-12	-20	4	-4	20	12	36	28	52	48	-	-
	0.7	-	-	-	-	-	-	-3	-18	13	-2	29	14	45	34	61	66
	0.6	-	-	-	-	-	-	-	-	2	-21	18	-5	34	15	50	47
	0.5	-	-	-	-	-	-	-	-	-	-	-12	-32	4	-12	20	20
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-35	-40	-11	-8

Note: Cell contents shaded in red are defined as 'not supported'.

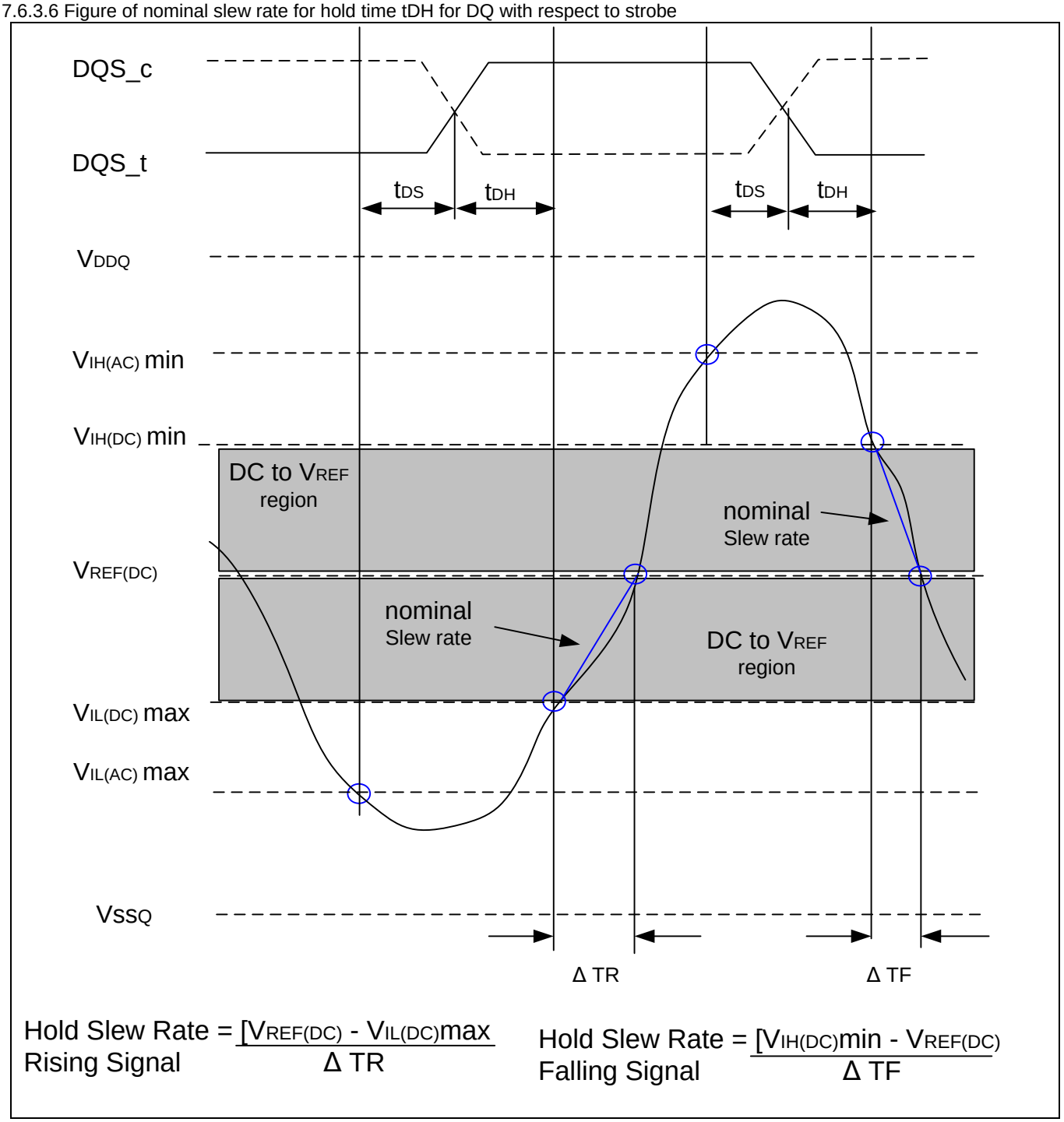
7.6.3.4 Table of Required time tVAC above VIH(ac) {below VIL(ac)} for valid transition

Slew Rate [V/ns]	t_{VAC} @ 300mV [ps]		t_{VAC} @ 220mV [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
< 0.5	0	-	150	-

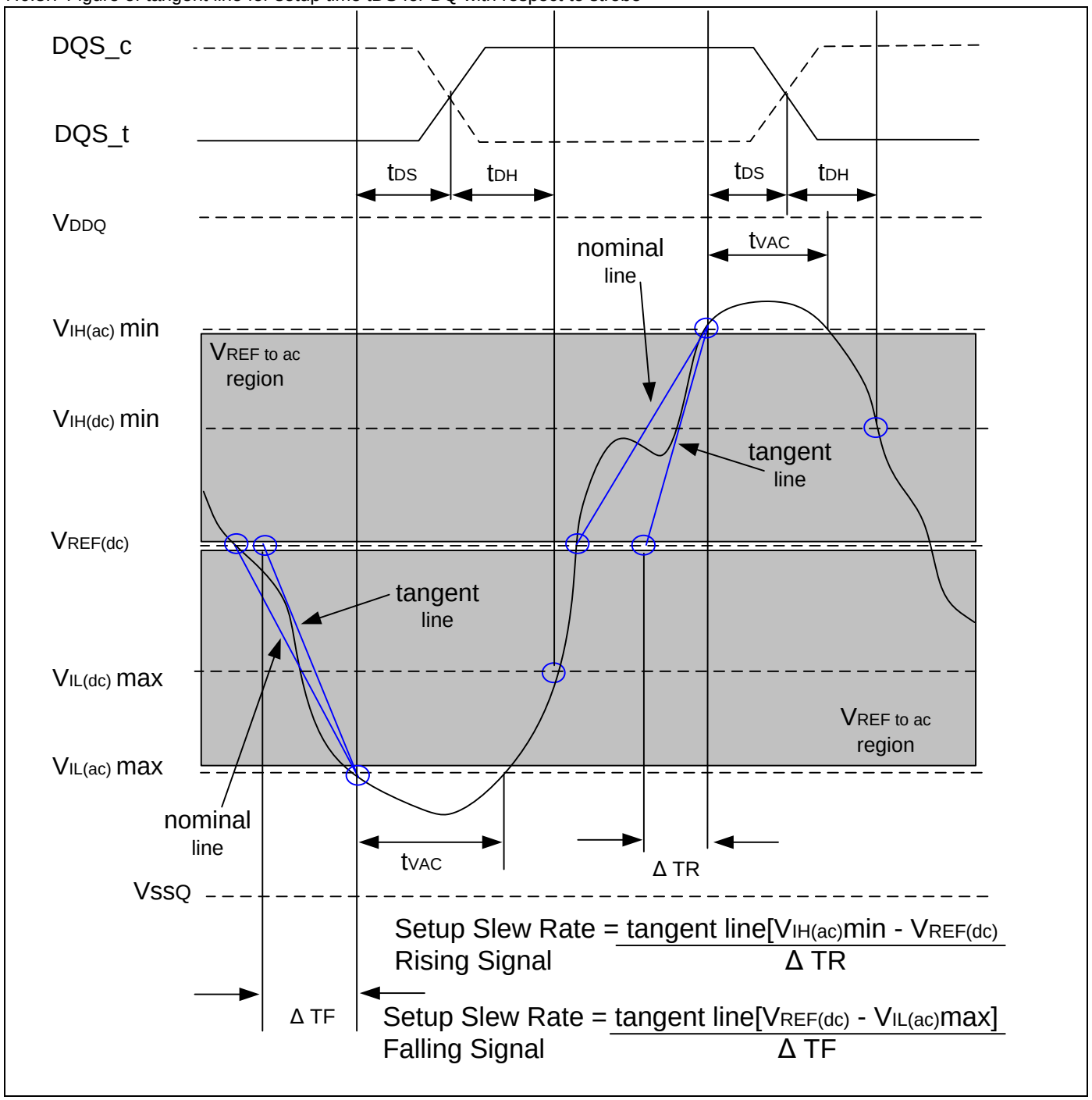
7.6.3.5 Figure of nominal slew rate and tVAC for setup time tDS for DQ with respect to strobe



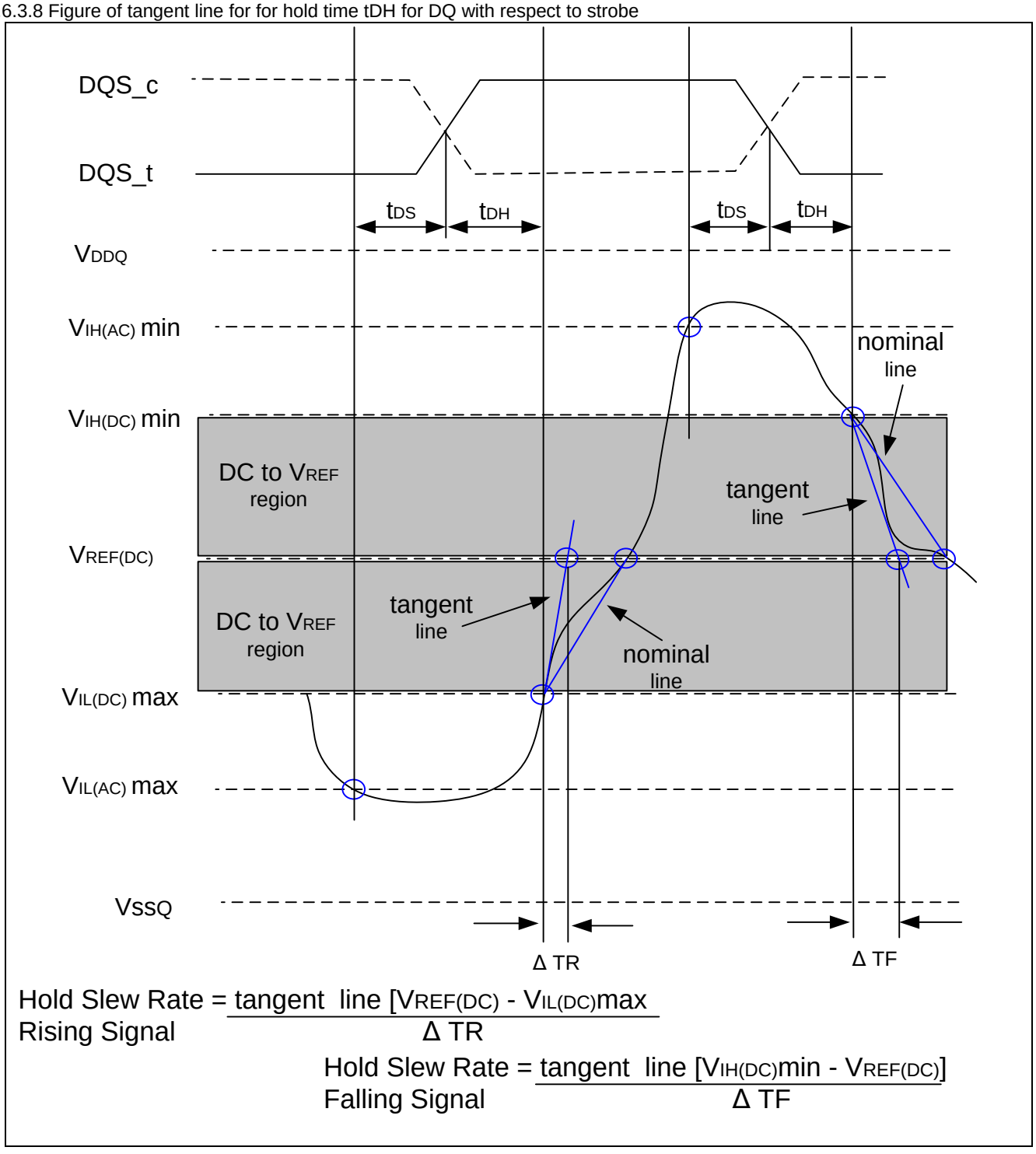
7.6.3.6 Figure of nominal slew rate for hold time tDH for DQ with respect to strobe



7.6.3.7 Figure of tangent line for setup time tDS for DQ with respect to strobe



7.6.3.8 Figure of tangent line for for hold time tDH for DQ with respect to strobe



$$\text{Hold Slew Rate}_{\text{Rising Signal}} = \frac{\text{tangent line } [V_{REF(DC)} - V_{IL(DC)}\text{max}}{\Delta \text{ TR}}$$

$$\text{Hold Slew Rate}_{\text{Falling Signal}} = \frac{\text{tangent line } [V_{IH(DC)}\text{min} - V_{REF(DC)}]}{\Delta \text{ TF}}$$

8. REVISION HISTORY

Version	Date	Page	Description
P01-001	05/18/2012	All	New create document.
P01-002	06/14/2013	1,9,78,99 2 15 36 59 1 1,45~48,78,106 8 100	Update Temp. Add ordering Info & update part#. Add tZQINIT(8.2.2) Add 6.4.7.2 note 2. Update 6.4.22.2 bank MRR:Idle to Active. Remove "option" text. Update Tc to Tj. Add DQ text. Remove IDD4RQ.
P01-003	10/24/2013	99~101	Add IDDx value (400 MHz).
P01-004	11/15/2013	99~101	Update typical IDDx value for 400MHz.
P01-004A	7/15/2014	N/A	Document modified for MCP implementation.

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