

# MOSFET - P-Channel, PowerTrench®, Logic Level -40 V, -25 A, 21 mΩ

## FDD9511L-F085

### Features

- Typ  $r_{DS(on)} = 17 \text{ m}\Omega$  at  $V_{GS} = -10 \text{ V}$ ;  $I_D = -25 \text{ A}$
- Typ  $Q_{g(\text{tot})} = 17 \text{ nC}$  at  $V_{GS} = -10 \text{ V}$ ;  $I_D = -25 \text{ A}$
- UIS Capability
- Qualified to AEC Q101
- These Devices are Pb-Free and are RoHS Compliant

### Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electrical Power Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12 V Systems

### ABSOLUTE MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain to Source Voltage	$V_{DSS}$	-40	V
Gate to Source Voltage	$V_{GS}$	$\pm 16$	V
Drain Current – Continuous ( $V_{GS} = -10 \text{ V}$ ) ( $T_C = 25^\circ\text{C}$ ) (Note 1)	$I_D$	-25	A
Pulsed Drain Current ( $T_C = 25^\circ\text{C}$ )	$I_D$	See Figure 4	A
Single Pulse Avalanche Energy (Note 2)	$E_{AS}$	25	mJ
Power Dissipation	$P_D$	48.4	W
Derate above 25°C	$P_D$	0.32	W/°C
Operating and Storage Temperature Range	$T_J, T_{STG}$	-55 to +175	°C
Thermal Resistance (Junction to Case)	$R_{\theta JC}$	3.1	°C/W
Maximum Thermal Resistance (Junction to Ambient) (Note 3)	$R_{\theta JA}$	52	°C/W

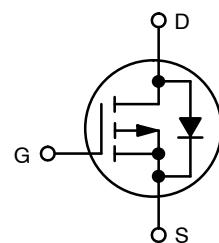
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by wirebond configuration
2. Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.08 \text{ mH}$ ,  $I_{AS} = -25 \text{ A}$ ,  $V_{DD} = -40 \text{ V}$  during inductor charging and  $V_{DD} = 0 \text{ V}$  during time in avalanche
3.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in<sup>2</sup> pad of 2 oz copper.



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### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDD9511L-F085

## PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FDD9511L-F085	FDD9511L	D-PAK (TO-252)	13"	12 mm	2500 Units

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$\text{BV}_{\text{DSS}}$	Drain to Source Breakdown Voltage	$V_{\text{GS}} = 0 \text{ V}$ , $I_D = -250 \mu\text{A}$	-40	-	-	V
$\text{I}_{\text{DSS}}$	Drain to Source Leakage Current	$V_{\text{DS}} = -40 \text{ V}$ , $V_{\text{GS}} = 0 \text{ V}$	-	-	-1	$\mu\text{A}$
		$T_J = 175^\circ\text{C}$ (Note 4)	-	-	-1	mA
$\text{I}_{\text{GSS}}$	Gate to Source Leakage Current	$V_{\text{GS}} = \pm 16 \text{ V}$	-	-	$\pm 100$	nA

### ON CHARACTERISTICS

$V_{\text{GS(th)}}$	Gate to Source Threshold Voltage	$V_{\text{GS}} = V_{\text{DS}}$ , $I_D = 250 \mu\text{A}$	-1	-1.8	-3	V
$R_{\text{DS(on)}}$	Drain to Source On-Resistance	$V_{\text{GS}} = -4.5 \text{ V}$ , $I_D = -12.5 \text{ A}$ , $T_J = 25^\circ\text{C}$	-	24	32	$\text{m}\Omega$
		$V_{\text{GS}} = -10 \text{ V}$ , $I_D = -25 \text{ A}$	-	17	21	$\text{m}\Omega$
		$T_J = 175^\circ\text{C}$ (Note 4)	-	28	36	$\text{m}\Omega$

### DYNAMIC CHARACTERISTICS

$C_{\text{iss}}$	Input Capacitance	$V_{\text{DS}} = -20 \text{ V}$ , $V_{\text{GS}} = 0 \text{ V}$ , $f = 100 \text{ KHz}$	-	1200	-	pF
$C_{\text{oss}}$	Output Capacitance		-	480	-	pF
$C_{\text{rss}}$	Reverse Transfer Capacitance		-	27	-	pF
$R_g$	Gate Resistance	$V_{\text{GS}} = -0.5 \text{ V}$ , $f = 1 \text{ MHz}$	-	38	-	$\Omega$
$Q_{\text{g(tot)}}$	Total Gate Charge	$V_{\text{DD}} = -20 \text{ V}$ , $I_D = -25 \text{ A}$	$V_{\text{GS}} = 0 \text{ V to } -10 \text{ V}$	-	17	nC
$Q_{\text{g}(-4.5)}$	Total Gate Charge		$V_{\text{GS}} = 0 \text{ V to } -4.5 \text{ V}$	-	8	nC
$Q_{\text{g(th)}}$	Threshold Gate Charge		$V_{\text{GS}} = 0 \text{ V to } -1 \text{ V}$	-	1	nC
$Q_{\text{gs}}$	Gate to Source Gate Charge	$V_{\text{DD}} = -20 \text{ V}$ , $I_D = -25 \text{ A}$	-	4	-	nC
$Q_{\text{gd}}$	Gate to Drain "Miller" Charge		-	2.5	-	nC

### SWITCHING CHARACTERISTICS

$t_{\text{on}}$	Turn-On Time	$V_{\text{DD}} = -20 \text{ V}$ , $I_D = -25 \text{ A}$ , $V_{\text{GS}} = -10 \text{ V}$ , $R_{\text{GEN}} = 6 \Omega$	-	-	45	ns
$t_{\text{d(on)}}$	Turn-On Delay Time		-	7	-	ns
$t_r$	Turn-On Rise Time		-	24	-	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time		-	120	-	ns
$t_f$	Turn-Off Fall Time		-	40	-	ns
$t_{\text{off}}$	Turn-Off Time		-	-	235	ns

### DRAIN-SOURCE DIODE CHARACTERISTICS

$V_{\text{SD}}$	Source to Drain Diode Voltage	$V_{\text{GS}} = 0 \text{ V}$ , $I_{\text{SD}} = -25 \text{ A}$	-	-0.95	-1.25	V
		$V_{\text{GS}} = 0 \text{ V}$ , $I_{\text{SD}} = -12.5 \text{ A}$	-	-0.9	-1.2	V
$T_{\text{rr}}$	Reverse Recovery Time	$I_F = -25 \text{ A}$ , $dI_{\text{SD}}/dt = 100 \text{ A}/\mu\text{s}$	-	36	54	ns
			-	22	33	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at  $T_J = 175^\circ\text{C}$ . Product is not tested to this condition in production

## TYPICAL CHARACTERISTICS

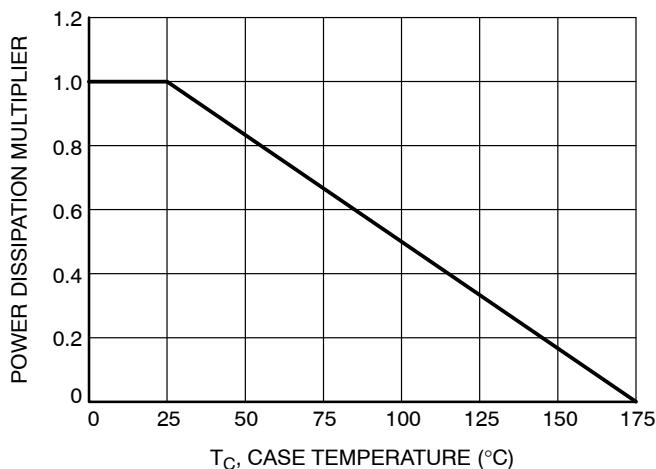


Figure 1. Normalized Power Dissipation vs.  
Case Temperature

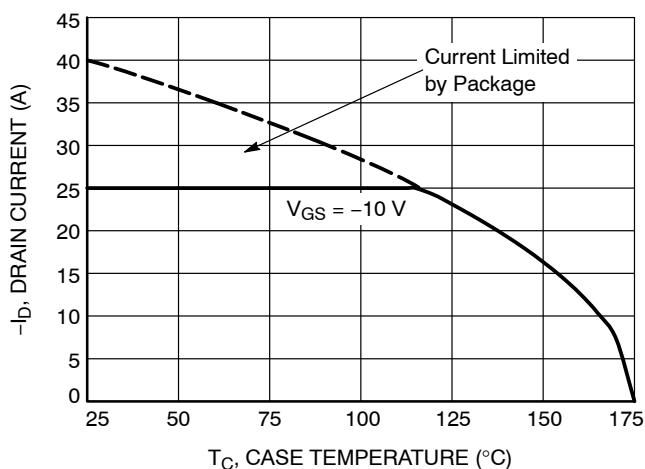


Figure 2. Maximum Continuous Drain Current  
vs. Case Temperature

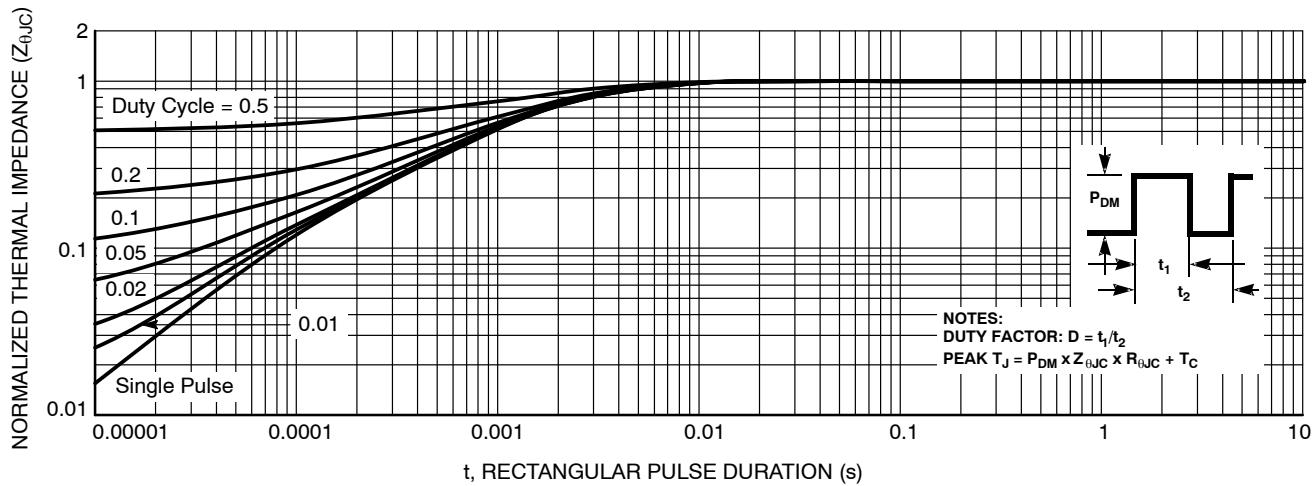


Figure 3. Normalized Maximum Transient Thermal Impedance

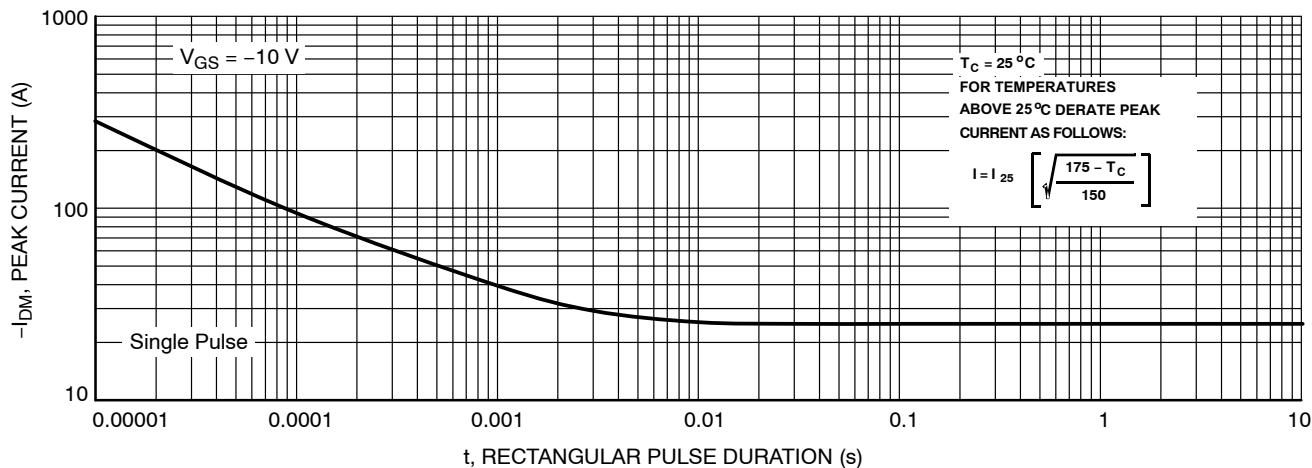
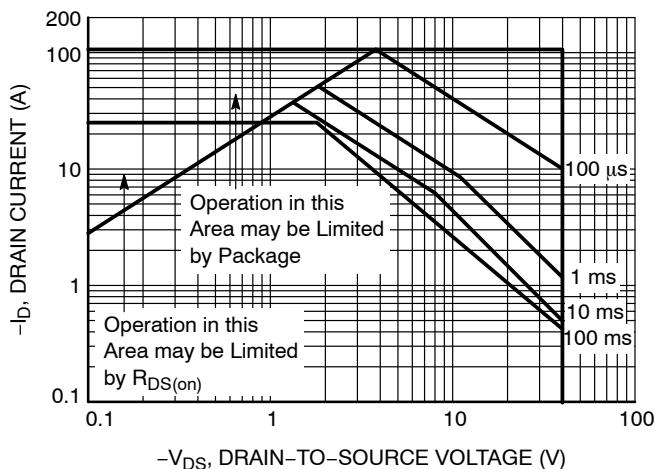
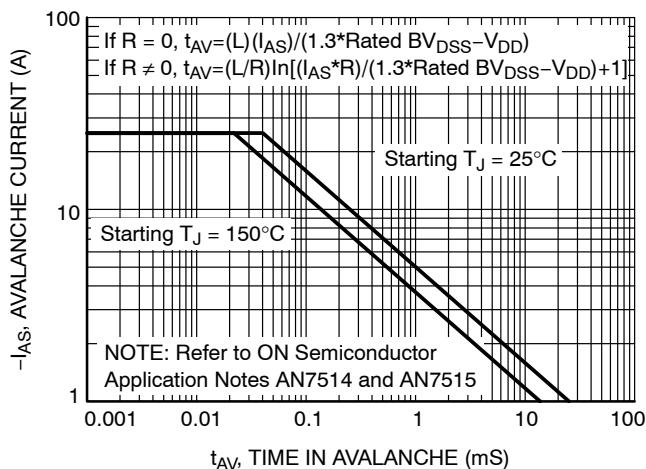
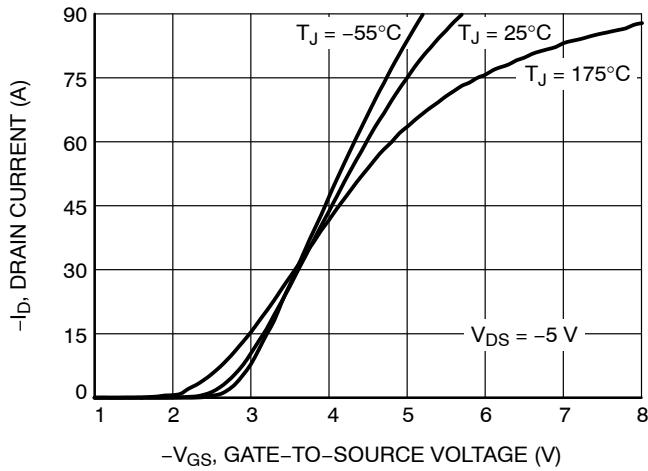
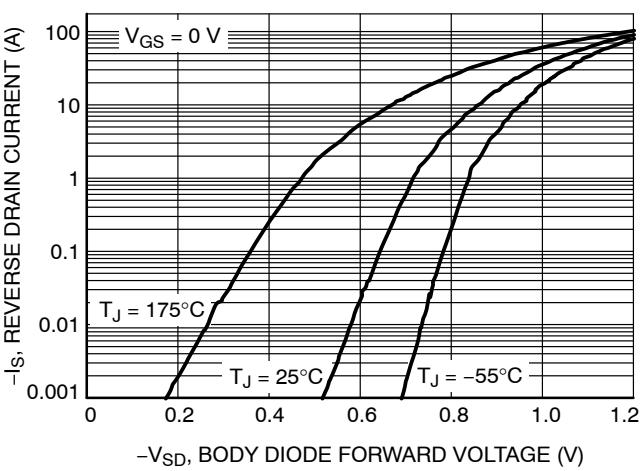
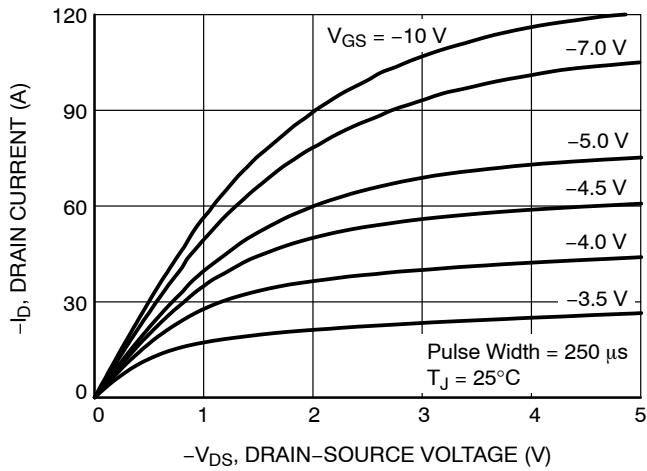
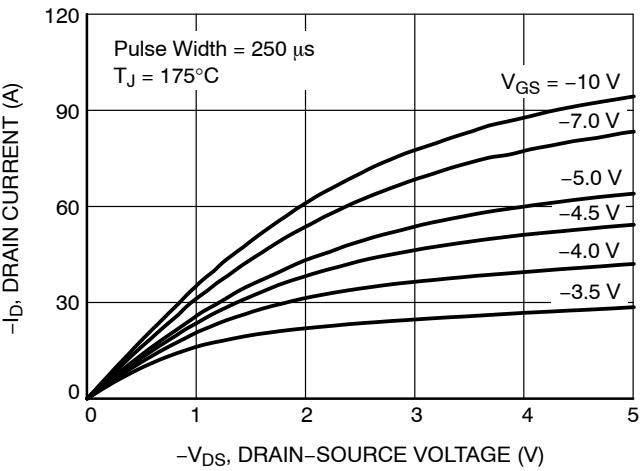


Figure 4. Peak Current Capability

**TYPICAL CHARACTERISTICS**

**Figure 5. Forward Bias Safe Operating Area**

**Figure 6. Unclamped Inductive Switching Capability**

**Figure 7. Transfer Characteristics**

**Figure 8. Forward Diode Characteristics**

**Figure 9. Saturation Characteristics**

**Figure 10. Saturation Characteristics**

TYPICAL CHARACTERISTICS

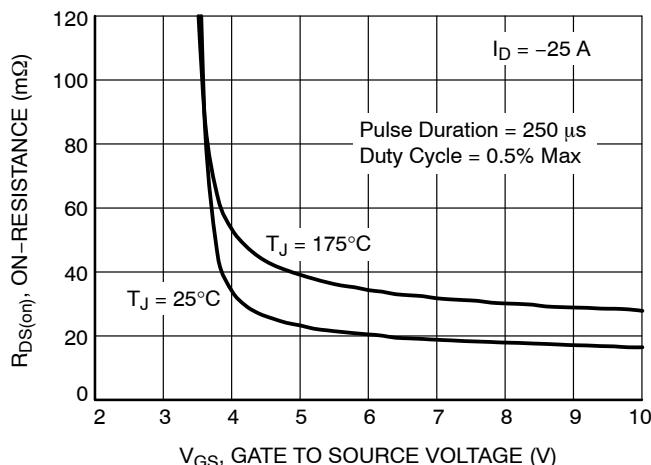


Figure 11.  $R_{DS(on)}$  vs. Gate Voltage

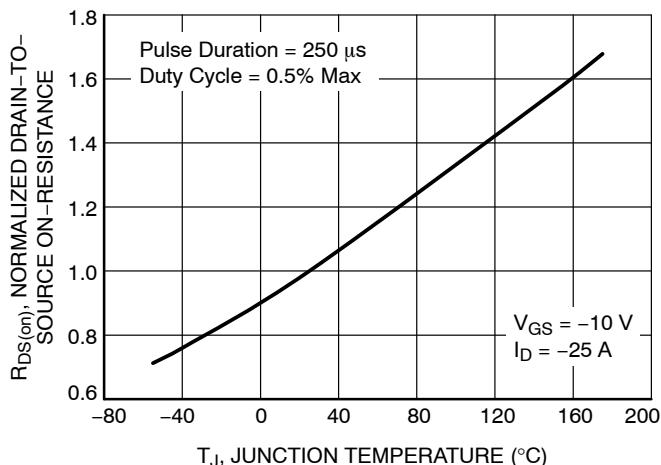


Figure 12. Normalized  $R_{DS(on)}$  vs. Junction Temperature

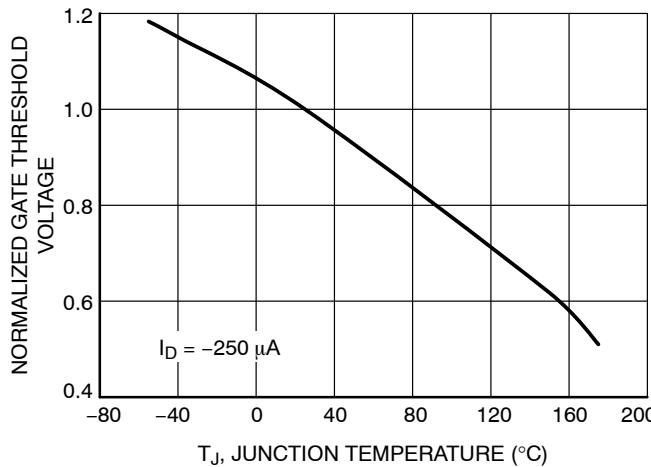


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

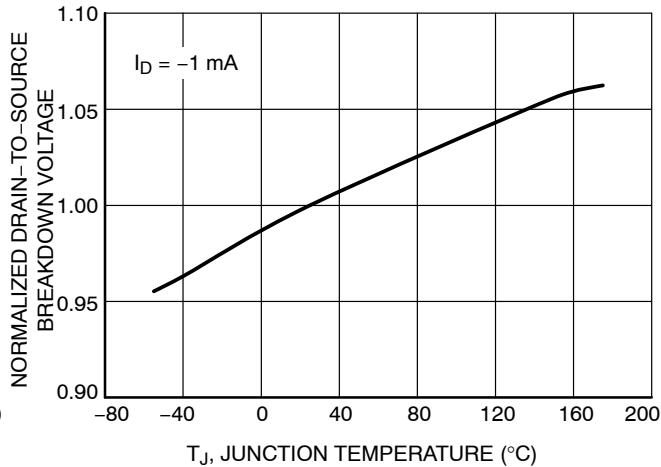


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

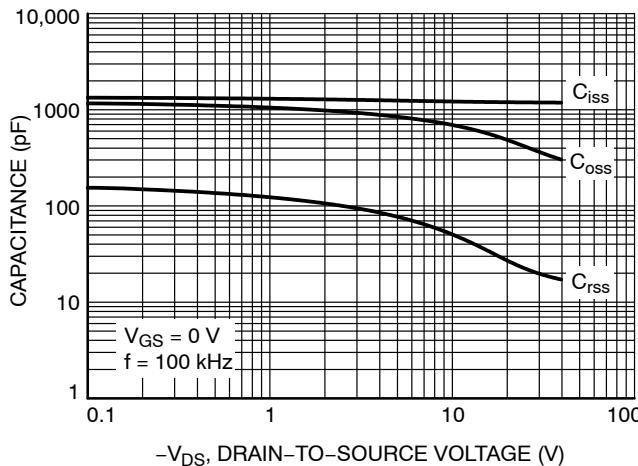


Figure 15. Capacitance vs. Drain-to-Source Voltage

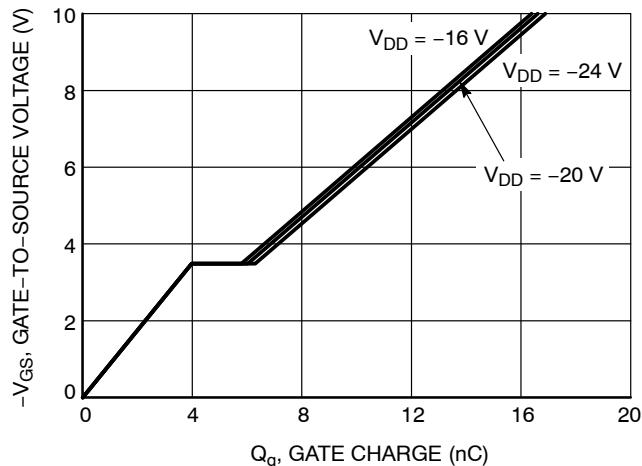
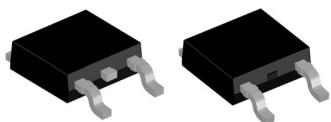
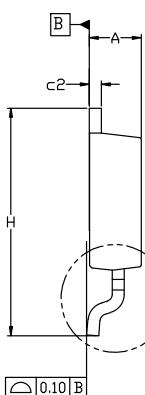
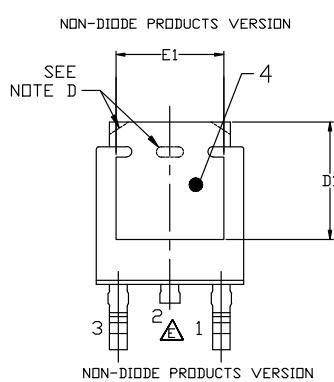
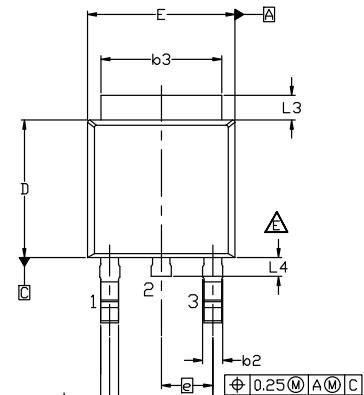


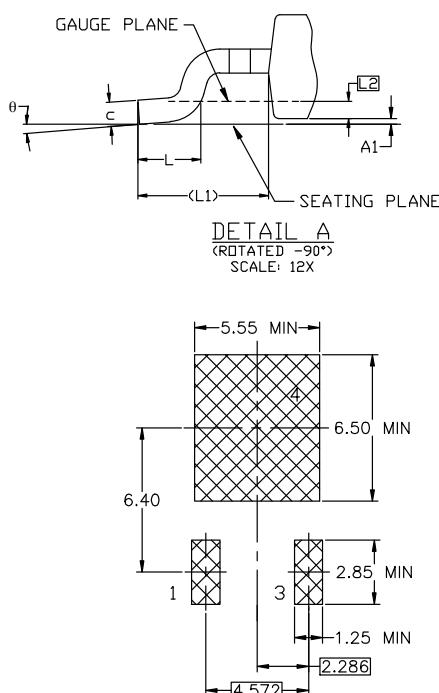
Figure 16. Gate Charge vs. Gate-to-Source Voltage


**DPAK3 6.10x6.54x2.29, 4.57P**  
CASE 369AS  
ISSUE B

DATE 20 DEC 2023



NOTES: UNLESS OTHERWISE SPECIFIED  
A) THIS PACKAGE CONFORMS TO JEDEC, TD-252,  
ISSUE F, VARIATION AA.  
B) ALL DIMENSIONS ARE IN MILLIMETERS.  
C) DIMENSIONING AND TOLERANCING PER  
ASME Y14.5M-2018.  
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED  
CORNERS OR EDGE PROTRUSION.  
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY  
STUB WITHOUT CENTER LEAD.  
F) DIMENSIONS ARE EXCLUSIVE OF BURRS,  
MOLD FLASH AND TIE BAR EXTRUSIONS.  
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD  
TD228P991X239-3N.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	—	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	—	—
E	6.35	6.54	6.73
E1	4.32	—	—
e	2.286	BSC	
e1	4.572	BSC	
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90	REF	
L2	0.51	BSC	
L3	0.89	1.08	1.27
L4	—	—	1.02
θ	0°	—	10°

## LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR  
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PLEASE DOWNLOAD THE ON SEMICONDUCTOR  
SOLDERING AND MOUNTING TECHNIQUES  
REFERENCE MANUAL, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

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