S-575D B Series

125°C OPERATION, HIGH-WITHSTAND VOLTAGE, HIGH-SPEED, OMNIPOLAR DETECTION TYPE HALL EFFECT SWITCH IC

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Rev.1.2_00

This IC, developed by CMOS technology, is a high-accuracy Hall effect switch IC that operates with high temperature and high-withstand voltage.
The output voltage level changes when this IC detects the intensity level of magnetic flux density. Using this IC with a magnet makes it possible to detect the open / close in various devices.

ABLIC Inc. offers a "magnetic simulation service" that provides the ideal combination of magnets and our Hall effect ICs for customer systems. Our magnetic simulation service will reduce prototype production, development period and development costs. In addition, it will contribute to optimization of parts to realize high cost performance.
For more information regarding our magnetic simulation service, contact our sales representatives.

■ Features

- Uses a thin (t0.80 mm max.) TSOT-23-3S or ultra-thin (t0.50 mm max.) HSNT-6(2025) package, contributing to the enhancement of the designs of devices
- Contributes to accurate mechanism operation with high-accuracy magnetic characteristics (Refer to "**■ Magnetic Characteristics**" for details.)
- Contributes to device safe design with a built-in output current limit circuit

■ Specifications

- Pole detection: Omnipolar detection
- Output logic*1: Active "L"
  Active "H"
- Output form*1: Nch open-drain output
  Nch driver + built-in pull-up resistor (1.2 kΩ typ.)
- Magnetic sensitivity*1: B_{OP} = 3.0 mT typ.
  B_{OP} = 6.0 mT typ.
  B_{OP} = 10.0 mT typ.
  B_{OP} = 15.0 mT typ.
- Chopping frequency: f_C = 500 kHz typ.
- Output delay time: t_D = 16.0 µs typ.
- Power supply voltage range*2: V_{DD} = 2.7 V to 26.0 V
- Built-in regulator
- Built-in output current limit circuit
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free

■ Applications

- Home appliance
- Housing equipment
- Industrial equipment

■ Packages

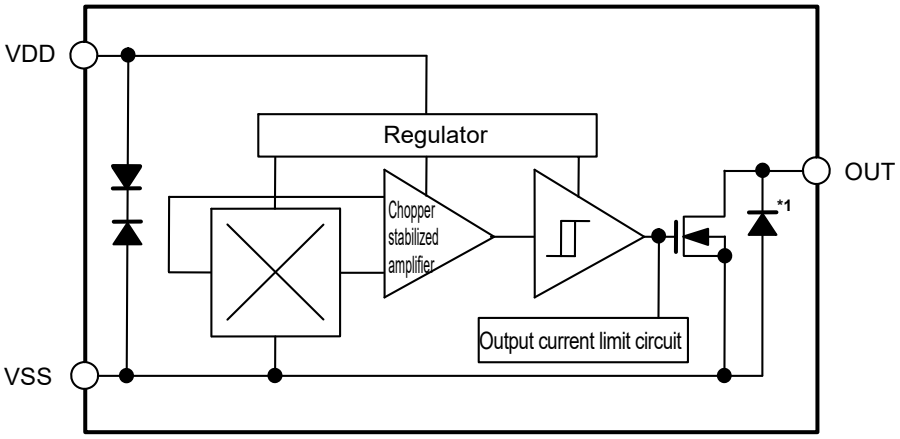
- TSOT-23-3S
- HSNT-6(2025)

***1.** The option can be selected.
***2.** V_{DD} = 2.7 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (1.2 kΩ typ.)

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■ Block Diagrams

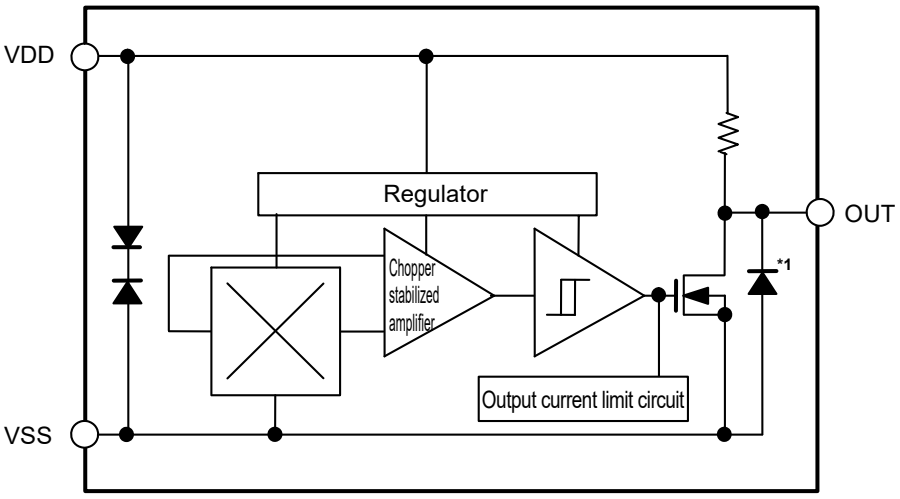
1. Nch open-drain output product



***1.** Parasitic diode

Figure 1

2. Nch driver + built-in pull-up resistor product



***1.** Parasitic diode

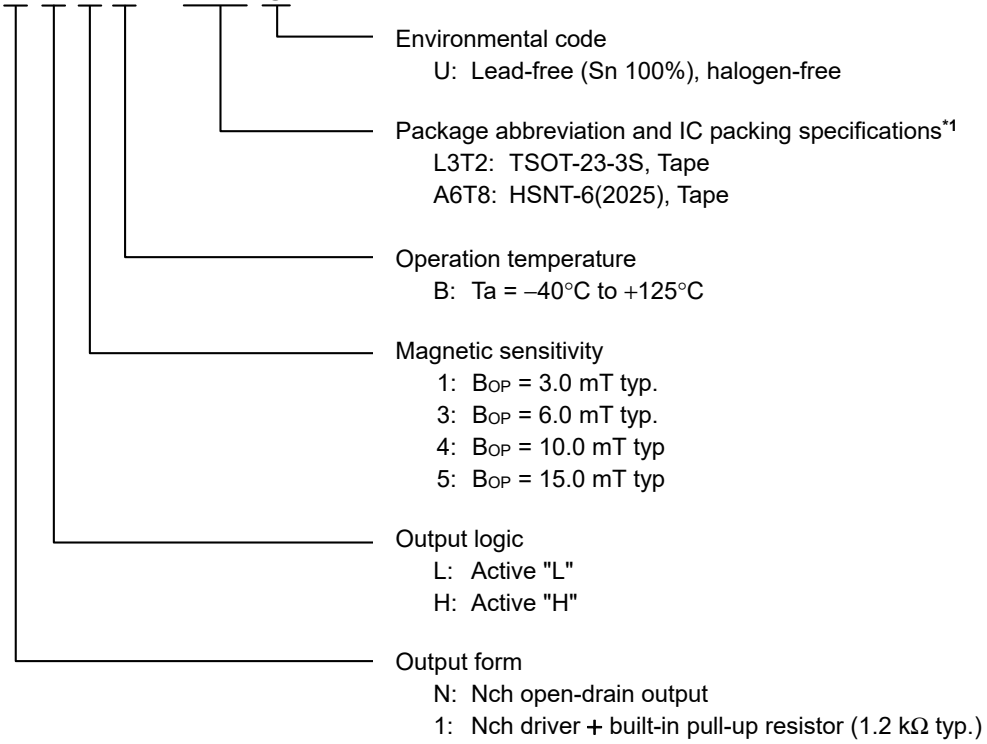
Figure 2

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■ Product Name Structure

1. Product name

S-575D x x x B - xxxx U



***1.** Refer to the tape drawing.

2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land	Stencil Opening
TSOT-23-3S	MP003-E-P-SD	MP003-E-C-SD	MP003-E-R-SD	–	–
HSNT-6(2025)	PJ006-B-P-SD	PJ006-B-C-SD	PJ006-B-R-SD	PJ006-B-LM-SD	PJ006-B-LM-SD

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3. Product name list

3. 1 TSOT-23-3S

Table 2

Product Name	Output Form	Power Supply Voltage Range	Output Logic	Magnetic Sensitivity (B_{OP})
S-575DNL1B-L3T2U	Nch open-drain output	V_{DD} = 2.7 V to 26.0 V	Active "L"	3.0 mT typ.
S-575DNL3B-L3T2U	Nch open-drain output	V_{DD} = 2.7 V to 26.0 V	Active "L"	6.0 mT typ.
S-575DNL5B-L3T2U	Nch open-drain output	V_{DD} = 2.7 V to 26.0 V	Active "L"	15.0 mT typ.

Remark Please contact our sales representatives for products other than the above.

3. 2 HSNT-6(2025)

Table 3

Product Name	Output Form	Power Supply Voltage Range	Output Logic	Magnetic Sensitivity (B_{OP})
S-575DNL1B-A6T8U	Nch open-drain output	V_{DD} = 2.7 V to 26.0 V	Active "L"	3.0 mT typ.
S-575DNL3B-A6T8U	Nch open-drain output	V_{DD} = 2.7 V to 26.0 V	Active "L"	6.0 mT typ.
S-575DNL5B-A6T8U	Nch open-drain output	V_{DD} = 2.7 V to 26.0 V	Active "L"	15.0 mT typ.

Remark Please contact our sales representatives for products other than the above.

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■ Pin Configurations

1. TSOT-23-3S

Top view

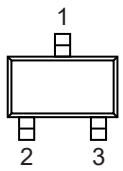


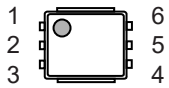
Figure 3

Table 4

Pin No.	Symbol	Description
1	VSS	GND pin
2	VDD	Power supply pin
3	OUT	Output pin

2. HSNT-6(2025)

Top view



Bottom view

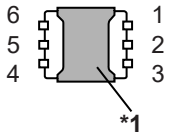


Figure 4

Table 5

Pin No.	Symbol	Description
1	VDD	Power supply pin
2	NC*2	No connection
3	OUT	Output pin
4	NC*2	No connection
5	VSS	GND pin
6	NC*2	No connection

***1.** Connect the heatsink of backside at shadowed area to the board, and set electric potential open or GND. However, do not use it as the function of electrode.

***2.** The NC pin is electrically open.
The NC pin can be connected to the VDD pin or the VSS pin.

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■ Absolute Maximum Ratings

Table 6

Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage	Nch open-drain output product	V_{DD}	V_{SS} – 0.3 to V_{SS} + 28.0	V
	Nch driver + built-in pull-up resistor (1.2 kΩ typ.) product		V_{SS} – 0.3 to V_{SS} + 9.0	V
Power supply current		I_{DD}	±10	mA
Output current		I_{OUT}	±10	mA
Output voltage	Nch open-drain output product	V_{OUT}	V_{SS} – 0.3 to V_{SS} + 28.0	V
	Nch driver + built-in pull-up resistor (1.2 kΩ typ.) product		V_{SS} – 0.3 to V_{DD} + 0.3	V
Operation ambient temperature		T_{opr}	–40 to +125	°C
Storage temperature		T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 7

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	TSOT-23-3S	Board A	–	225	–	°C/W
			Board B	–	190	–	°C/W
			Board C	–	–	–	°C/W
			Board D	–	–	–	°C/W
			Board E	–	–	–	°C/W
		HSNT-6(2025)	Board A	–	180	–	°C/W
			Board B	–	128	–	°C/W
			Board C	–	43	–	°C/W
			Board D	–	44	–	°C/W
			Board E	–	36	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Power Dissipation**" and "**Test Board**" for details.

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■ Electrical Characteristics

1. Nch open-drain output product

Table 8

(Ta = +25°C, V_{DD} = 12.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–	2.7	12.0	26.0	V	–
Current consumption	I_{DD}	–	–	4.0	4.5	mA	1
Low level output voltage	V_{OL}	I_{OUT} = 5 mA, V_{OUT} = "L"	–	–	0.4	V	2
Leakage current	I_{LEAK}	V_{OUT} = "H"	–	–	1.0	µA	3
Output limit current	I_{OM}	V_{OUT} = 12.0 V	11	–	35	mA	3
Output delay time*1	t_D	–	–	16	32	µs	–
Chopping frequency*1	f_C	–	250	500	–	kHz	–
Start up time*1	t_{PON}	–	–	25	40	µs	4
Output rise time*1	t_R	C = 20 pF, R = 820 Ω	–	–	1.0	µs	5
Output fall time*1	t_F	C = 20 pF, R = 820 Ω	–	–	1.0	µs	5

***1.** This item is guaranteed by design.

2. Nch driver + built-in pull-up resistor (1.2 kΩ typ.) product

Table 9

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	–	2.7	5.0	5.5	V	–
Current consumption	I_{DD}	V_{OUT} = "H"	–	4.0	4.5	mA	1
Low level output voltage	V_{OL}	I_{OUT} = 0 mA, V_{OUT} = "L"	–	–	0.4	V	2
High level output voltage	V_{OH}	I_{OUT} = 0 mA, V_{OUT} = "H"	$V_{DD} \times 0.9$	–	–	V	2
Output limit current	I_{OM}	V_{DD} = V_{OUT} = 5.0 V	11	–	35	mA	3
Output delay time*1	t_D	–	–	16	32	µs	–
Chopping frequency*1	f_C	–	250	500	–	kHz	–
Start up time*1	t_{PON}	–	–	25	40	µs	4
Output rise time*1	t_R	C = 20 pF	–	–	1.0	µs	5
Output fall time*1	t_F	C = 20 pF	–	–	1.0	µs	5
Pull-up resistor	R_L	–	0.9	1.2	1.5	kΩ	–

***1.** This item is guaranteed by design.

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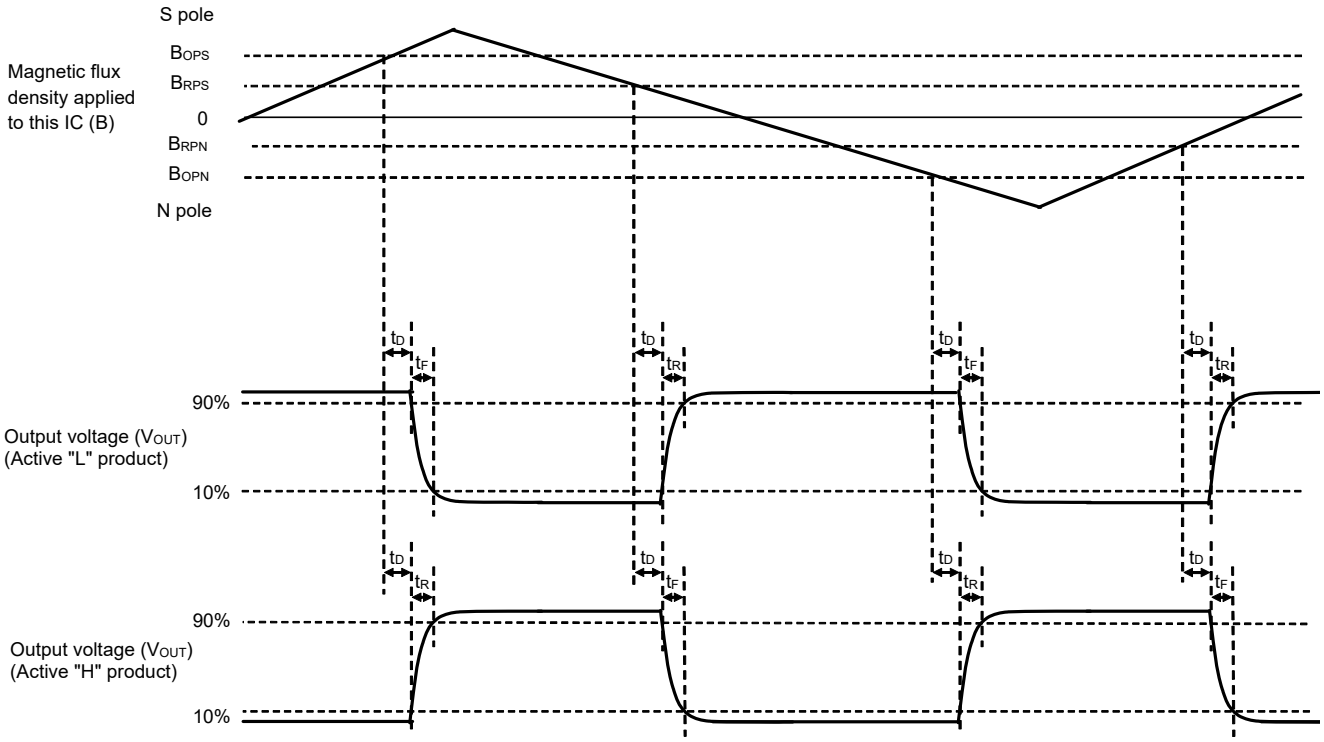


Figure 5 Operation Timing

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■ Magnetic Characteristics

1. TSOT-23-3S

1. 1 Product with B_{OP} = 3.0 mT typ.

Table 10

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	2.0	3.0	4.3	mT	4
	N pole	B_{OPN}	–	–4.3	–3.0	–2.0	mT	4
Release point*2	S pole	B_{RPS}	–	1.2	2.2	3.2	mT	4
	N pole	B_{RPN}	–	–3.2	–2.2	–1.2	mT	4
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	0.8	–	mT	4
	N pole	B_{HYSN}	$B_{HYSN} = \|B_{OPN} - B_{RPN}\|$	–	0.8	–	mT	4

1. 2 Product with B_{OP} = 6.0 mT typ.

Table 11

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	4.0	6.0	8.0	mT	4
	N pole	B_{OPN}	–	–8.0	–6.0	–4.0	mT	4
Release point*2	S pole	B_{RPS}	–	3.0	4.5	6.0	mT	4
	N pole	B_{RPN}	–	–6.0	–4.5	–3.0	mT	4
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	1.5	–	mT	4
	N pole	B_{HYSN}	$B_{HYSN} = \|B_{OPN} - B_{RPN}\|$	–	1.5	–	mT	4

1. 3 Product with B_{OP} = 10.0 mT typ.

Table 12

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	7.2	10.0	12.6	mT	4
	N pole	B_{OPN}	–	–12.6	–10.0	–7.2	mT	4
Release point*2	S pole	B_{RPS}	–	5.2	7.5	9.8	mT	4
	N pole	B_{RPN}	–	–9.8	–7.5	–5.2	mT	4
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	2.5	–	mT	4
	N pole	B_{HYSN}	$B_{HYSN} = \|B_{OPN} - B_{RPN}\|$	–	2.5	–	mT	4

1. 4 Product with B_{OP} = 15.0 mT typ.

Table 13

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	11.2	15.0	19.2	mT	4
	N pole	B_{OPN}	–	–19.2	–15.0	–11.2	mT	4
Release point*2	S pole	B_{RPS}	–	8.4	12.0	15.0	mT	4
	N pole	B_{RPN}	–	–15.0	–12.0	–8.4	mT	4
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	3.0	–	mT	4
	N pole	B_{HYSN}	$B_{HYSN} = \|B_{OPN} - B_{RPN}\|$	–	3.0	–	mT	4

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2. HSNT-6(2025)

2. 1 Product with B_{OP} = 3.0 mT typ.

Table 14

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	1.7	3.0	4.7	mT	4
	N pole	B_{OPN}	–	–4.7	–3.0	–1.7	mT	4
Release point*2	S pole	B_{RPS}	–	0.7	2.2	3.6	mT	4
	N pole	B_{RPN}	–	–3.6	–2.2	–0.7	mT	4
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	0.8	–	mT	4
	N pole	B_{HYSN}	$B_{HYSN} = \lvert B_{OPN} - B_{RPN} \rvert$	–	0.8	–	mT	4

2. 2 Product with B_{OP} = 6.0 mT typ.

Table 15

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	3.7	6.0	8.3	mT	4
	N pole	B_{OPN}	–	–8.3	–6.0	–3.7	mT	4
Release point*2	S pole	B_{RPS}	–	2.5	4.5	6.5	mT	4
	N pole	B_{RPN}	–	–6.5	–4.5	–2.5	mT	4
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	1.5	–	mT	4
	N pole	B_{HYSN}	$B_{HYSN} = \lvert B_{OPN} - B_{RPN} \rvert$	–	1.5	–	mT	4

2. 3 Product with B_{OP} = 10.0 mT typ.

Table 16

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	7.4	10.0	13.1	mT	4
	N pole	B_{OPN}	–	–13.1	–10.0	–7.4	mT	4
Release point*2	S pole	B_{RPS}	–	5.1	7.5	10.1	mT	4
	N pole	B_{RPN}	–	–10.1	–7.5	–5.1	mT	4
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	2.5	–	mT	4
	N pole	B_{HYSN}	$B_{HYSN} = \lvert B_{OPN} - B_{RPN} \rvert$	–	2.5	–	mT	4

2. 4 Product with B_{OP} = 15.0 mT typ.

Table 17

(Ta = +25°C, V_{DD} = 5.0 V, V_{SS} = 0 V unless otherwise specified)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Operation point*1	S pole	B_{OPS}	–	10.6	15.0	19.9	mT	4
	N pole	B_{OPN}	–	–19.9	–15.0	–10.6	mT	4
Release point*2	S pole	B_{RPS}	–	8.1	12.0	15.8	mT	4
	N pole	B_{RPN}	–	–15.8	–12.0	–8.1	mT	4
Hysteresis width*3	S pole	B_{HYSS}	$B_{HYSS} = B_{OPS} - B_{RPS}$	–	3.0	–	mT	4
	N pole	B_{HYSN}	$B_{HYSN} = \lvert B_{OPN} - B_{RPN} \rvert$	–	3.0	–	mT	4

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***1.** B_{OPN}, B_{OPS}: Operation points
B_{OPN} and B_{OPS} are the values of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to this IC by the magnet (N pole or S pole) is increased (by moving the magnet closer).
Even when the magnetic flux density exceeds B_{OPN} or B_{OPS}, V_{OUT} retains the status.

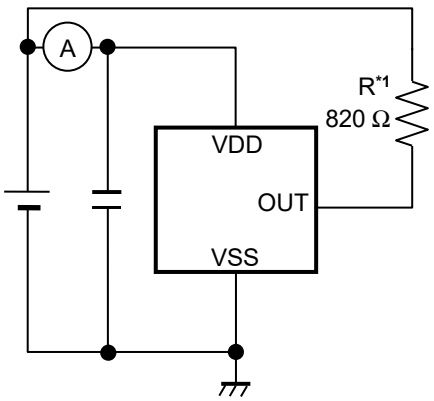
***2.** B_{RPN}, B_{RPS}: Release points
B_{RPN} and B_{RPS} are the values of magnetic flux density when the output voltage (V_{OUT}) changes after the magnetic flux density applied to this IC by the magnet (N pole or S pole) is decreased (the magnet is moved further away).
Even when the magnetic flux density falls below B_{RPN} or B_{RPS}, V_{OUT} retains the status.

***3.** B_{HYSN}, B_{HYSS}: Hysteresis widths
B_{HYSN} and B_{HYSS} are the difference between B_{OPN} and B_{RPN}, and B_{OPS} and B_{RPS}, respectively.

Remark The unit of magnetic density mT can be converted by using the formula 1 mT = 10 Gauss.

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■ Test Circuits



*1. Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

Figure 6 Test Circuit 1

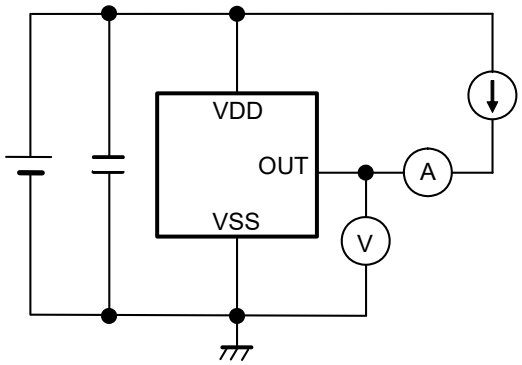


Figure 7 Test Circuit 2

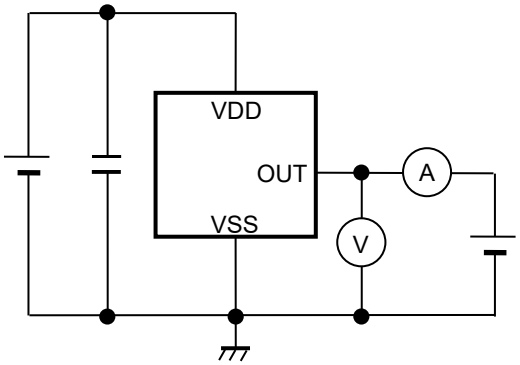
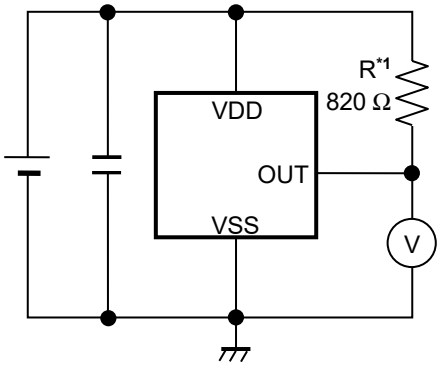
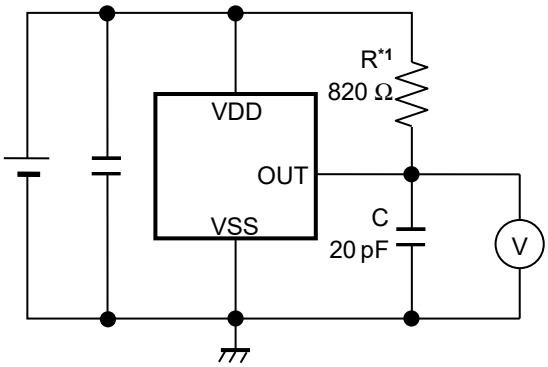


Figure 8 Test Circuit 3



*1. Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

Figure 9 Test Circuit 4

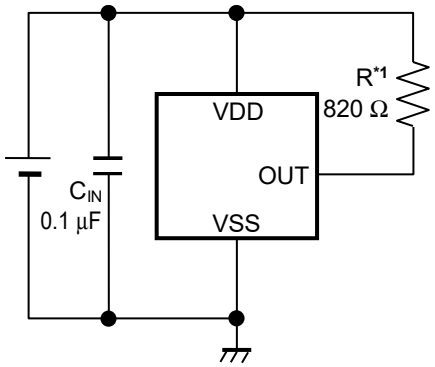


*1. Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

Figure 10 Test Circuit 5

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■ Standard Circuit



***1**. Resistor (R) is unnecessary for Nch driver + built-in pull-up resistor product.

Figure 11

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

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■ Operation

1. Direction of applied magnetic flux

This IC detects the magnetic flux density which is perpendicular to the package marking surface. A magnetic field is defined as positive when marking side of the package is the S pole, and negative when it is the N pole.
Figure 12 and **Figure 13** show polarity in a magnetic field and direction in which magnetic flux is being applied.

1. 1 TSOT-23-3S

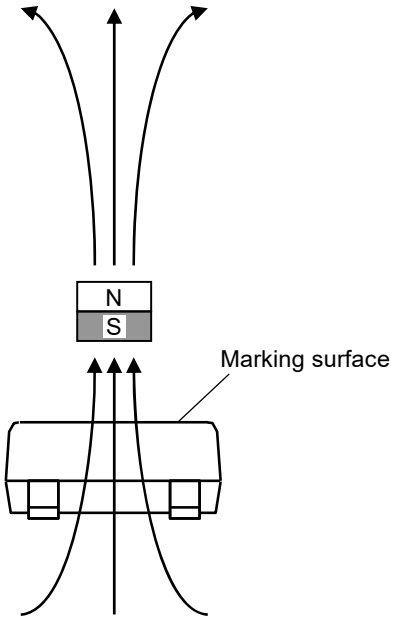


Figure 12

1. 2 HSNT-6(2025)

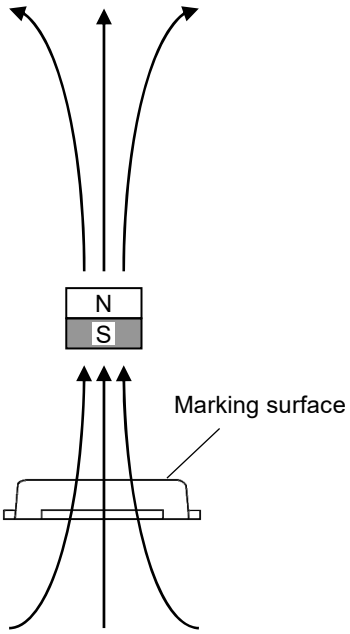


Figure 13

2. Position of Hall sensor

Figure 14 and **Figure 15** show the position of Hall sensor.
The center of this Hall sensor is located in the area indicated by a circle, which is in the center of a package as described below.
The following also shows the distance (typ. value) between the marking surface and the chip surface of a package.

2. 1 TSOT-23-3S

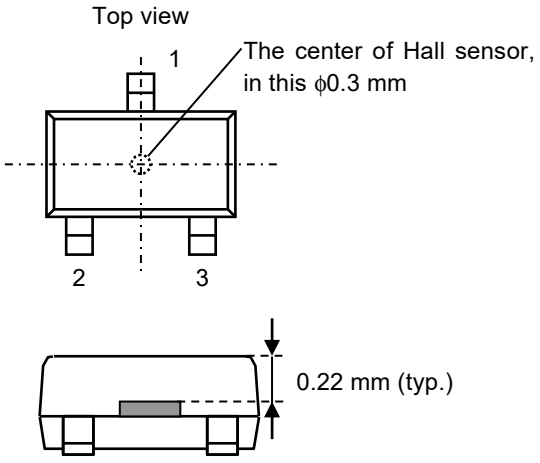


Figure 14

2. 2 HSNT-6(2025)

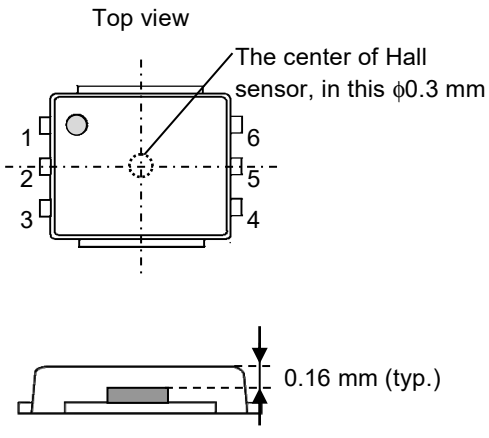


Figure 15

Downloaded from Arrow.com.

3. Basic operation

This IC changes the output voltage (V_{OUT}) according to the level of the magnetic flux density (N pole or S pole) applied by a magnet.

3. 1 Active "L" product

When the magnetic flux density perpendicular to the marking surface exceeds the operation point (B_{OPN} or B_{OPS}) after the S pole or N pole of a magnet is moved closer to the marking surface of this IC, V_{OUT} changes from "H" to "L". When the S pole or N pole of a magnet is moved further away from the marking surface of this IC and the magnetic flux density is lower than the release point (B_{RPN} or B_{RPS}), V_{OUT} changes from "L" to "H".
Figure 16 shows the relationship between the magnetic flux density and V_{OUT}.

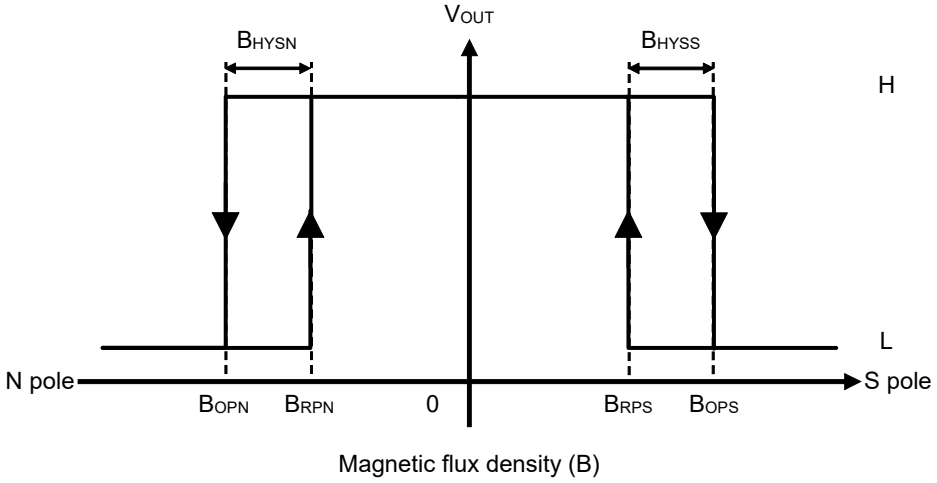


Figure 16

3. 2 Active "H" product

When the magnetic flux density perpendicular to the marking surface exceeds the operation point (B_{OPN} or B_{OPS}) after the S pole or N pole of a magnet is moved closer to the marking surface of this IC, V_{OUT} changes from "L" to "H". When the S pole or N pole of a magnet is moved further away from the marking surface of this IC and the magnetic flux density is lower than the release point (B_{RPN} or B_{RPS}), V_{OUT} changes from "H" to "L".
Figure 17 shows the relationship between the magnetic flux density and V_{OUT}.

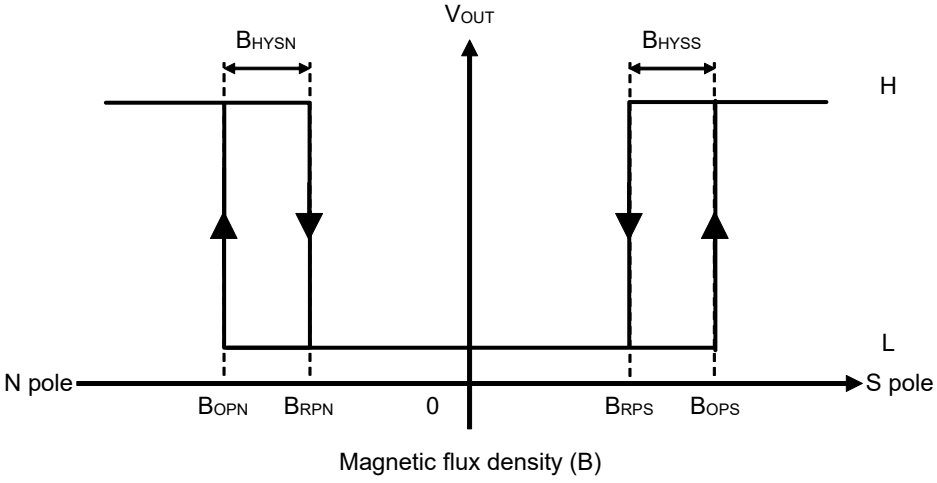


Figure 17

Downloaded from Arrow.com.

4. Power-on operation

The output voltage (V_{OUT}) of this IC immediately after power-on is "H". After the start up time (t_{PON}) is passed, the IC changes V_{OUT} according to the level of the magnetic flux density (N pole or S pole) applied by a magnet.

4. 1 Active "L" product

Figure 18 shows the timing chart at power-on for active "L" product.
The initial output voltage at rising of power supply voltage (V_{DD}) is "H".
In case of $B > B_{OPS}$ or $B < B_{OPN}$ at the time when t_{PON} is passed after rising of V_{DD}, V_{OUT} changes from "H" to "L".
In case of $B_{OPN} < B < B_{OPS}$ at the time when t_{PON} is passed after rising of V_{DD}, V_{OUT} retains "H".

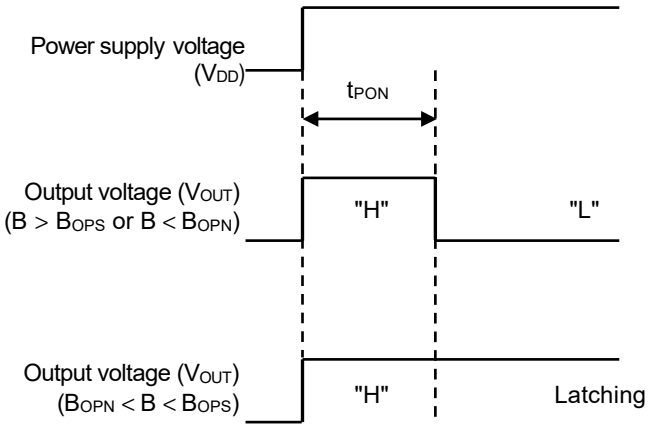


Figure 18

4. 2 Active "H" product

Figure 19 shows the timing chart at power-on for active "H" product.
The initial output voltage at rising of power supply voltage (V_{DD}) is "H".
In case of $B > B_{OPS}$ or $B < B_{OPN}$ at the time when t_{PON} is passed after rising of V_{DD}, V_{OUT} retains "H".
In case of $B_{OPN} < B < B_{OPS}$ at the time when t_{PON} is passed after rising of V_{DD}, V_{OUT} changes from "H" to "L".

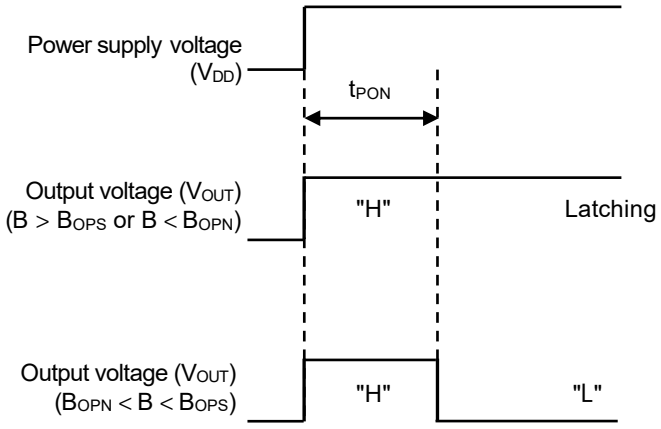


Figure 19

Downloaded from Arrow.com.

■ Precautions

- If the impedance of the power supply is high, the IC may malfunction due to a supply voltage drop caused by feed-through current. Take care with the pattern wiring to ensure that the impedance of the power supply is low.
- Note that the IC may malfunction if the power supply voltage rapidly changes. When the IC is used under the environment where the power supply voltage rapidly changes, it is recommended to judge the output voltage of the IC by reading it multiple times.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- Note that the output voltage may rarely change if the magnetic flux density between the operation point and the release point is applied to this IC continuously for a long time.
- Although this IC has a built-in output current limit circuit, it may suffer physical damage such as product deterioration under the environment where the absolute maximum ratings are exceeded.
- The application conditions for the power supply voltage, the pull-up voltage, and the pull-up resistor should not exceed the power dissipation.
- Large stress on this IC may affect the magnetic characteristics. Avoid large stress which is caused by the handling during or after mounting the IC on a board.
- Since the package heat radiation differs according to the conditions of the application, perform thorough evaluation with actual applications to confirm no problems occur.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

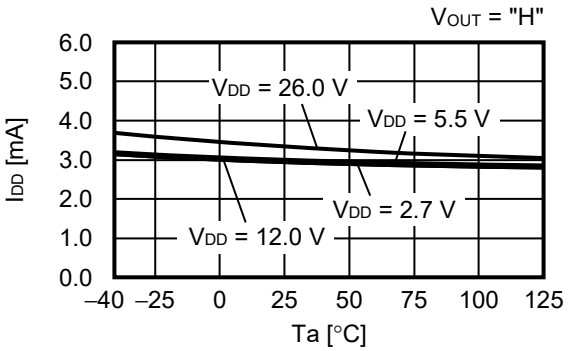
Downloaded from Arrow.com.

■ Characteristics (Typical Data)

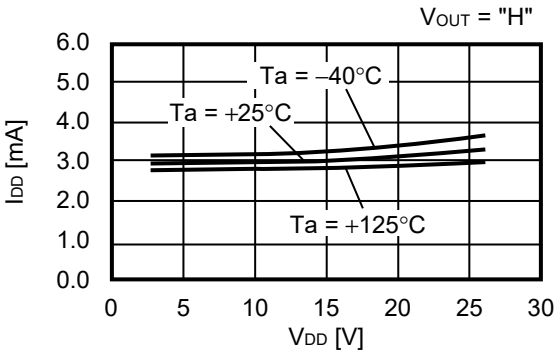
1. Electrical Characteristics

1. 1 S-575DxxxB

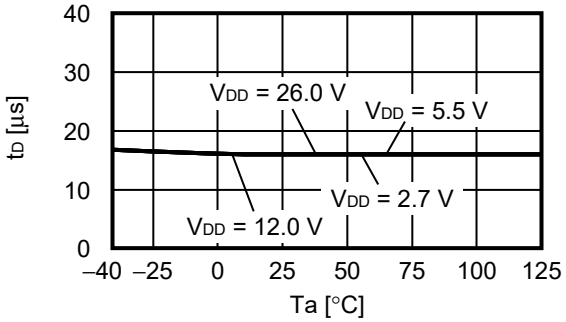
1. 1. 1 Current consumption (I_{DD}) vs. Temperature (Ta)



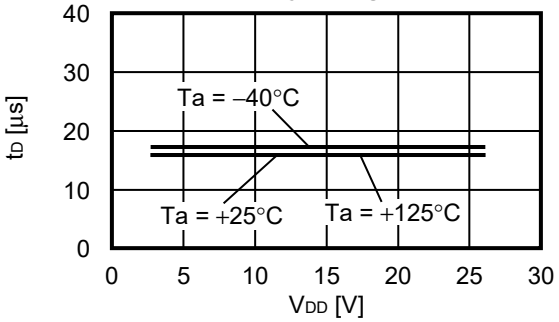
1. 1. 2 Current consumption (I_{DD}) vs. Power supply voltage (V_{DD})



1. 1. 3 Output delay time (t_D) vs. Temperature (Ta)



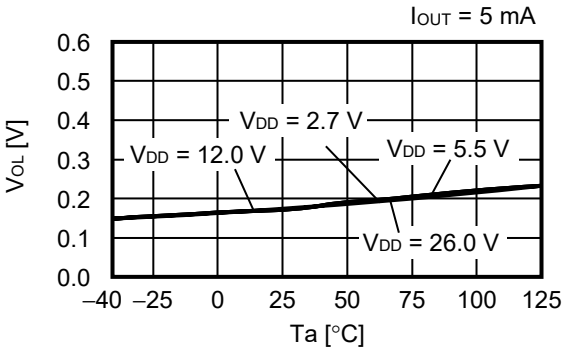
1. 1. 4 Output delay time (t_D) vs. Power supply voltage (V_{DD})



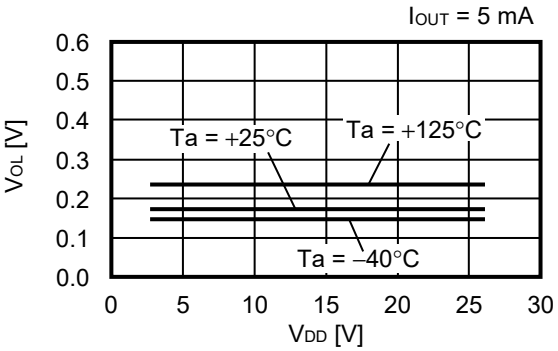
Caution **V_{DD} = 2.7 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (1.2 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.**

1. 2 S-575DNxxB

1. 2. 1 Low level output voltage (V_{OL}) vs. Temperature (Ta)



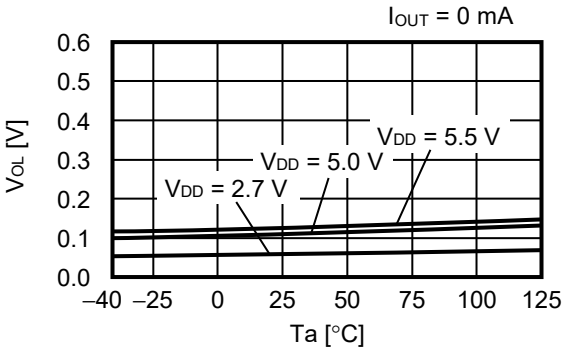
1. 2. 2 Low level output voltage (V_{OL}) vs. Power supply voltage (V_{DD})



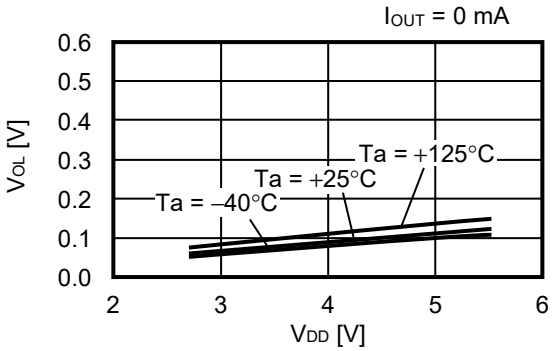
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1. 3 S-575D1xxB

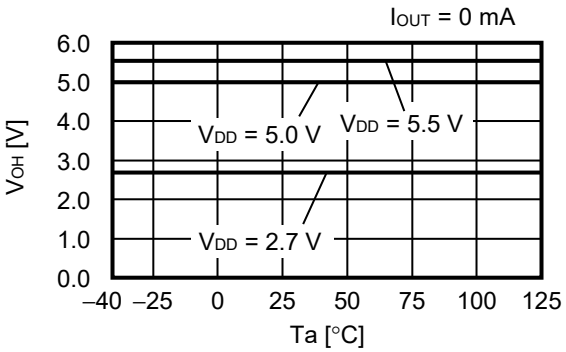
1. 3. 1 Low level output voltage (V_{OL}) vs. Temperature (Ta)



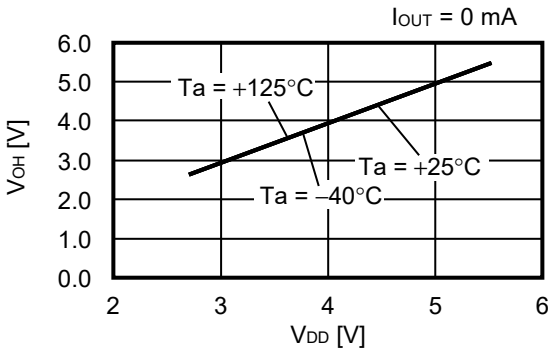
1. 3. 2 Low level output voltage (V_{OL}) vs. Power supply voltage (V_{DD})



1. 3. 3 High level output voltage (V_{OH}) vs. Temperature (Ta)



1. 3. 4 High level output voltage (V_{OH}) vs. Power supply voltage (V_{DD})

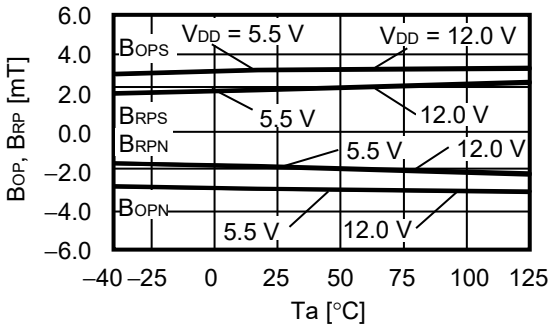


Downloaded from Arrow.com.

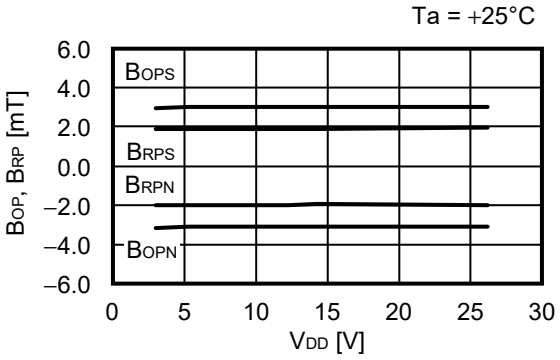
2. Magnetic Characteristics

2. 1 S-575Dxx1B-L3T2U

2. 1. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

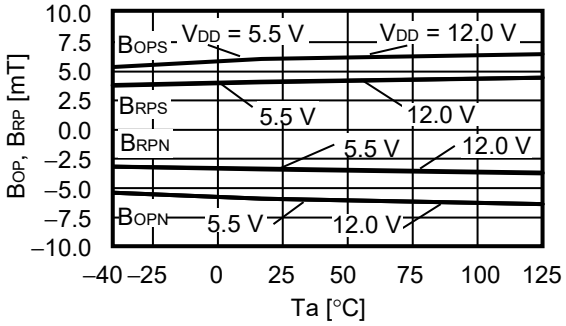


2. 1. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

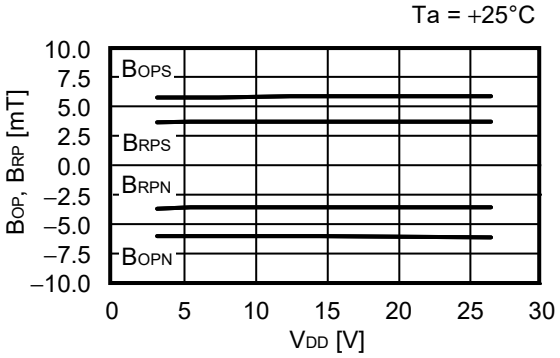


2. 2 S-575Dxx3B-L3T2U

2. 2. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



2. 2. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

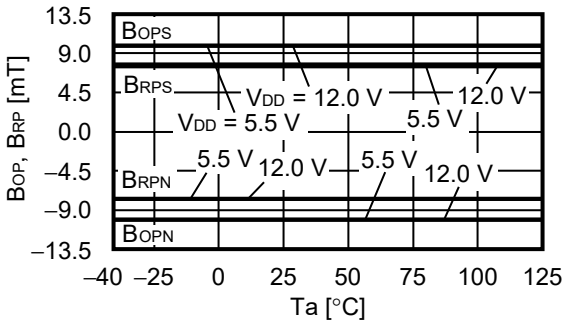


Caution **V_{DD} = 2.7 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (1.2 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.**

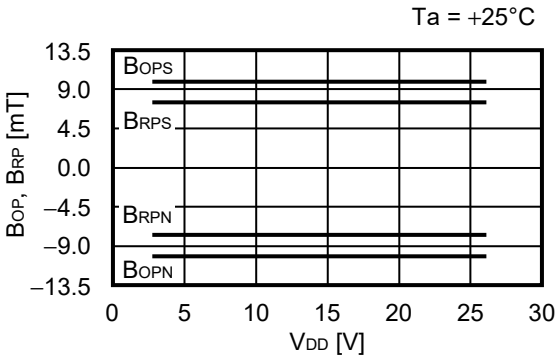
Downloaded from Arrow.com.

2. 3 S-575Dxx4B-L3T2U

2. 3. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

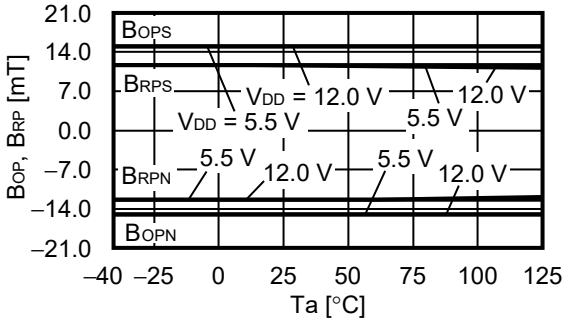


2. 3. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

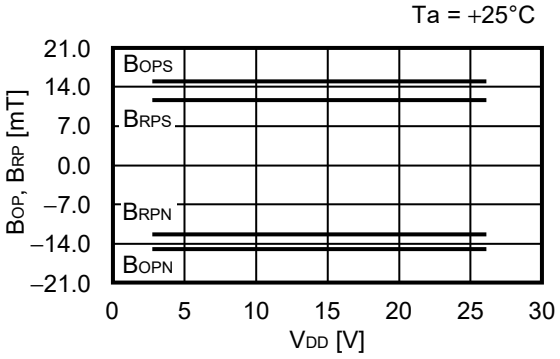


2. 4 S-575Dxx5B-L3T2U

2. 4. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



2. 4. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

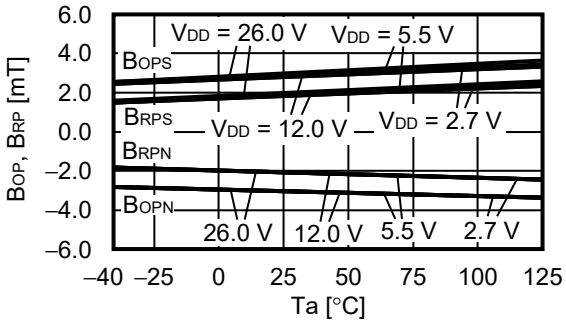


Caution **V_{DD} = 2.7 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (1.2 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.**

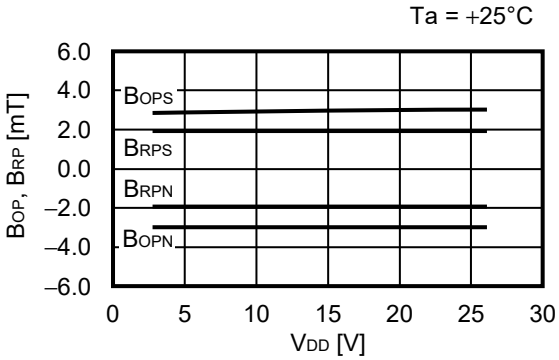
Downloaded from Arrow.com.

2. 5 S-575Dxx1B-A6T8U

2. 5. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

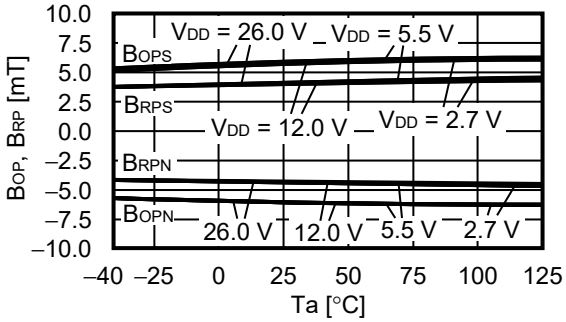


2. 5. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

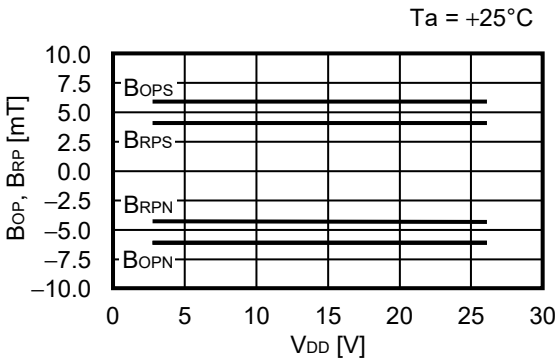


2. 6 S-575Dxx3B-A6T8U

2. 6. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



2. 6. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

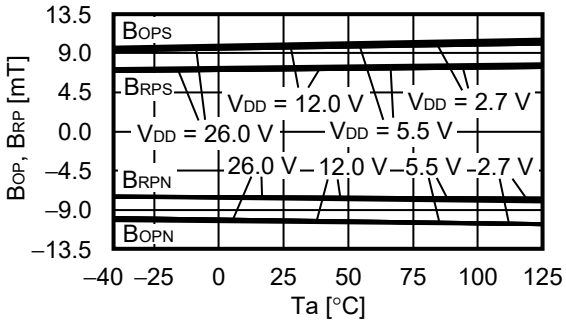


Caution **V_{DD} = 2.7 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (1.2 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.**

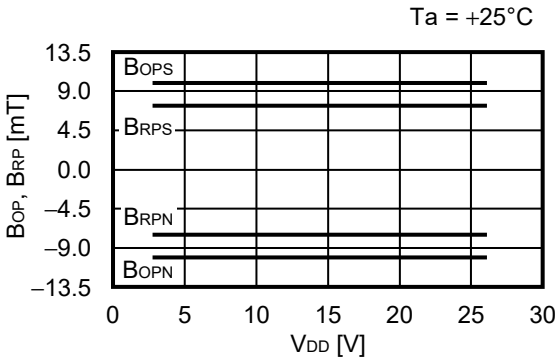
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2. 7 S-575Dxx4B-A6T8U

2. 7. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)

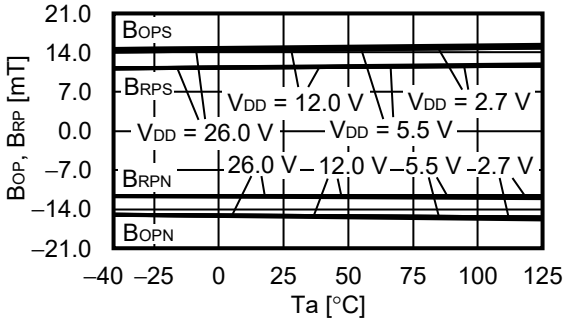


2. 7. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

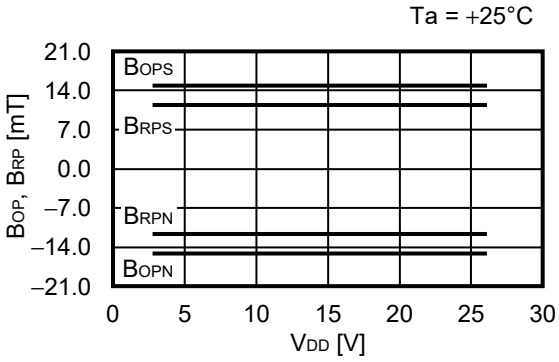


2. 8 S-575Dxx5B-A6T8U

2. 8. 1 Operation point, release point (B_{OP}, B_{RP}) vs. Temperature (Ta)



2. 8. 2 Operation point, release point (B_{OP}, B_{RP}) vs. Power supply voltage (V_{DD})

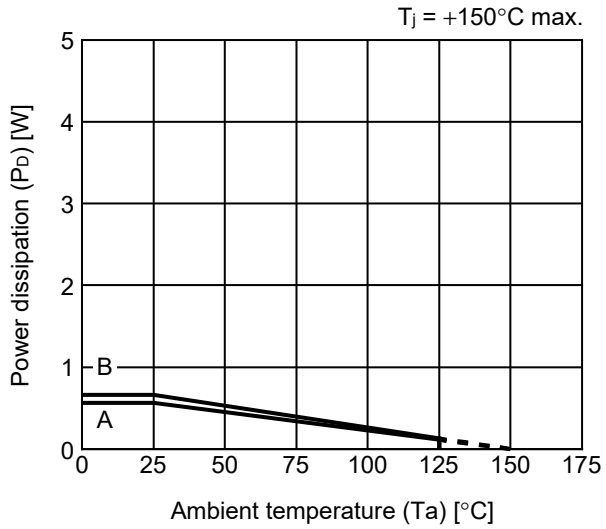


Caution **V_{DD} = 2.7 V to 5.5 V when output form is Nch driver + built-in pull-up resistor (1.2 kΩ typ.). Comply with power supply voltage range and do not exceed absolute maximum ratings.**

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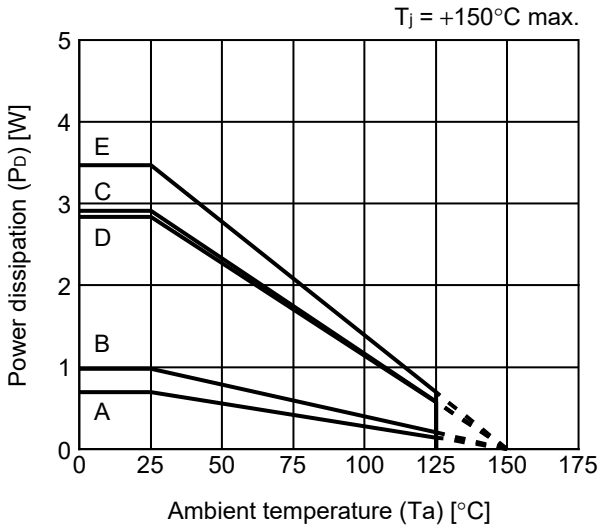
■ Power Dissipation

TSOT-23-3S



Board	Power Dissipation (P_D)
A	0.56 W
B	0.66 W
C	–
D	–
E	–

HSNT-6(2025)



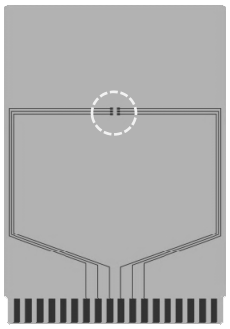
Board	Power Dissipation (P_D)
A	0.69 W
B	0.98 W
C	2.91 W
D	2.84 W
E	3.47 W

Downloaded from Arrow.com.

TSOT-23-3S Test Board

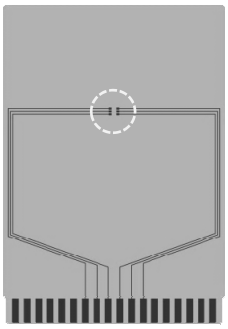
IC Mount Area

(1) Board A



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

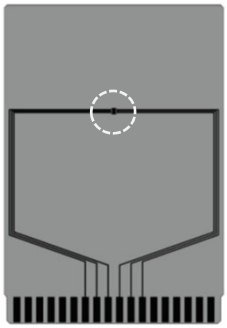
No. TSOT23x-A-Board-SD-1.0

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HSNT-6(2025) Test Board

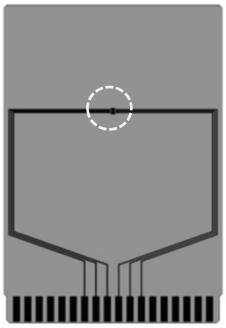
IC Mount Area

(1) Board A



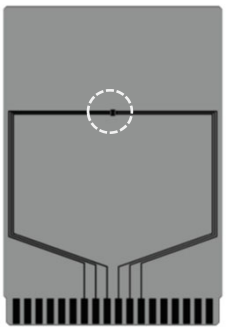
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm



enlarged view

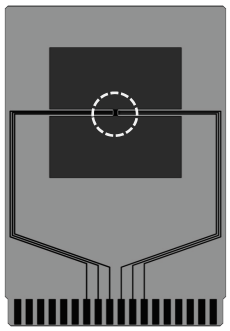
No. HSNT6-B-Board-SD-1.0

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HSNT-6(2025) Test Board

IC Mount Area

(4) Board D

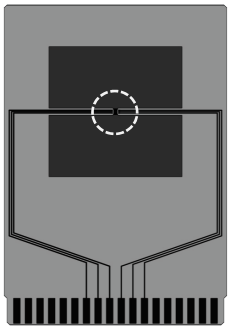




enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E



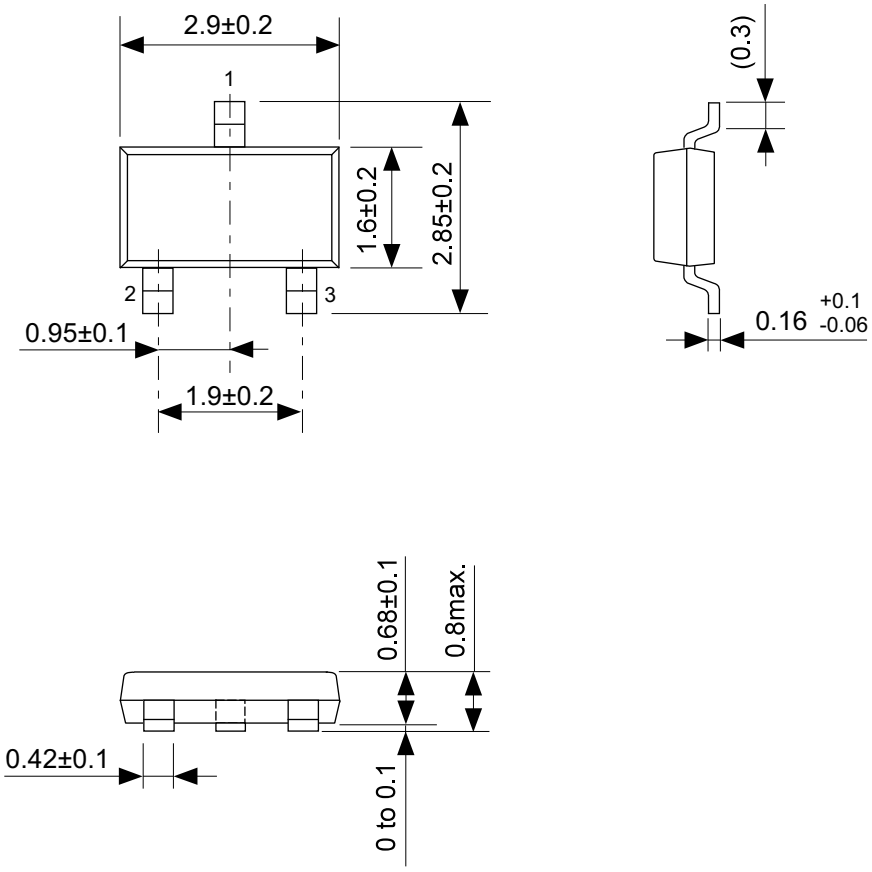


enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HSNT6-B-Board-SD-1.0

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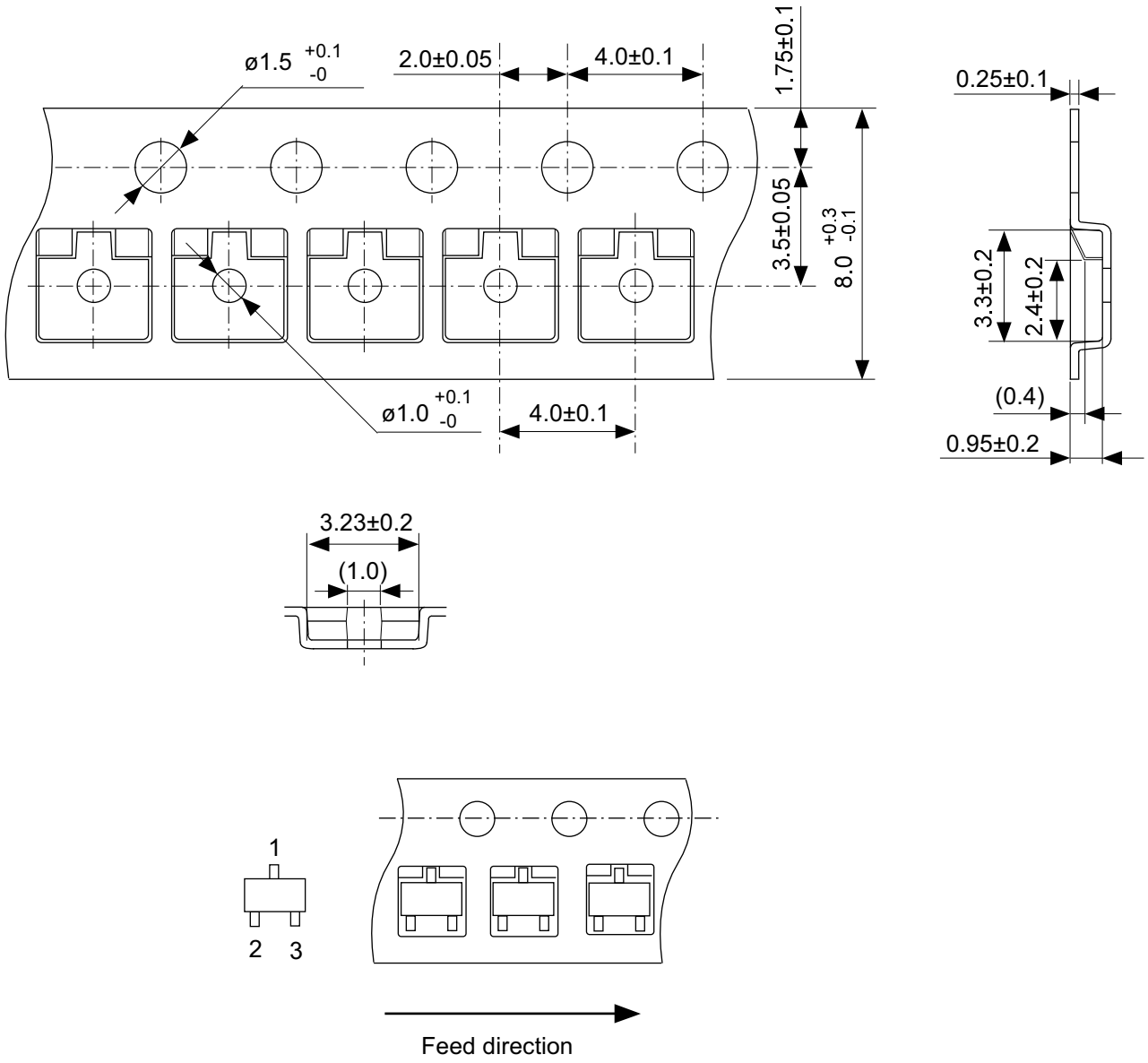


No. MP003-E-P-SD-1.0

TITLE	TSOT233S-A-PKG Dimensions
No.	MP003-E-P-SD-1.0
ANGLE	
UNIT	mm

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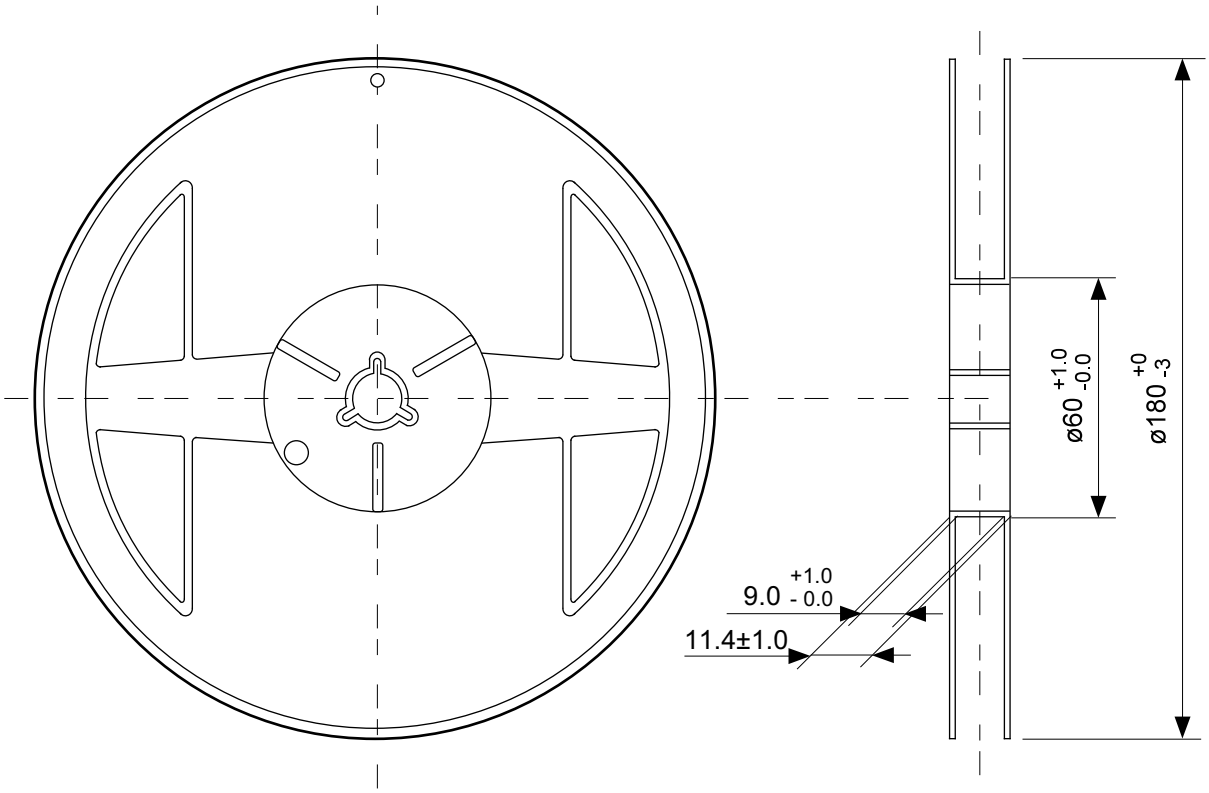
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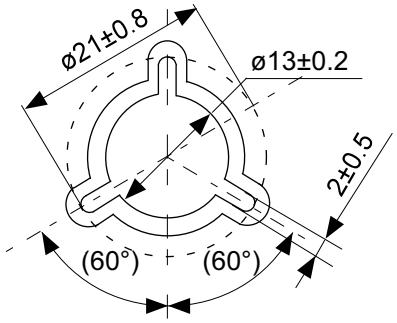
No. MP003-E-C-SD-1.0

TITLE	TSOT233S-A-Carrier Tape
No.	MP003-E-C-SD-1.0
ANGLE	
UNIT	mm
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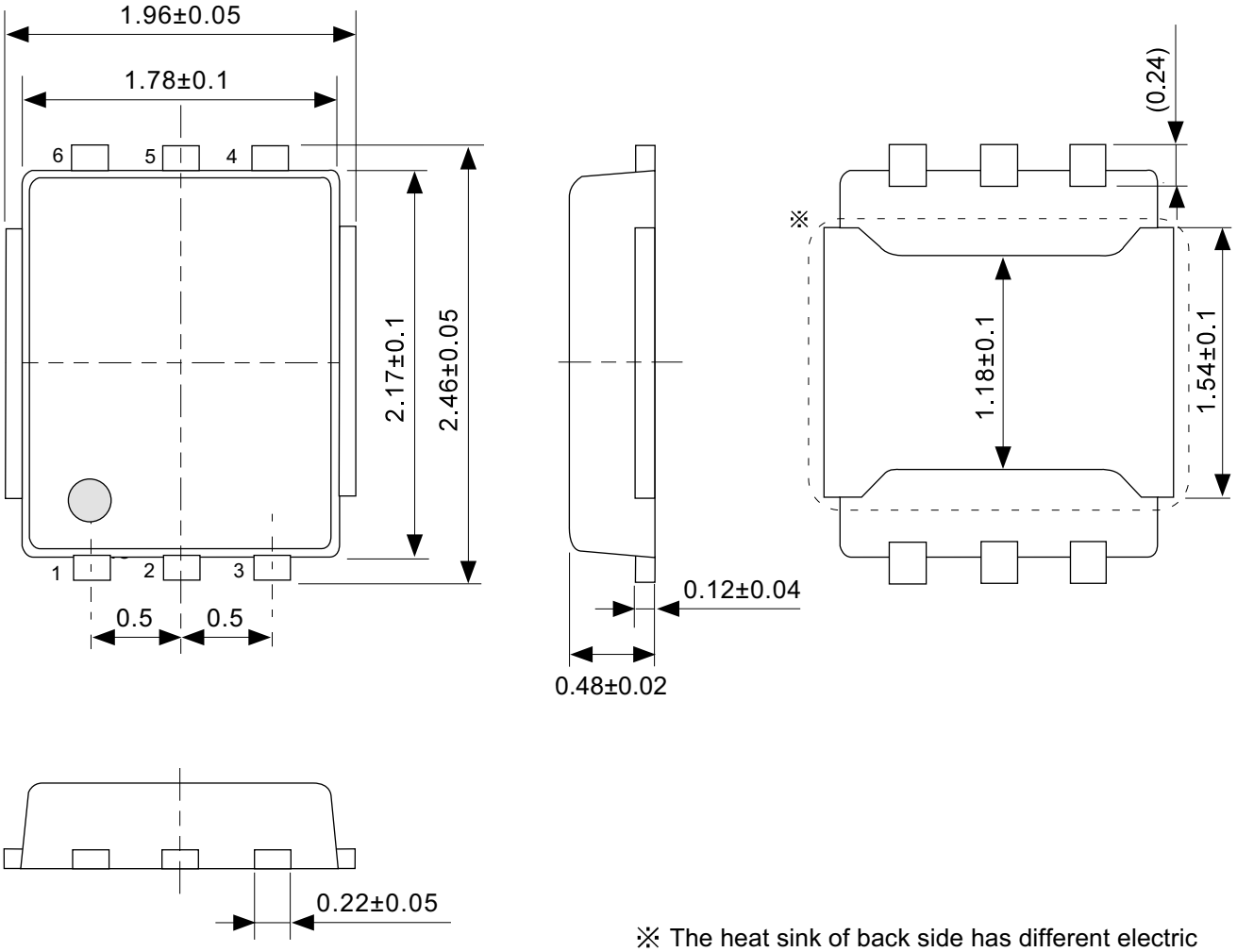
Enlarged drawing in the central part



No. MP003-E-R-SD-1.0

TITLE	TSOT233S-A-Reel		
No.	MP003-E-R-SD-1.0		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			

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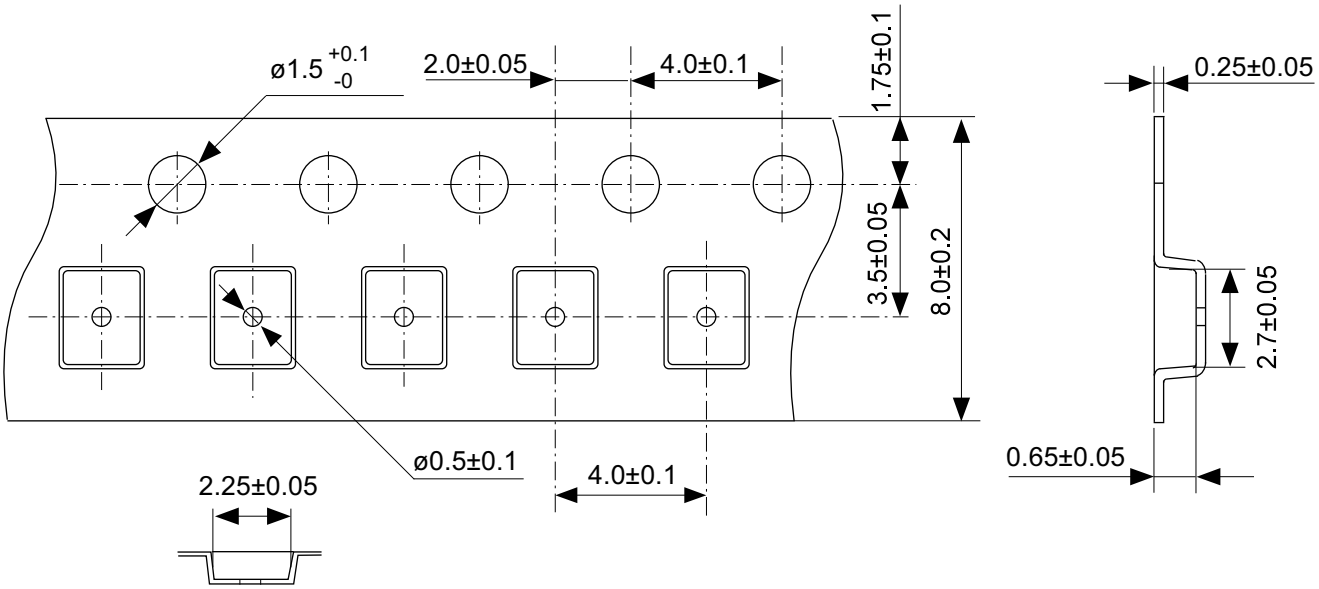


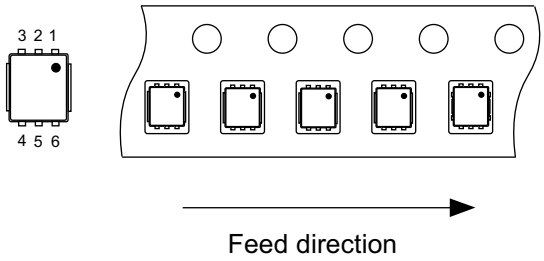
※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PJ006-B-P-SD-1.0

TITLE	HSNT-6-C-PKG Dimensions
No.	PJ006-B-P-SD-1.0
ANGLE	
UNIT	mm
	ABLIC Inc.

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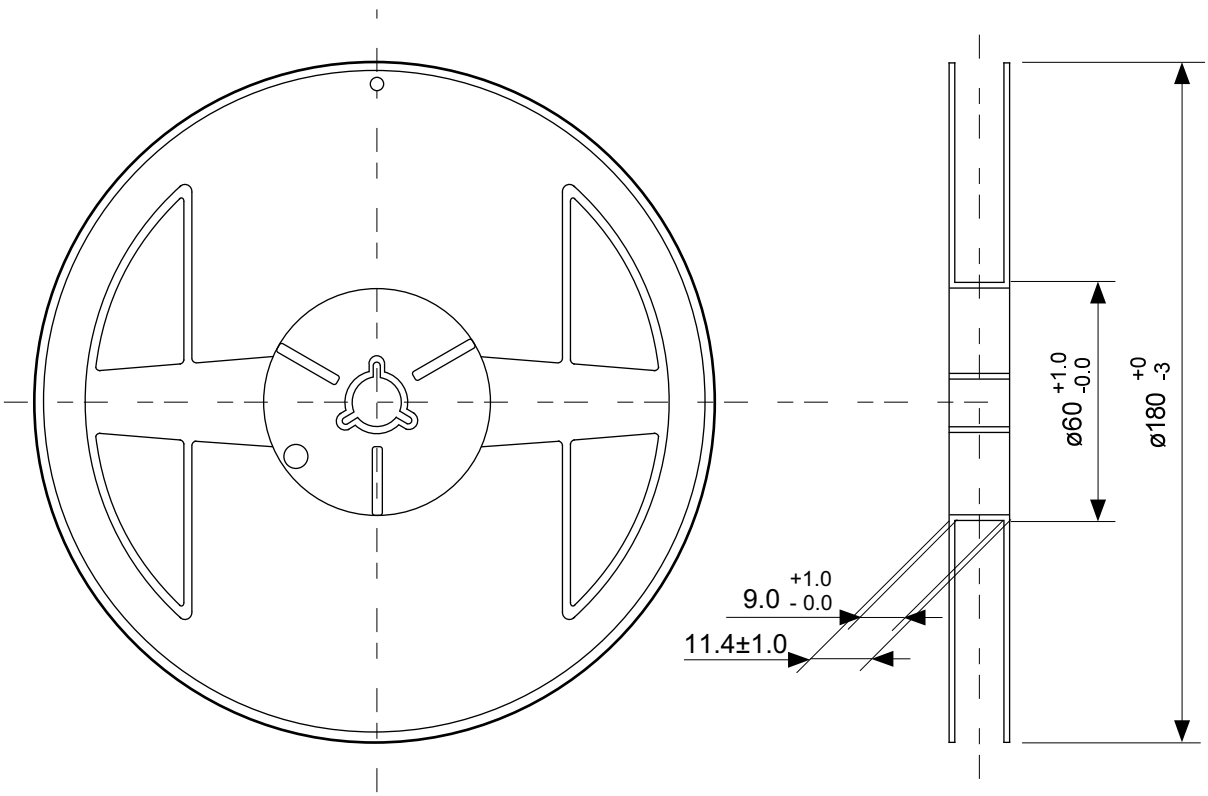




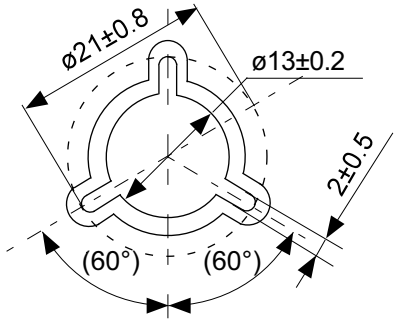
No. PJ006-B-C-SD-1.0

TITLE	HSNT-6-C-Carrier Tape
No.	PJ006-B-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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Enlarged drawing in the central part

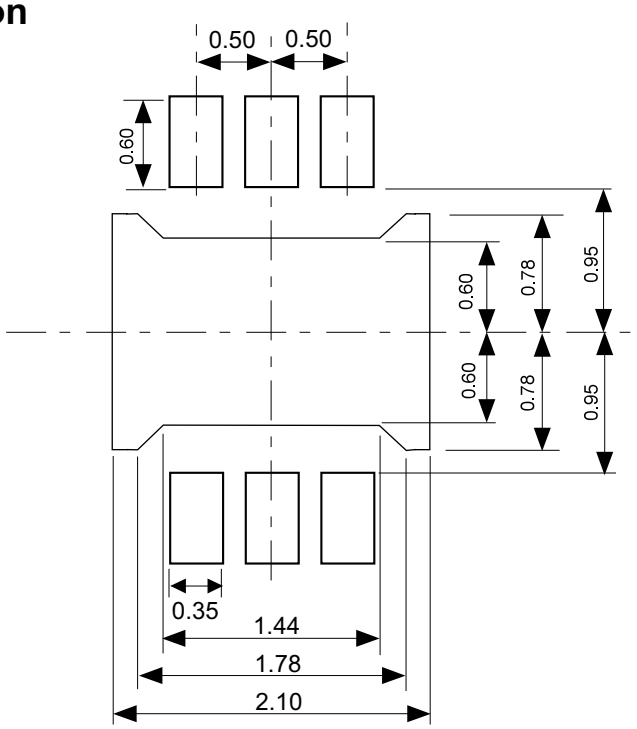


No. PJ006-B-R-SD-1.0

TITLE	HSNT-6-C-Reel		
No.	PJ006-B-R-SD-1.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			

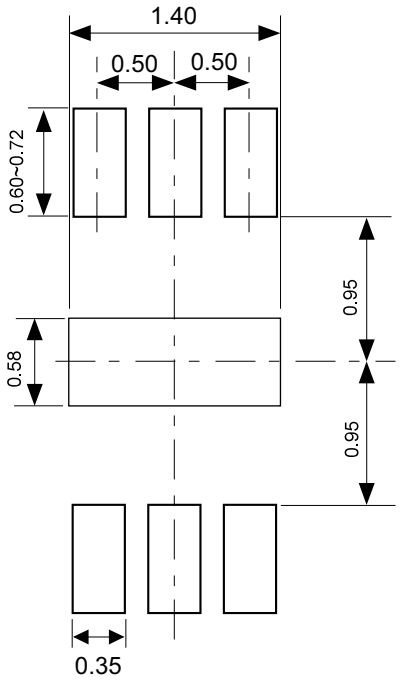
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Land Recommendation



Caution It is recommended to solder the heat sink to a board in order to ensure the heat radiation.
注意　放熱性を確保する為に、PKGの裏面放熱板（ヒートシンク）を基板に半田付けする事を推奨いたします。

Stencil Opening



No. PJ006-B-LM-SD-1.0

Caution
① Mask aperture ratio of the lead mounting part is 100~120%.
② Mask aperture ratio of the heat sink mounting part is 30%.
③ Mask thickness: t0.12 mm
④ Reflow atmosphere: Nitrogen atmosphere is recommended.
(Oxygen concentration: 1000ppm or less)

注意
①リード実装部のマスク開口率は100~120%です。
②放熱板実装のマスク開口率は30%です。
③マスク厚み：t0.12 mm
④リフロー雰囲気・窒素雰囲気（酸素濃度1000ppm以下）推奨

TITLE	HSNT-6-C -Land &Stencil Opening
No.	PJ006-B-LM-SD-1.0
ANGLE	
UNIT	mm

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