

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 58 W asymmetrical Doherty RF power LDMOS transistor is designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 1880 to 2025 MHz.

- Typical Doherty Single-Carrier W-CDMA Performance: $V_{DD} = 28$ Vdc, $I_{DQA} = 700$ mA, $V_{GSB} = 0.3$ Vdc, $P_{out} = 58$ W Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

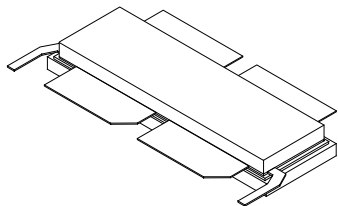
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)
1880 MHz	16.5	50.9	7.9	-33.1
1960 MHz	16.9	50.5	7.8	-36.0
2025 MHz	16.3	50.1	7.8	-36.8

Features

- Advanced High Performance In-Package Doherty
- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Able to Withstand Extremely High Output VSWR and Broadband Operating Conditions
- Designed for Digital Predistortion Error Correction Systems

A2T20H330W24SR6

**1880–2025 MHz, 58 W AVG., 28 V
AIRFAST RF POWER LDMOS
TRANSISTOR**



NI-1230S-4L2L

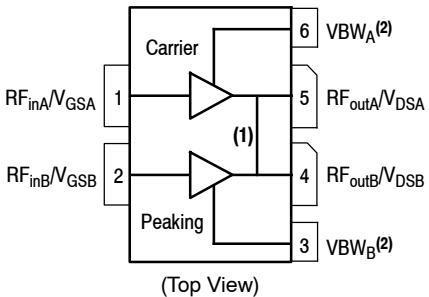


Figure 1. Pin Connections

- Pin connections 4 and 5 are DC coupled and RF independent.
- Device cannot operate with V_{DD} current supplied through pin 3 and pin 6.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +125	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C
CW Operation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	CW	268 1.2	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 79°C , 58 W W-CDMA, 28 Vdc, $I_{DQA} = 700\text{ mA}$, $V_{GSB} = 0.3\text{ Vdc}$, $f = 1960\text{ MHz}$	$R_{\theta JC}$	0.25	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Off Characteristics (4)

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 65\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 32\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	5	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

On Characteristics - Side A, Carrier (4)

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 140\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	1.4	1.3	2.2	Vdc
Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_D = 700\text{ mAdc}$, Measured in Functional Test)	$V_{GSA(Q)}$	2.2	2.6	3.0	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.4\text{ Adc}$)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

On Characteristics - Side B, Peaking (4)

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 180\text{ }\mu\text{Adc}$)	$V_{GS(th)}$	0.8	1.2	1.6	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.8\text{ Adc}$)	$V_{DS(on)}$	0.1	0.15	0.3	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf/calculators>.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf> and search for AN1955.
4. V_{DDA} and V_{ddb} must be tied together and powered by a single DC power supply.

(continued)

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests ^(1,2,3) (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQA} = 700\text{ mA}$, $V_{GSB} = 0.3\text{ Vdc}$, $P_{out} = 58\text{ W Avg.}$, $f = 1880\text{ MHz}$, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	G_{ps}	15.5	16.5	18.5	dB
Drain Efficiency	η_D	48.5	50.9	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.2	7.9	—	dB
Adjacent Channel Power Ratio	ACPR	—	-33.1	-29.0	dBc

Load Mismatch ⁽³⁾ (In Freescale Doherty Test Fixture, 50 ohm system) $I_{DQA} = 700\text{ mA}$, $V_{GSB} = 0.3\text{ Vdc}$, $f = 1960\text{ MHz}$

VSWR 10:1 at 32 Vdc, 354 W Pulse Output Power (3 dB Input Overdrive from 240 W Pulse Rated Power)	No Device Degradation
--	-----------------------

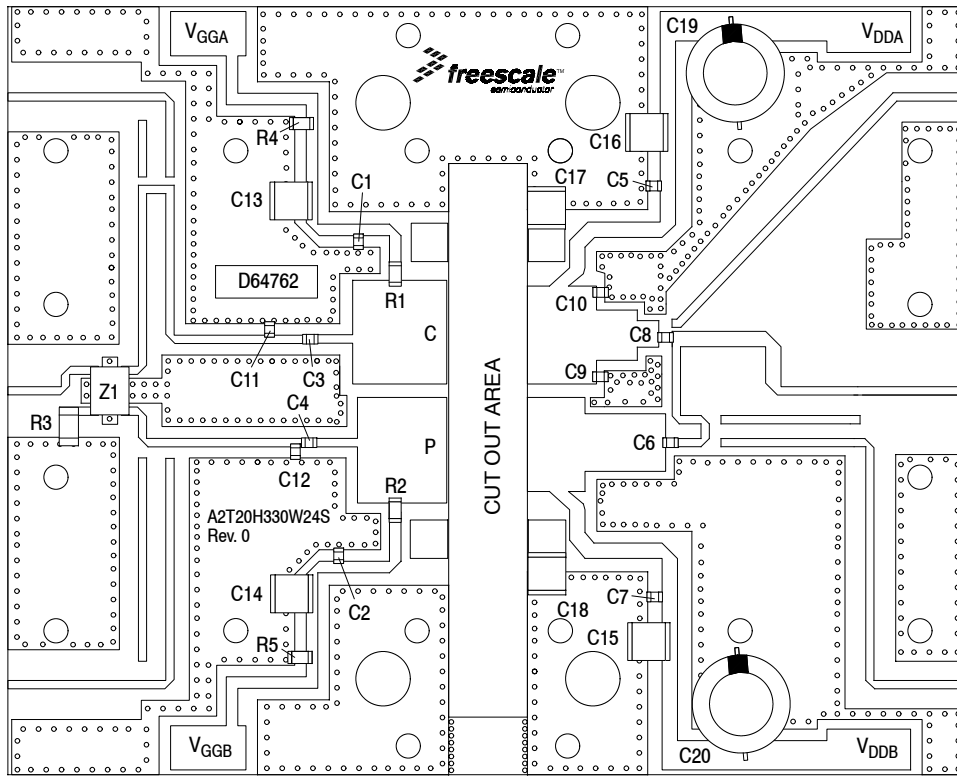
Typical Performance ⁽³⁾ (In Freescale Doherty Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQA} = 700\text{ mA}$, $V_{GSB} = 0.3\text{ Vdc}$, 1880–2025 MHz Bandwidth

P_{out} @ 1 dB Compression Point, CW	P1dB	—	240	—	W
P_{out} @ 3 dB Compression Point ⁽⁴⁾	P3dB	—	380	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1880–2025 MHz bandwidth)	Φ	—	-19	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	140	—	MHz
Gain Flatness in 145 MHz Bandwidth @ $P_{out} = 58\text{ W Avg.}$	G_F	—	0.6	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.005	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C) ⁽⁵⁾	$\Delta P1dB$	—	0.006	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A2T20H330W24SR6	R6 Suffix = 150 Units, 56 mm Tape Width, 13-Reel	NI-1230S-4L2L

1. V_{DDA} and V_{ddb} must be tied together and powered by a single DC power supply.
2. Part internally matched both on input and output.
3. Measurement made with device in an asymmetrical Doherty configuration.
4. $P3dB = P_{avg} + 7.0\text{ dB}$ where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.
5. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.



Note: V_{DDA} and V_{DDB} must be tied together and powered by a single DC power supply.

Figure 2. A2T20H330W24SR6 Test Circuit Component Layout

Table 6. A2T20H330W24SR6 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5, C6, C7	8.2 pF Chip Capacitors	ATC600F8R2BT250XT	ATC
C8	5.6 pF Chip Capacitor	ATC600F5R6BT250XT	ATC
C9, C10	0.8 pF Chip Capacitors	ATC600F0R8BT250XT	ATC
C11, C12	0.6 pF Chip Capacitors	ATC600F0R6AT250XT	ATC
C13, C14, C15, C16, C17, C18	10 μ F Chip Capacitors	C5750X7S2A106K230KB	TDK
C19, C20	220 μ F, 63 V Electrolytic Capacitors	SK063M0220B5S-1012	Yageo
R1, R2	2.2 Ω , 1/4 W Chip Resistor	CRCW12062R20JNEA	Vishay
R3	50 Ω , 10 W Chip Resistor	CW12010T0050GBK	ATC
R4, R5	1 K Ω , 1/4 W Chip Resistors	CRCW12061K00FKEA	Vishay
Z1	1700–2000 MHz Band, 90°, 5 dB Directional Coupler	X3C19P1-05S	Anaren
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.66$	D64762	MTL

TYPICAL CHARACTERISTICS

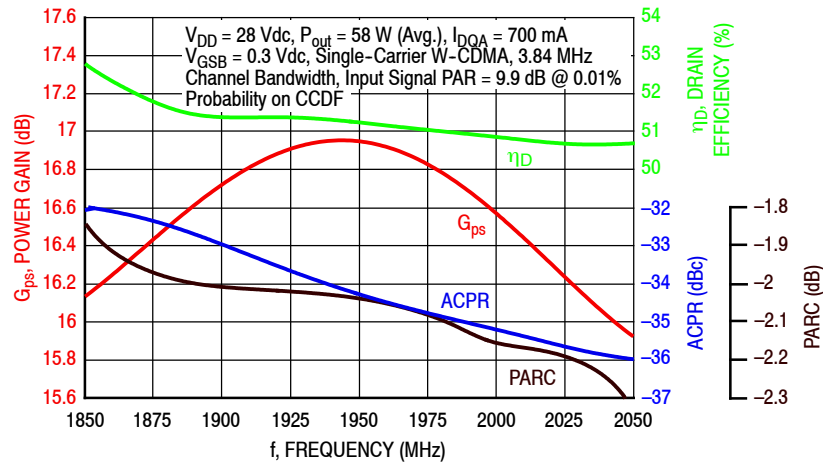


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ $P_{out} = 58$ Watts Avg.

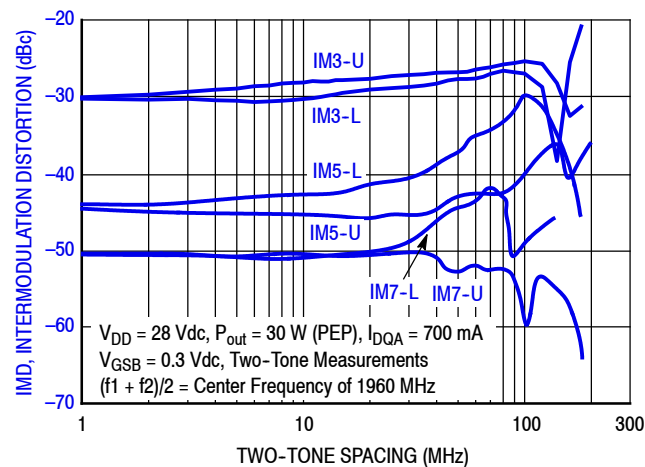


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

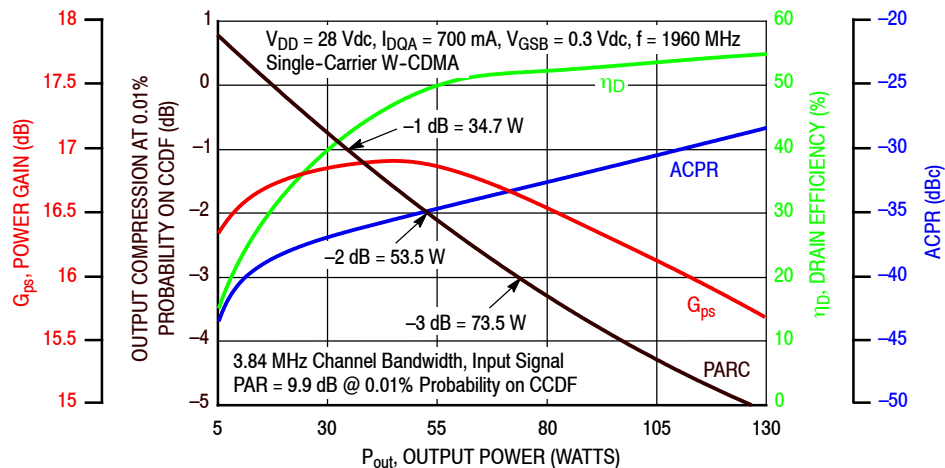


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

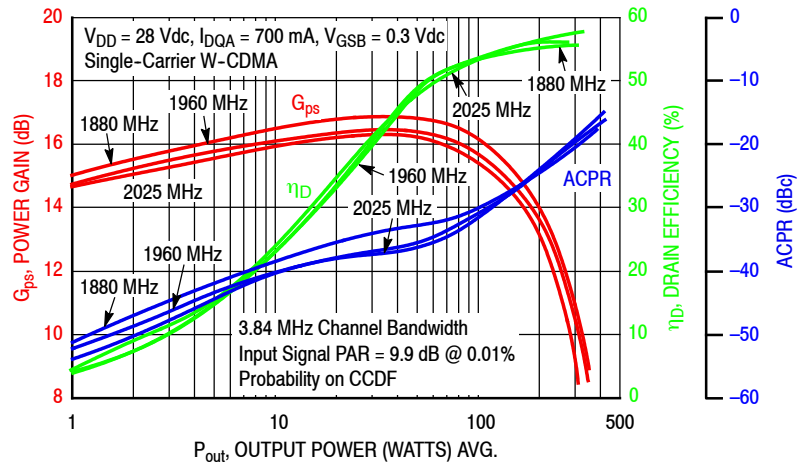


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

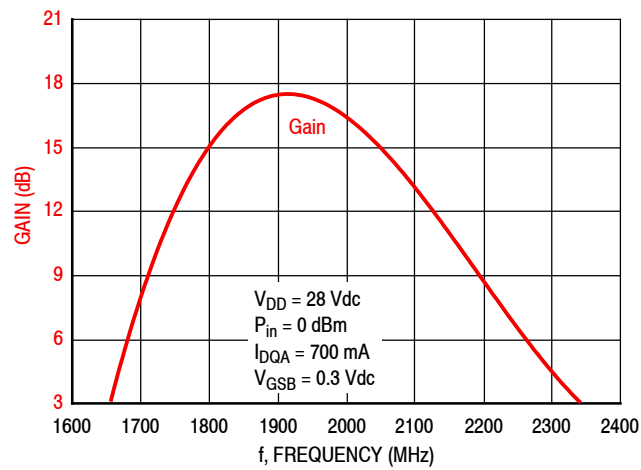


Figure 7. Broadband Frequency Response

Table 7. Carrier Side Load Pull Performance — Maximum Power Tuning
 $V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = 774 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	1.73 – j3.99	1.65 + j4.16	1.09 – j3.27	19.2	52.2	167	59.4	–12
1960	3.43 – j5.25	3.31 + j5.46	1.18 – j3.50	19.3	52.2	165	59.6	–13
2025	6.42 – j5.02	6.81 + j5.80	1.20 – j3.67	19.5	52.1	163	58.7	–13

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	1.73 – j3.99	1.54 + j4.30	1.07 – j3.44	17.0	53.0	199	61.1	–16
1960	3.43 – j5.25	3.22 + j5.82	1.15 – j3.65	17.0	52.9	196	60.6	–17
2025	6.42 – j5.02	7.20 + j6.40	1.22 – j3.82	17.3	52.9	194	60.2	–17

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 8. Carrier Side Load Pull Performance — Maximum Drain Efficiency Tuning
 $V_{DD} = 28 \text{ Vdc}$, $I_{DQA} = 774 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	1.73 – j3.99	1.80 + j4.54	2.56 – j2.40	22.3	50.1	103	72.8	–18
1960	3.43 – j5.25	3.81 + j5.93	2.29 – j2.45	22.2	50.2	104	71.5	–19
2025	6.42 – j5.02	8.06 + j5.78	2.00 – j2.60	22.2	50.4	110	69.8	–18

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	1.73 – j3.99	1.73 + j4.63	2.72 – j2.37	20.4	50.6	114	74.9	–25
1960	3.43 – j5.25	3.70 + j6.23	2.29 – j2.41	20.3	50.8	120	73.0	–26
2025	6.42 – j5.02	8.59 + j6.16	2.06 – j2.48	20.4	50.9	123	72.0	–25

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

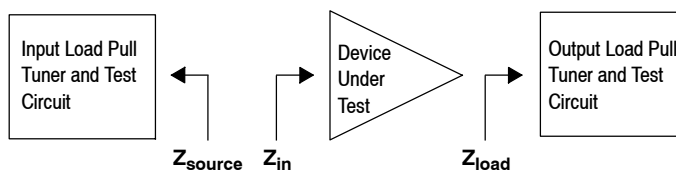
 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.


Table 9. Peaking Side Load Pull Performance — Maximum Power Tuning
 $V_{DD} = 28 \text{ Vdc}$, $V_{GSB} = 0.6 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	1.21 – j4.59	1.07 + j4.59	1.71 – j3.44	14.6	53.5	222	57.0	–33
1960	1.99 – j5.85	1.82 + j6.09	1.77 – j3.38	15.0	53.5	226	57.7	–33
2025	3.66 – j7.62	3.48 + j7.91	1.67 – j3.37	15.2	53.7	235	59.4	–35

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	1.21 – j4.59	1.07 + j4.78	1.63 – j3.56	12.4	54.3	268	58.0	–39
1960	1.99 – j5.85	1.92 + j6.43	1.77 – j3.58	12.8	54.3	270	58.5	–40
2025	3.66 – j7.62	3.91 + j8.48	1.82 – j3.65	13.0	54.4	276	60.0	–42

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Table 10. Peaking Side Load Pull Performance — Maximum Drain Efficiency Tuning
 $V_{DD} = 28 \text{ Vdc}$, $V_{GSB} = 0.6 \text{ mA}$, Pulsed CW, 10 $\mu\text{sec}(\text{on})$, 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	1.21 – j4.59	0.93 + j4.56	3.89 – j2.29	15.8	51.9	156	67.3	–37
1960	1.99 – j5.85	1.61 + j6.06	3.07 – j2.05	16.2	52.3	170	67.7	–37
2025	3.66 – j7.62	3.07 + j7.90	2.72 – j1.91	16.3	52.3	170	69.5	–39

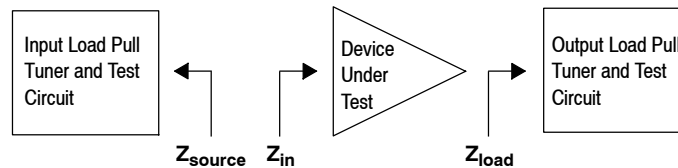
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)}$ (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1880	1.21 – j4.59	0.99 + j4.78	3.44 – j3.07	13.6	53.1	204	66.8	–44
1960	1.99 – j5.85	1.75 + j6.42	3.25 – j2.35	14.1	53.0	200	67.7	–46
2025	3.66 – j7.62	3.60 + j8.50	2.92 – j2.29	14.2	53.2	207	68.8	–47

(1) Load impedance for optimum P1dB efficiency.

(2) Load impedance for optimum P3dB efficiency.

 Z_{source} = Measured impedance presented to the input of the device at the package reference plane.

 Z_{in} = Impedance as measured from gate contact to ground.

 Z_{load} = Measured impedance presented to the output of the device at the package reference plane.


P1dB – TYPICAL CARRIER LOAD PULL CONTOURS — 1960 MHz

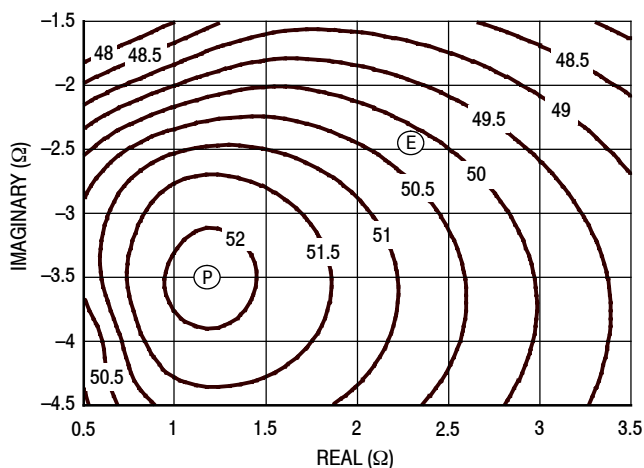


Figure 8. P1dB Load Pull Output Power Contours (dBm)

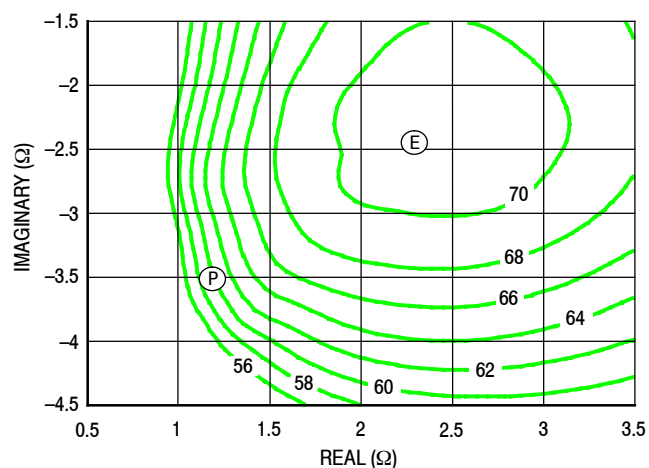


Figure 9. P1dB Load Pull Efficiency Contours (%)

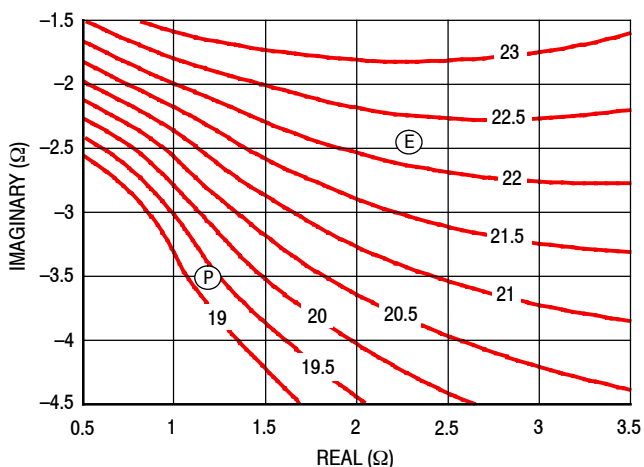


Figure 10. P1dB Load Pull Gain Contours (dB)

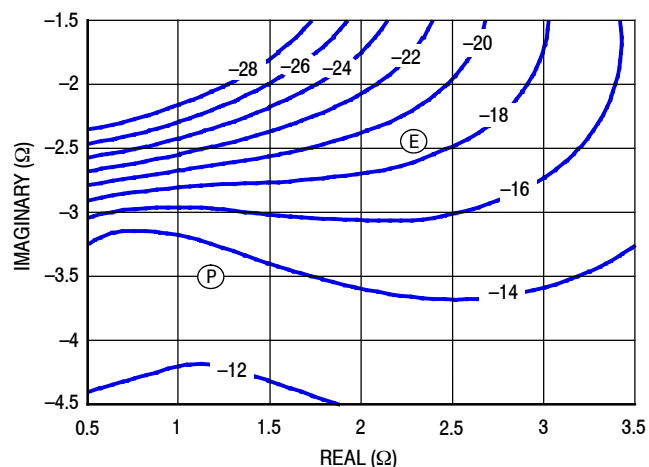


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB – TYPICAL CARRIER LOAD PULL CONTOURS — 1960 MHz

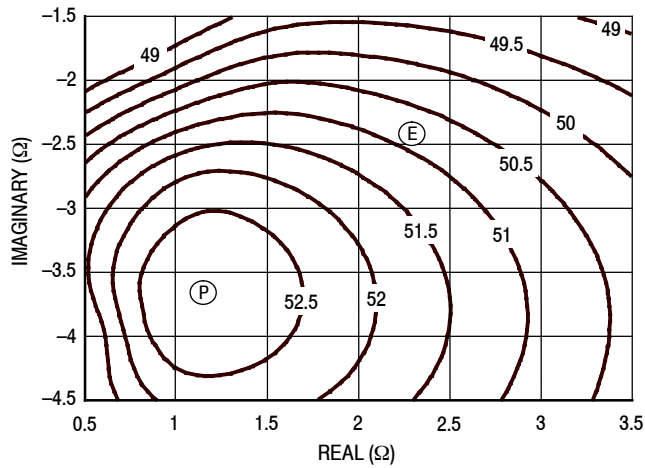


Figure 12. P3dB Load Pull Output Power Contours (dBm)

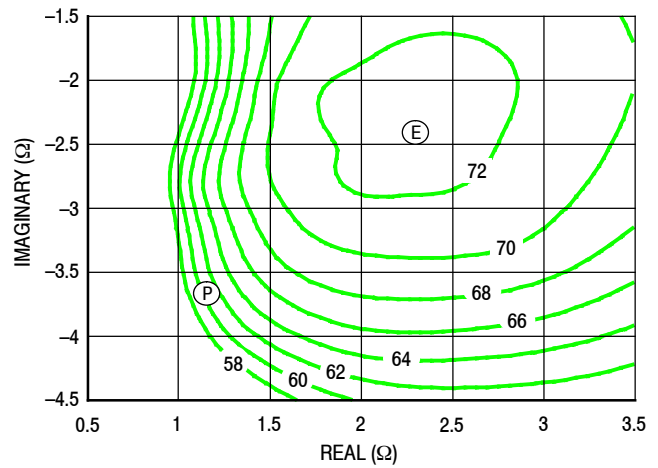


Figure 13. P3dB Load Pull Efficiency Contours (%)

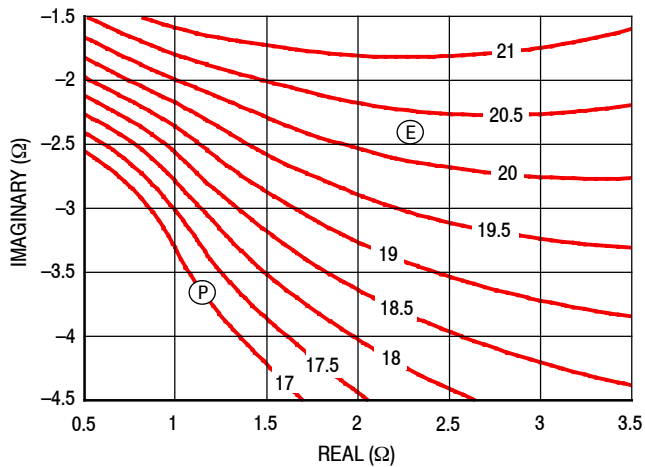


Figure 14. P3dB Load Pull Gain Contours (dB)

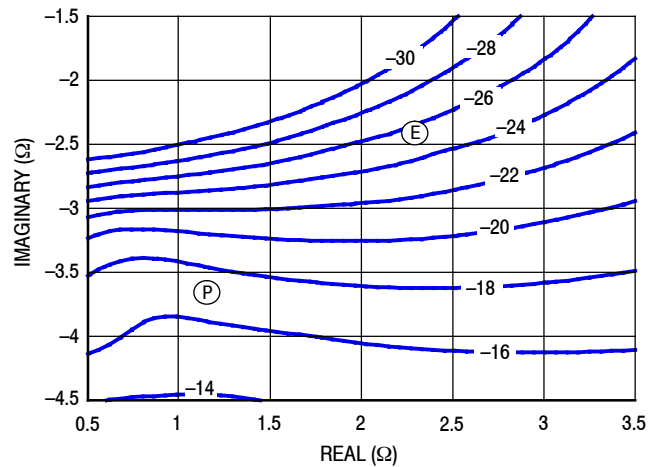


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P1dB – TYPICAL PEAKING LOAD PULL CONTOURS — 1960 MHz

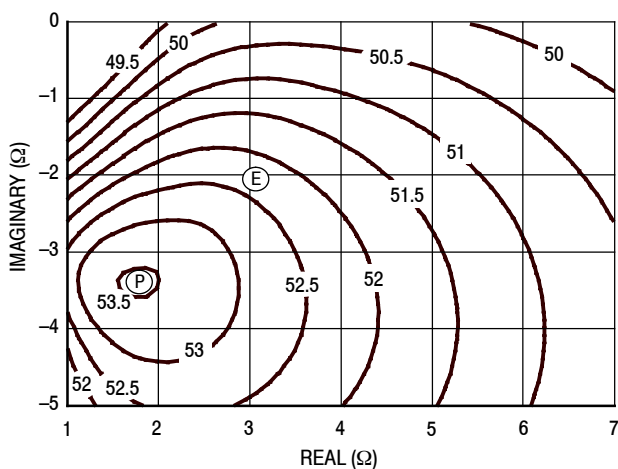


Figure 16. P1dB Load Pull Output Power Contours (dBm)

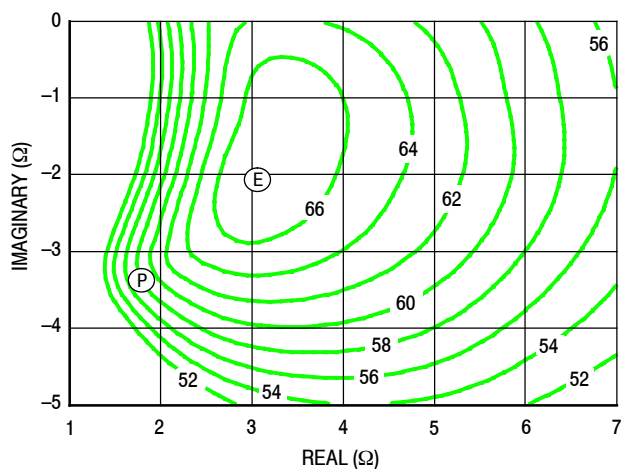


Figure 17. P1dB Load Pull Efficiency Contours (%)

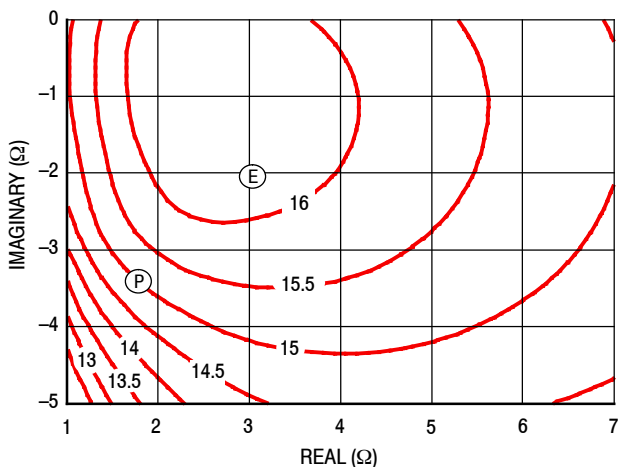


Figure 18. P1dB Load Pull Gain Contours (dB)

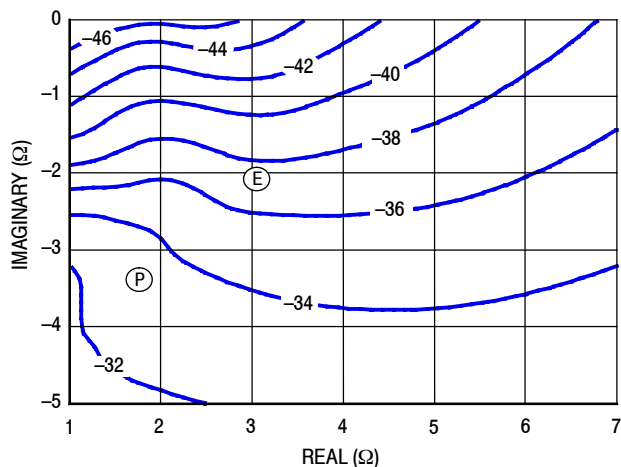


Figure 19. P1dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

P3dB – TYPICAL PEAKING LOAD PULL CONTOURS — 1960 MHz

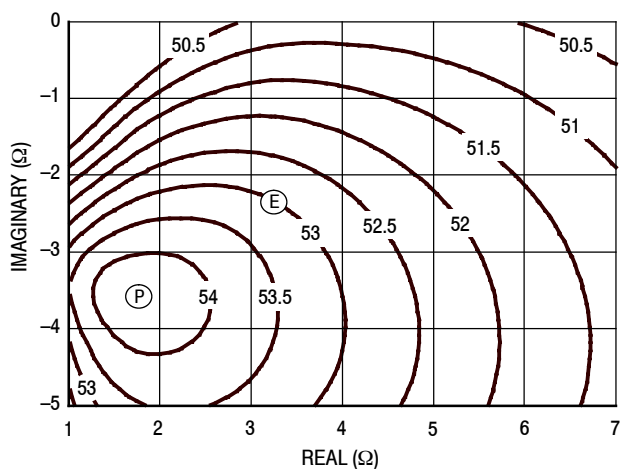


Figure 20. P3dB Load Pull Output Power Contours (dBm)

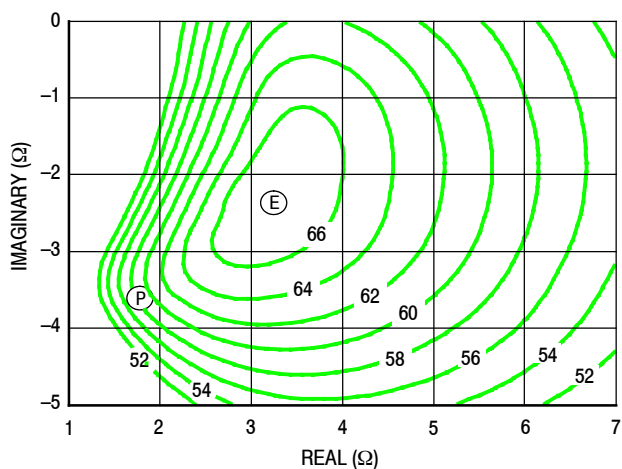


Figure 21. P3dB Load Pull Efficiency Contours (%)

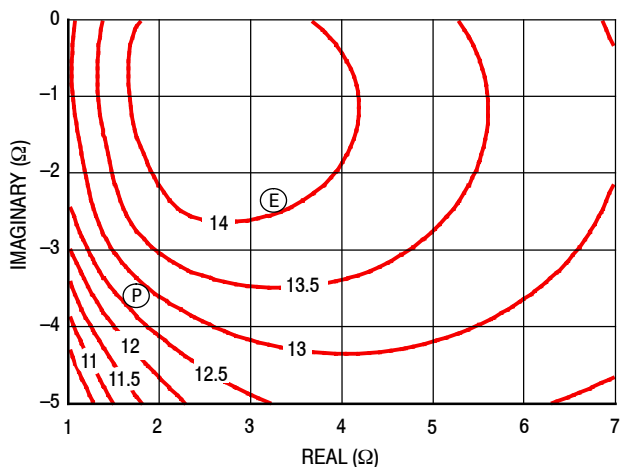


Figure 22. P3dB Load Pull Gain Contours (dB)

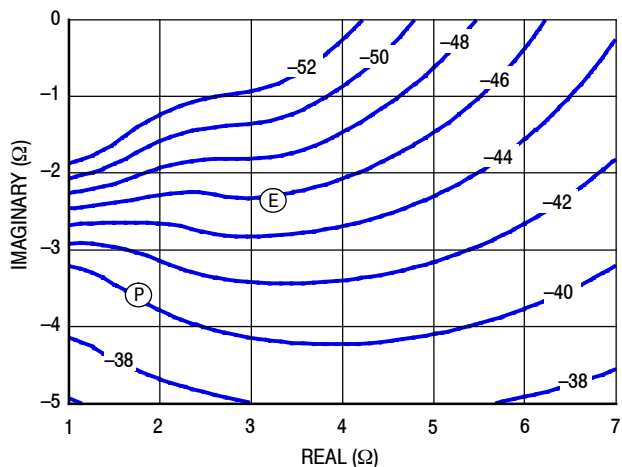
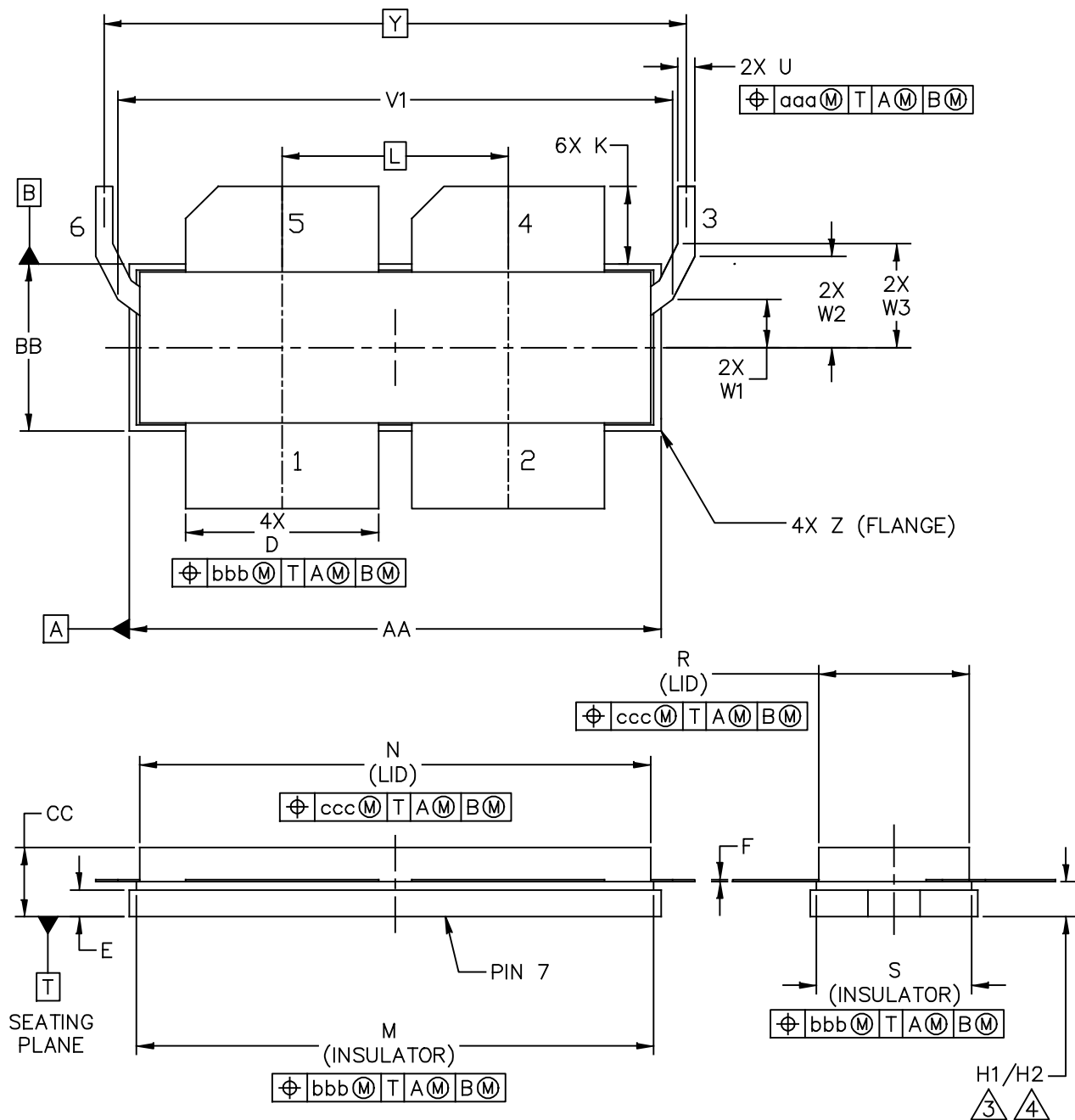


Figure 23. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: NI-1230-4LS2L	DOCUMENT NO: 98ASA00513D	REV: A
	STANDARD: NON-JEDEC	
		08 MAR 2013

A2T20H330W24SR6

NOTES:

1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

2. CONTROLLING DIMENSION: INCH

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 1, 2, 4 & 5. H2 APPLIES TO PINS 3 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

INCH			MILLIMETER		INCH			MILLIMETER	
DIM	MIN	MAX	MIN	MAX	DIM	MIN	MAX	MIN	MAX
AA	1.265	1.275	32.13	32.39	N	1.218	1.242	30.94	31.55
BB	.395	.405	10.03	10.29	R	.365	.375	9.27	9.53
CC	.170	.190	4.32	4.83	S	.365	.375	9.27	9.53
D	.455	.465	11.56	11.81	U	.035	.045	0.89	1.14
E	.062	.066	1.57	1.68	V1	1.320	1.330	33.53	33.78
F	.004	.007	0.10	0.18	W1	.110	.120	2.79	3.05
H1	.082	.090	2.08	2.29	W2	.213	.223	5.41	5.66
H2	.078	.094	1.98	2.39	W3	.243	.253	6.17	6.43
K	.175	.195	4.45	4.95	Y	1.390 BSC		35.31 BSC	
L	.540 BSC		13.72 BSC		Z	R.000	R.040	R0.00	R1.02
M	1.219	1.241	30.96	31.52	aaa	.015		0.38	
					bbb	.010		0.25	
					ccc	.020		0.51	
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.			MECHANICAL OUTLINE			PRINT VERSION NOT TO SCALE			
TITLE: NI-1230-4LS2L					DOCUMENT NO: 98ASA00513D REV: A				
					STANDARD: NON-JEDEC				
					08 MAR 2013				

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to <http://www.freescale.com/rf>
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2015	• Initial Release of Data Sheet

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: freescale.com/SalesTermsandConditions.

Freescale and the Freescale logo are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. Airfast is a trademark of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.
© 2015 Freescale Semiconductor, Inc.