EPC2152 – ePower™ Stage IC

V_{IN}, 80 V

I_{Load}, 15 A

EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Rev. 2, Revised November 26, 2024

The ePower™ Stage IC Product Family integrates input logic interface, high-side level shifting, synchronous bootstrap charging and gate drivers along with eGaN output FETs into one monolithic integrated-circuit using EPC's proprietary GaN IC technology. The result is a Power Stage IC that translates logic level control signals into a high voltage and high current power stage that is simpler to design, smaller in size and easier to manufacture while being more efficient to operate.

Key Parameters		
PARAMETER	**VALUE**	**UNIT**
Power Stage Load Current (1 MHz) (1)	15	A
Operating PWM Frequency (Maximum) (2)	3	MHz
Absolute Maximum Input Voltage	80	V
Operating Input Voltage Range	60	
Nominal Bias Supply Voltage	12	

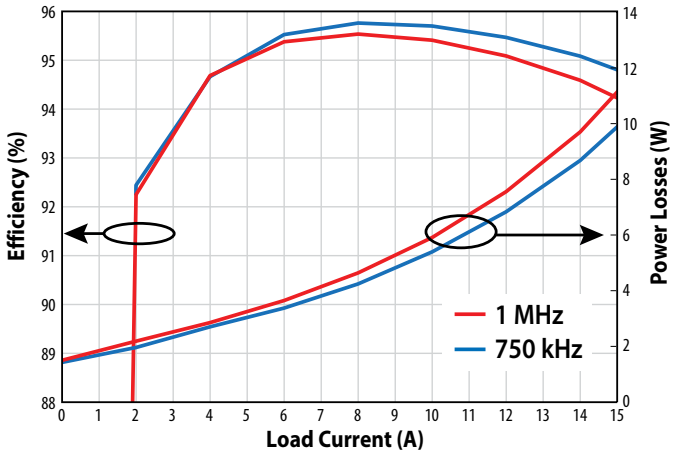
Output Current and PWM Frequency Ratings are specified at ambient temperature of 25°C. See Application Information section for rating methodologies, test conditions, thermal management techniques and thermal derating curves.

Device Information		
PART NUMBER	**Rated $R_{DS(on)}$ for HS and LS FETs at 25 °C**	**CSP Package Size (mm)**
EPC2152	10 mΩ + 10 mΩ	2.59 x 3.85

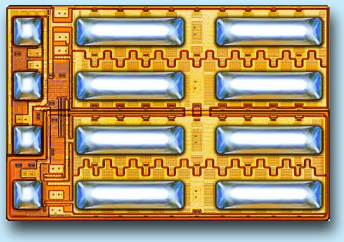
(1) Achieved when using proper heatsink. Output current and PWM frequency ratings are function of operating conditions, see "Load current rating" in the application section for more information.

(2) Operating PWM switching frequency range is a function of power dissipation, maximum allowed junction temperature and minimum duty cycle.

Figure 1: Performance Curves



Buck Converter, V_{IN} = 48 V, V_{OUT} = 12 V, Deadtime = 10 ns, L = 2.2 µH, DCR = 700 µΩ, with heatsink attached, airflow = 400 LFM, TA = 25°C, using **EPC90120 evaluation board**.



Package size: 2.59 x 3.85 mm

EPC2152 ePower™ Stage IC

Applications

- Buck, boost, buck-boost converters
- Half-bridge, full bridge LLC converters
- Motor drive inverter
- Class D audio amplifier

Features

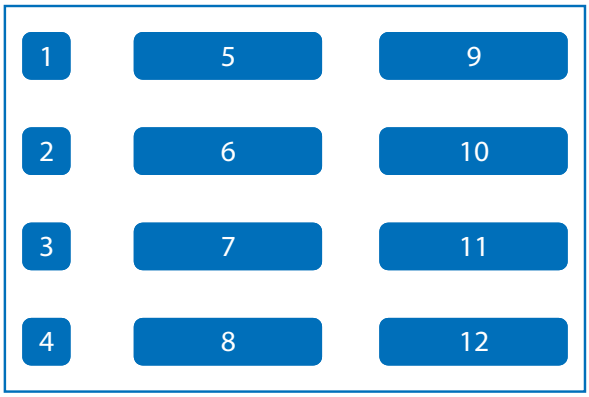
- Integrated high side eGaN® FET with internal gate driver and level shifter
- 3.3 V or 5 V CMOS input logic levels
- Independent high side and low side control inputs
- Logic lockout commands both FETs off when inputs are both high at same time
- Internally regulated gate drive voltage
- Tuned to 1.5 ns switching time
- Controlled over-voltage transient at switching node
- Robust level shifter operation for hard and soft switching conditions
- False trigger immunity from fast switching transients
- Synchronous charging for high-side bootstrap supply
- Undervoltage lockout for high side and low side power supplies

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://bit.ly/EPC2152

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Figure 2: EPC2152 Chip Scale Package
(transparent top view)

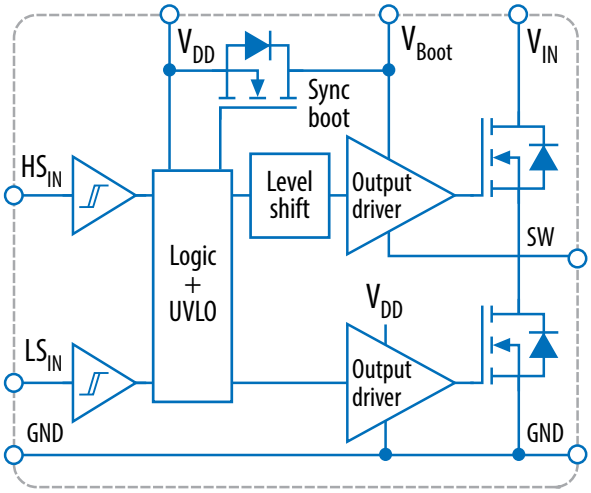


EPC2152 Pinout Description

Pin	Pin Name	Pin Type	Description
1	V_{BOOT}	S	Floating bootstrap power supply referenced to SW. Connect an external bootstrap capacitor, C_{BOOT}, between V_{BOOT} and SW.
2	V_{DD}	S	Internal power supply referenced to GND, connect an external bypass capacitor from V_{DD} to GND.
3	HS_{IN}	L	High-side PWM logic input referenced to GND. Internal pull-down resistor is connected between HS_{IN} and GND.
4	LS_{IN}	L	Low-side PWM logic input referenced to GND. Internal pull-down resistor is connected between LS_{IN} and GND.
5, 9	V_{IN}	P	Power bus input. Connected to drain terminal of internal high side eGaN FET. Connect power loop capacitors from V_{IN} to GND
6, 7, 10 ,11	SW	P	Output switching node. Connected to output of half-bridge power stage. SW pin connects the source terminal of high-side eGaN FET to the drain terminal of the low-side eGaN FET.
8, 12	GND	P	Power ground. Connected to low side eGaN FET source terminal. The operating power supply, V_{DD}, is also referenced to GND. Connect bypass capacitors between operating bias supply, V_{DD}, to GND, and power loop bypass capacitor from V_{IN} to GND.

Pin Type: P = Power, S = Bias Supplies, L = Logic Inputs/Outputs

Figure 3: Functional Block Diagram



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Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur and device reliability may be affected. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise.

Absolute Maximum Ratings				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
V_{IN}	Input voltage		80	V
SW (continuous)	Output switching node (SW to GND), continuous		80	
V_{DD}	Internal low side supply voltage		14	
V_{BOOT} – SW	Internal high side supply voltage (V_{BOOT} to SW)		14	
HS_{IN}, LS_{IN}	PWM logic inputs	-1	5.5	
T_J	Junction temperature	-40	125	°C
T_{STG}	Storage temperature	-55	150	

ESD Ratings

ESD Ratings				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
HBM	Human-body model (JEDEC JS-001)	+/-500		V
CDM	Charged-device model (JEDEC JESD22-C101)	+/-1000		

Thermal Characteristics

$R_{\theta JA_JEDEC}$ is defined according to JESD51-2 standard. Based on this standard, the device is placed on 4-layer PCB with 2 oz copper for outer layers and 1 oz copper for inner layers. This assembly is placed in a 1 cubic foot enclosure with no forced air cooling, only natural convection.

$R_{\theta JA_EVB}$ is based on EPC90120, a real evaluation board with no forced air cooling. This thermal resistance is more indicative of an actual application environment.

$R_{\theta JA}$ is determined with the device mounted on 1 in^2 of copper pad, single layer 2 oz copper on FR4 board.

Thermal Characteristics			
SYMBOL	**PARAMETER**	**TYP**	**UNITS**
$R_{\theta JC_Top}$	Thermal Resistance, Junction-to-Case (Top surface of exposed die substrate)	0.47	°C/W
$R_{\theta JB_Bottom}$	Thermal Resistance, Junction-to-Board (At solder joints of V_{IN} and SW PCB pads)	3	
$R_{\theta JA_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	43	
$R_{\theta JA_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC90142 EVB)	25	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	46	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise.

Recommended Operating Conditions					
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{IN}	Input voltage	0		60	V
SW (Q3 Mode)	Output switch node, 3rd quadrant mode	-2.5		V_{IN} + 2.5	
SW (pulse2ns)	Output switch node, transient PW < 2 ns	-10		V_{IN} +10	
V_{DD}	Internal low side supply voltage	11	12	13	
V_{BOOT} – SW	Internal high side supply voltage (V_{BOOT} to SW)	11	12	13	
HS_{IN}, LS_{IN}	PWM logic inputs	0		5	
$T_{J, op}$	Operating Junction Temperature	-40		125	°C

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Electrical Characteristics

Nominal V_{IN} = 48 V, V_{DD} = 12 V and (V_{BOOT} – SW) = 12 V. All typical ratings are specified at T_A = 25°°C unless otherwise indicated. All voltage parameters are absolute voltages referenced to GND unless indicated otherwise. (1)

Electrical Characteristics						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Power Supply						
I_{DD_Q}	Off state total quiescent current	HS_{IN} /LS_{IN} = 0 V, V_{DD} = 12 V, SW floating		14	21	mA
I_{DD_1MHz}	Total operating current @1 MHz	PWM = 1 MHz, 50% On-Time, includes bootstrap current		25	37	
I_{DD_3MHz}	Total operating current @3 MHz	PWM = 1 MHz, 50% On-Time, includes bootstrap current		28	40	
Bootstrap Power Supply						
I_{BOOT_Q}	Off state bootstrap supply current	HS_{IN} = 0 V, (V_{BOOT} – V_{SW}) = 5 V		9	12.5	mA
I_{BOOT_1MHz}	Bootstrap supply current @1 MHz	HS PWM = 100 kHz, 50% On-Time		12	17	
I_{BOOT_3MHz}	Bootstrap supply current @3 MHz	HS PWM = 1 MHz, 50% On-Time		17	24	
V_{SYNC_DROP}	Voltage across Synch-boot FET	I_{SYNC_BOOT} = 20 mA	320	400	480	mV
$R_{ON_SYNC_BOOT}$	On resistance of Synch-boot FET	I_{SYNC_BOOT} = 20 mA	16	20	24	Ω
Undervoltage Lockout						
V_{DD_UVLO+}	UVLO Trip Level V_{DD} Rising	LS_{IN} = 5 V, V_{DD} Ramps Up		6.5		V
V_{DD_HYST}	UVLO V_{DD} Falling Hysteresis	LS_{IN} = 5 V, V_{DD} Ramps Down		0.5		
V_{BOOT_UVLO+}	UVLO Trip Level (V_{BOOT} - SW) Rising	HS_{IN} = 5 V, V_{BOOT} Ramps Up		6.25		
V_{BOOT_HYST}	UVLO (V_{BOOT} - SW) Falling Hysteresis	HS_{IN} = 5 V, V_{BOOT} Ramps Down		0.5		
Logic Input Pins						
V_{IH}	High-level Logic Threshold	HS_{IN}, LS_{IN} Rising	2.4			V
V_{IL}	Low-level Logic Threshold	HS_{IN}, LS_{IN} Falling			0.8	
V_{IHYST}	Logic Threshold Hysteresis	V_{IH} Rising – V_{IL} Falling		0.5		
R_{IN}	HS_{IN} and LS_{IN} Pull-Down Resistance	HS_{IN}, LS_{IN} = 5 V	4.5	7	11	kΩ
Dynamic Characteristics (Logic Input to output switching node) See Figure 4a and 4b for timing diagram and test circuit)						
$t_delay_{HS_on}$	High side on propagation delay	SW = 0 V and HS FET turn-on		30		ns
$t_delay_{LS_on}$	Low side on propagation delay	SW = 60 V and LS FET turn-on		30		
$t_delay_{HS_off}$	High side off propagation delay	SW = 60 V and HS FET turn-off		30		
$t_delay_{LS_off}$	Low side off propagation delay	SW = 0 V and LS FET turn-off		30		
$t_{matchon}$	Delay matching LS_{OFF} to HS_{ON}	LS turn-off to HS turn-on		0		
$t_{matchoff}$	Delay matching HS_{OFF} to LS_{ON}	HS turn-off to LS turn-on		0		
$t_{lockout}$	Cross-conduction lockout time	LS turn-off to HS turn-on or HS turn-off to LS turn-on		5		
PWM_min	Minimum input pulse width	50% to 50% width		15		
dV/dt	SW to GND voltage slew rate	LS_{IN} = 0 V, HS_{IN} = 0 V → 5 V, V_{IN} = 48 V, I_{OUT} = 10 A (2)(3)		27		V/ns
High Side Internal Power FET						
$R_{DS(on)_HS}$	High side FET $R_{DS(on)}$	I_{LOAD} = +/-10 A, HS_{IN} = 5 V, LS_{IN} = 0 V		10	14.5	mΩ
$V_{HS_DS_Clamp}$	High side 3rd quadrant clamp	I_{LOAD} = - 10 A, HS_{IN} & LS_{IN} = 0 V		-2	-2.5	V
I_{LEAK_VIN-SW}	Leakage current (V_{IN} to SW)	HS_{IN} = 0 V, SW = 80 V, SW = 0 V		100	210	µA
C_{OSS_HSFET}	Output capacitance (V_{IN} to SW)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 0 V		339		pF
Q_{OSS_HSFET}	Output charge (V_{IN} to SW)	HS_{IN} = 0 V, SW = 48 V, SW = 0 V		26		nC
Low Side Internal Power FET						
$R_{DS(on)_LS}$	Low side FET $R_{DS(on)}$	I_{LOAD} = +/-10 A, LS_{IN} = 5 V, HS_{IN} = 0 V		10	14.5	mΩ
$V_{HS_DS_Clamp}$	Low side 3rd quadrant clamp	I_{LOAD} = - 10 A, HS_{IN} & LS_{IN} = 0 V		-2	-2.5	V
I_{LEAK_SW-GND}	Leakage current (SW to GND)	LS_{IN} = 0 V, SW = 80 V		150	310	µA
C_{WELL}	HV well capacitance (SW to GND)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 48 V		57		pF
C_{OSS_LSFET}	Output capacitance (SW to GND)	LS_{IN} = 0 V, SW = 48 V		396		
Q_{OSS_LSFET}	Output charge (SW to GND)	LS_{IN}= 0 V, SW = 48 V		31		nC

(1) Parameters that show only typical value are guaranteed by design and may not be tested in production
(2) Measured using EPC90120 configured in a Buck converter operating at V_{IN} = 48 V to V_{OUT} = 12 V, f_{SW} = 1 MHz, L = 2.2 µH, I_{OUT} = 10 A
(3) Maximum turn-on dV/dt is defined by an internal resistor limiting the gate charging current

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Figure 4a: Timing Diagram Test Circuit

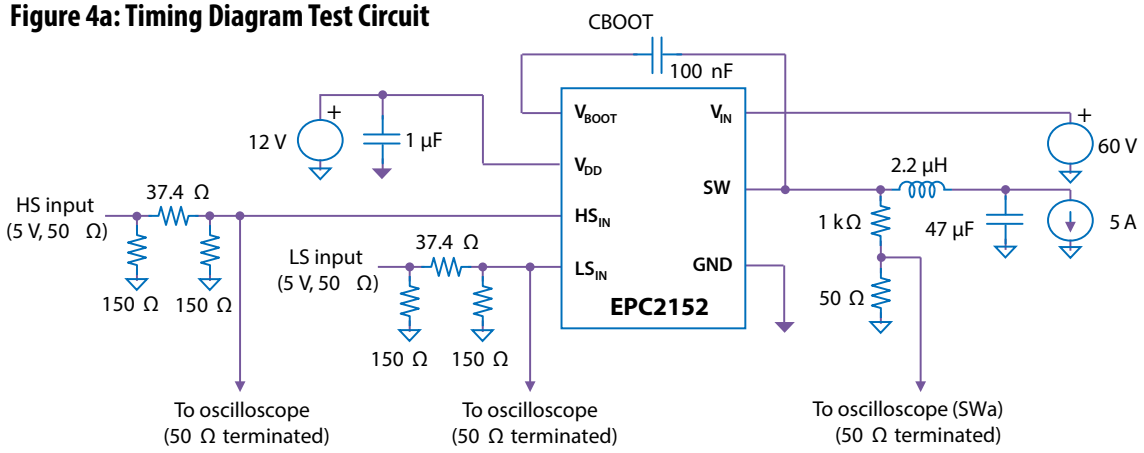


Figure 4b: Logic Input to Switch-node Waveforms

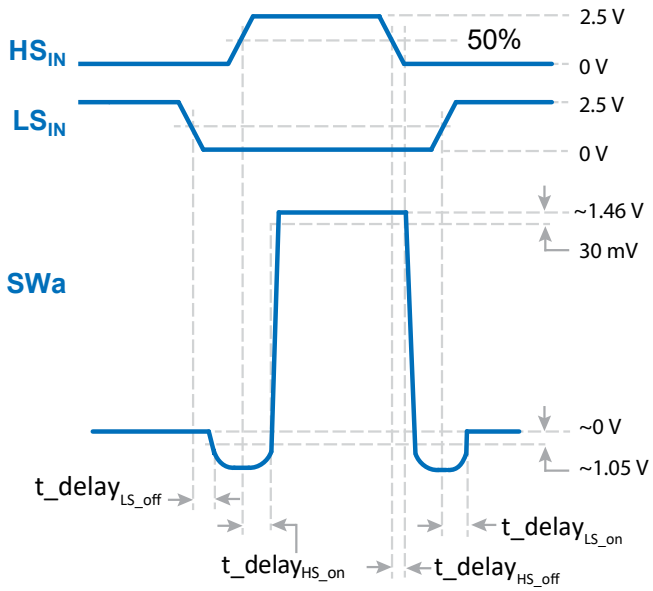


Table 1: Operational Truth Table

Truth Table					
V_{DD}	V_{BOOT} –SW	HS_{IN}	LS_{IN}	HS FET	LS FET
<UVLO	–	–	–	OFF	OFF
>UVLO	<UVLO	–	0	OFF	OFF
		–	1	OFF	ON
>UVLO		0	0	OFF	OFF
		0	1	OFF	ON
		1	0	ON	OFF
		1	1	OFF	

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Application Information

General Description

The EPC2152 ePower™ Stage IC integrates a half-bridge gate driver with internal high side and low side FETs. Integration is implemented using EPC's proprietary GaN IC technology. The monolithic chip integrates input logic interface, level shifting, bootstrap charging and gate drive buffer circuits for controlling the high side and low side eGaN output FETs, configured as a half-bridge power stage.

Synchronous bootstrap FET

The IC uses a synchronous bootstrap FET between V_{DD} and V_{BOOT} to charge the bootstrap capacitor. This bootstrap FET is activated only after the LS power FET is turned on, to avoid overcharging the bootstrap capacitor during deadtimes, when the switch-node voltage can be negative. The use of a GaN FET in the charging path eliminates reverse recovery and reduces power dissipation. Another advantage of the synchronous bootstrap FET is the lower voltage drop of approximately 100 mV compared to the 0.6 – 0.7 V of a typical Si bootstrap diode. As a result, the V_{BOOT} voltage is maintained close to the V_{DD} voltage, allowing the HS and LS gate drive circuits to have similar gate drive currents and dynamic performance.

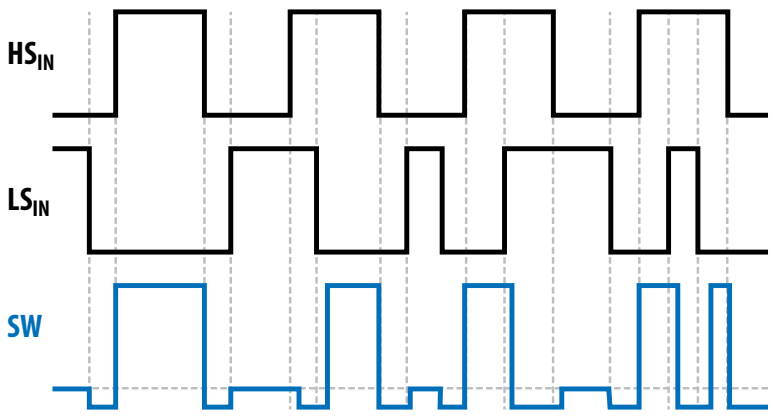
Protection Circuits

The EPC2152 integrates driver protection and under voltage lockout (UVLO) circuits for V_{DD} and V_{BOOT}. These protection circuits allow for the proper operation of the driver as shown in Table 1.

Separate and independent high side (HS_{IN}) and low side (LS_{IN}) logic control inputs allow external controllers to set the desired deadtimes for optimal operating efficiency. Cross conduction lockout logic commands both FETs off when both logic inputs are simultaneously high. Figure 5 shows how the logic inputs interact with each other. Here the timing diagram applies to HS FET and LS FET in half-bridge configuration and current is in the positive direction going out of the half-bridge.

When HSIN and LSIN are logic high at the same time, both HS FET and LS FET will shut off. A built-in lockout time of t_lockout is added to guarantee a minimum deadtime.

Figure 5: Input-to-Output Timing Diagram
(Current flowing OUT of SW node)



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Layout Guidelines

Monolithic integration of the half-bridge output FETs as well as their associated gate drivers significantly reduce parasitic common source inductance (CSI) and gate drive loop inductance. What remains is the high frequency power loop inductance, controlled by the PCB layout and the components in the loop, the DC input capacitors and the power stage. Experimental data confirmed that the efficiency curves can be impacted by as much as 4% depending on the power loop inductance varying from 0.4 nH to 3 nH. Another negative effect of excessive power loop inductance is the over-voltage spike at the SW node. Decreasing the high frequency loop inductance results in lower voltage overshoot, increased input voltage capability, and reduced EMI.

A recommended layout for the EPC2152 device is shown in Figure 6a based on **EPC90120 development board**. This PCB layout uses the concept of creating a low-profile magnetic field cancellation loop in a multilayer PCB as shown in Figure 6b. The design utilizes the first inner layer connected to the GND plane as a power loop return path. Separated only by a thin substrate, the top layer power loop and first inner layer current return path directly underneath generate opposing magnetic fields with induced currents that have opposite direction. The result is a cancellation of magnetic fields that translates into a reduction in parasitic inductance.

Figure 6a: Top View

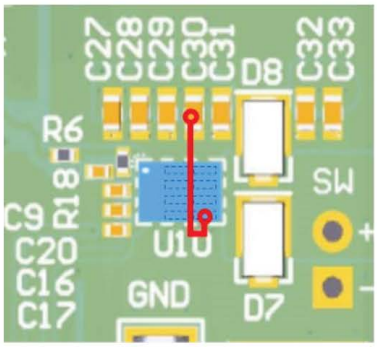
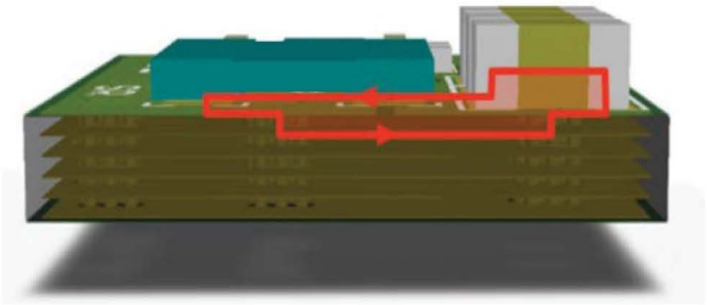


Figure 6b: Side View



Switching Speed

The EPC2152 device is tuned to switch at around 1.5 ns at 48 V V_{IN} to minimize output FET switching losses while keeping the voltage overshoot at the SW pin within an acceptable level. Using the recommended layout guidelines, shown in Figure 6, the parasitic loop inductance can be reduced to less than 0.2 nH, as demonstrated in **EPC90120 development board**.

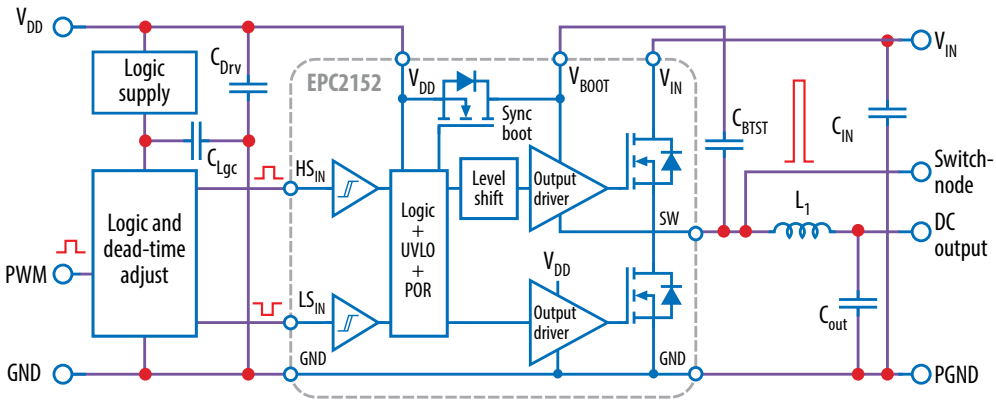
EPC90120 Development Board

To simplify the evaluation of EPC2152, EPC offers the EPC90120 development board. A photo with a top view of the board and its functional block diagram are shown in Figure 7. The board can be easily configured to operate the power stage in either a buck or boost converter. The layout supports optimal switching performance using the recommended layout guideline. And various probe points are included to facilitate waveforms and efficiency measurement.

Figure 7a: EPC90120 Development Board
(see EPC90120 Quick Start Guide for details)



Figure 7b: EPC90120 Functional Block Diagram



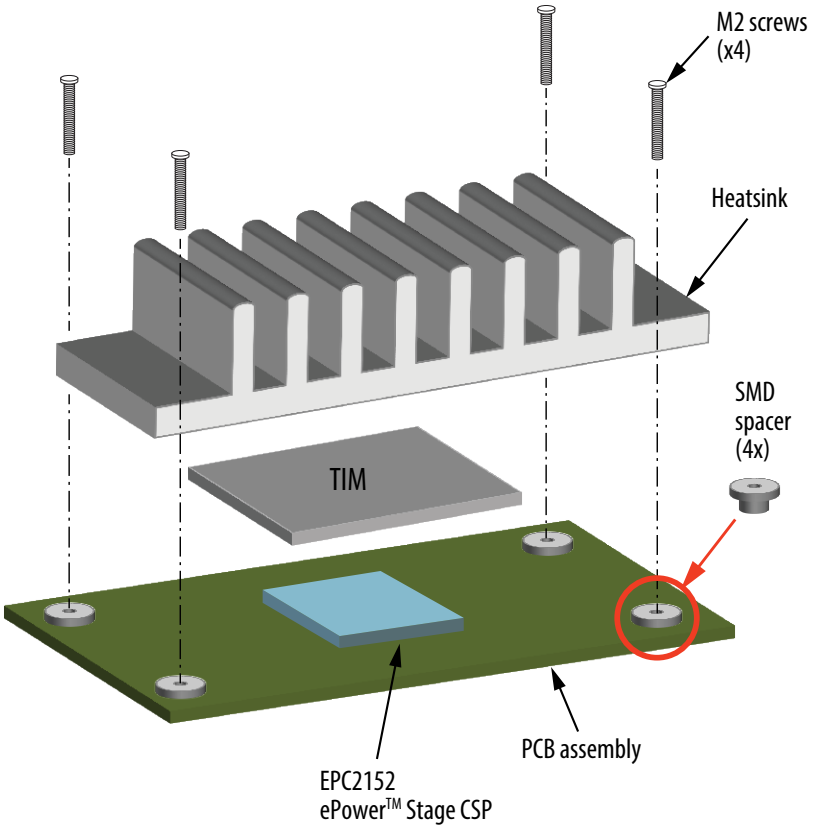
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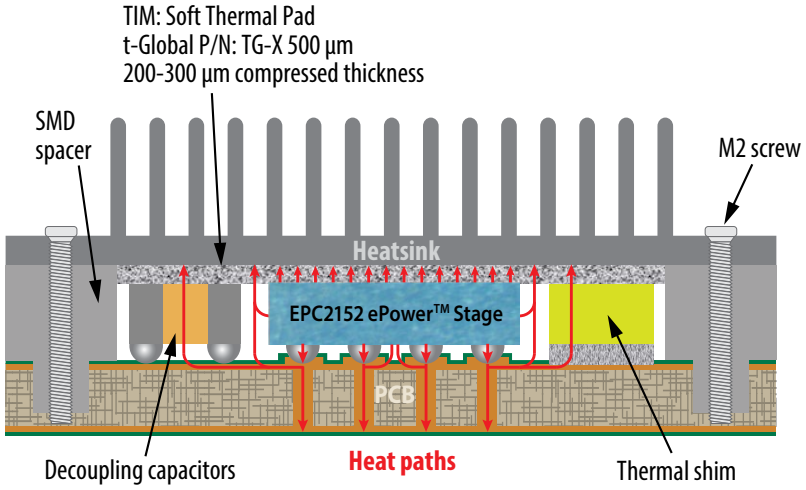
Load Current Rating

The Power Stage Load Current listed in this datasheet is defined as the load current of a Buck converter using EPC2152 that results in a device case temperature of 100°C (assuming 400 LFM of forced cooling and no heatsink). The data is based on experimental measurements of the EPC90120 development board configured as a Buck converter with V_{IN} = 48 V, V_{OUT} = 12 V, L = 2.2 µH, and 1 MHz of switching frequency. Without a heatsink installed, most of the energy dissipated within the EPC2152 device flows towards the PCB through the solder pads, and from there, to the ambient.

For higher current, dual sided cooling can be implemented by installing a heatsink as shown in Figure 8. With this configuration, heat can flow from the junction towards the solder bumps and the board, or in the opposite direction, to the case and heatsink. This dual heat flow path translates into lower thermal resistance and therefore lower junction temperature for the same power dissipation. To maximize heat dissipation to the heatsink, a thin thermal interface material (TIM) with high-thermal conductivity, is recommended. More details and recommended part numbers can be found in the Thermal Considerations sections of the **EPC90120 Quick Start Guide**.

Figure 8: Thermal Concept of Dual Sided Cooling



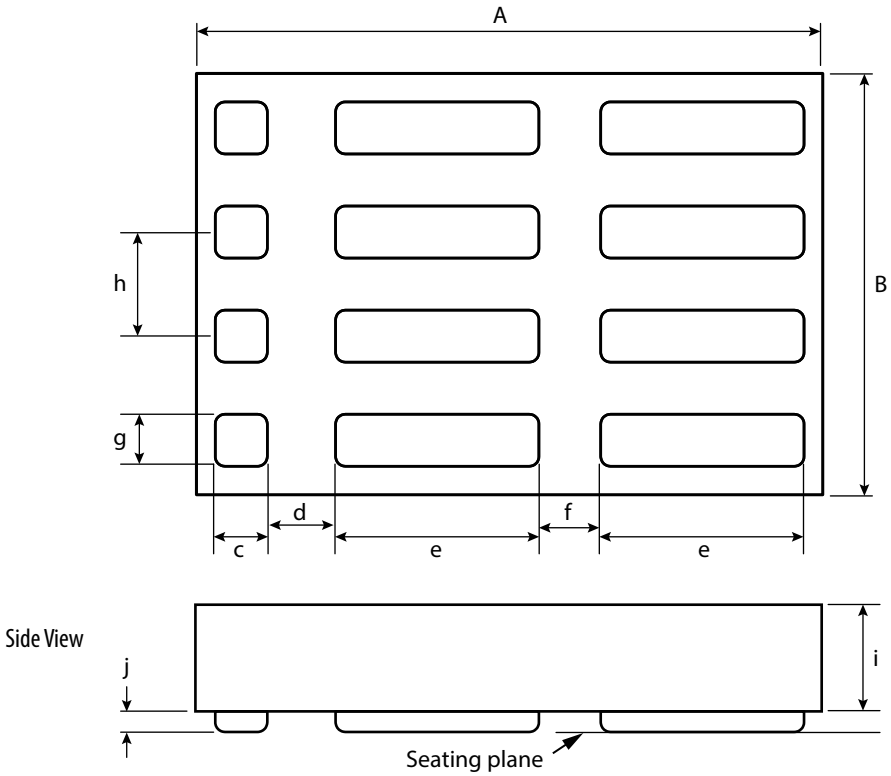


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Packaging information

DIE OUTLINE - PAD VIEW

(All dimensions in µm)



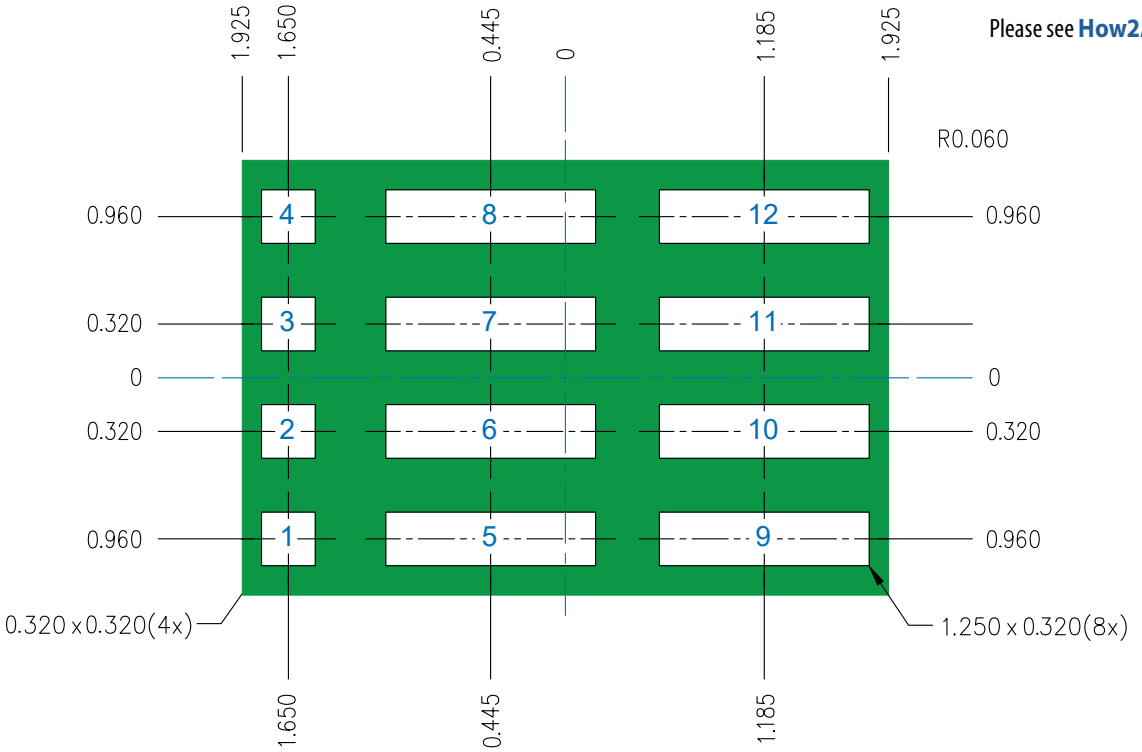
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	3820	3850	3880
B	2560	2590	2620
c		320	
d		420	
e		1250	
f		380	
g		320	
h		640	
i	493	518	543
j	108	120	132

RECOMMENDED SOLDER MASK

(All dimensions in mm)

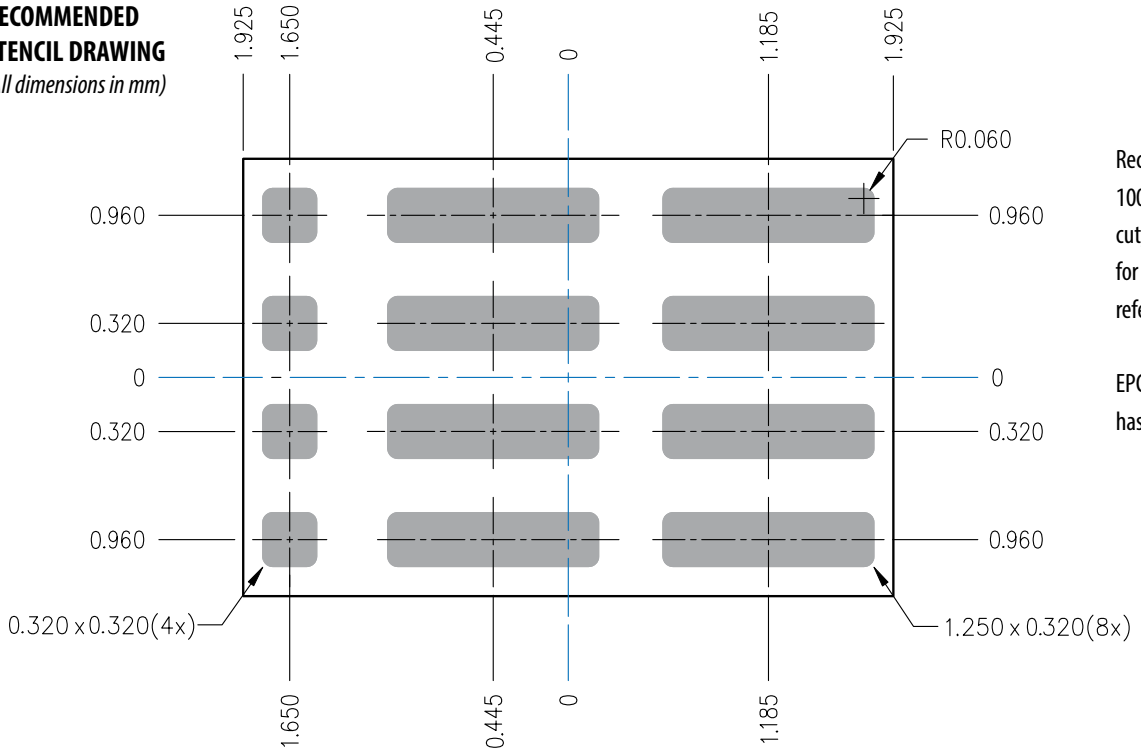
This land pattern recommendation is solder-mask defined (SMD).

Please see **How2AppNote 008** for details.



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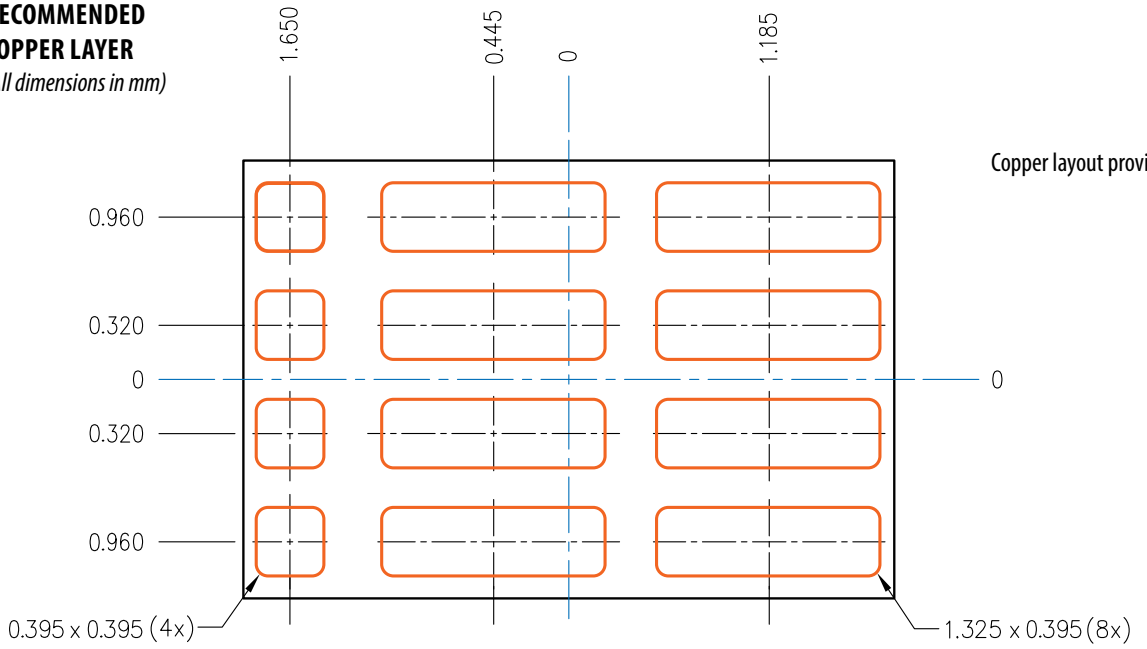
RECOMMENDED STENCIL DRAWING
(All dimensions in mm)



Recommended stencil should be 100 µm (4 mil) thick, must be laser cut, openings per drawing. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

EPC has tested this stencil design and has not found any scooping issues.

RECOMMENDED COPPER LAYER
(All dimensions in mm)

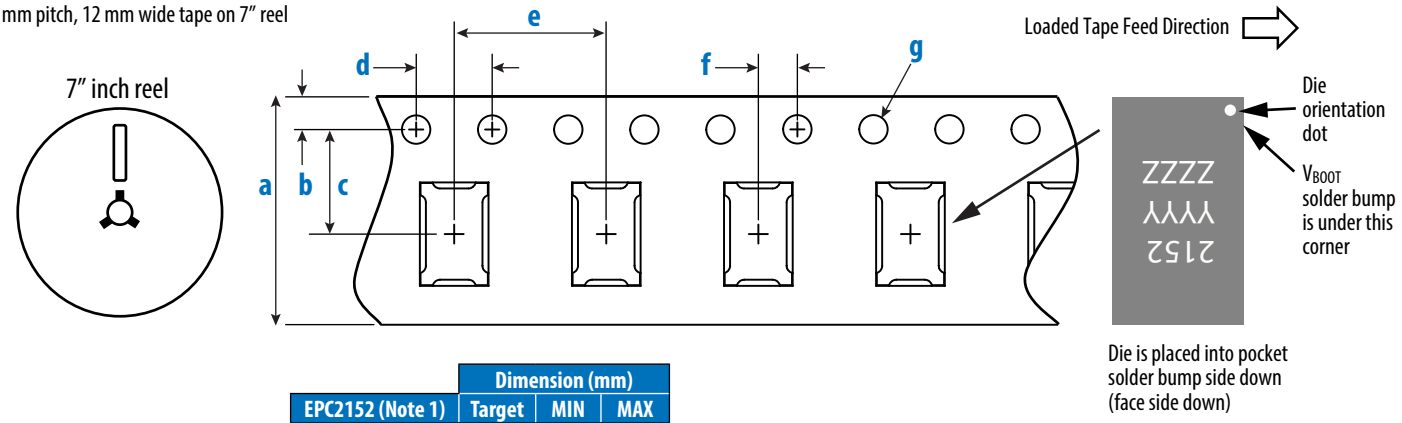


Copper layout provided as a typical example layout.

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TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7″ reel

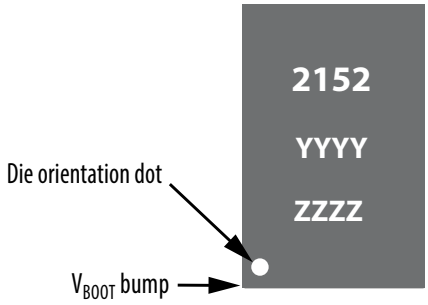


EPC2152 (Note 1)	Dimension (mm) Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE MARKINGS



Part Number	Laser Markings Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2152	2152	YYYY	ZZZZ

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