LatticeECP3 I/O Protocol Evaluation Board & ADC-DAC Interface Card

I/O Protocol Evaluation Board

The LatticeECP3 IO Protocol Evaluation Board provides a convenient platform to evaluate, test and debug user designs and IP cores targeted for the LatticeECP3 FPGA. The LatticeECP3 I/Os are connected to a rich variety of both generic and application-specific interfaces.

Front: I/O Protocol Board

Back: I/O Protocol Board

Some common uses for the LatticeECP3 IO Protocol Evaluation board include:

- Applications requiring large DDR3 memory width and depth
- High-speed parallel ADC/DAC Interface
- SERDES data transfer with external devices
- 1000base-T PHY/RJ45 networking
- A single-board computer system
- A platform for evaluating the Input/Output (I/O) characteristics of the FPGA
- A platform for evaluation and development with Lattice IP cores

Board Features

- SPI Serial Flash device included for low-cost, non-volatile LatticeECP3 configuration storage
- Two 64-bit DDR3 DIMM module sockets
- Tri-speed (10/100/1000 Mbit) Ethernet PHY with RJ-45 (includes 12 core magnetics)
- USB 2.0 transceiver
- Built-in USB 2.0 download for LatticeECP3 and ispPAC® bitstreams.
- Also includes ispDOWNLOAD™ JTAG headers for LatticeECP3, ispPAC, and MachXO™ bitstreams
- High-speed HMZD connector with 80 differential pair connections and selectable VTT voltage
- 8-pin DIP switch and three user-definable debounced pushbuttons
- Discrete LEDs and 7-segment LED
- LCD module connector
- Prototyping areas with 125 spare test point I/O pins
- 1 selectable user I/O bank voltage with access to 2 VREF test points
- Logic analyzer probe connection
- 5 pairs of high-speed differential I/O using SMA connectors
- 5 crystal oscillators
- 2 selectable high-speed differential external clock sources with PLL feed back inputs
- 4 channels (1 quad) of differential SERDES (TX and RX) using SMA connectors
- 1 high-current high-speed I/O connection using an SMA connector
- 3.3V, 2.5V, 1.5V, 1.2V and DDR3 voltages are generated from a single 12V power source
- 3 fixed or adjustable DDR3 reference voltages
- 1 Mbit serial EEPROM for general data storage over I2C bus
- Power Manager II ispPAC-POWR1220AT8 chip for monitoring input power and regulator outputs to be within nominal tolerance with programmable trims
- ispVM™ System programming support
- Multi-board JTAG programming capability and sysCONFIG™ connector

Downloads

Default Programming Files	

ADC-DAC Interface Card

The **ADC-DAC interface card** connects to the HMZD connector on the IO protocol board, and has two connectors that match ADC and DAC boards from TI.

ADC-DAC interface card

Ordering Information

Order now on the **Lattice online store:**

LatticeECP3 IO Protocol Board - **LFE3-150EA-IO-EVN**

ADC-DAC Interface Card - **LFE3-ADC-DAC-EVN**

For other ordering options contact your **local Lattice sales representative**.

I/O Protocol Board with ADC-DAC interface card