

LP2987/LP2988 Micropower, 200 mA Ultra Low-Dropout Voltage Regulator with Programmable Power-On Reset Delay; Low Noise Version Available (LP2988)

Check for Samples: [LP2987](#), [LP2988](#)

FEATURES

- Ultra Low Dropout Voltage
- Power-ON Reset Delay Requires Only One Component
- Bypass Pin for Reduced Output Noise (LP2988)
- Specified Continuous Output Current 200 mA
- Specified Peak Output Current > 250 mA
- SOIC-8 and VSSOP-8 Surface Mount Packages
- <2 μ A Quiescent Current when Shutdown
- Low Ground Pin Current at All Loads
- 0.5% Output Voltage Accuracy ("A" Grade)
- Wide Supply Voltage Range (16V Max)
- Overtemperature/overcurrent Protection
- -40°C to +125°C Junction Temperature Range

APPLICATIONS

- Cellular Phone
- Palmtop/Laptop Computer
- Camcorder, Personal Stereo, Camera

DESCRIPTION

The LP2987/8 are fixed-output 200 mA precision LDO voltage regulators with power-ON reset delay which can be implemented using a single external capacitor.

The LP2988 is specifically designed for noise-critical applications. A single external capacitor connected to the Bypass pin reduces regulator output noise.

Using an optimized VIP (Vertically Integrated PNP) process, these regulators deliver superior performance:

Dropout Voltage: 180 mV @ 200 mA load, and 1 mV @ 1 mA load (typical).

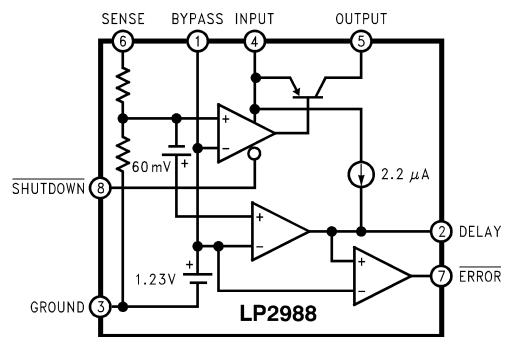
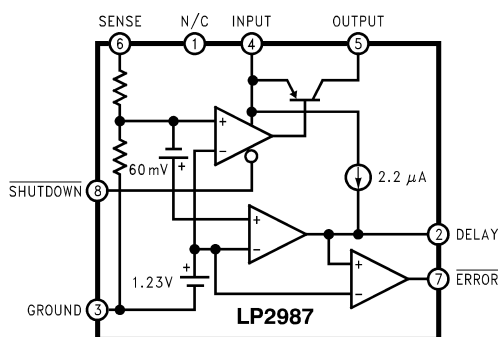
Ground Pin Current: 1 mA @ 200 mA load, and 200 μ A @ 10 mA load (typical).

Sleep Mode: The LP2987/8 draws less than 2 μ A quiescent current when shutdown pin is held low.

Error Flag/Reset: The error flag goes low when the output drops approximately 5% below nominal. This pin also provides a power-ON reset signal if a capacitor is connected to the DELAY pin.

Precision Output: Standard product versions of the LP2987 and LP2988 are available with output voltages of 5.0V, 3.8V, 3.3V, 3.2V, 3.0V, or 2.8V, with specified accuracy of 0.5% ("A" grade) and 1% (standard grade) at room temperature.

Block Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1999–2013, Texas Instruments Incorporated

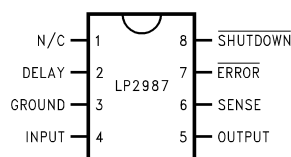
Connection Diagram (LP2987)

Figure 1. Top View
SOIC-8/VSSOP-8 Package
Surface Mount Packages
 See Package Drawing Number D0008A/DGK0008A

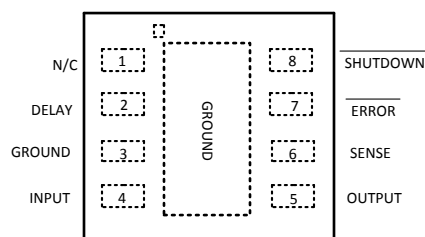


Figure 2. Top View
8-Lead WSON Surface Mount Package
 See Package Drawing Number NGN0008A

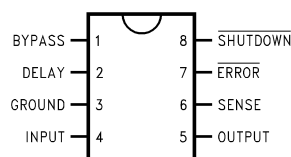
Connection Diagram (LP2988)

Figure 3. Top View
SOIC-8/VSSOP-8 Package
Surface Mount Packages
 See Package Drawing Number D0008A/DGK0008A

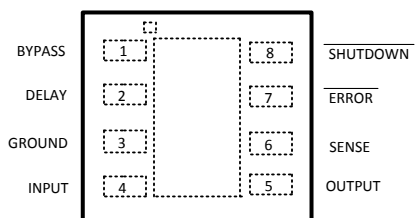


Figure 4. Top View
8-Lead WSON Surface Mount Package
 See Package Drawing Number NGN0008A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾⁽²⁾

Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	–40°C to +125°C
Lead Temperature (Soldering, 5 seconds)	260°C
ESD Rating ⁽³⁾	2 kV
Power Dissipation ⁽⁴⁾	Internally Limited
Input Supply Voltage (Survival)	–0.3V to +16V
Input Supply Voltage (Operating)	2.1V to +16V
Shutdown Pin	–0.3V to +16V
Sense Pin	–0.3V to +6V
Output Voltage (Survival) ⁽⁵⁾	–0.3V to +16V
I _{OUT} (Survival)	Short Circuit Protected
Input-Output Voltage (Survival) ⁽⁶⁾	–0.3V to +16V

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (3) The ESD rating of the Bypass pin is 500V (LP2988 only). The ESD rating of the V_{IN} pin is 1kV and the Delay pin is ESD rated at 1.5kV.
- (4) The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA} , and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using:

$$P(MAX) = \frac{T_J(MAX) - T_A}{\theta_{JA}}$$
The value of θ_{JA} for the SOIC-8 (D) package is 160°C/W, and the VSSOP-8 (DGK) package is 200°C/W. The value θ_{JA} for the WSON (NGN) package is specifically dependent on PCB trace area, trace material, and the number of layers and thermal vias. For improved thermal resistance and power dissipation for the WSON package, refer to Application Note AN-1187 (literature number [SNOA401](#)). Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
- (5) If used in a dual-supply system where the regulator load is returned to a negative supply, the LM2987/8 output must be diode-clamped to ground.
- (6) The output PNP structure contains a diode between the V_{IN} and V_{OUT} terminals that is normally reverse-biased. Forcing the output above the input will turn on this diode and may induce a latch-up mode which can damage the part (see [APPLICATION HINTS](#)).

ELECTRICAL CHARACTERISTICS

Limits in standard typeface are for T_J = 25°C, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: V_{IN} = V_O(NOM) + 1V, I_L = 1 mA, C_{OUT} = 4.7 µF, C_{IN} = 2.2 µF, V_{SD} = 2V.

Symbol	Parameter	Conditions	Typical	LM2987/8AI-X.X ⁽¹⁾		LM2987/8I-X.X ⁽¹⁾		Units
				Min	Max	Min	Max	
ΔV _O	Output Voltage Tolerance	0.1 mA < I _L < 200 mA		–0.5	0.5	–1.0	1.0	%V _{NOM}
				–0.8	0.8	–1.6	1.6	
				–1.8	1.8	–2.8	2.8	
ΔV _O /ΔV _{IN}	Output Voltage Line Regulation	V _O (NOM) + 1V ≤ V _{IN} ≤ 16V	0.007		0.014		0.014	%/V
					0.032		0.032	

- (1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for $T_J = 25^\circ\text{C}$, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_O(\text{NOM}) + 1\text{V}$, $I_L = 1\text{ mA}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, $V_{S/D} = 2\text{V}$.

Symbol	Parameter	Conditions	Typical	LM2987/8AI-X.X ⁽¹⁾		LM2987/8I-X.X ⁽¹⁾		Units
				Min	Max	Min	Max	
V _{IN} –V _O	Dropout Voltage ⁽²⁾	I _L = 100 μA	1		2.0		2.0	mV
					3.5		3.5	
		I _L = 75 mA	90		120		120	
					170		170	
		I _L = 200 mA	180		230		230	
					350		350	
I _{GND}	Ground Pin Current	I _L = 100 μA	100		120		120	μA
					150		150	
		I _L = 75 mA	500		800		800	
					1400		1400	mA
		I _L = 200 mA	1		2.1		2.1	
					3.7		3.7	
	V _{S/D} < 0.3V	0.05		1.5		1.5	μA	
I _O (PK)	Peak Output Current	V _{OUT} ≥ V _O (NOM) – 5%	400	250		250		mA
I _O (MAX)	Short Circuit Current	R _L = 0 (Steady State) ⁽³⁾	400					
e _n	LP2987 Output Noise Voltage (RMS)	BW = 300 Hz to 50 kHz, V _{OUT} = 3.3V C _{OUT} = 10 μF	100					μV(RMS)
	LP2988 Output Noise Voltage (RMS)	BW = 300 Hz to 50 kHz, V _{OUT} = 3.3V C _{OUT} = 10 μF C _{BYPASS} = .01 μF	20					
ΔV _{OUT} /ΔV _{IN}	Ripple Rejection	f = 1 kHz, C _{OUT} = 10 μF C _{BYP} = 0 (LP2988)	65					dB
ΔV _{OUT} /ΔT	Output Voltage Temperature Coefficient	⁽⁴⁾	20					ppm/°C
I _{DELAY}	Delay Pin Current Source		2.2	1.6	2.8	1.6	2.8	μA
		1.4		3.0	1.4	3.0		
SHUTDOWN INPUT								
V _{S/D}	S/D Input Voltage ⁽⁵⁾	V _H = O/P ON	1.4	1.6		1.6		V
		V _L = O/P OFF	0.55		0.18		0.18	
I _{S/D}	S/D Input Current	V _{S/D} = 0	0		–1		–1	μA
		V _{S/D} = 5V	5		15		15	

- (2) Dropout voltage is defined as the input to output differential at which the output voltage drops 100 mV below the value measured with a 1V differential.
- (3) See [TYPICAL PERFORMANCE CHARACTERISTICS](#) curves.
- (4) Temperature coefficient is defined as the maximum (worst-case) change divided by the total temperature range.
- (5) To prevent mis-operation, the Shutdown input must be driven by a signal that swings above V_H and below V_L with a slew rate not less than 40 mV/ μs (see [APPLICATION HINTS](#)).

ELECTRICAL CHARACTERISTICS (continued)

Limits in standard typeface are for $T_J = 25^\circ\text{C}$, and limits in **boldface type** apply over the full operating temperature range. Unless otherwise specified: $V_{IN} = V_{O(NOM)} + 1\text{V}$, $I_L = 1\text{ mA}$, $C_{OUT} = 4.7\text{ }\mu\text{F}$, $C_{IN} = 2.2\text{ }\mu\text{F}$, $V_{S/D} = 2\text{V}$.

Symbol	Parameter	Conditions	Typical	LM2987/8AI-X.X ⁽¹⁾		LM2987/8I-X.X ⁽¹⁾		Units
				Min	Max	Min	Max	
ERROR COMPARATOR								
I _{OH}	Output "HIGH" Leakage	V _{OH} = 16V	0.01		1		1	μA
					2		2	
V _{OL}	Output "LOW" Voltage	V _{IN} = V _O (NOM) – 0.5V, I _O (COMP) = 300 μA	150		220		220	mV
					350		350	
V _{THR} (MAX)	Upper Threshold Voltage		–4.6	–5.5 –7.7	–3.5 –2.5	–5.5 –7.7	–3.5 –2.5	%V _{OUT}
V _{THR} (MIN)	Lower Threshold Voltage		–6.6	–8.9 –13.0	–4.9 –3.3	–8.9 –13.0	–4.9 –3.3	
HYST	Hysteresis		2.0					

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $C_{OUT} = 4.7\ \mu\text{F}$, $C_{IN} = 2.2\ \mu\text{F}$, S/D is tied to V_{IN} , $V_{IN} = V_O(\text{NOM}) + 1\text{V}$, $I_L = 1\text{ mA}$.

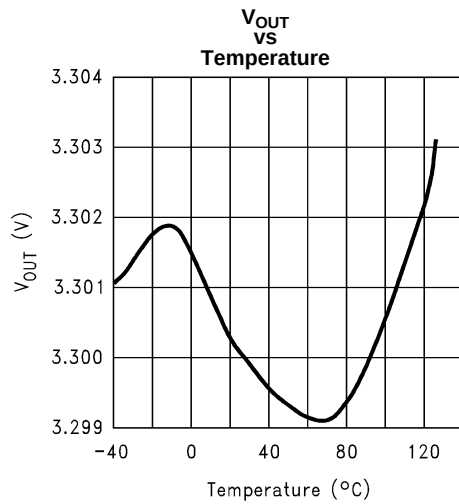


Figure 5.

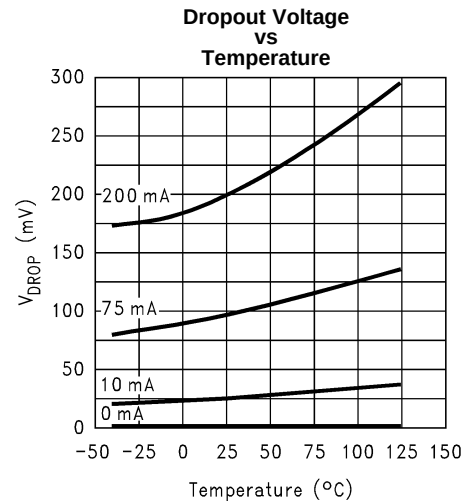


Figure 6.

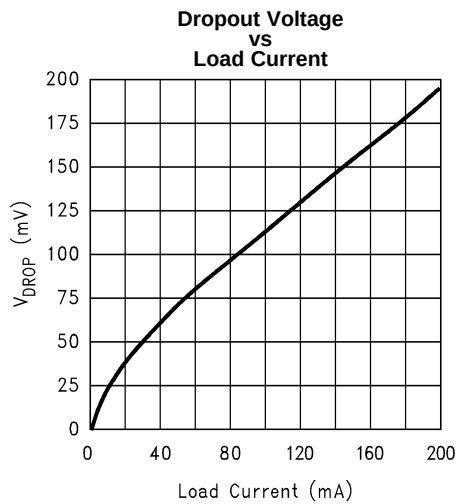


Figure 7.

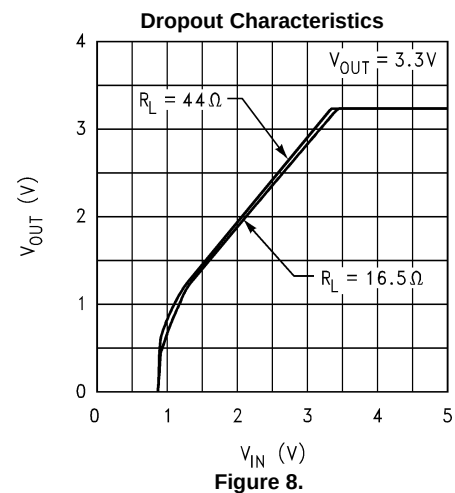


Figure 8.

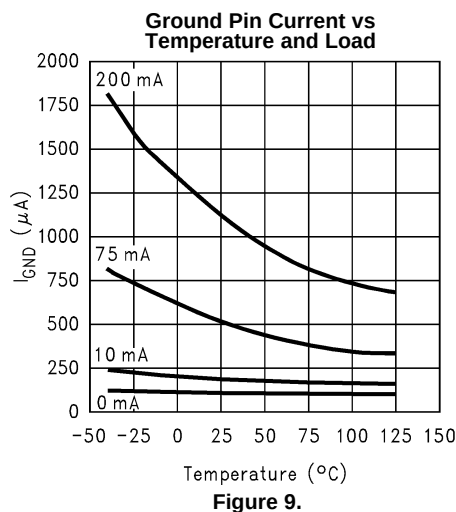


Figure 9.

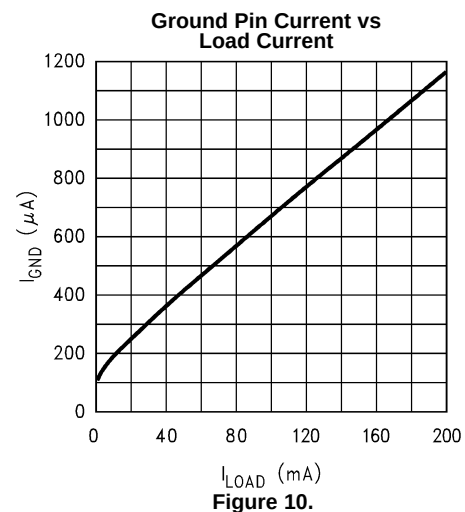


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $C_{OUT} = 4.7\ \mu\text{F}$, $C_{IN} = 2.2\ \mu\text{F}$, S/D is tied to V_{IN} , $V_{IN} = V_{O(NOM)} + 1\text{V}$, $I_L = 1\ \text{mA}$.

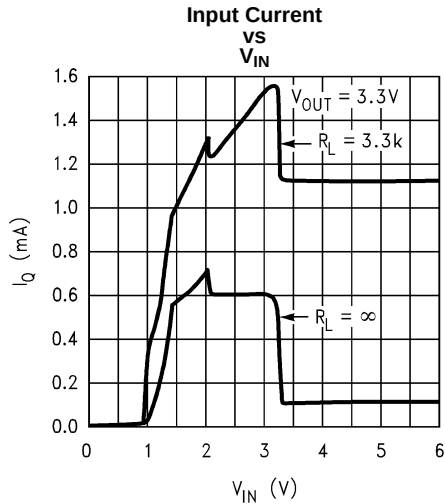


Figure 11.

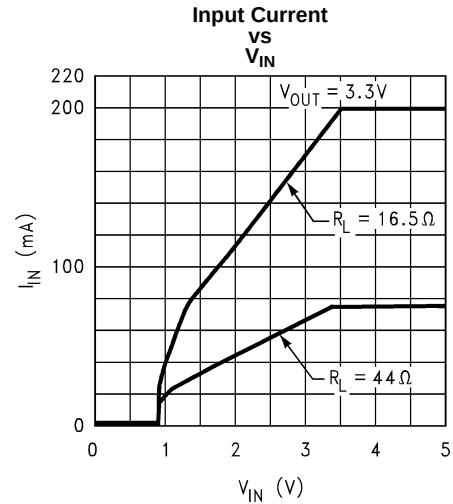


Figure 12.

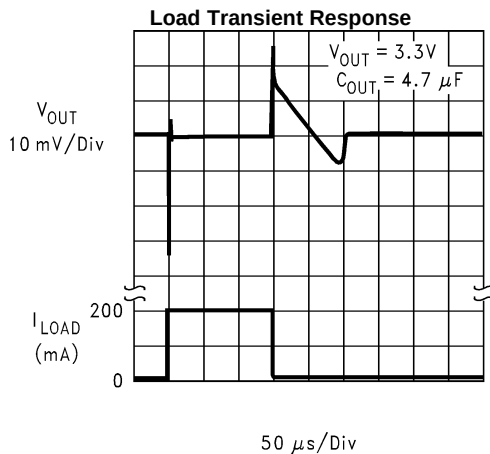


Figure 13.

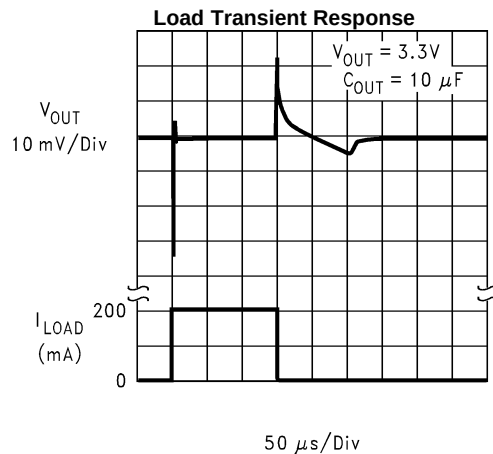


Figure 14.

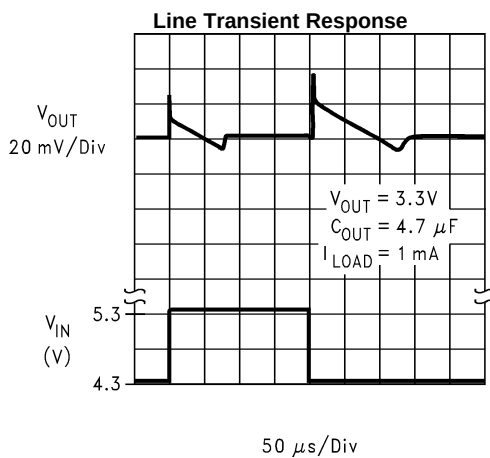


Figure 15.

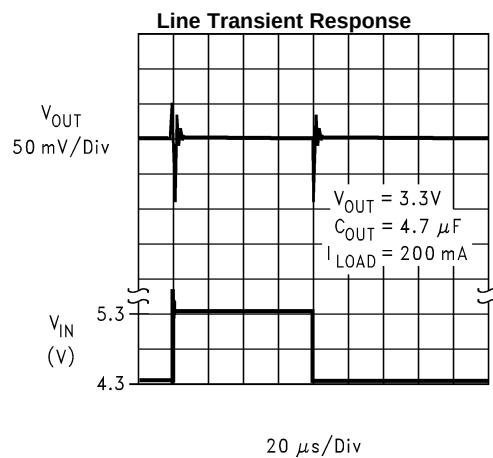
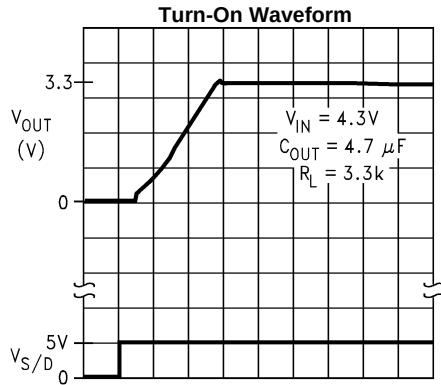


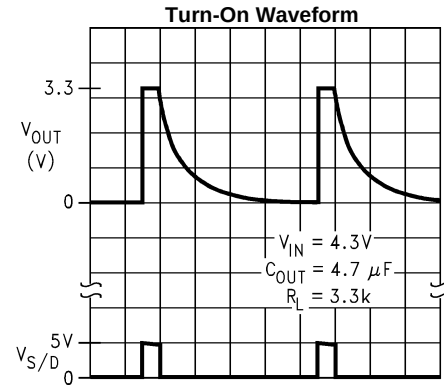
Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

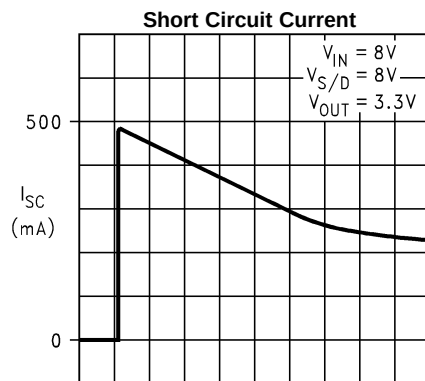
Unless otherwise specified: $T_A = 25^\circ\text{C}$, $C_{OUT} = 4.7\ \mu\text{F}$, $C_{IN} = 2.2\ \mu\text{F}$, S/D is tied to V_{IN} , $V_{IN} = V_O(\text{NOM}) + 1\text{V}$, $I_L = 1\ \text{mA}$.



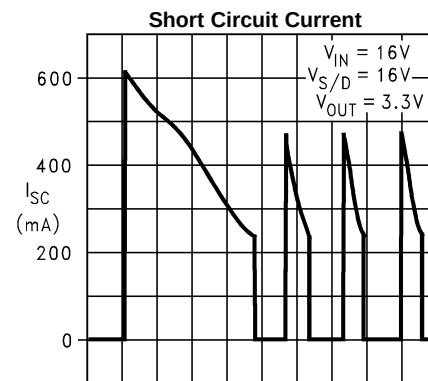
20 $\mu\text{s}/\text{Div}$
Figure 17.



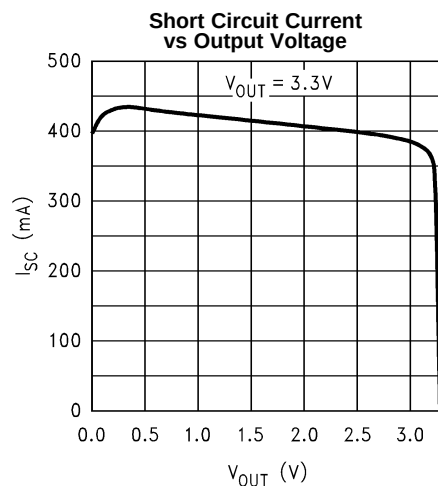
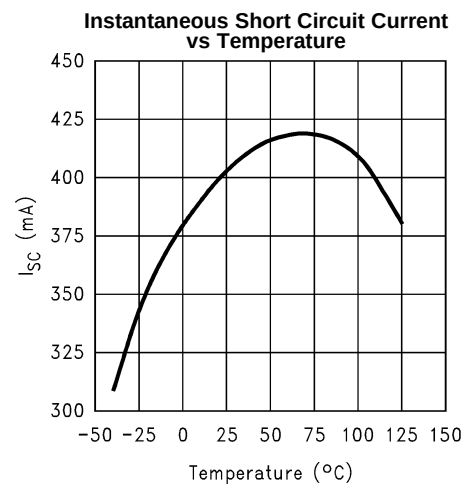
20 ms/Div
Figure 18.



500 ms/Div
Figure 19.



200 ms/Div
Figure 20.

**Figure 21.****Figure 22.**

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $C_{OUT} = 4.7\ \mu\text{F}$, $C_{IN} = 2.2\ \mu\text{F}$, S/D is tied to V_{IN} , $V_{IN} = V_{O(NOM)} + 1\text{V}$, $I_L = 1\ \text{mA}$.

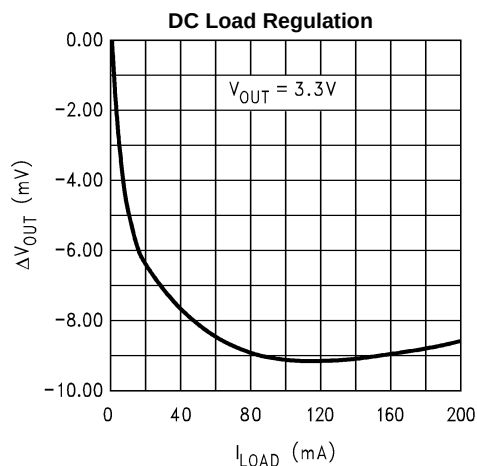


Figure 23.

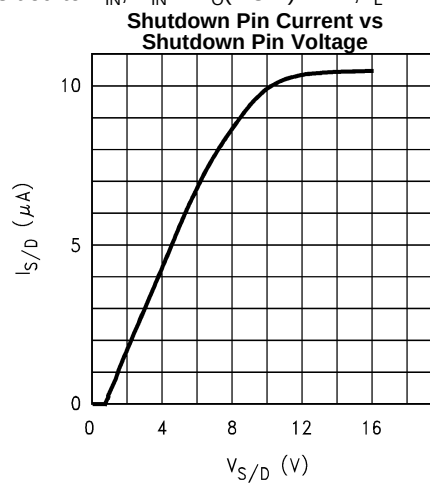


Figure 24.

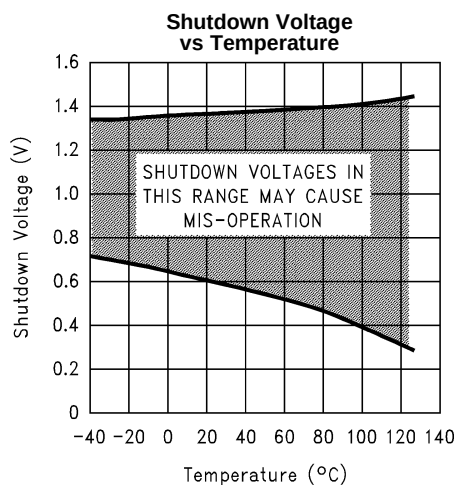


Figure 25.

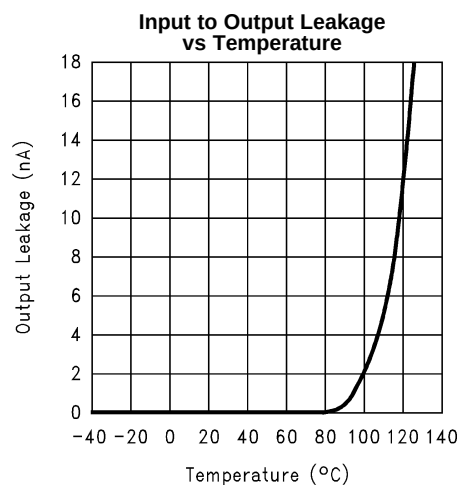


Figure 26.

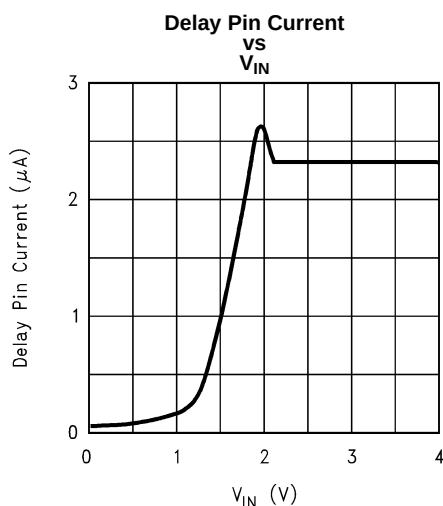


Figure 27.

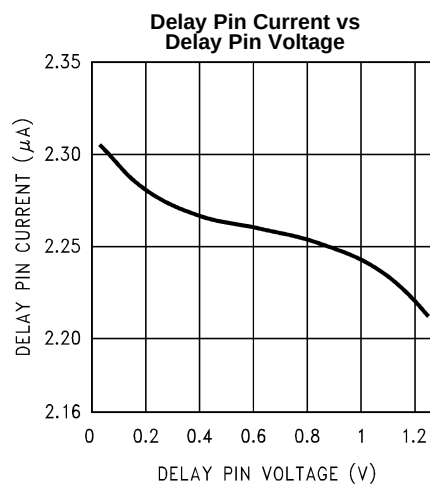
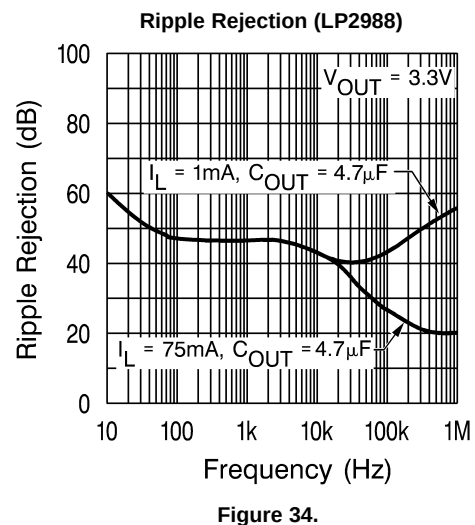
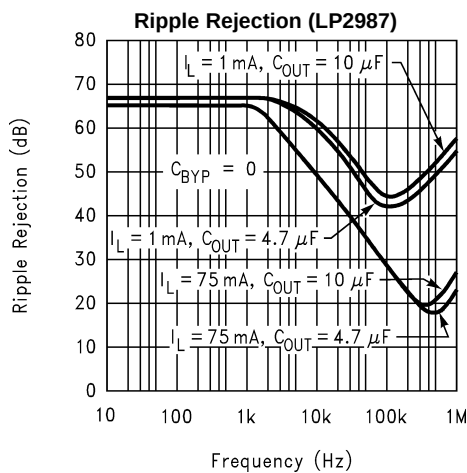
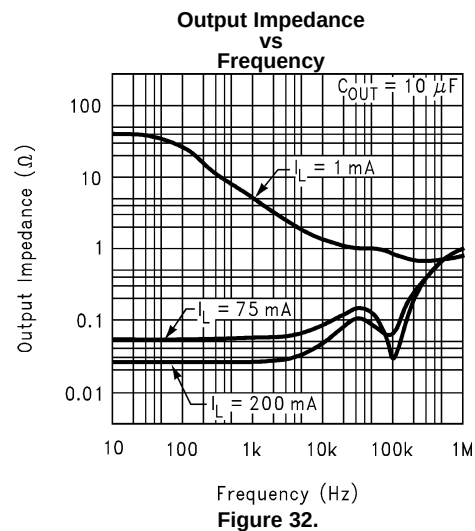
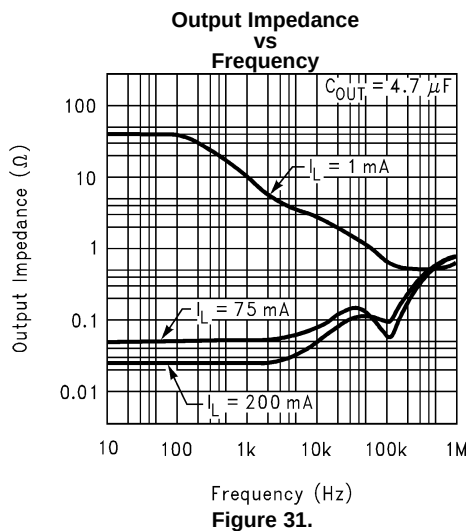
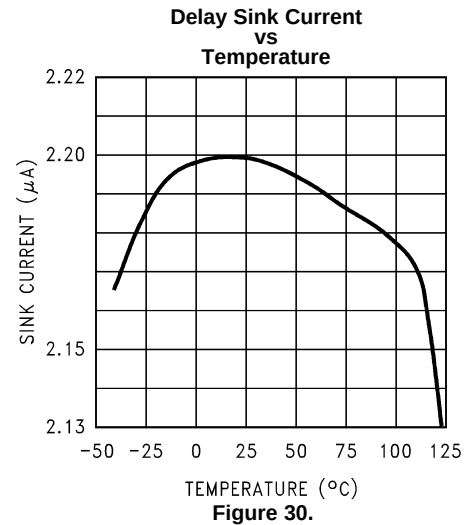
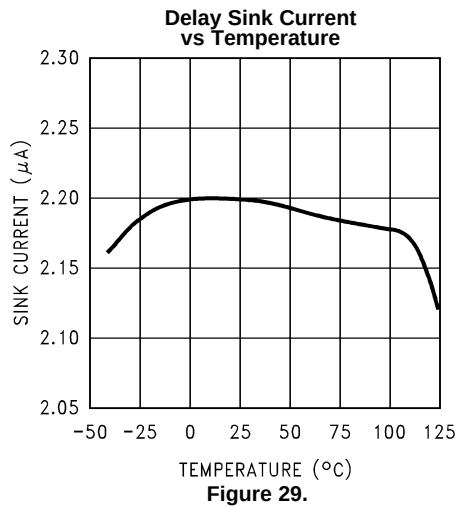


Figure 28.

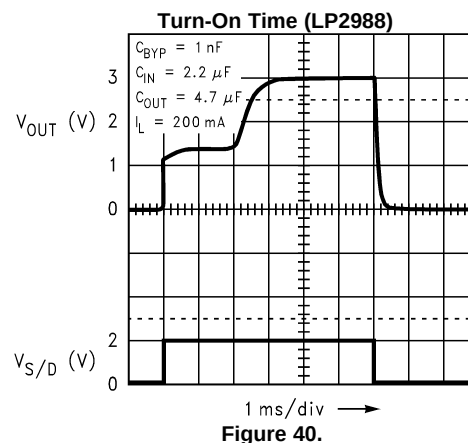
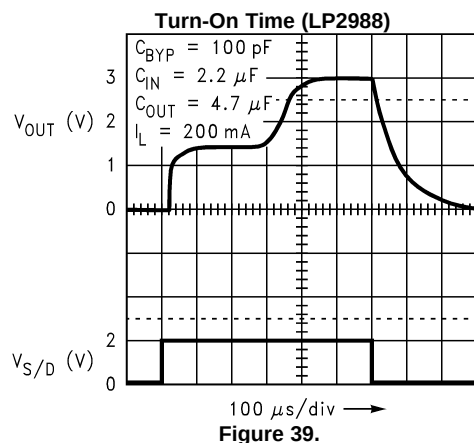
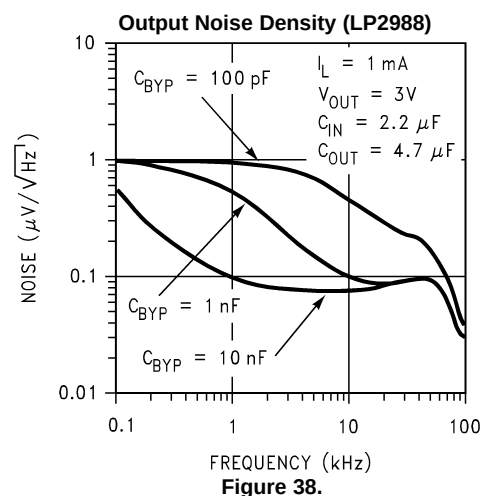
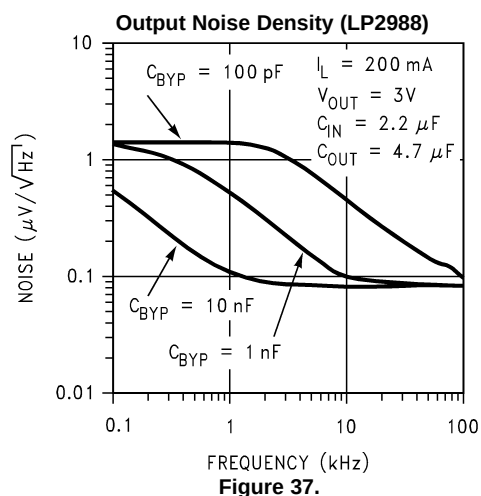
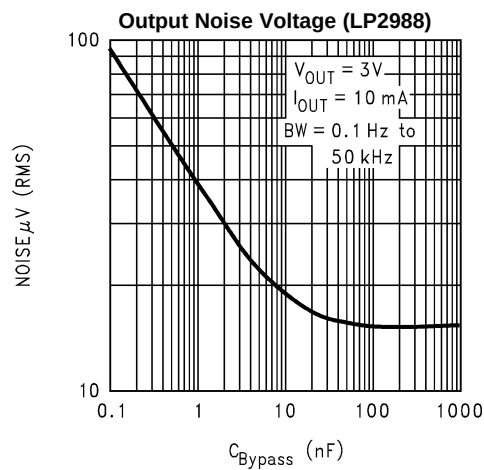
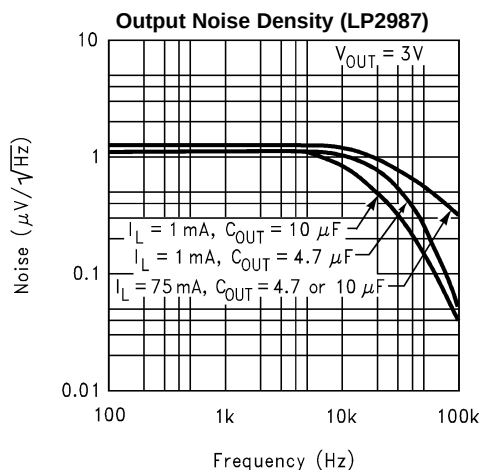
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $C_{OUT} = 4.7\ \mu\text{F}$, $C_{IN} = 2.2\ \mu\text{F}$, S/D is tied to V_{IN} , $V_{IN} = V_O(\text{NOM}) + 1\text{V}$, $I_L = 1\ \text{mA}$.



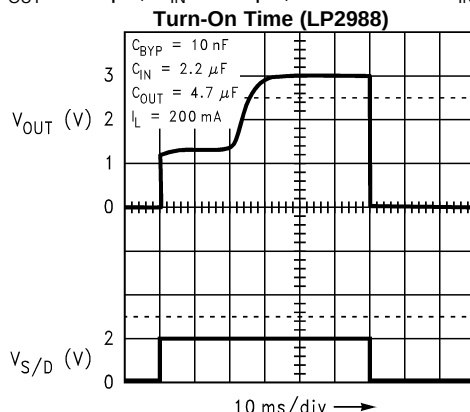
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $C_{OUT} = 4.7\ \mu\text{F}$, $C_{IN} = 2.2\ \mu\text{F}$, S/D is tied to V_{IN} , $V_{IN} = V_O(\text{NOM}) + 1\text{V}$, $I_L = 1\ \text{mA}$.



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified: $T_A = 25^\circ\text{C}$, $C_{OUT} = 4.7\ \mu\text{F}$, $C_{IN} = 2.2\ \mu\text{F}$, S/D is tied to V_{IN} , $V_{IN} = V_O(\text{NOM}) + 1\text{V}$, $I_L = 1\ \text{mA}$.

**Figure 41.**

BASIC APPLICATION CIRCUITS

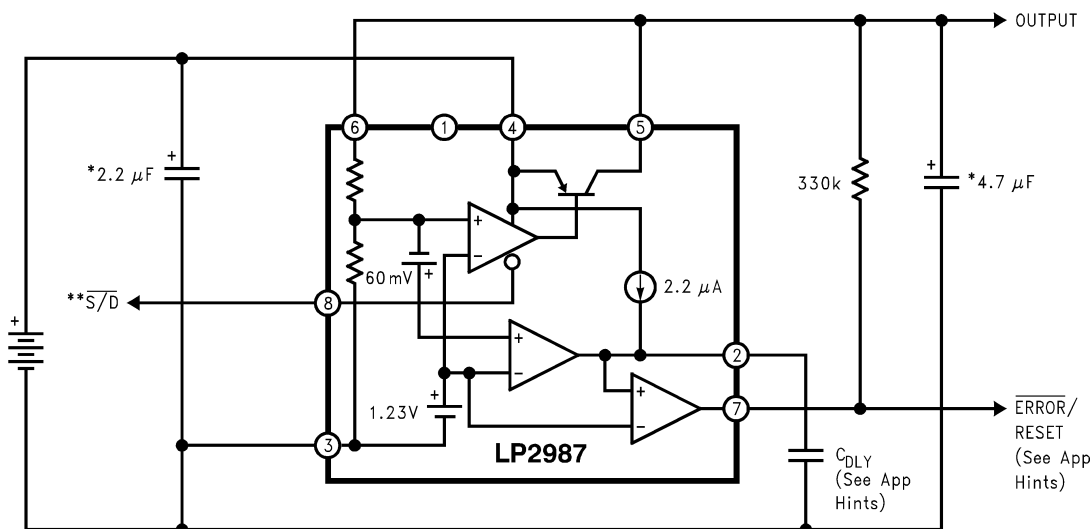
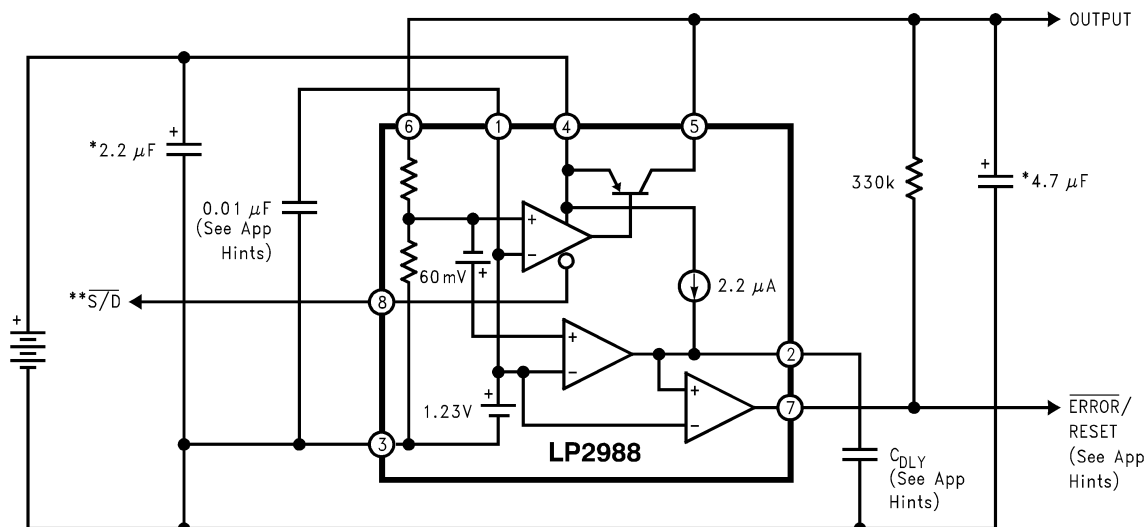


Figure 42.



*Capacitance value shown is minimum required to assure stability, but may be increased without limit. Larger output capacitor provides improved dynamic response.

**Shutdown must be actively terminated (see [APPLICATION HINTS](#)). Tie to INPUT (pin 4) if not used.

Figure 43.

APPLICATION HINTS

WSO Package Devices

The LP2987/LP2988 is offered in the 8 lead WSO surface mount package to allow for increased power dissipation compared to the SOIC-8 and the VSSOP-8. For details on thermal performance as well as mounting and soldering specifications, refer to Application Note AN-1187 (literature number [SNOA401](#)).

EXTERNAL CAPACITORS

As with any low-dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

INPUT CAPACITOR: An input capacitor ($\geq 2.2 \mu\text{F}$) is required between the LP2987/8 input and ground (amount of capacitance may be increased without limit).

This capacitor must be located a distance of not more than 0.5" from the input pin and returned to a clean analog ground. Any good quality ceramic or tantalum may be used for this capacitor.

OUTPUT CAPACITOR: The output capacitor must meet the requirement for minimum amount of capacitance and also have an appropriate E.S.R. (equivalent series resistance) value.

Curves are provided which show the allowable ESR range as a function of load current for 3V and 5V outputs.

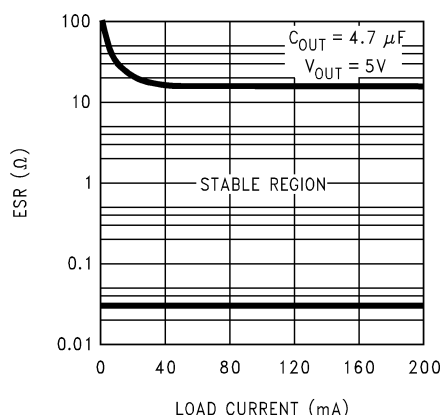


Figure 44. ESR Curves For 5V Output

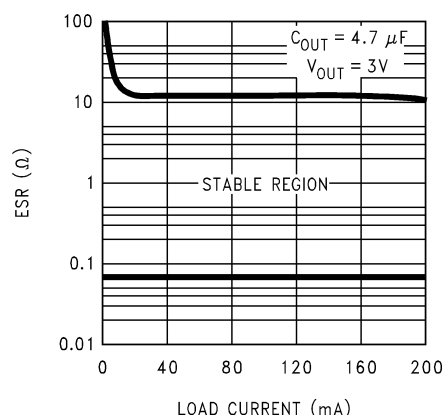


Figure 45. ESR Curves For 3V Output

IMPORTANT: The output capacitor must maintain its ESR in the stable region over the full operating temperature range of the application to assure stability.

The minimum required amount of output capacitance is $4.7 \mu\text{F}$. Output capacitor size can be increased without limit.

It is important to remember that capacitor tolerance and variation with temperature must be taken into consideration when selecting an output capacitor so that the minimum required amount of output capacitance is provided over the full operating temperature range. A good Tantalum capacitor will show very little variation with temperature, but a ceramic may not be as good (see next section).

The output capacitor should be located not more than 0.5" from the output pin and returned to a clean analog ground.

CAPACITOR CHARACTERISTICS

TANTALUM: A solid tantalum capacitor is the best choice for the output capacitor on the LM2987/8. Available from many sources, their typical ESR is very close to the ideal value required on the output of many LDO regulators.

Tantalums also have good temperature stability: a 4.7 μF was tested and showed only a 10% decline in capacitance as the temperature was decreased from +125°C to –40°C. The ESR increased only about 2:1 over the same range of temperature.

However, it should be noted that the increasing ESR at lower temperatures present in all tantalums can cause oscillations when marginal quality capacitors are used (where the ESR of the capacitor is near the upper limit of the stability range at room temperature).

CERAMIC: The ESR of ceramic capacitor can be low enough to cause an LDO regulator to oscillate: a 2.2 μF ceramic was measured and found to have an ESR of 15 m Ω .

If a ceramic capacitor is to be used on the LP2987/8 output, a 1 Ω resistor should be placed in series with the capacitor to provide a minimum ESR for the regulator.

A disadvantage of ceramic capacitors is that their capacitance varies a lot with temperature: Large ceramic capacitors are typically manufactured with the Z5U temperature characteristic, which results in the capacitance dropping by 50% as the temperature goes from 25°C to 80°C.

This means you have to buy a capacitor with twice the minimum C_{OUT} to assure stable operation up to 80°C.

ALUMINUM: The large physical size of aluminum electrolytics makes them unsuitable for most applications. Their ESR characteristics are also not well suited to the requirements of LDO regulators. The ESR of a typical aluminum electrolytic is higher than a tantalum, and it also varies greatly with temperature.

A typical aluminum electrolytic can exhibit an ESR increase of 50X when going from 20°C to –40°C. Also, some aluminum electrolytics can not be used below –25°C because the electrolyte will freeze.

POWER-ON RESET DELAY

A power-on reset function can be easily implemented using the LP2987/8 by adding a single external capacitor to the Delay pin. The Error output provides the power-on reset signal when input power is applied to the regulator.

The reset signal stays low for a pre-set time period after power is applied to the regulator, and then goes high (see Timing Diagram below).

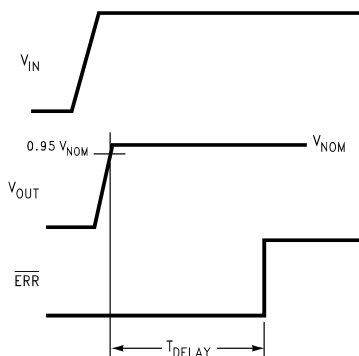
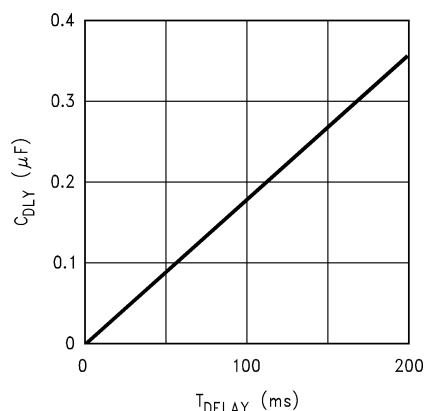


Figure 46. Timing Diagram for Power-Up

The external capacitor C_{DLY} sets the delay time (T_{DELAY}). The value of capacitor required for a given time delay may be calculated using the formula:

$$C_{\text{DLY}} = T_{\text{DELAY}} / (5.59 \times 10^5)$$

To simplify design, a plot is provided below which shows values of C_{DLY} versus delay time.

Figure 47. Plot of C_{DLY} vs T_{DELAY}

DETAILS OF ERR/RESET CIRCUIT OPERATION: (Refer to LP2987/8 Equivalent Circuit).

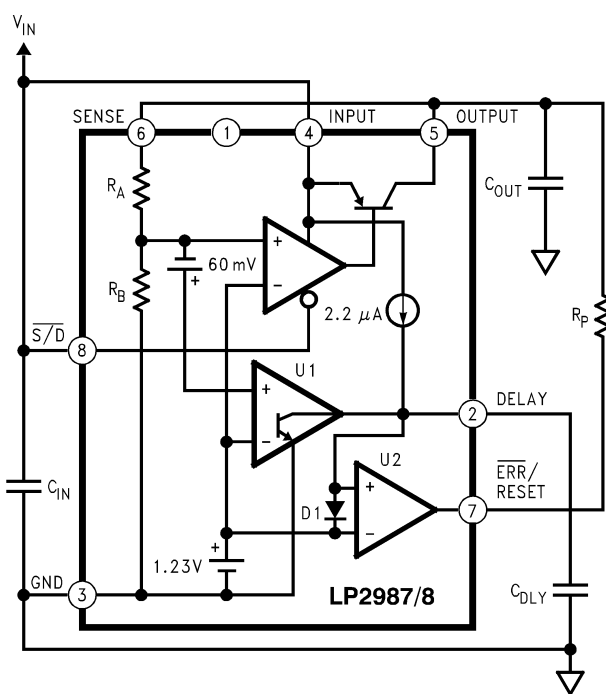


Figure 48. LP2987/8 Equivalent Circuit

The output of comparator U2 is the ERR/RESET flag. Since it is an open-collector output, it requires the use of a pull-up resistor (R_P). The 1.23V reference is tied to the inverting input of U2, which means that its output is controlled by the voltage applied to the non-inverting input.

The output of U1 (also an open-collector) will force the non-inverting input of U2 to go low whenever the LP2987/8 regulated output drops about 5% below nominal.

U1's inverting input is also held at 1.23V. The other input samples the regulated output through a resistive divider (R_A and R_B). When the regulated output is at nominal voltage, the voltage at the divider tap point will be 1.23V. If this voltage drops about 60 mV below 1.23V, the output of U1 will go low forcing the output of U2 low (which is the ERROR state).

Power-ON reset delay occurs when a capacitor (shown as C_{DLY}) is connected to the Delay pin. At turn-ON, this capacitor is initially fully discharged (which means the voltage at the Delay pin is 0V). The output of U1 keeps C_{DLY} fully discharged (by sinking the 2.2 μ A from the current source) until the regulator output voltage comes up to within about 5% of nominal. At this point, U1's output stops sinking current and the 2.2 μ A starts charging up C_{DLY} .

When the voltage across C_{DLY} reaches 1.23V, the output of U2 will go high (note that D1 limits the maximum voltage to about 2V).

SELECTING C_{DLY} : The maximum recommended value for this capacitor is 1 μ F. The capacitor must not have excessively high leakage current, since it is being charged from a 2.2 μ A current source.

Aluminum electrolytics can not be used, but good-quality tantalum, ceramic, mica, or film types will work.

SHUTDOWN INPUT OPERATION

The LP2987/8 is shut off by driving the Shutdown input low, and turned on by pulling it high. If this feature is not to be used, the Shutdown input should be tied to V_{IN} to keep the regulator output on at all times.

To assure proper operation, the signal source used to drive the Shutdown input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed as V_H and V_L , respectively (see [Electrical Characteristics](#)).

It is also important that the turn-on (and turn-off) voltage signals applied to the Shutdown input have a slew rate which is not less than 40 mV/ μ s.

CAUTION

The regulator output state can not be ensured if a slow-moving AC (or DC) signal is applied that is in the range between V_H and V_L .

REVERSE INPUT-OUTPUT VOLTAGE

The PNP power transistor used as the pass element in the LP2987/8 has an inherent diode connected between the regulator output and input.

During normal operation (where the input voltage is higher than the output) this diode is reverse-biased.

However, if the output is pulled above the input, this diode will turn ON and current will flow into the regulator output.

In such cases, a parasitic SCR can latch which will allow a high current to flow into V_{IN} (and out the ground pin), which can damage the part.

In any application where the output may be pulled above the input, an external Schottky diode must be connected from V_{IN} to V_{OUT} (cathode on V_{IN} , anode on V_{OUT}), to limit the reverse voltage across the LP2987/8 to 0.3V (see [Absolute Maximum Ratings](#)).

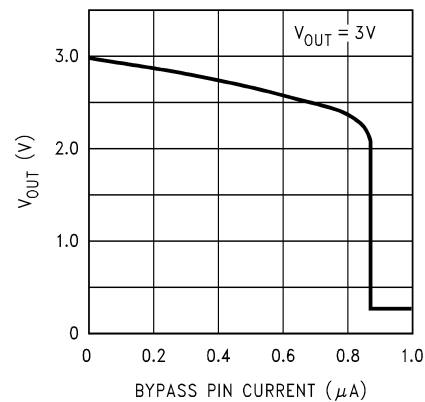
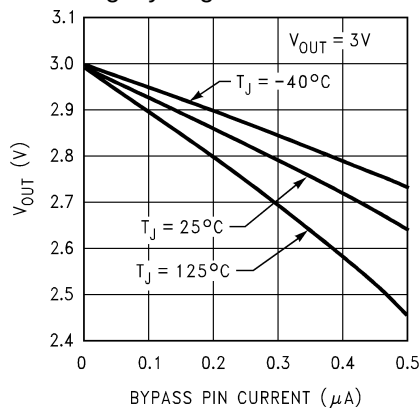
BYPASS CAPACITOR (LP2988)

The capacitor connected to the Bypass pin must have very low leakage. The current flowing out of the Bypass pin comes from the Bandgap reference, which is used to set the output voltage. Since the Bandgap circuit has only a few microamps flowing in it, loading effects due to leakage current will cause a change in the regulated output voltage.

Curves are provided which show the effect of loading the Bypass pin on the regulated output voltage.

Care must be taken to ensure that the capacitor selected for bypass will not have significant leakage current over the operating temperature range of the application.

A high quality ceramic capacitor which uses either NPO or COG type dielectric material will typically have very low leakage. Small surface-mount polypropylene or polycarbonate film capacitors also have extremely low leakage, but are slightly larger in size than ceramics.



REVISION HISTORY

Changes from Revision I (April 2013) to Revision J

Page

- Changed layout of National Data Sheet to TI format [18](#)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2987AILD-3.0/NOPB	ACTIVE	WSON	NGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L007A	Samples
LP2987AILD-5.0/NOPB	ACTIVE	WSON	NGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L009A	Samples
LP2987AILD-5.0/NOPB	ACTIVE	WSON	NGN	8	4500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L009A	Samples
LP2987AIMM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L44A	Samples
LP2987AIMX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2987A IM5.0	Samples
LP2987ILD-3.3/NOPB	ACTIVE	WSON	NGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L008A B	Samples
LP2987IM-3.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.0	Samples
LP2987IM-3.3/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.3	Samples
LP2987IM-5.0	NRND	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	2987I M5.0	
LP2987IM-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2987I M5.0	Samples
LP2987IMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L43B	Samples
LP2987IMM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L44B	Samples
LP2987IMMX-3.3/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L43B	Samples
LP2987IMX-3.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2987I M3.0	Samples
LP2987IMX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2987I M5.0	Samples
LP2988AIM-5.0	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	-40 to 125	2988A IM5.0	
LP2988AIM-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2988A IM5.0	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2988A1MM-2.8/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L01A	Samples
LP2988A1MM-3.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L49A	Samples
LP2988A1MM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L50A	Samples
LP2988A1MM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L51A	Samples
LP2988A1MX-3.3/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2988A IM3.3	Samples
LP2988ILD-3.8/NOPB	ACTIVE	WSO	NGN	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	L083A B	Samples
LP2988IM-5.0/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2988I M5.0	Samples
LP2988IMM-3.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L49B	Samples
LP2988IMM-3.3/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L50B	Samples
LP2988IMM-5.0	NRND	VSSOP	DGK	8	1000	TBD	Call TI	Call TI	-40 to 125	L51B	
LP2988IMM-5.0/NOPB	ACTIVE	VSSOP	DGK	8	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L51B	Samples
LP2988IMMX-3.0/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L49B	Samples
LP2988IMMX-3.3/NOPB	ACTIVE	VSSOP	DGK	8	3500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L50B	Samples
LP2988IMX-5.0/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	2988I M5.0	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

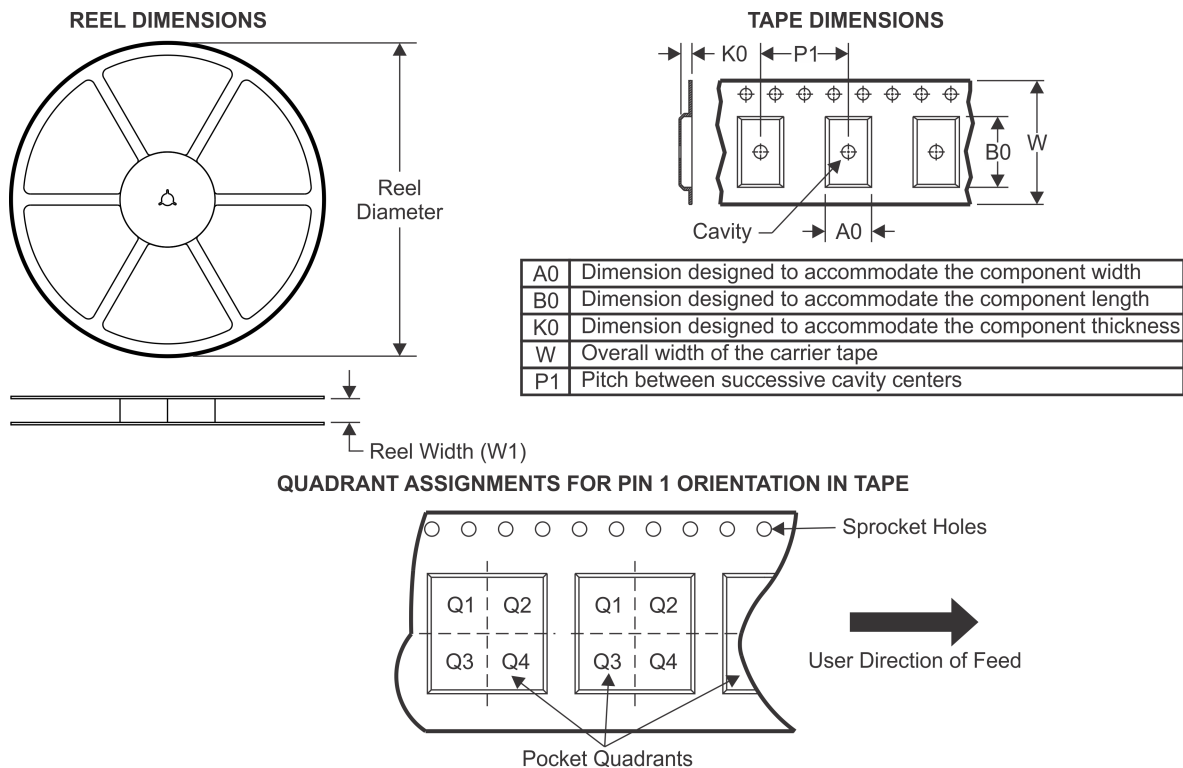
⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

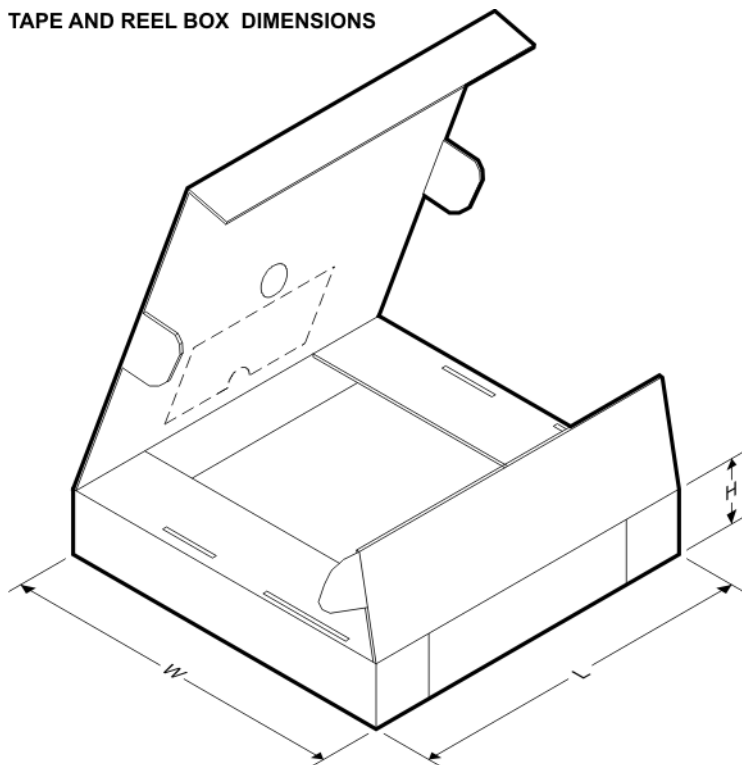
TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2987AILD-3.0/NOPB	WSO	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2987AILD-5.0/NOPB	WSO	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2987AILD-5.0/NOPB	WSO	NGN	8	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2987AIMM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2987AIMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2987ILD-3.3/NOPB	WSO	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2987IMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2987IMM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2987IMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2987IMX-3.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2987IMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2988AIMM-2.8/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988AIMM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988AIMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988AIMM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988AIMX-3.3/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2988ILD-3.8/NOPB	WSO	NGN	8	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2988IMM-3.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2988IMM-3.3/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMM-5.0	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMM-5.0/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMMX-3.0/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMMX-3.3/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LP2988IMX-5.0/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



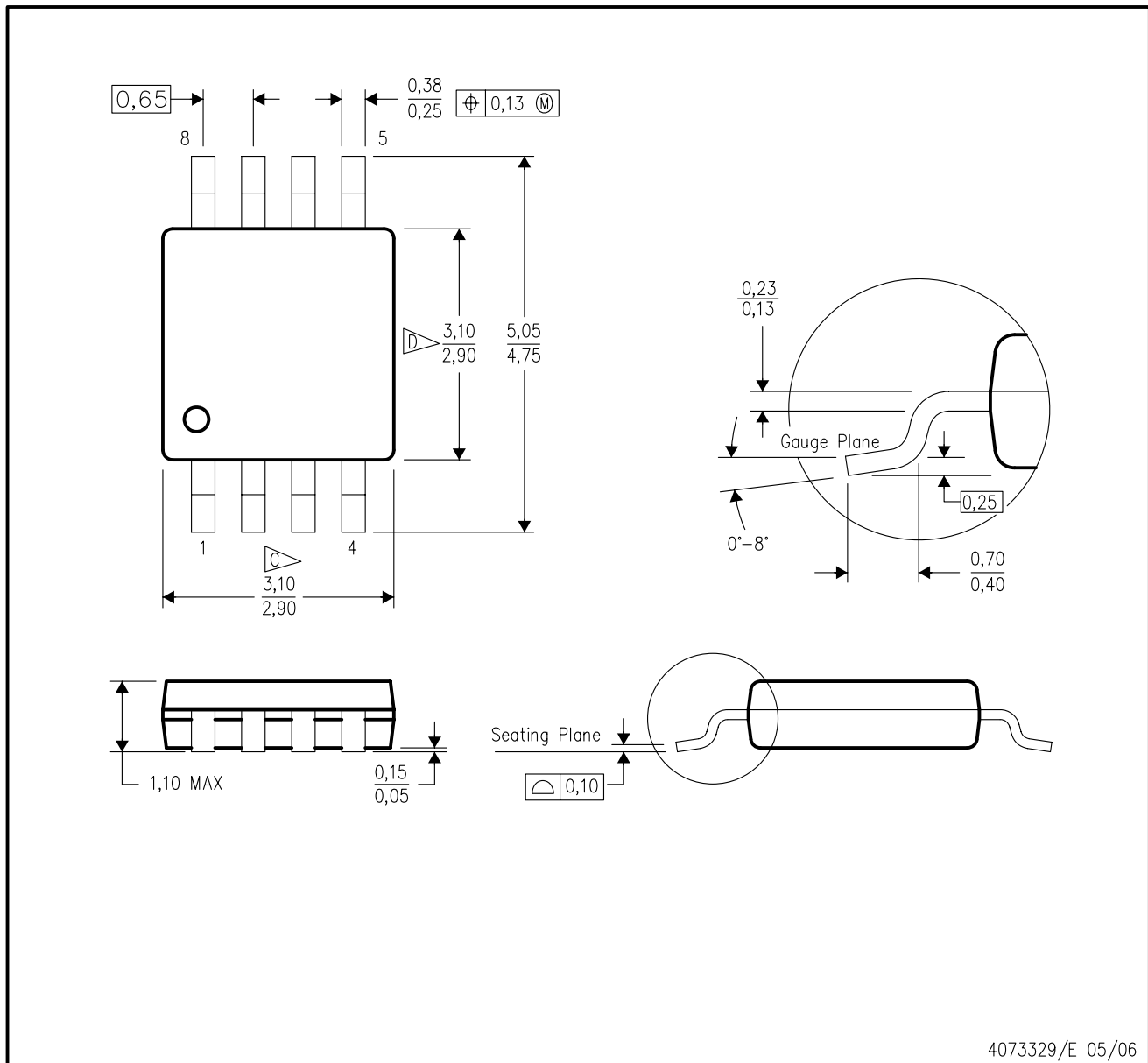
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2987AILD-3.0/NOPB	WSON	NGN	8	1000	210.0	185.0	35.0
LP2987AILD-5.0/NOPB	WSON	NGN	8	1000	210.0	185.0	35.0
LP2987AILD-5.0/NOPB	WSON	NGN	8	4500	367.0	367.0	35.0
LP2987AIMM-5.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2987AIMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2987ILD-3.3/NOPB	WSON	NGN	8	1000	210.0	185.0	35.0
LP2987IMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2987IMM-5.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2987IMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2987IMX-3.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2987IMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2988AIMM-2.8/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988AIMM-3.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988AIMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988AIMM-5.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988AIMX-3.3/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LP2988ILD-3.8/NOPB	WSON	NGN	8	1000	210.0	185.0	35.0
LP2988IMM-3.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988IMM-3.3/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988IMM-5.0	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988IMM-5.0/NOPB	VSSOP	DGK	8	1000	210.0	185.0	35.0
LP2988IMMX-3.0/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2988IMMX-3.3/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LP2988IMX-5.0/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

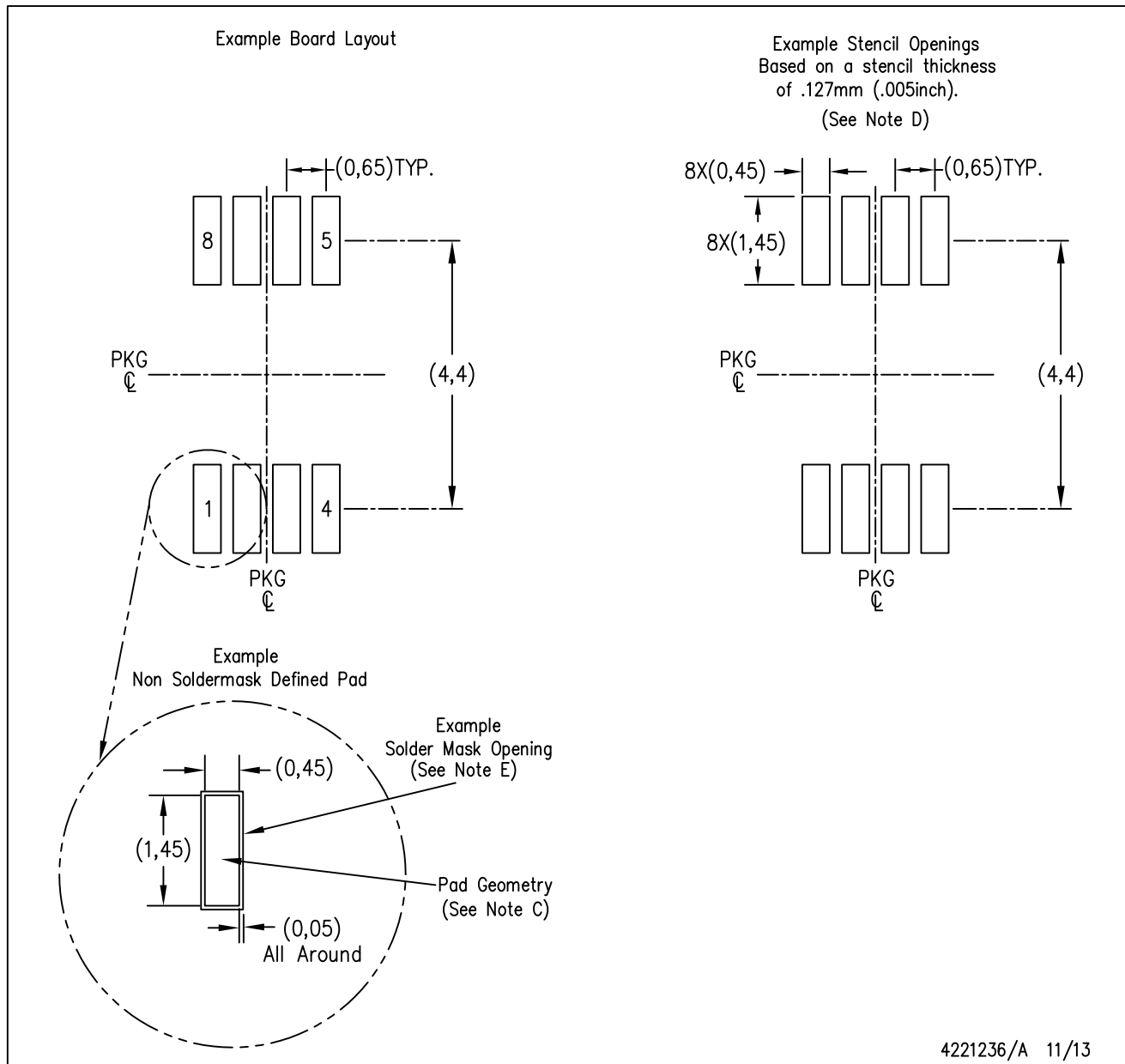


4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

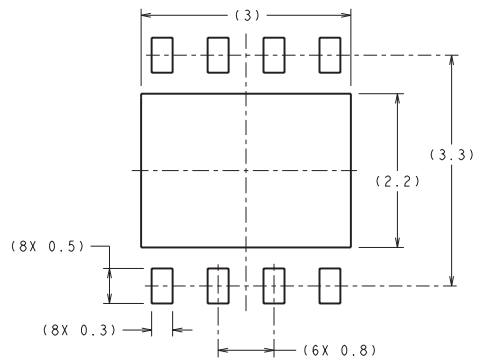
DGK (S-PDSO-G8)

PLASTIC SMALL OUTLINE PACKAGE

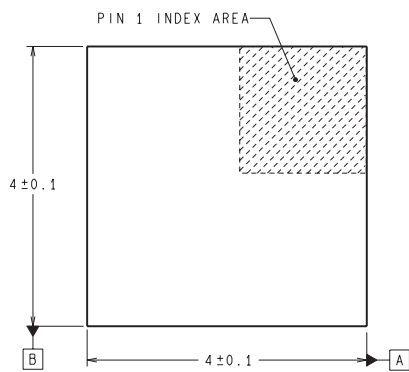


- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

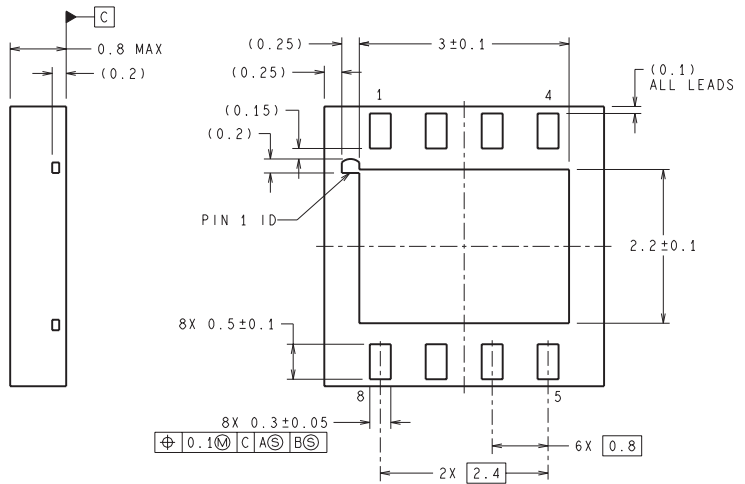
NGN0008A



RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS



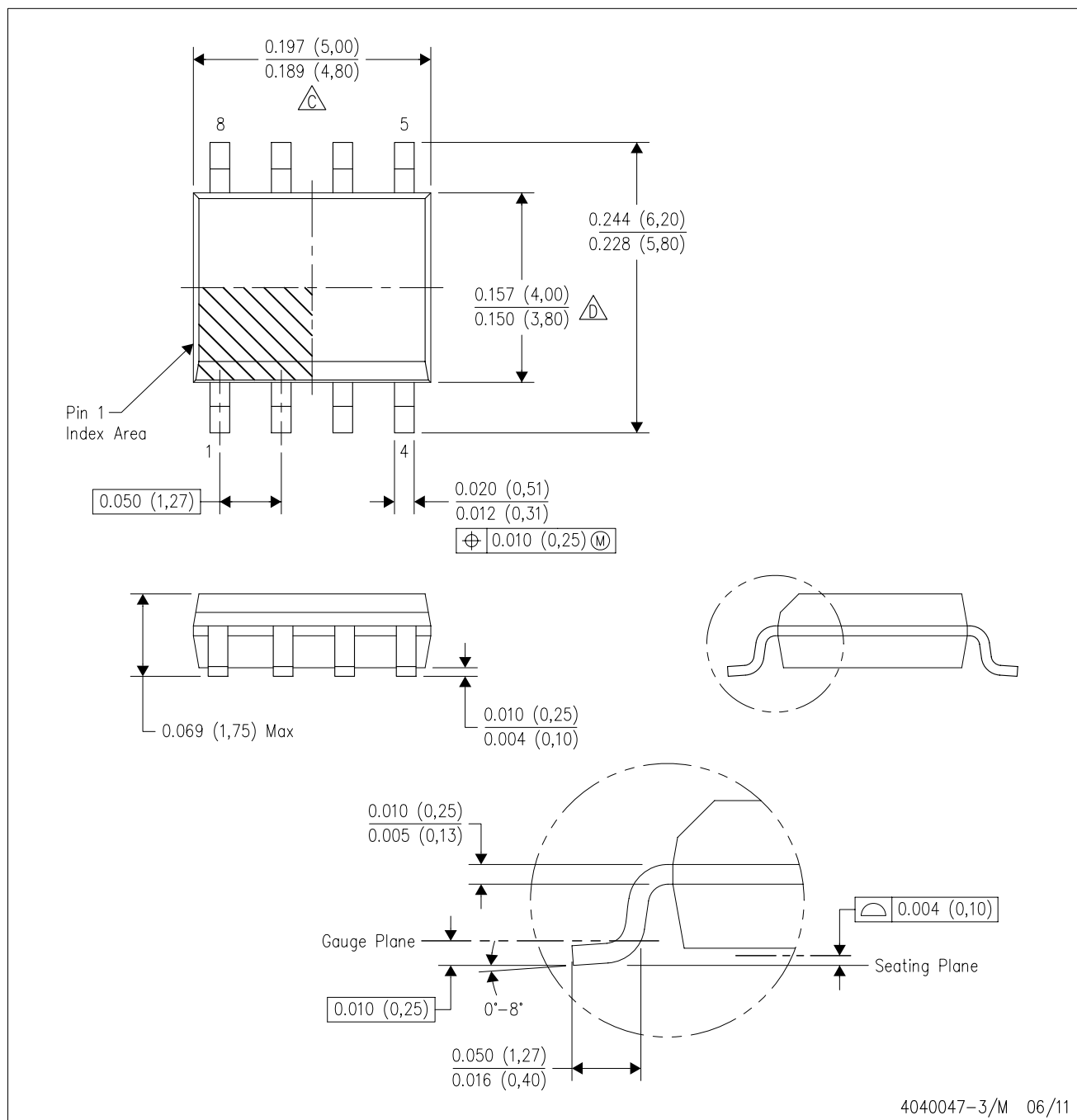
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN () FOR REFERENCE ONLY



LDC08A (Rev B)

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated