NCP4352

Secondary Side SMPS ECO Mode Controller for Low Standby Power

The NCP4352 is a secondary side SMPS controller designed for use in applications which require extremely low consumption. The device is capable of detecting “light load” conditions and entering the power supply into low consumption “ECO mode”.

During ECO mode, the output voltage decreases to an adjustable level, allowing higher efficiency for light load condition while keeping lower but regulated voltage supply. Once more energy is required, the NCP4352 automatically switches back to the normal mode regulation of output voltage.

During normal power supply operation, the NCP4352 provides integrated voltage and current feedback regulation, replacing the need for a shunt regulator. Feedback control is provided through optocoupler to primary side SMPS controller.

The NCP4352 is available in TSOP−6 package.

Features

- Operating Input Voltage Range: 2.5 V to 36.0 V
- Supply Current < 155 μA
- ±0.5% Reference Voltage Accuracy (T_J = 25°C)
- Constant Voltage Control Loop
- Constant Current Control Loop
- Designed for Use with Any Primary SMPS Controller
- These are Pb−free Devices

Typical Applications

- Offline Adapters for Notebooks, Game Stations and Printers
- High Power AC−DC Converters for TVs, Set−Top Boxes, Monitors etc.

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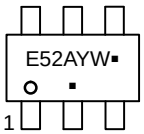
MARKING DIAGRAM

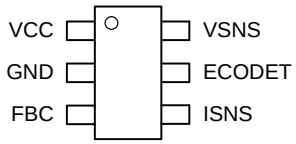
TSOP−6
SN SUFFIX
CASE 318G



E52 = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

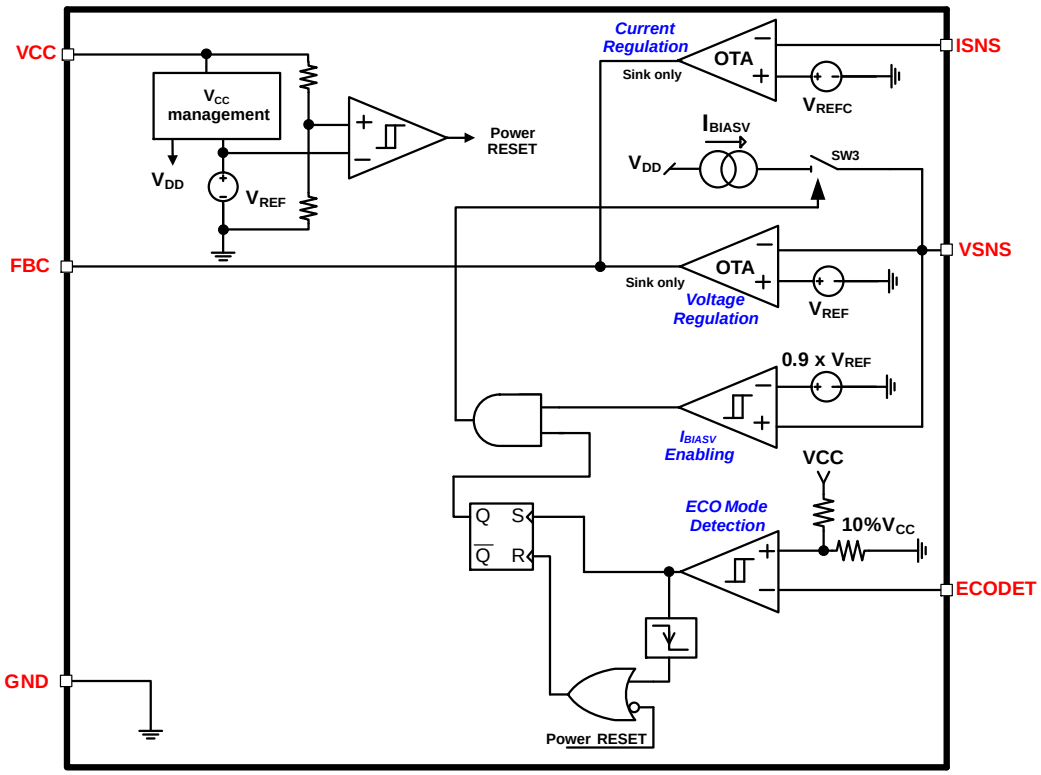


Figure 1. Simplified Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

NCP4352	Pin Name	Description
1	VCC	Supply voltage pin
2	GND	Ground
6	VSNS	Output voltage sensing pin, connected to output voltage divider
5	ECODET	ECO mode detection input. Voltage divider provides adjustable ECO mode detection threshold
4	ISNS	Current sensing input for output current regulation, connect it to shunt resistor in ground branch.
3	FBC	Output of current sinking OTA amplifiers driving feedback optocoupler's LED. Connect here compensation network (networks) as well.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage	V_{CC}	−0.3 to 40.0	V
FBC Voltage	V_{FBC}	−0.3 to V_{CC} + 0.3	V
VSNS, ISNS, ECODET Voltage	V_{SNS},V_{ISNS},V_{ECODET}	−0.3 to 10.0	V
Thermal Resistance – Junction−to−Air (Note 1)	$R_{\theta JA}$	315	°C/W
Junction Temperature	T_J	−40 to 150	°C
Storage Temperature	T_{STG}	−60 to 150	°C
ESD Capability, Human Body Model (Note 1)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 1)	ESD_{MM}	250	V
ESD Capability, Charged Device Model (Note 1)	ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. 50 mm^2, 1.0 oz. Copper spreader.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JESD22A−114F
   ESD Charged Device Model tested per JESD22−C101F
   Latch−up Current Maximum Rating tested per JEDEC standard: JESD78 class I.

Table 3. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Maximum Operating Input Voltage	V_{CCMAX}		36.0	V
Operating Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS

−40°C ≤ T_J ≤ 125°C; V_{CC} = 15 V; unless otherwise noted. Typical values are at T_J = +25°C.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VCC UVLO	V_{CC} rising	V_{CCUVLO}	3.3	3.5	3.7	V
	V_{CC} falling		2.3	2.5	2.7	
VCC UVLO Hysteresis		$V_{CCUVLOHYS}$	0.8	1.0		V
Quiescent Current	V_{ECODET} = 2 V, In regulation	I_{CC}		105	140	μA
	V_{ECODET} = 0 V, V_{SNS} < $V_{SNSBIASTH}$			90	125	
	V_{ECODET} = 1 V, In regulation			120	155	
VOLTAGE CONTROL LOOP OTA						
Transconductance	Sink current only	gm_V		1		S
Reference Voltage	2.8 V ≤ V_{CC} ≤ 36.0 V, T_J = 25°C	V_{REF}	1.244	1.250	1.256	V
	2.8 V ≤ V_{CC} ≤ 36.0 V, T_J = 0 − 125°C		1.230	1.250	1.270	
Sink Current Capability	V_{FBC} > 1.5 V, V_{ECODET} = 2 V	I_{SINKV}	2.5	3.0	3.5	mA
	V_{FBC} > 1.5 V, V_{ECODET} = 1 V		1.2	1.5	2.0	
Inverting Input Bias Current	V_{SNS} = V_{REF}, V_{ECODET} = 2 V	I_{BIASV}	−100		100	nA
	V_{SNS} > $V_{SNSBIASTH}$, V_{ECODET} = 1 V		−35	−31	−27	μA
Inverting Input Bias Current Threshold	V_{ECODET} = 1 V	$V_{SNSBIASTH}$	1.07	1.12	1.17	V
CURRENT CONTROL LOOP OTA						
Transconductance	Sink current only	gm_C		3		S
Reference Voltage		V_{REFC}	60.0	62.5	65.0	mV
Sink Current Capability	V_{FBC} > 1.5 V, V_{ECODET} = 2 V	I_{SINKC}	2.5	3.0	3.5	mA
Inverting Input Bias Current	V_{ISNS} = V_{REFC}	I_{BIASC}	−100		100	nA
ECO MODE DETECTION COMPARATOR						
Threshold Value	2.5 V ≤ V_{CC} ≤ 36.0 V	$V_{ECODETTH}$		10% V_{CC}		V
	V_{CC} = 15 V		1.47	1.50	1.53	
Hysteresis	Output change from logic high to logic low	$V_{ECODETH}$		40		mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

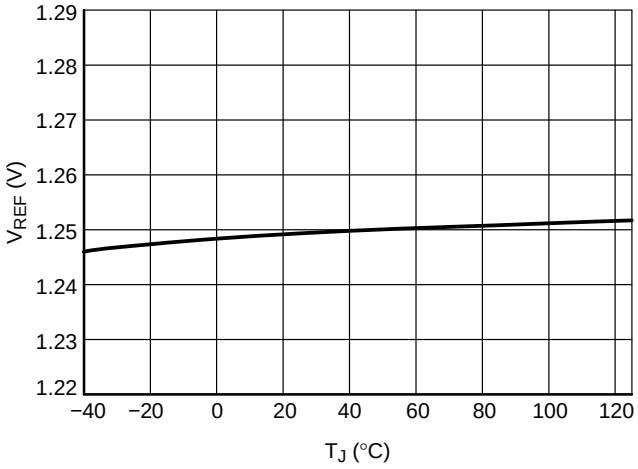


Figure 2. V_{REF} at V_{CC} = 15 V

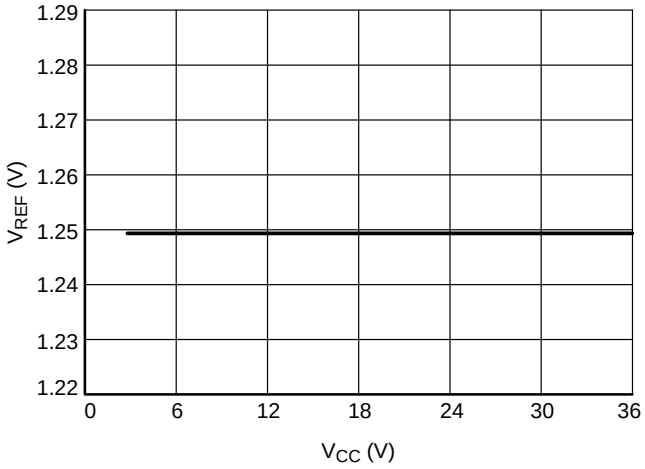


Figure 3. V_{REF} at T_J = 25°C

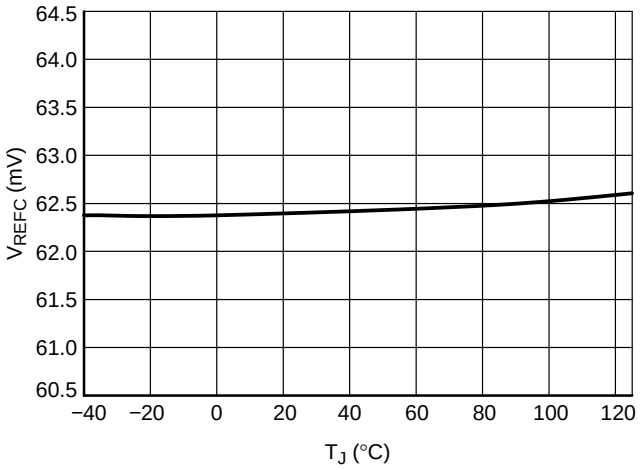


Figure 4. V_{REFC} at V_{CC} = 15 V

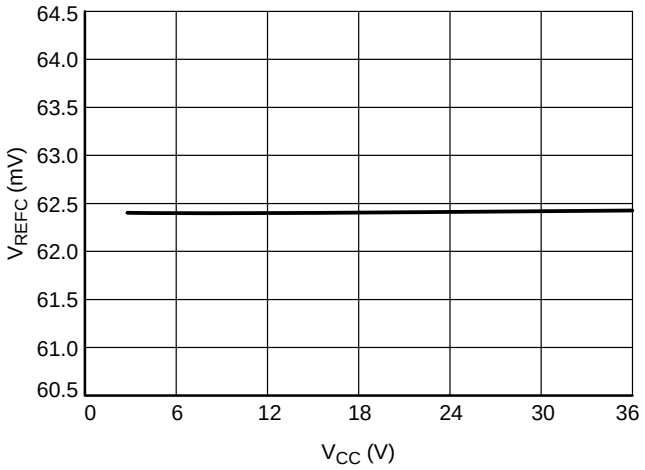


Figure 5. V_{REFC} at T_J = 25°C

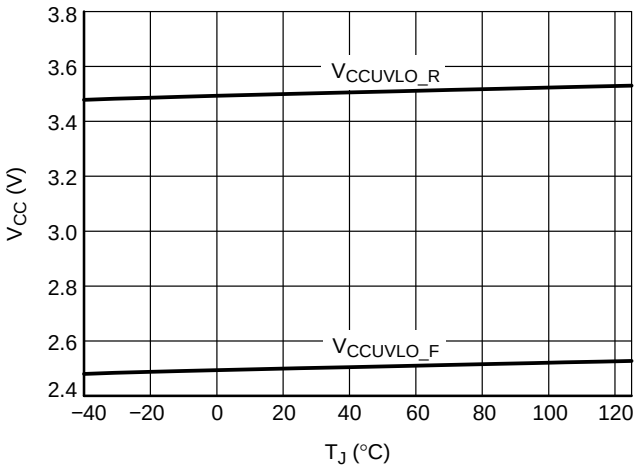


Figure 6. V_{CCUVLO} Rise and Fall Threshold

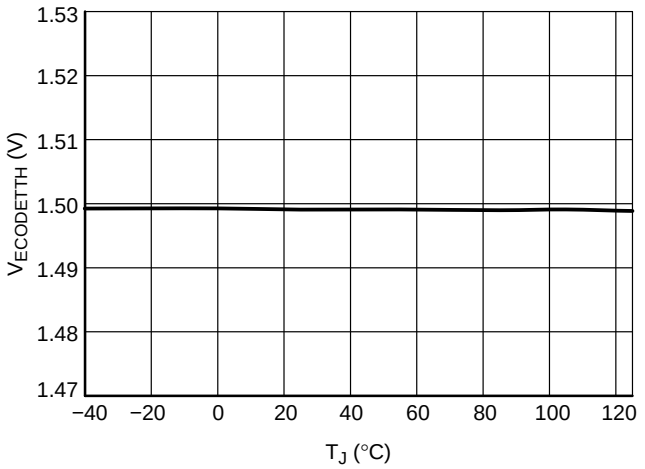


Figure 7. $V_{ECODETTH}$ at V_{CC} = 15 V

TYPICAL CHARACTERISTICS

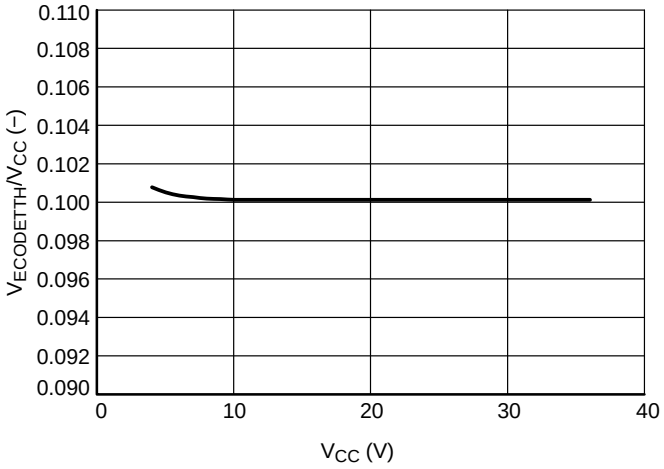


Figure 8. $V_{ECODETTH}/V_{CC}$ Ratio at T_J = 25°C

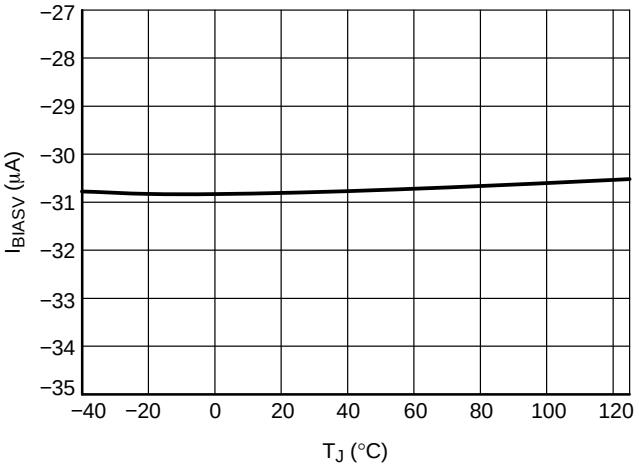


Figure 9. I_{BIASV} at V_{CC} = 15 V, V_{SNS} > $V_{SNSBIASTH}$, V_{ECODET} < 10% V_{CC}

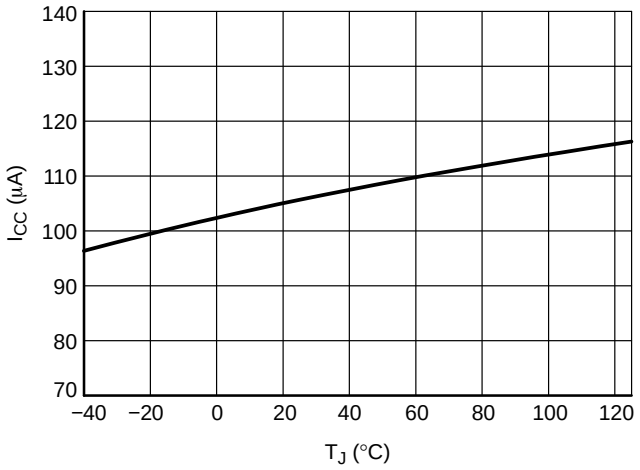


Figure 10. I_{CC} in Regulation, V_{CC} = 15 V, V_{ECODET} = 2 V

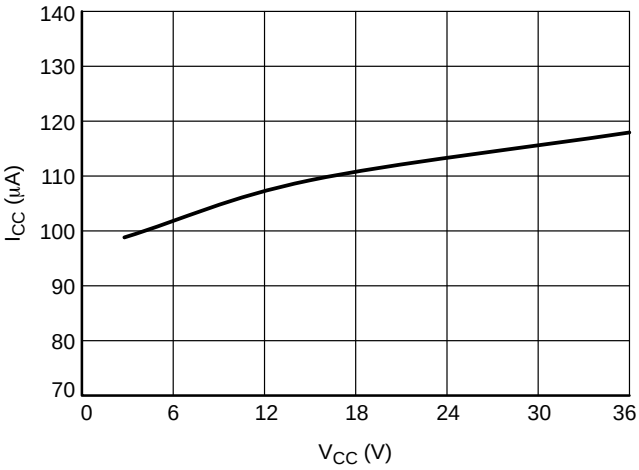


Figure 11. I_{CC} in Regulation, T_J = 25°C, V_{ECODET} > 10% V_{CC}

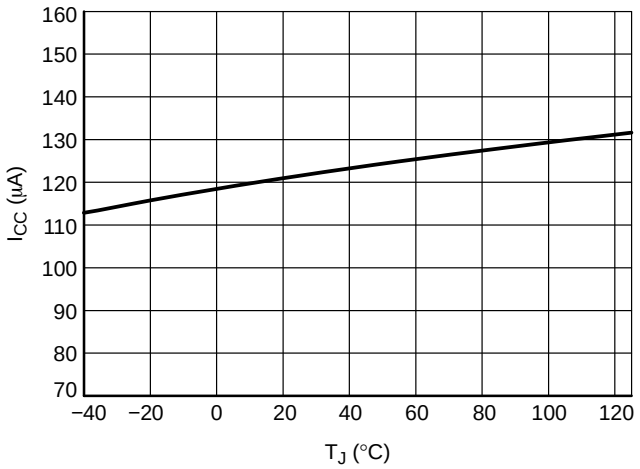


Figure 12. I_{CC} in ECO Mode, V_{CC} = 15 V, V_{ECODET} = 1 V, V_{SNS} = V_{REF}

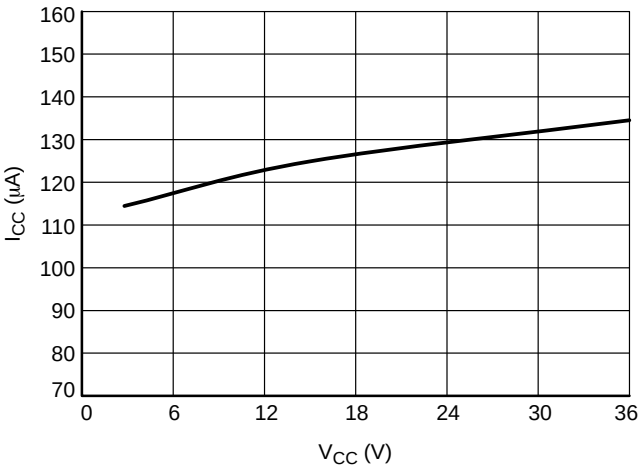


Figure 13. I_{CC} in ECO Mode, T_J = 25°C, V_{ECODET} = 1 V, V_{SNS} = V_{REF}

TYPICAL CHARACTERISTICS

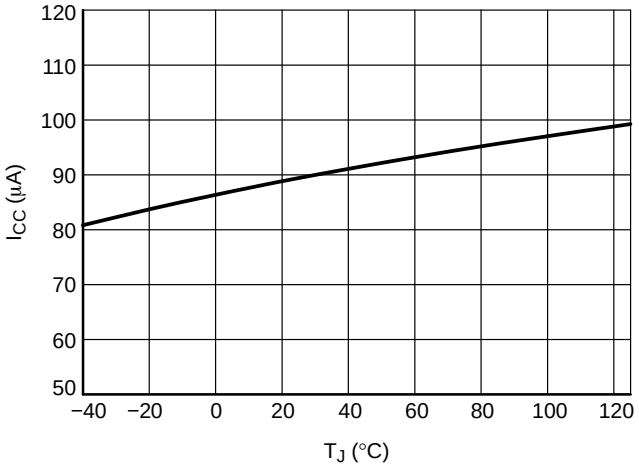


Figure 14. I_{CC} in ECO Mode, V_{CC} = 15 V, V_{ECODET} = 0 V, V_{SNS} < $V_{SNSBIASTH}$

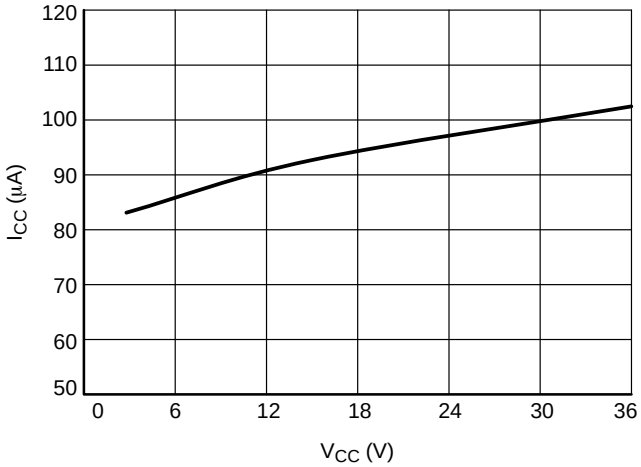


Figure 15. I_{CC} in ECO Mode, T_J = 25°C, V_{ECODET} = 1 V, V_{SNS} < $V_{SNSBIASTH}$

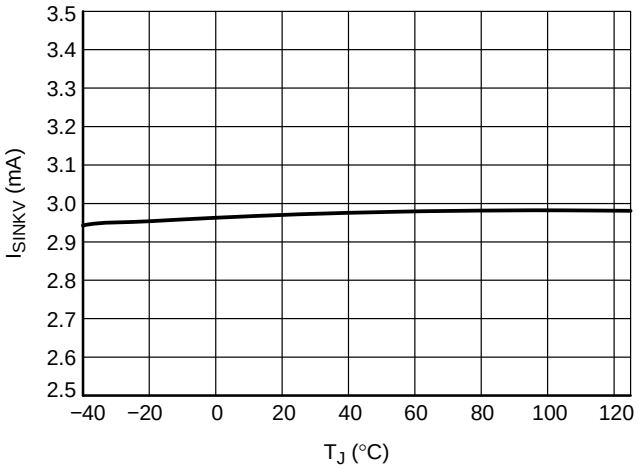


Figure 16. Voltage OTA Current Sink Capability in Normal Mode, V_{CC} = 15 V, V_{ECODET} = 2 V

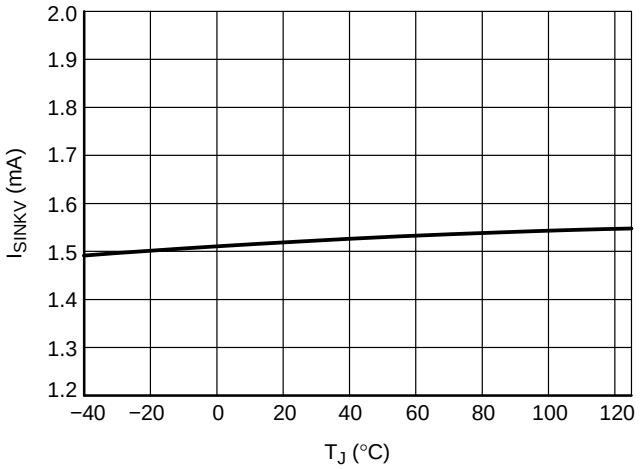


Figure 17. Voltage OTA Current Sink Capability in ECO Mode, V_{CC} = 15 V, V_{ECODET} = 1 V

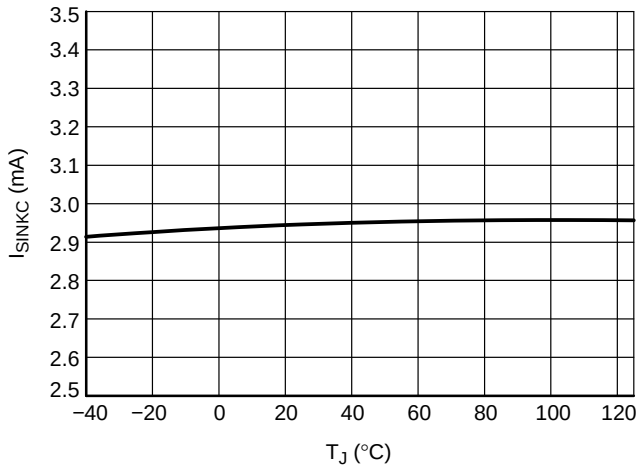


Figure 18. Current OTA Current Sink Capability in Normal Mode, V_{CC} = 15 V, V_{ECODET} = 2 V

APPLICATION INFORMATION

A typical application circuits for NCP4352 series is shown in Figure 19. Pin functions are available in pin description table.

Figure 20 shows possible connection to flyback primary controller. This schematic uses one single optocoupler for both voltage and current regulation functions.

Those schematics provide all possible functionalities.

Power Supply

The NCP4352 is designed to operate from a single supply up to 36 V. It starts to operate when VCC voltage reaches 3.5 V and stops when VCC voltage drops below 2.5 V. VCC can be supplied by direct connection to the VOUT voltage of the power supply. It is recommended to add a RC filter (R1 and C3) in series from VOUT to VCC pin to reduce voltage spikes and drops that are produced at the converter's output capacitors. Recommended values for this filter are 220 Ω and 1 μF.

Voltage Regulation Path

The output voltage is detected on the VSNS pin by the R3 and R4 voltage divider. This voltage is compared with the internal precise voltage reference. The voltage difference is amplified by gm_V of the transconductance amplifier. The amplifier output current is connected to the FBC pin. The compensation network is also connected to this pin to provide frequency compensation for the voltage regulation path. This FBC pin drives an optocoupler to prove the secondary side regulation. The optocoupler is supplied via direct connection to VOUT line through resistor R1.

Regulation information is transferred through the optocoupler to the primary side controller where its FB pin is usually pulled down to reduce energy transferred to secondary output.

The output voltage can be computed by Equation 1.

$$V_{OUT} = V_{REF} \frac{R3 + R4}{R4} \quad \text{(eq. 1)}$$

Current Regulation Path

The output current is sensed by the shut resistor R11 in series with the load. Voltage drop on R11 is compared with internal precise voltage reference V_{REFC} at ISNS transconductance amplifier input.

Voltage difference is amplified by gm_C to output current of amplifier, connected to FBC pin. Compensation network is connected between this pin and ISNS input to provide frequency compensation for current regulation path.

Current regulation OTA is activated only in normal mode, during ECO mode is turned−off to save energy. It doesn't make any issue, because ECO mode is activated just in case of light load so current regulation path is not needed.

Current regulation point is set to current given by Equation 2.

$$I_{OUTLIM} = \frac{V_{REFC}}{R11} \quad \text{(eq. 2)}$$

ECO Mode Detection

ECO mode operation is advantageous for ultra low output current condition. The reduced output voltage with very long skip off time and the low power mode of the whole regulation system reduces strongly the overall consumption.

The output voltage is reduced to a second regulation point in ECO mode. When output voltage decreases, the overall output and regulation power are reduced.

The ECO mode detection is based on comparison of output voltage and voltage loaded with fixed resistances (D2, R6, R7, R8 and C2).

Figure 21 shows detection waveforms. When output voltage is loaded with very low current, primary controller goes into skip mode (primary controller stops switching for some time). While output power is reduced, thanks to the serial resistance R6, the voltage on capacitor C2 provides a voltage proportional to output power, allowing power level detection.

Ones ECODET pin voltage goes lower than $V_{ECODETTH}$ (this threshold is derived from $V_{OUT} = V_{CC}$), ECO mode is detected. This means that ECO mode is not activated until falling edge comes at ECODET pin.

To reduce output voltage on C1 down to the new regulation point, the current I_{BIASV} injected into VSNS pin provides the requested offset (VSNS voltage is higher than V_{REF}). This offset, defined by R4, R5 and the internal current source, allows keeping the same output voltage resistances divider defined for the normal mode. Reduced output voltage in ECO mode can be computed by Equation 3.

$$I_{R3} = \frac{V_{REF} + (R4 + R5) \cdot I_{BIASV}}{R4} \quad \text{(eq. 3)}$$

$$V_{OUT\_ECO} = I_{R3} \cdot R3 + \left(I_{R3} - I_{BIASV}\right) \cdot R4$$

The sink current on primary FB pin is so adjusted to keep primary controller FB in line with the new working point with reduced output voltage.

Primary IC should be kept supplied from auxiliary winding of the transformer despite overall voltage reduction. This may ask for serial voltage regulator to avoid over voltage in normal mode.

If output power increases such that ECODET pin voltage is higher than 10% of V_{CC}, the ECO mode is ended and regulation is switched back to original normal mode. The IC also starts in normal mode after UVLO event.

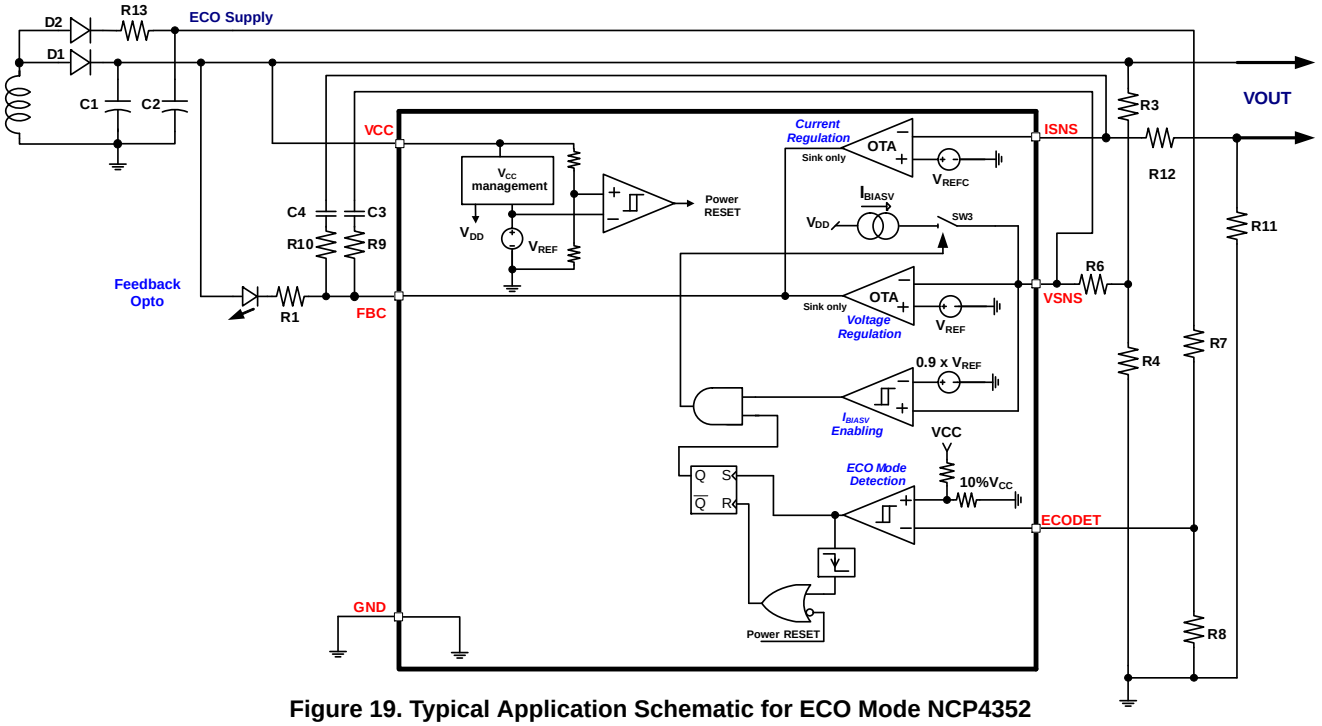


Figure 19. Typical Application Schematic for ECO Mode NCP4352

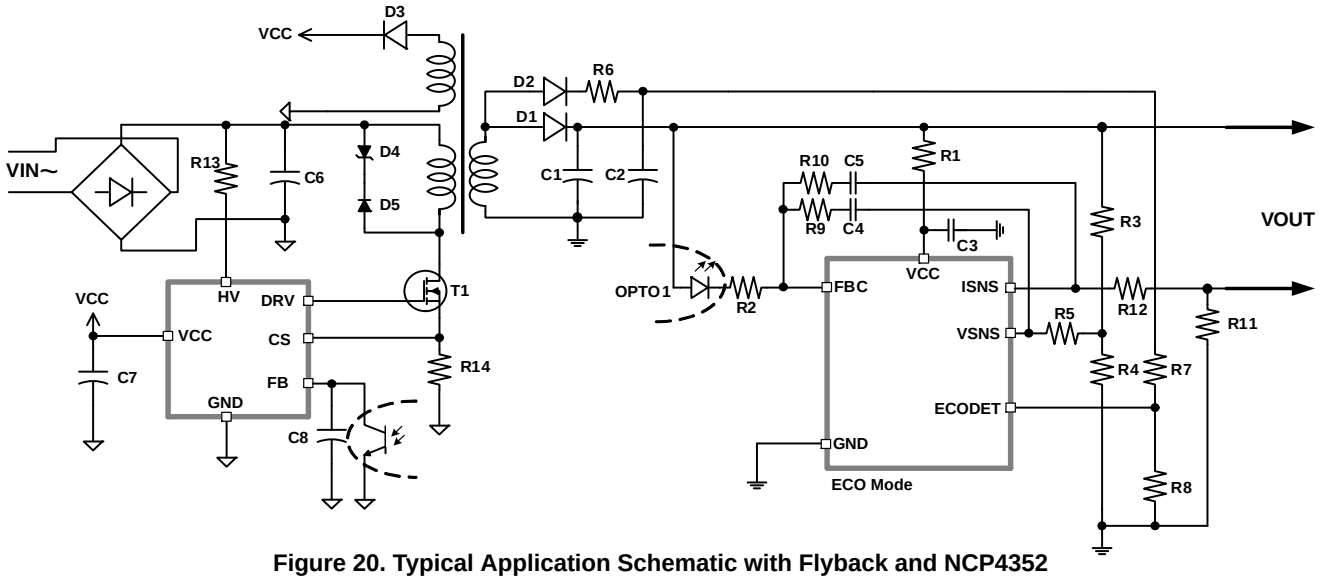


Figure 20. Typical Application Schematic with Flyback and NCP4352

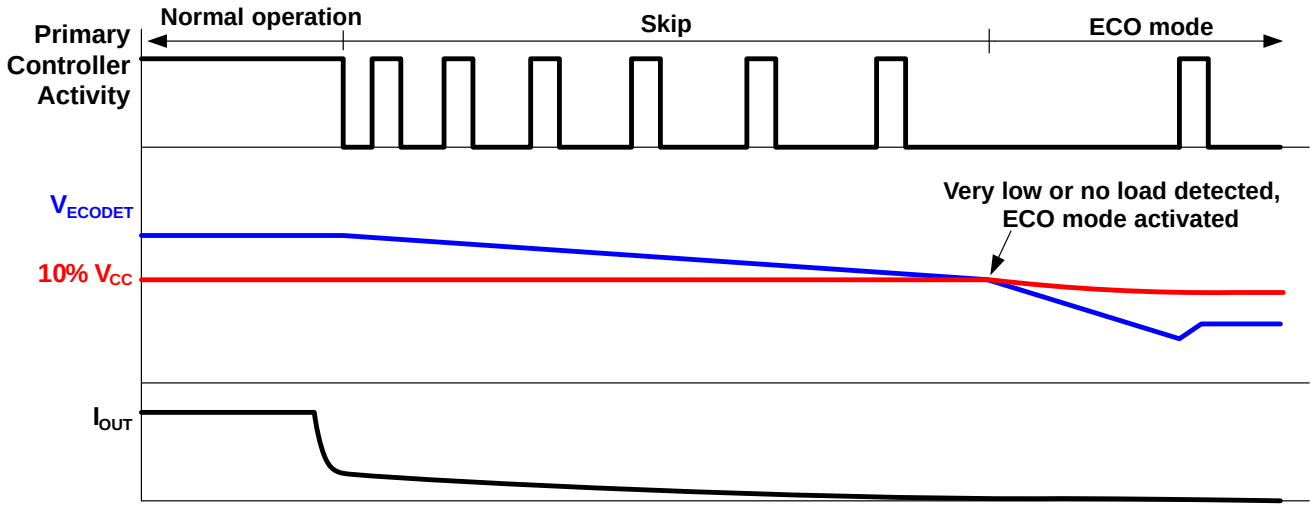


Figure 21. ECO Mode Detection

ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP4352SNT1G	E52	TSOP−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

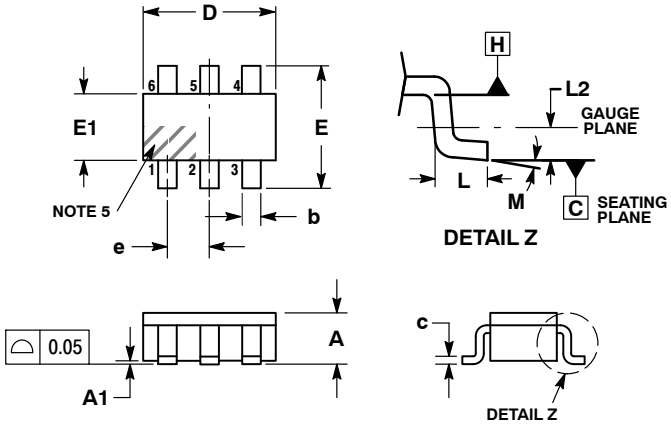
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2		0.25 BSC	
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

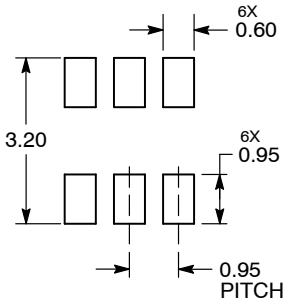
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

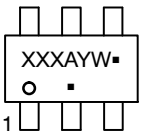
RECOMMENDED SOLDERING FOOTPRINT*



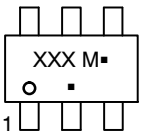
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

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