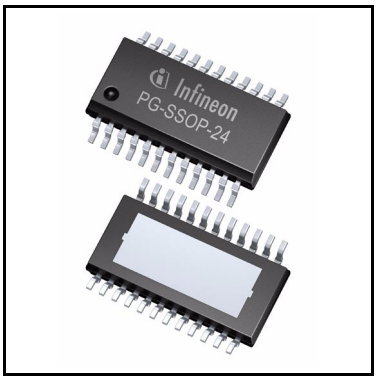
TLE8080EM

Engine Management IC for Small Engines



1 Overview

Features

- Supply 5 V (+/-2%), 250 mA
- K-line transceiver (ISO 9141)
- Serial Peripheral Interface (SPI)
- 4 low side driver for inductive loads with overtemperature and overcurrent protection and open load/short to GND in off diagnosis:
  - 2 low side switches with maximum operation of 2.6 A
  - 2 low side switches with maximum operation of 350 mA
- 1 low side driver for resistive loads with maximum operation current of 3 A including overtemperature and overcurrent protection
- Configurable variable reluctance sensor interface
- Reset output and 5 V undervoltage detection
- Watchdog
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE8080EM is an engine management IC based on Infineon Smart Power Technology (SPT). It is protected by embedded protection functions and integrates a power supply, K-line, SPI, variable reluctance sensor interface and power stages to drive different loads in an engine management system. It provides a compact and cost optimized solution for engine management systems. It is very suitable for one cylinder motorcycle engine management systems.

TLE8080-2EM and TLE8080-3EM

TLE8080-2EM differs from the main version in parameters "**V5DD reset threshold for TLE8080-2EM and TLE8080-3EM**" and "**Power on reset delay time for TLE8080-2EM**" in **Chapter 5.4**.

TLE8080-3EM differs from the main version in parameter "**V5DD reset threshold for TLE8080-2EM and TLE8080-3EM**" in **Chapter 5.4**.

Type	Package	Marking
TLE8080EM	PG-SSOP24	TLE8080EM
TLE8080-2EM	PG-SSOP24	TLE8080-2EM
TLE8080-3EM	PG-SSOP24	TLE8080-3EM

Table of contents

2 Block diagram

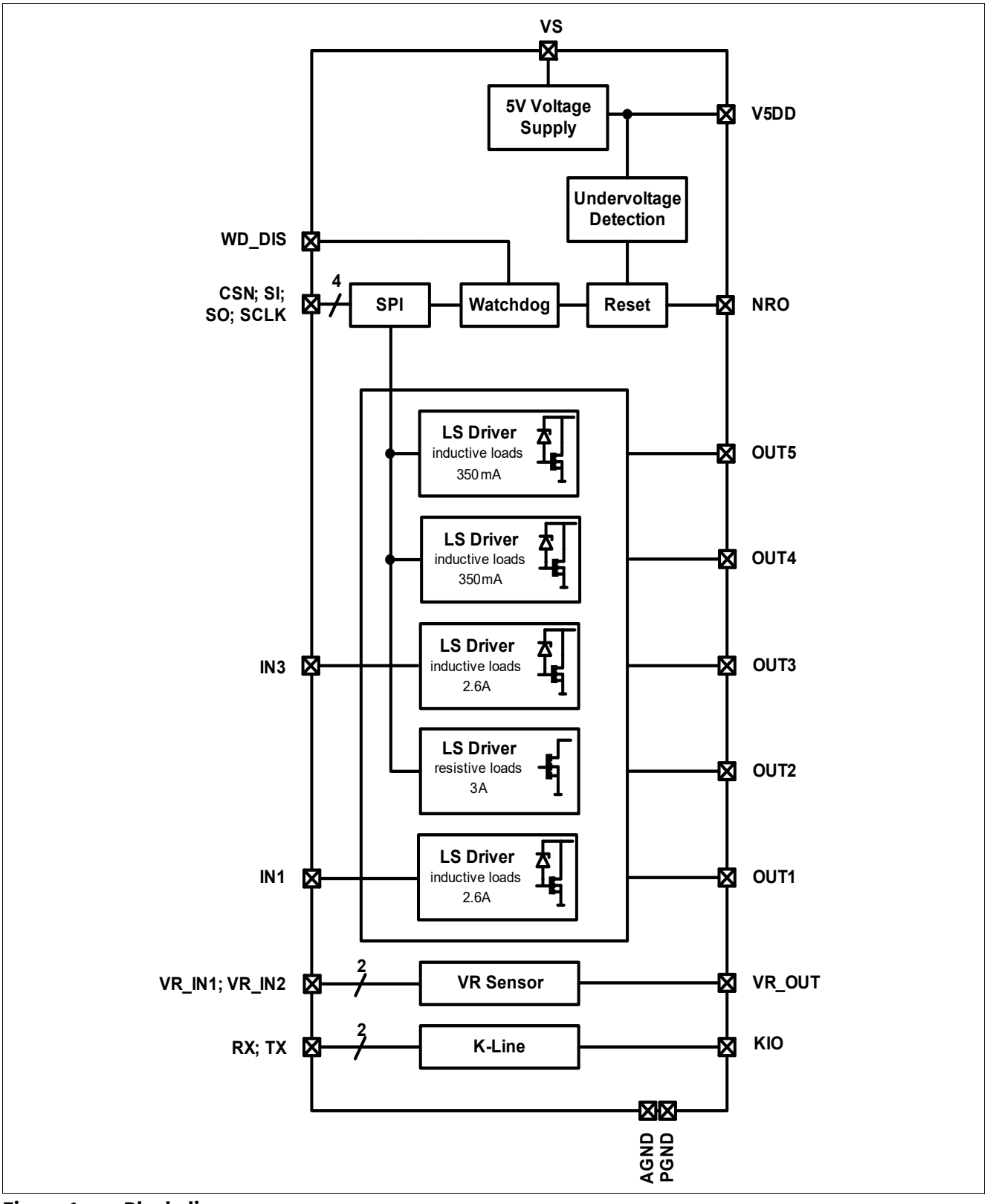


Figure 1 Block diagram

3 Pin configuration

3.1 Pin assignment

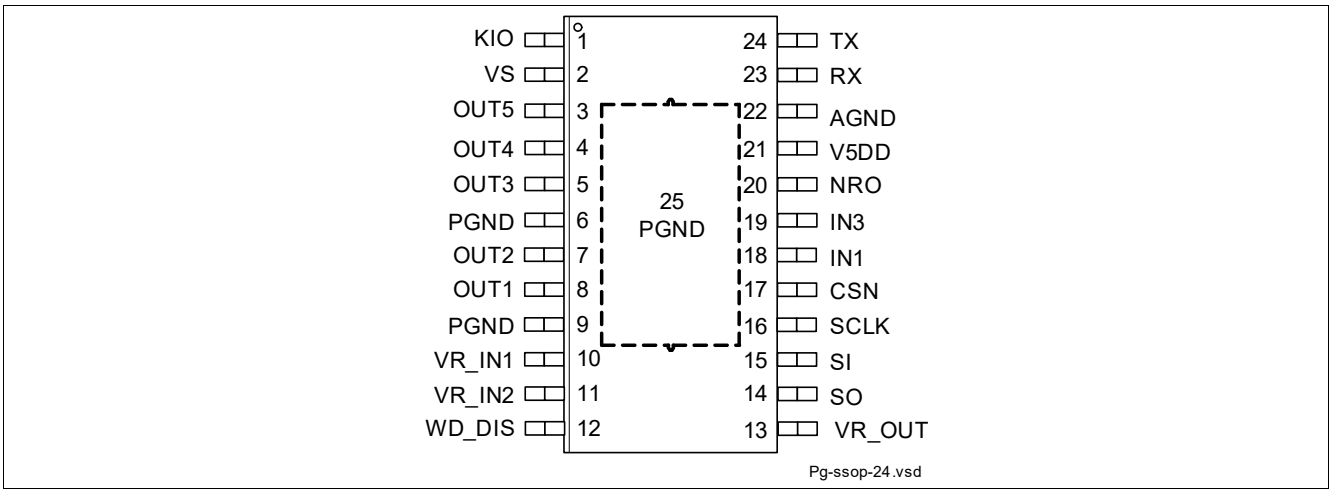


Figure 2 Pin configuration

3.2 Pin definitions and functions

Pin	Symbol	Function
1	KIO	**K-Line Bus Connection**
2	VS	**Battery Voltage:** Block to AGND directly at the IC with min. 100nF ceramic capacitor
3	OUT5	**Output Channel 5**
4	OUT4	**Output Channel 4**
5	OUT3	**Output Channel 3**
6	PGND	**Power Ground:** internally connected to pin 9, connect externally to pin 9
7	OUT2	**Output Channel 2**
8	OUT1	**Output Channel 1**
9	PGND	**Power Ground:** internally connected to pin 6, connect externally to pin 6
10	VR_IN1	**VR Sensor Interface Input 1**
11	VR_IN2	**VR Sensor Interface Input 2**
12	WD_DIS	**Watchdog Disable:** high active; internal pull down
13	VR_OUT	**VR Sensor Output**
14	SO	**SPI Slave Output:** high impedance
15	SI	**SPI Slave Input:** internal pull down
16	SCLK	**SPI Clock Input:** internal pull down
17	CSN	**SPI Chip Select Input:** low active; internal pull up
18	IN1	**Control Input Channel 1:** internal pull down

Pin configuration

Pin	Symbol	Function
19	IN3	**Control Input Channel 3:** internal pull down
20	NRO	**Reset Output:** low active, open drain
21	V5DD	**5V Supply Output:** connected to external blocking capacitor
22	AGND	**Analog Ground:** connected to system logic ground
23	RX	**K-Line Receive Output:** logic output of data received from the K-Line bus KIO
24	TX	**K-Line Transmit Input:** logic level input for data to be transmitted on the K-Line bus KIO; internal pull up
25	Exposed Pad	**Substrate Connection:** must be connected to PGND externally on PCB

4 General product characteristics

Table 1 Absolute maximum ratings [1)]

T_j = -40°C to +150°C: All voltages with respect to ground unless otherwise specified. Positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage VS	V_{VS}	-0.3	–	40	V	–	P_4.1.1
Supply voltage V5DD	V_{V5DD}	-0.3	–	5.5	V	–	P_4.1.2
Input voltage on pins IN1, IN3, SCLK, SI, WD_DIS	V_x	-0.3	–	5.5	V	–	P_4.1.3 a
Input voltage on pins CSN, TX	V_x	-0.3	–	V5DD +0.3 V	V	–	P_4.1.3 b
Input voltage VR_IN1, VR_IN2	$V_{VR\_IN1/2}$	-0.3	–	5.5	V	see also 4.2.1 and 4.2.2	P_4.1.4
DC voltage on pins OUT1-5	V_x	-0.3	–	30	V	respect to PGND all channels are switched off	P_4.1.5
DC voltage on pins VR_OUT, SO, RX, NRO	V_x	-0.3	–	5.5	V	I_x < 1 mA	P_4.1.6
DC voltage AGND to PGND	V_x	-0.3	–	0.3	V		P_4.1.7
DC voltage on pin KIO	V_{KIO}	-1	–	35	V	respect to PGND KIO is switched off	P_4.1.8
Currents							
Input current between VR_IN1 and VR_IN2	I_{VR_IN1,VR_IN2}	--	–	50	mA	–	P_4.2.1
Input current VR_IN1, VR_IN2 to GND	$I_{VR\_IN1/2,GND}$	--	–	10	mA	–	P_4.2.2
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.3.1
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.3.2
ESD susceptibility							
ESD resistivity all Pins to GND	V_{ESD}	-2	–	2	kV	HBM [2)]	P_4.4.1
ESD resistivity all Pins to GND	V_{ESD}	-500	–	500	V	CDM [3)]	P_4.4.2
ESD resistivity Pin 1, 12, 13, 24 (corner pins) to GND	$V_{ESD1,19,20,36}$	-750	–	750	V	CDM [3)]	P_4.4.3

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to EIA/JESD 22-A114B.
3) ESD susceptibility, Charged Device Model “CDM” EIA/JESD22-C101 or ESDA STM5.3.1.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

Table 2 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage	V_S	6	–	40	V	–	P_4.5.1
Junction Ttemperature	T_j	-40	–	150	°C	–	P_4.5.2

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

Table 3 Thermal resistance

Parameter	Symbol	Values			Unit	NoteorTest Condition	Number
		Min.	Typ.	Max.			
Junction to case	RthJC	–	7	–	K/W	1)	P_4.6.1
Junction to ambient	RthJA	–	29	–	K/W	1) 2)	P_4.6.2

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70 µm Cu, 2 x 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

5 5 V supply, reset and supervision

5.1 5 V supply

The TLE8080EM integrates a voltage regulator for load currents up to 250 mA. The input voltage at VS is regulated to 5 V on V5DD with a precision of ±2%. The design allows to achieve stable operation even with ceramic output capacitors down to 470 nF. It is protected against overload, short circuit, and over temperature conditions. For low drop operation, a charge pump is implemented.

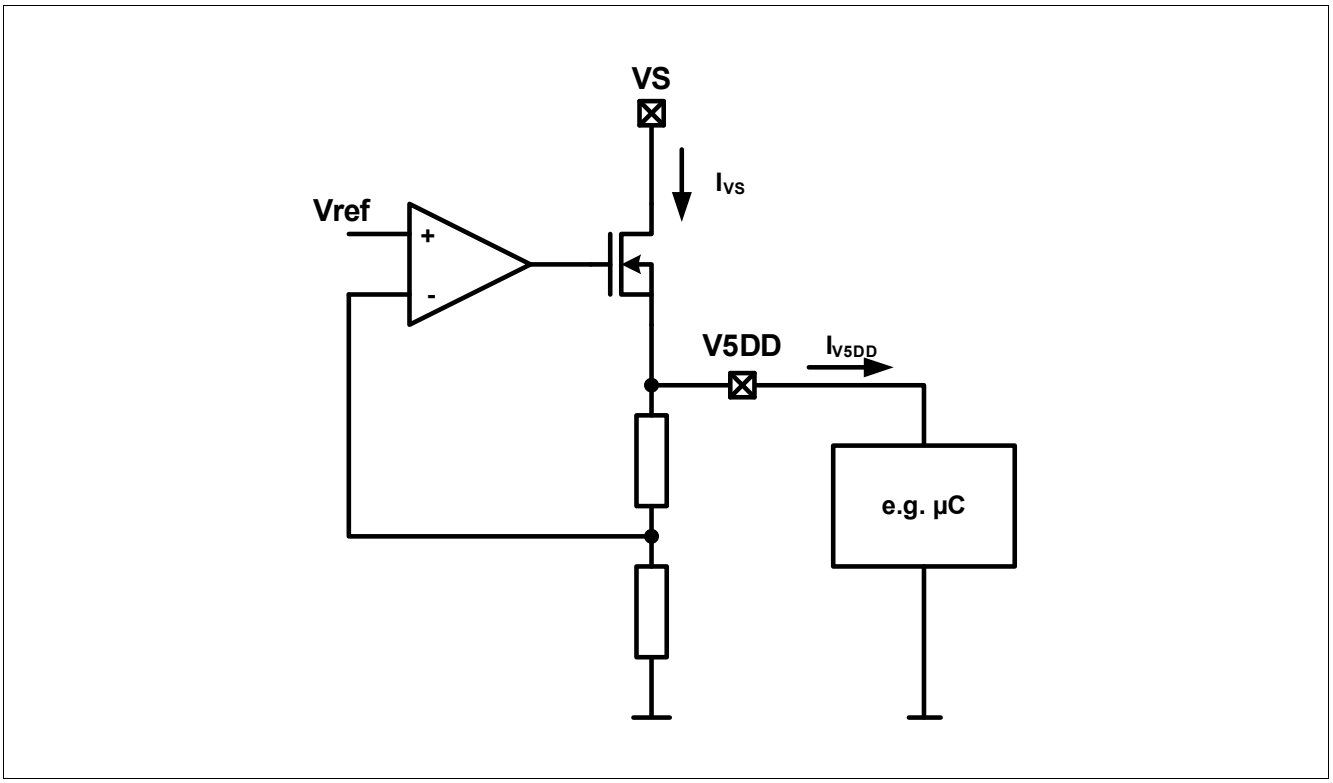


Figure 3 5 V supply

5.2 Power on reset and reset output

The reset output NRO is an open drain output. When the level of V_{V5DD} reaches the reset threshold (V_{RT}) (increasing voltage V_{V5DD}) the signal at NRO remains low for the power-up reset delay time (t_{RD}). The reset function and timing is illustrated in **Figure 4**. The reset reaction time (t_{RR}) avoids wrong triggering caused by short “glitches” on the V5DD-line. In case of V5DD power down (decreasing voltage; $V_{V5DD} < V_{RT}$ for $t < t_{RR}$) a logic low signal is generated at the pin NRO to reset an external micro controller. The level of the reset threshold for increasing V_{V5DD} is for the hysteresis (V_{RH}) higher than the level for decreasing V_{V5DD}.

With an active reset all power stages and the K-Line output are disabled and SPI commands are ignored.

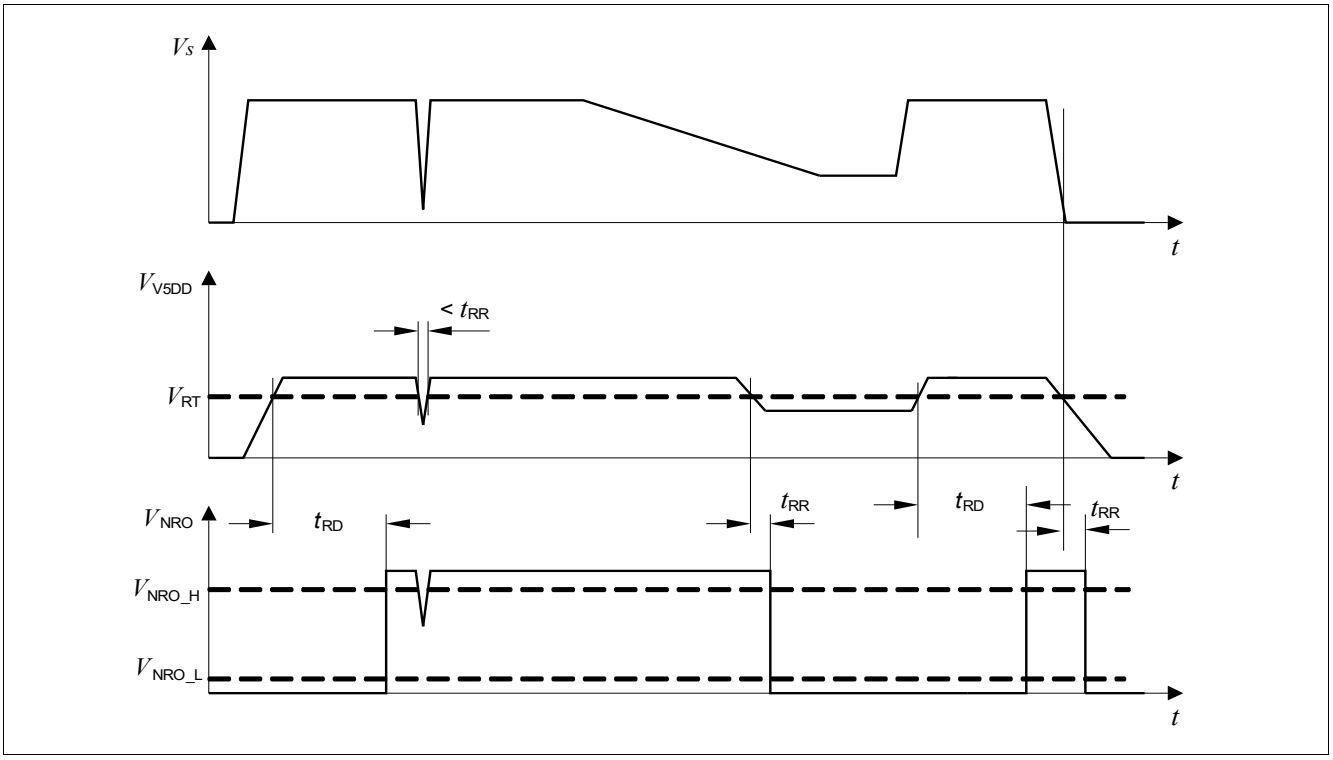


Figure 4 Reset Timing Diagram

5.3 Watchdog operation

The TLE8080EM integrates a watchdog function which monitors the correct SPI communication with the micro controller. A watchdog disable pin (WD_DIS) with an internal pull down current source is implemented. With a high level the watchdog function is disabled.

For enabled watchdog function after power-up reset delay time (t_{RD}), valid SPI communication from the micro controller must occur within the watchdog period (t_{WP}) specified in the electrical characteristics. A restart of the watchdog period is done with a low to high transition of the CSN pin of a valid transmission of a 16 bit message.

A reset is generated (NRO goes LOW) for the time (t_{WR}) if there is no restart during the watchdog period as shown in **Figure 5**.

Status after watchdog overflow:

- all outputs are switched off
- SPI registers are not influenced
- Watchdog Time Out bit in SPI status register is set
- first answer to SPI communication is the content of the status register

Switching of Outputs and reset of Watchdog Time Out Bit after watchdog overflow:

- Outputs 1 and 3 will be switched on with an positive edge at IN1 respectively IN3
- Outputs 2, 4 and 5 will be switched on with a write command to CMD register
- the watchdog time out bit will be reset with the rising edge of CSN of the first read command of the status register

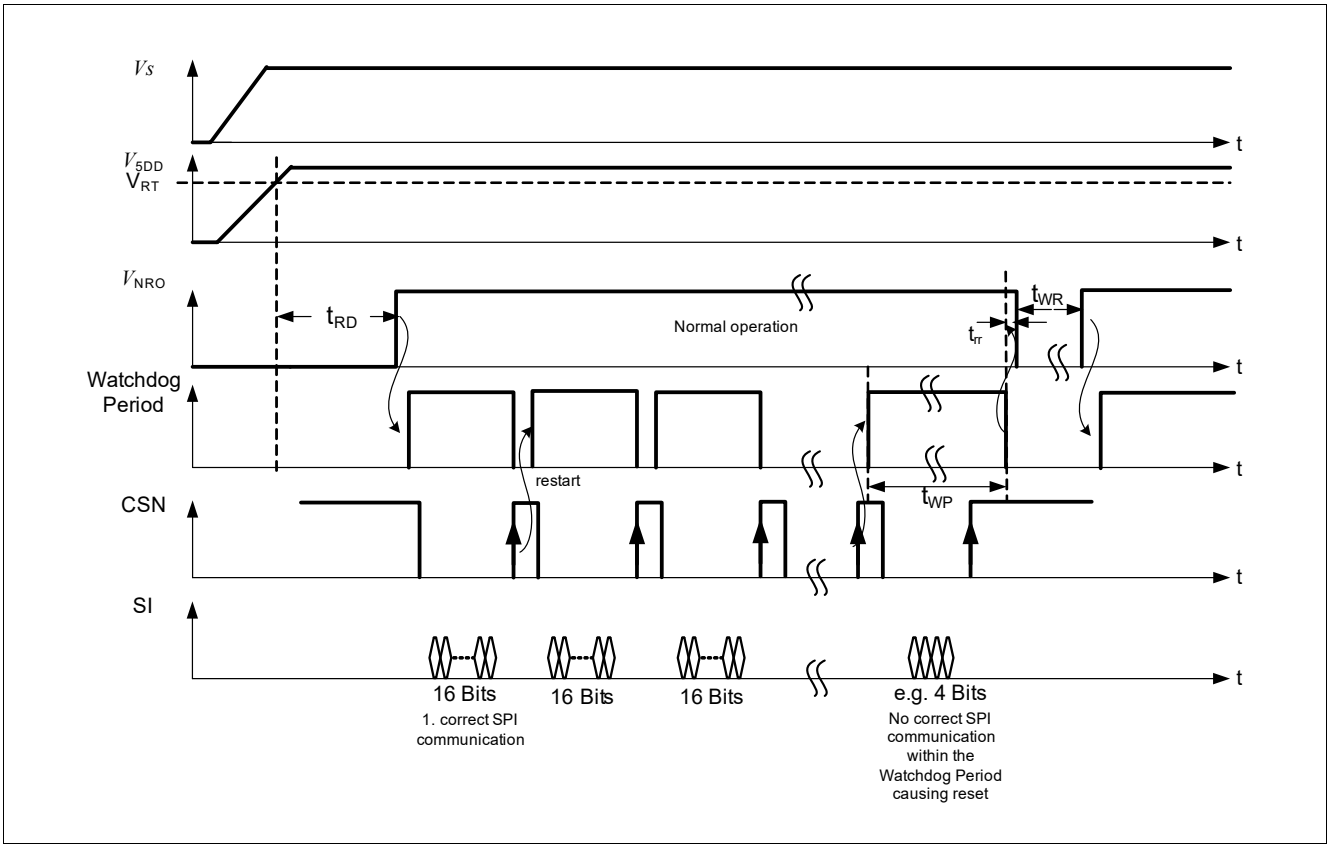


Figure 5 Watchdog timing diagram

5.4 Electrical characteristics 5 V supply, reset and supervision

Table 4 Electrical characteristics: 5 V supply, reset and supervision

V_S = 13.5 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
5 V supply							
Output voltage	V_{V5DD}	4.9	5	5.1	V	0 mA < I_{V5DD} < 250 mA, 6 V < V_S < 40 V	P_5.1.1
Output current limitation	I_{V5DD}	250	–	650	mA	V_{V5DD} = 0 V	P_5.1.2
Load regulation	$\Delta V_{V5DD, Lo}$	–	–	20	mV	1 mA < I_{V5DD} < 250 mA	P_5.1.3
Line regulation	$\Delta V_{V5DD, Li}$	–	–	10	mV	I_{V5DD} = 1 mA, 6 V < V_S < 40 V	P_5.1.4
Power supply rejection	*PSRR*	–	60	–	dB	f = 100 Hz, $V_{S, ripple}$ = 0.5 Vpp [1]	P_5.1.5
Output capacitor	C_{V5DD}	470	–	–	nF	[1]	P_5.1.6
Output capacitor ESR	$ESR(C_{V5DD})$	–	–	10	Ω	[1]	P_5.1.7
Current consumption	I_{VS}	–	5.5	8	mA	I_{V5DD}= 0 mA, all channels and K-Line off	P_5.1.8
Low drop resistance	$R_{DSon,V5}$	–	–	1.2	Ω	V_S ≥ 4.8 V I ≤ 250 mA	P_5.1.11
Over temperature protection							
Over temperature threshold	T_{OT}	150	–	200	°C	[1]	P_5.2.1
Over temperature hysteresis	$T_{OT,Hys}$	–	20	–	°C	[1]	P_5.2.2

Table 4 Electrical characteristics: 5 V supply, reset and supervision (cont'd)

V_S = 13.5 V, T_j = -40°C to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Under voltage detection							
V5DD reset threshold for TLE8080EM	V_{RT}	4.00	4.25	4.50	V	V_{V5DD} decreasing, only at version TLE8080EM	P_5.3.1
Reset hysteresis	V_{RH}	10	–	150	mV		P_5.3.2
V5DD reset threshold for TLE8080-2EM and TLE8080-3EM	V_{RT}	3.4	3.65	3.9	V	V_{V5DD} decreasing, only at versions TLE8080-2EM and TLE8080-3EM	P_5.3.3
Power on reset							
Power on reset delay time for TLE8080EM and TLE8080-3EM	t_{RD}	10	15	20	ms	only at versions TLE8080EM and TLE8080-3EM	P_5.4.1
Power on reset delay time for TLE8080-2EM	t_{RD}	30	40	50	ms	only at version TLE8080-2EM	P_5.4.2
Reset reaction time	t_{RR}	10	15	20	µs		P_5.4.3
Reset output NRO							
Low level output voltage	$V_{NRO,L}$	–	–	1.1	V	I_{NRO} = 1 mA	P_5.5.1
Watchdog							
Watchdog period	t_{WP}	50	60	70	ms		P_5.6.1
Watchdog reset time	t_{WR}	120	240	360	µs		P_5.6.2
Input characteristics WD_DIS							
Low level input voltage	$V_{WD\_DIS,L}$	–	–	1	V		P_5.7.1
High level input voltage	$V_{WD\_DIS,H}$	2	–	–	V		P_5.7.2
Pull down current	$I_{WD\_DIS,pd}$	20	50	100	µA	at V_{IN} = 5 V	P_5.7.3
Pull down current	$I_{WD\_DIS,pd}$	2.4	–	–	µA	at V_{IN} = 0.6 V	P_5.7.4
Hysteresis	$V_{WD\_DIS,Hys}$	30		250	mV		P_5.7.5

1) Not subject to production test, specified by design.

6 Power stages

6.1 Low side switches

The power stages are built by N-channel power MOSFET transistors. The channels are universal multi channel switches, but are mostly suitable to be used in engine management systems. Within an engine management system, the best fit of the channels to the typical loads is:

- Channel 1 and 3 for injector valves or similar sized solenoids with a maximum operation current requirement of 2.6 A.
- Channel 2 for malfunction indication lamps or other resistive loads with a maximum current requirement of 3 A.
- Channel 4 and 5 for relays or other inductive loads with a maximum current requirement of 350 mA.

The channels are switched off while reset is active (pin NRO is low). After an power on reset the channels will be switched on with a positive edge at IN1 respectively IN3 or with a switch on command over SPI.

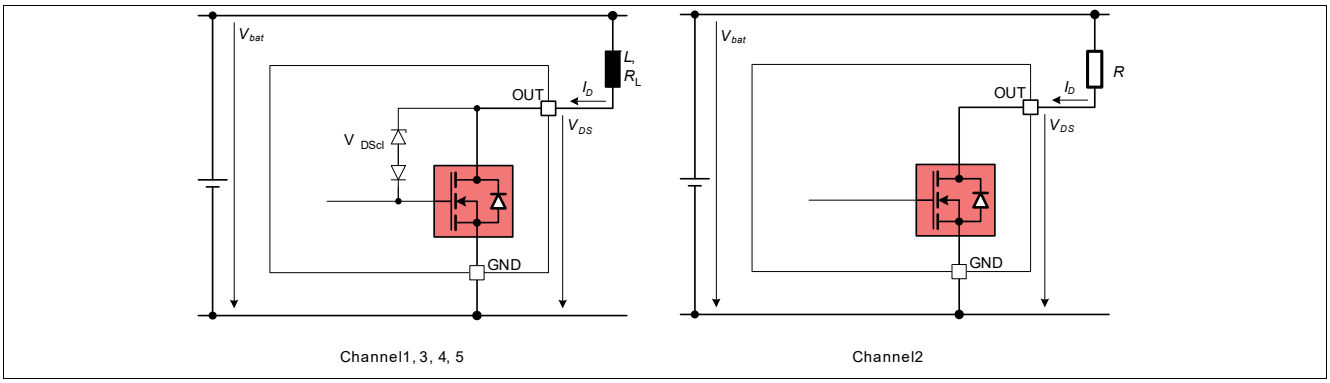


Figure 6 Low side switches

In **Table 5** the control concept, typical loads, the implemented protection and monitor functions are illustrated.

Table 5 Overview diagnosis function

Channel	Control	Recommended Load	Over Temperature	Over Current	Open Load/ ShorttoGND
1	Pin IN1	Injector valve	x	Latch [1]	x
2	SPI CMD register bit 0	MIL (max. 3W)	x	repetitive switching; off time $t_{oc,off}$ [1]	–
3	Pin IN3	Valve	x	Latch [1]	x
4	SPI CMD register bit 1	Relay	one temperature sensor for channel 4 and channel 5	Latch [1]	x
5	SPI CMD register bit 2	Relay	one temperature sensor for channel 4 and channel 5	Latch [1]	x

1) Reset behavior of the diagnosis bits see **Chapter 8.2**.

Power stages

In overcurrent condition the affected channel will be switched off. There are two different implementations for switching on again after an over current event.

For channels 1, 3, 4 and 5 the switch off state is latched. The input pins IN1, IN3 must be set to low to reset the latch before the channel can be switched on again.
For channels 4 and 5 the over current status is reset with a write command to the CMD register after a Diagnosis Read Command has been sent. The switching state is according to the status of bit 1 and 2.

Channel 2 will be switched off and after t_{oc_off} = 5 ms typically the channel will be switched on again automatically. The result is repetitive switching with a fixed off time of $t_{oc,off}$. The overcurrent status of channel 2 is internally latched. For releasing the over current diagnosis bit after over current condition, channel 2 must stay switched on for at least $t_{oc,St}$.

The bits 0 to 4 in the Stat register reflect the actual switching status of the channels. For detailed description see **Chapter 8.2.2**.
All the channels are protected from over temperature. In an overtemperature situation the affected channel will be switched off. The channel will restart operation if the junction temperature decreases by thermal shutdown hysteresis $T_{OT,Hys}$. Channels 4 and 5 are using a common temperature sensor. Therefore, the two channels are switched together during over temperature.

For channels 1, 3, 4 and 5 an open load/short to GND in off detection with a pull down current source (active in off) and a comparator is implemented. In case of switch off and the output voltage is below the open load detection threshold ($V_{outx} < V_{ol,th}$), the open load in off timer is started. After the open load in off delay time $t_{ol,d}$, the open load is detected (timing see **Figure 9** and **Figure 10**).

The diagnosis status of the channels is monitored in the SPI Diagnosis Register DIAG (see **Chapter 8.2**).

6.2 Electrical characteristics low side switches

Table 6 Electrical characteristics: power stage

V_S = 13.5 V, T_j = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output channel 1 and 3							
On resistance	R_{OUTx_on}	–	0.6	0.7	Ω	I_{OUTx_nom} = 1.3 A, T_j = 150°C	P_6.1.1
Output clamping voltage	V_{OUTx_cl}	30	35	40	V	I_{OUTx} = 0.02 A	P_6.1.2
Over-current switch off threshold	I_{OUTx_oc}	2.6	–	5	A		P_6.1.3
Over-current switch off filter time	$t_{oc,f}$	0.5	–	3	µs		P_6.1.4
Over temperature switch off	T_{OT}	150	–	200	°C		P_6.1.5
Over temperature yysteresis	$T_{OT,Hys}$	–	20	–	°C		P_6.1.6
Open load in off detection threshold	$V_{ol,th}$	2	2.8	3.2	V		P_6.1.7
Open load in off pull down diagnosis current	I_{ol}	50	100	150	µA	V_{OUTx} = 13.5 V	P_6.1.8
Open load in off diagnosis delay time	$t_{ol,d}$	100	–	200	µs		P_6.1.9
Turn on delay time	$t_{d,ON}$	–	0.25	1	µs	V_{OUTx} = 13.5 V, I_{OUTx} = 1.3 A, resistive load [1)]	P_6.1.10
Turn off delay time	$t_{d,OFF}$	–	0.9	1.5	µs	V_{OUTx} = 13.5 V, I_{OUTx} = 1.3 A, resistive load [1)]	P_6.1.11
Turn on time	$t_{s,ON}$	–	0.6	1.2	µs	V_{OUTx} = 13.5 V, I_{OUTx} = 1.3 A, resistive load [1)]	P_6.1.12
Turn off time	$t_{s,OFF}$	–	0.6	1.2	µs	V_{OUTx} = 13.5 V, I_{OUTx} = 1.3 A, resistive load [1)]	P_6.1.13
Output leakage current in off mode	I_{OUTx_off}	–	–	3	µA	V_{OUTx} = 13.5 V, T_j = 150°C [2)]	P_6.1.14
Output channel 2							
On resistance	R_{OUTx_on}	–	1.1	1.2	Ω	I_{OUTx_nom} = 0.3 A, T_j = 150°C	P_6.2.1
Over-current switch off threshold	I_{OUTx_oc}	3	–	6.5	A		P_6.2.2
Over-current switch off filter time	$t_{oc,f}$	0.5	–	3	µs		P_6.2.3
Over-current switch off time	$t_{oc,off}$	3	–	8	ms		P_6.2.4
Over-current status time	$t_{oc,St}$	1	–	12	ms		P_6.2.5
Over temperature switch off	T_{OT}	150	–	200	°C		P_6.2.6

Table 6 Electrical characteristics: power stage (cont'd)

V_S = 13.5 V, T_j = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Over temperature hysteresis	$T_{OT,Hys}$	–	20	–	°C		P_6.2.7
Turn on delay time	$t_{d,ON}$	–	0.6	1.2	µs	V_{OUTx} = 13.5 V, I_{OUTx} = 1.3 A, resistive load [1)]	P_6.2.8
Turn off delay time	$t_{d,OFF}$	–	0.7	1.5	µs	V_{OUTx} = 13.5 V, I_{OUTx} = 1.3 A, resistive load [1)]	P_6.2.9
Turn on time	$t_{s,ON}$	–	0.4	1	µs	V_{OUTx} = 13.5 V, I_{OUTx} = 1.3 A, resistive load [1)]	P_6.2.10
Turn off time	$t_{s,OFF}$	–	0.4	1	µs	V_{OUTx} = 13.5 V, I_{OUTx} = 1.3 A, resistive load [1)]	P_6.2.11
Output leakage current in off mode	I_{OUTx_off}	–	–	3	µA	V_{OUTx} = 13.5 V, T_j = 150°C	P_6.2.12
Output channel 4 and 5							
On resistance	R_{OUTx_on}	–	3.3	3.6	Ω	I_{OUTx_nom} = 0.3 A, T_j = 150°C	P_6.3.1
Output clamping voltage	V_{OUTx_cl}	30	35	40	V	I_{OUTx} = 0.02 A	P_6.3.2
Over-current switch off threshold	I_{OUTx_oc}	350	–	600	mA		P_6.3.3
Over-current switch off filter time	$t_{oc,f}$	0.8	–	2.4	µs		P_6.3.4
Over temperature switch off	T_{OT}	150	–	200	°C		P_6.3.5
Over temperature hysteresis	$T_{OT,Hys}$	–	20	–	°C		P_6.3.6
Open load in off detection threshold	$V_{ol,th}$	2	2.8	3.2	V		P_6.3.7
Open load in off pull down diagnosis current	I_{ol}	50	100	150	µA	V_{OUTx} = 13.5 V	P_6.3.8
Open load in off diagnosis delay time	$t_{ol,d}$	100	–	200	µs		P_6.3.9
Turn on delay time	$t_{d,ON}$	–	0.5	1.2	µs	V_{OUTx} = 13.5 V, I_{OUTx} = 0.3 A, resistive load[1)]	P_6.3.10
Turn off delay time	$t_{d,OFF}$	–	0.7	1.5	µs	V_{OUTx} = 13.5 V, I_{OUTx} = 0.3 A, resistive load[1)]	P_6.3.11
Turn on time	$t_{s,ON}$	–	0.1	0.8	µs	V_{OUTx} = 13.5 V I_{OUTx} = 0.3 A, resistive load[1)]	P_6.3.12
Turn off time	$t_{s,OFF}$	–	0.1	0.8	µs	V_{OUTx} = 13.5 V, I_{OUTx} = 0.3 A, resistive load [1)]	P_6.3.13

Table 6 Electrical characteristics: power stage (cont'd)

V_S = 13.5 V, T_j = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output leakage current in off mode	I_{OUTx_off}	–	–	2	µA	V_{OUTx} = 13.5 V, T_j = 150°C 2)	P_6.3.14
Input characteristic IN1 and IN3							
Low level input voltage	$V_{IN,L}$	–	–	1	V		P_6.4.1
High level input voltage	$V_{IN,H}$	2	–	–	V		P_6.4.2
Input voltage hysteresis	$V_{IN,Hys}$	50	110	250	mV		P_6.4.3
Pull down current	$I_{IN,PD}$	20	50	100	µA	V_{IN} = 5 V	P_6.4.4
Pull down current	$I_{IN,PD}$	2.4	–	–	µA	V_{IN} = 0.6 V	P_6.4.5

1) Definition of timing see **Figure 7** or **Figure 8**.

2) In OFF mode open load diagnosis pull down current active.

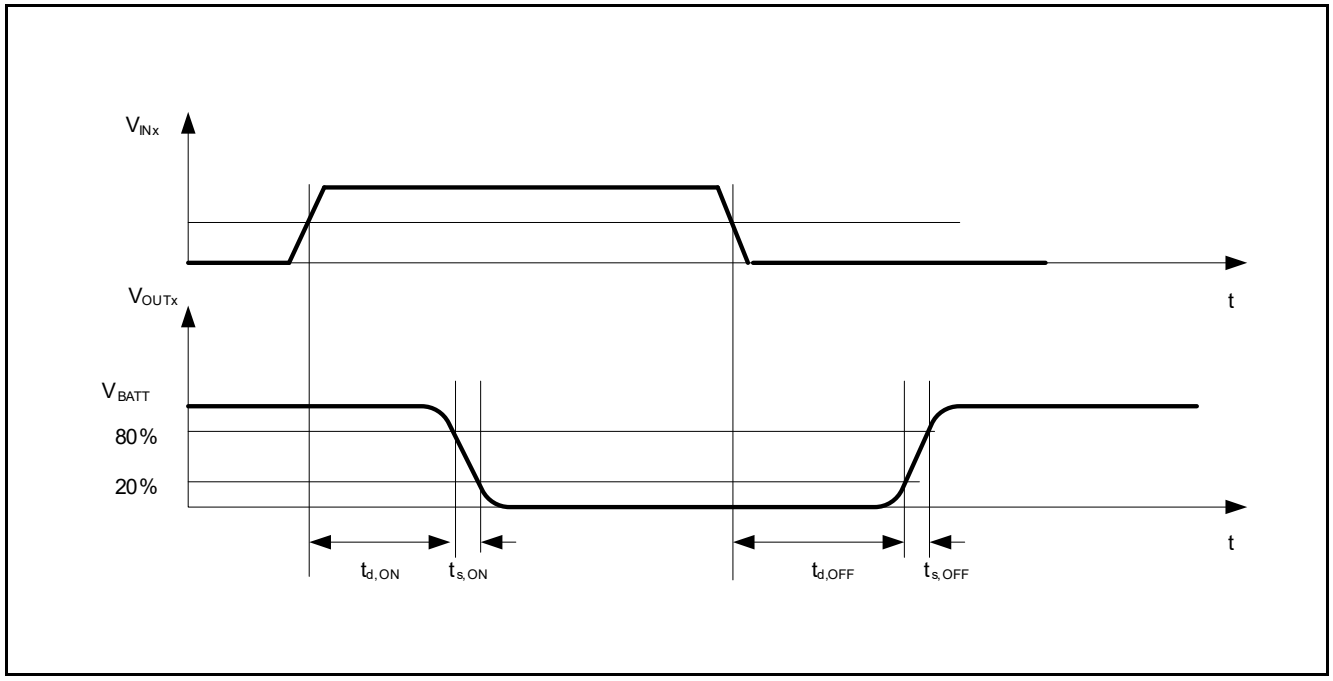


Figure 7 Timing low side switches channel 1 and 3

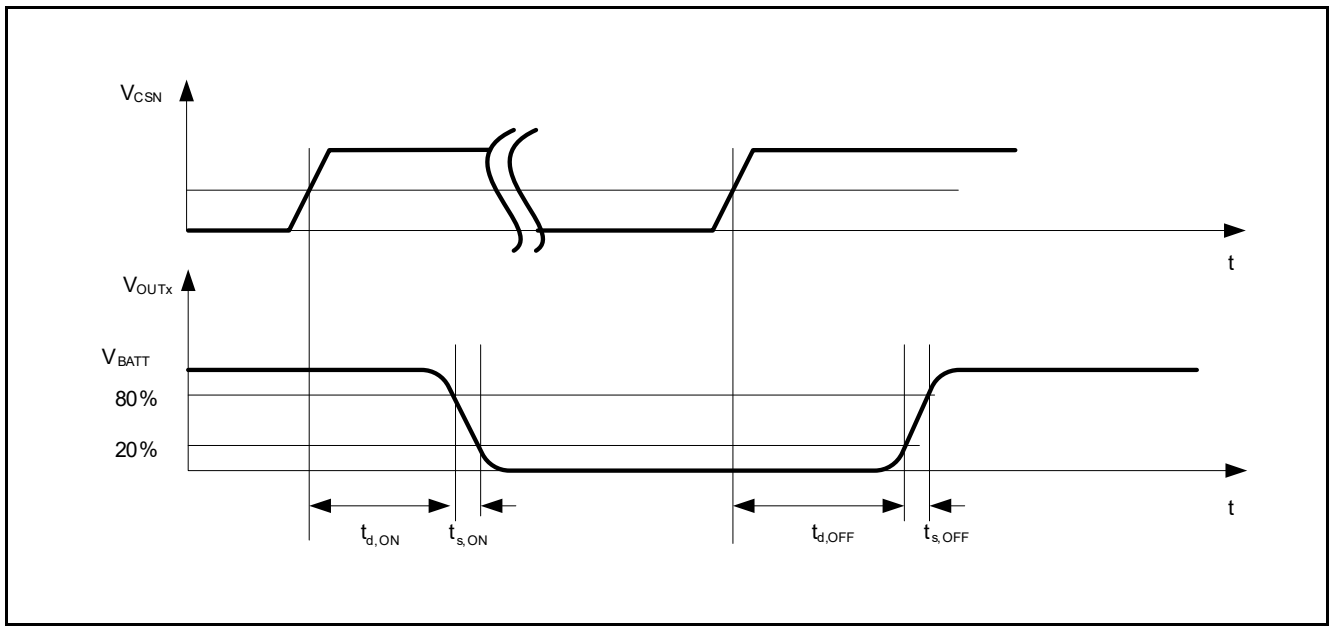


Figure 8 Timing low side switches channel 2, 4 and 5

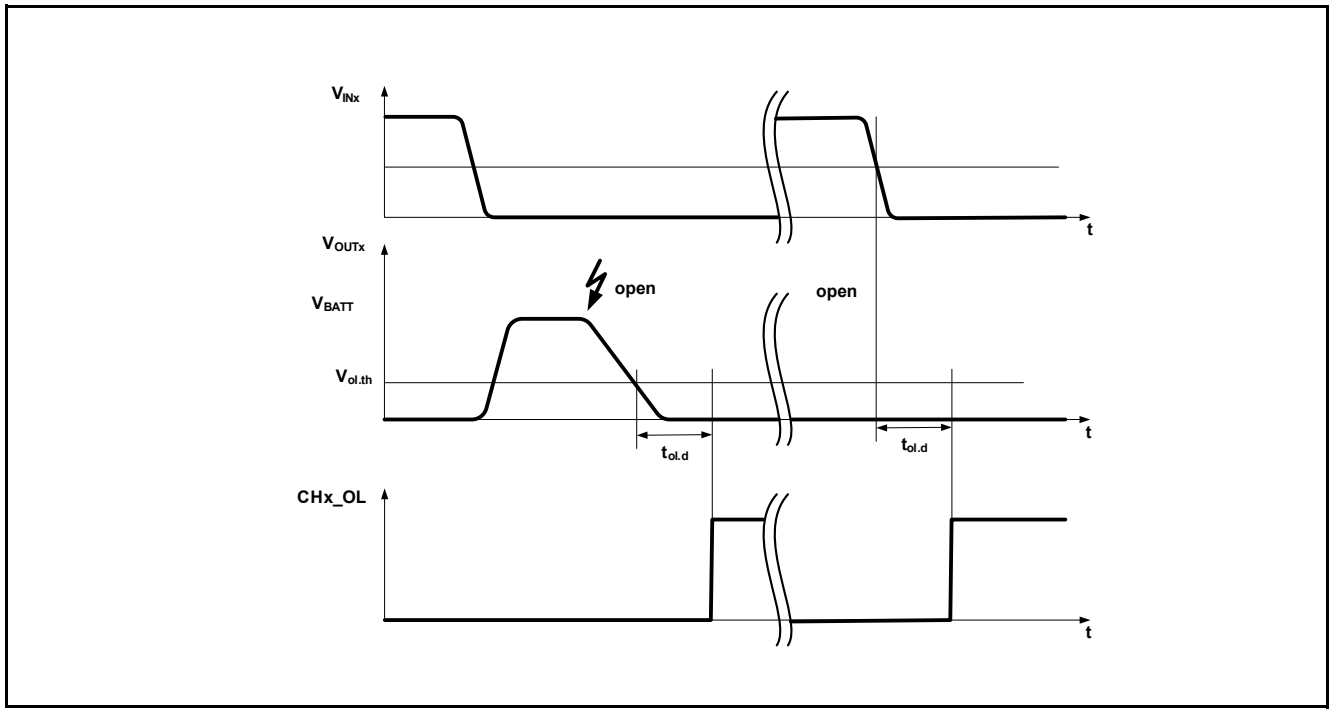


Figure 9 Timing open load/short to GND in off detection channel 1 and 3

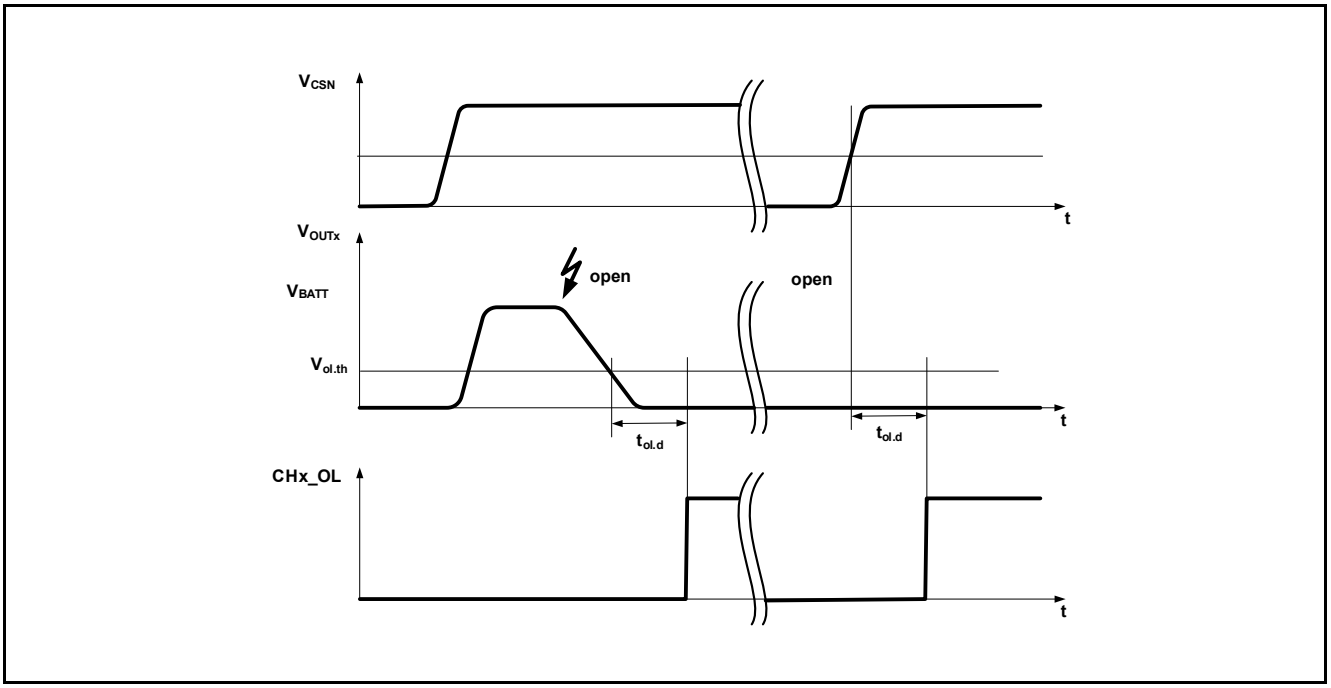


Figure 10 Timing open load/short to GND in off detection channel 2, 4 and 5

7 Variable reluctance sensor (VRS) interface

The variable reluctance (VR) sensor interface converts an output signal of a VR sensor into a logic level signal suited for µC 5 V input ports. The voltage difference between the two input pins, **VR_IN1** and **VR_IN2**, which are connected to the two output pins of the VR sensor, is detected and the output pin **VR_OUT** is switched depending on the sign of the voltage difference (see **Figure 12**). The amplitude of the VR sensor signal is limited by an internal clamping circuit to avoid damage of the device due to over voltage caused by the VR sensor signal.

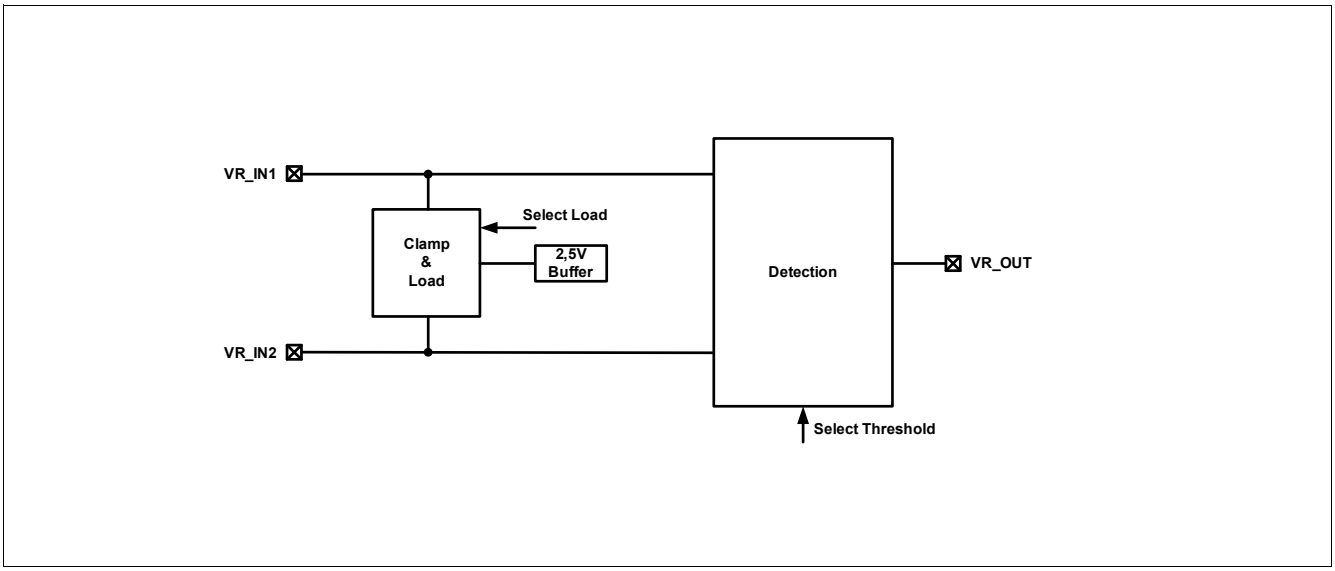


Figure 11 VR sensor interface block diagram

7.1 Electrical characteristics VR sensor interface

Table 7 Electrical Characteristics: VR Sensor Interface

V_S = 13.5 V, T_j = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input characteristics:							
Positive VR sensor interface detection threshold	V_{VR,th_pos}	-30	0	30	mV		P_7.1.1
Negative VR sensor interface detection threshold	V_{VR,th_neg}	-80	-50	-20	mV	CMD Register: VR_T[1:0] = “00” Reset State	P_7.1.2
Negative VR sensor interface detection threshold		-130	-100	-70	mV	CMD Register: VR_T[1:0] = “01”	P_7.1.3
Negative VR sensor interface detection threshold		-550	-500	-450	mV	CMD Register: VR_T[1:0] = “10”	P_7.1.4
Negative VR sensor interface detection threshold		-1.1	-1	-0.9	V	CMD Register: VR_T[1:0] = “11”	P_7.1.5
VR sensor interface load selection	$R_{VR,Load}$	30	75	120	kΩ	T_j = 25°C, CMD Register: VR_L[1:0] = “00” Reset State	P_7.1.6
			90		kΩ	T_j = -40°C, CMD Register: VR_L[1:0] = “00” Reset State	
			60		kΩ	T_j = 150°C, CMD Register: VR_L[1:0] = “00” Reset State	
VR sensor interface load selection		3	4.5	8	kΩ	CMD Register: VR_L[1:0] = “01”	P_7.1.7
VR sensor interface load selection		1.5	2.2	3.3	kΩ	CMD Register: VR_L[1:0] = “10”	P_7.1.8
VR sensor interface load selection		0.7	1.2	1.9	kΩ	CMD Register: VR_L[1:0] = “11”	P_7.1.9
VR sensor interface input clamping current	$I_{VR,clamp}$	–	–	±50	mA		P_7.1.10
VR sensor interface input clamping voltage	$V_{VR,clamp}$	±2.5	±3	±3.5	V	$I_{VR,clamp}$ = ±50 mA	P_7.1.11

Table 7 Electrical Characteristics: VR Sensor Interface (cont'd)

V_S = 13.5 V, T_j = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output characteristics:							
Low level output voltage	$V_{VR\_OUT,L}$	–	–	0.3	V	I_{VR_OUT} = 100 µA	P_7.2.1
High level output voltage	$V_{VR\_OUT,H}$	V5DD -0.3	–	–	V	I_{VR_OUT} = -100 µA	P_7.2.2
Transfer characteristics:							
Delay time input to VR_OUT falling edge	t_{dr}	1	1.5	2.5	µs		P_7.3.1
Delay time input to VR_OUT rising edge	t_{df}	1	1.5	2.5	µs		P_7.3.2

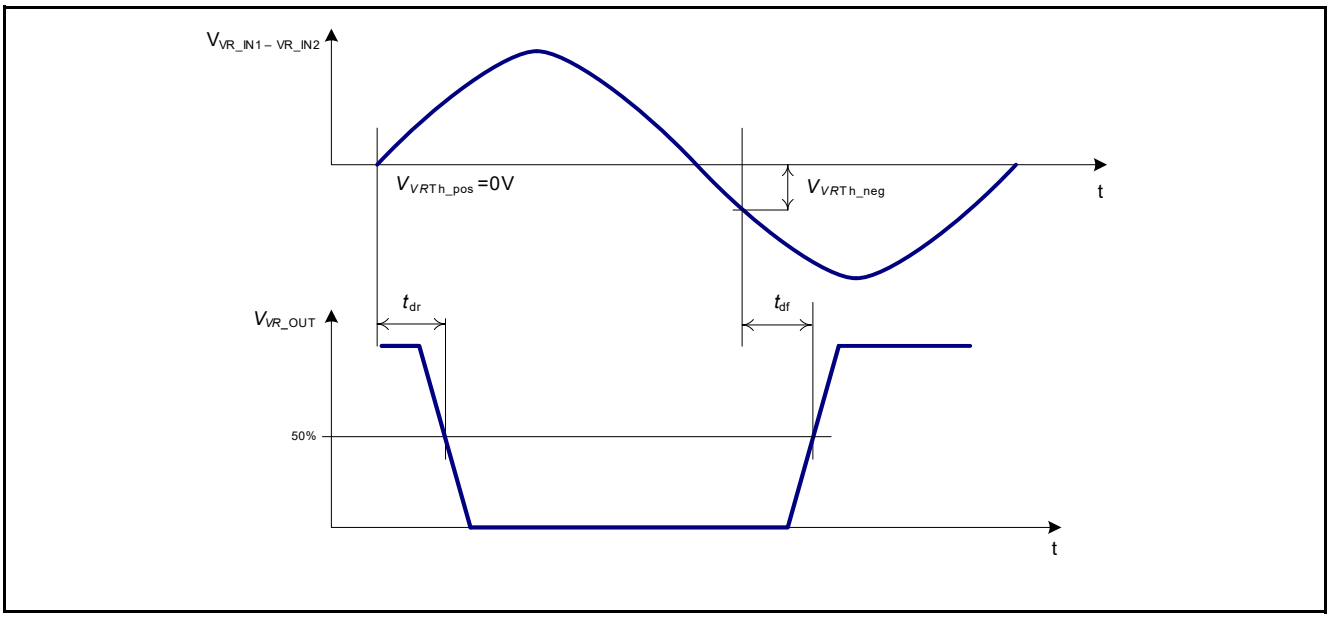


Figure 12 Timing characteristics of the VR sensor interface

8 Serial peripheral interface (SPI)

The diagnosis and control interface is based on a serial peripheral interface (SPI).
The SPI is a 16 bit full duplex synchronous serial slave interface, which uses four lines: **SI**, **SO**, **SCLK** and **CSN**.

8.1 SPI signal description

CSN - chip select:
The system micro controller selects the IC by means of the **CSN** pin. Whenever the pin is in low state, data transfer can take place. As long as **CSN** is in high state, all signals at the **SCLK** and **SI** pins are ignored and **SO** is forced to high impedance.

CSN - High to Low Transition:
SO changes from high impedance to high or low state depending on the Status Flag (see **Chapter 8.2**).

CSN - Low to High Transition:
End of transmission, the validation check of the communication is done (number of bits and valid command) and valid commands are executed.

SCLK - serial clock:
This input pin clocks the internal shift register. The serial input (SI) transfers data into the shift register on the falling edge of SCLK while the serial output (SO) shifts information out on the rising edge of the serial clock. It is essential that the SCLK pin is in low state whenever chip select CSN makes any transition.

SI - serial input:
Serial input data bits are shifted in at this pin, the most significant bit (MSB) first. SI information is read on the falling edge of SCLK. Please refer to **Section 8.2** for further information.

SO - serial output:
Data is shifted out serially at this pin, the MSB first. SO is in high impedance until the CSN pin goes to low. The output level before the first rising edge of SCLK depends on the status flag. New data will appear at the SO pin following the rising edge of SCLK. Please refer to **Section 8.2** for further information.

8.2 SPI protocol

The principle of the SPI communication is shown in **Figure 13**. The message from the micro controller must be sent MSB first. The data from the **SO** pin is sent MSB first. The TLE8080EM samples data from the SI pin on the falling edge of SCLK and shifts data out of the SO pin on the rising edge of SCLK. Each access must be terminated by a rising edge of CSN.

All SPI messages must be exactly 16-bits long, otherwise the SPI message is discarded.
There is a one message delay in the response to each message (i.e. the response for message N will be returned during message N+1).

The SPI protocol of the TLE8080EM provides three registers. The control register, the diagnosis, and the status register. The control register contains the set up bits for the VR sensor interface and the control bits of channels 2, 4 and 5. The diagnosis register contains the diagnosis bits of the five low side switches. The status register contains the status bits of the five low side switches, the watchdog status bit, and the watchdog time out bit. After power-on reset, all register bits are set to reset state (see **Chapter 8.2.1**).

There are four ways of valid access:

- Write access to the command register: the answer is 1 for the R/W bit, 00 for the address and the content of the register
- Read access to the command register: the answer is 0 for the R/W bit, 00 for the address and the content of the register
- Read access to the diagnosis register: the answer is 0 for the R/W bit, 01 for the address and the content of the register
- Read access to the status register: the answer is 0 for the R/W bit, 10 for the address and the content of the register

Any other access is recognized as an invalid message.

Status flag Indication: after the falling edge of **CSN** and before the first rising edge of **SCLK**, the level of the **SO** indicates the status of the diagnosis register:

- **SO** = “0”: no error condition detected; all diagnosis register bits are “0”
- **SO** = “1”: one or more error conditions are detected; one or more diagnosis register bits are “1”

With this feature during every SPI communication a check of the diagnosis status can be done without additional read access of the diagnosis register.

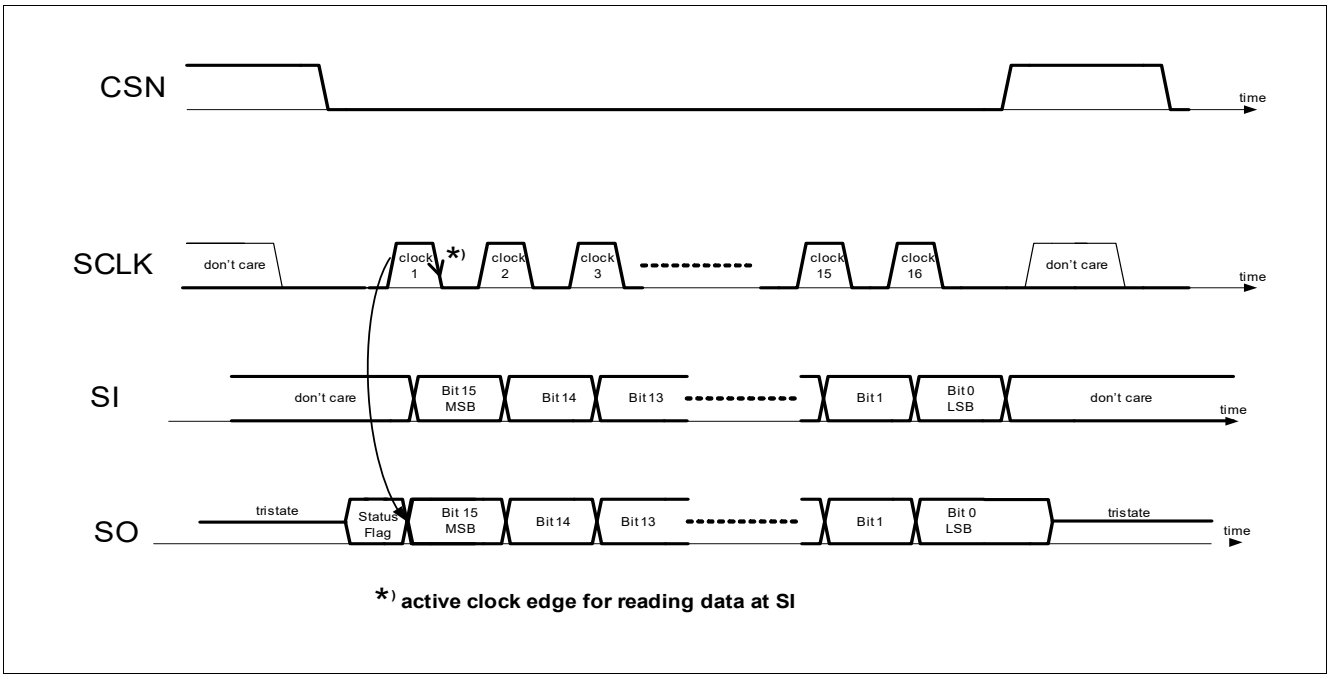


Figure 13 SPI Pprotocol

SPI answers:

- during power on reset: SPI commands are ignored, SO is always low
- after power on reset: the content of the command register is transmitted with the next SPI transmission
- during watchdog reset: SPI commands are ignored, SO has the value of the status flag
- after watchdog overflow: the content of the status register is transmitted with the first SPI transmission after the low to high transition of NRO

- after a read or write command: the content of the selected register is transmitted with the next SPI transmission
- after an invalid communication: the content of the diagnosis register is transmitted with the next SPI transmission

8.2.1 SPI register

Overview

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{R}$/W	**AD1**	**AD0**													

Field	Bits	Type	Description
AD1:AD0	[14:13]	w	**Address Bits:** 00_B Control Register 01_B Diagnosis Register 10_B Status Register
$\overline{R}$/W	15	w	**Read - Write Bit:** 0_B Read Access 1_B Write Access

CMD Register

Command Register (Identifier x00x xxxx xxxx xxxx$_B$) **Reset Value: 0_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{R}$/W	**AD1**	**AD0**	**VR_T1**	**VR_T0**	**VR_L1**	**VR_L0**							**CTR5**	**CTR4**	**CTR2**
			rw	rw	rw	rw							rw	rw	rw

Field	Bits	Type	Description
CTR2	0	rw	**Control Bit Channel 2:** 0_B Channel 2 is switched off (Reset State) 1_B Channel 2 is switched on
CTR4	1	rw	**Control Bit Channel 4:** 0_B Channel 4 is switched off (Reset State) 1_B Channel 4 is switched on
CTR5	2	rw	**Control Bit Channel 5:** 0_B Channel 5 is switched off (Reset State) 1_B Channel 5 is switched on

Field	Bits	Type	Description
VR_L1: VR_L0	[10:9]	rw	**Load Register of VR Interface:** (c.f. **VR sensor interface load selection**) 00_B R_{Load} = **75**kΩ (Reset State) 01_B R_{Load} = **4.5**kΩ 10_B R_{Load} = **2.2**kΩ 11_B R_{Load} = **1.2**kΩ
VR_T1: VR_T0	[12:11]	rw	**Threshold Register of VR Interface:** 00_B **-50**mV (Reset State) 01_B **-100**mV 10_B **-500**mV 11_B **-1**V

Diag Register

Diagnosis Register (Identifier x01x xxxx xxxx xxxx$_B$) **Reset Value: 0_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{R}$/W	**AD1**	**AD0**	**CH45_OT**	**CH5_OC**	**CH5_OL**	**CH4_OC**	**CH4_OL**	**CH3_OT**	**CH3_OC**	**CH3_OL**	**CH2_OT**	**CH2_OC**	**CH1_OT**	**CH1_OC**	**CH1_OL**
			r	r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
CH1_OL	0	r	**Open Load Diagnosis Bit of Channel 1:** 0_B no open load in off detected (Reset State) 1_B open load in off detected
CH1_OC	1	r	**Over Current Diagnosis Bit of Channel 1:** 0_B no over current detected (Reset State) 1_B over current detected
CH1_OT	2	r	**Over Temperature Diagnosis Bit of Channel 1:** 0_B no over temperature detected (Reset State) 1_B over temperature detected
CH2_OC	3	r	**Over Current Diagnosis Bit of Channel 2:** 0_B no over current detected (Reset State) 1_B over current detected
CH2_OT	4	r	**Over Temperature Diagnosis Bit of Channel 2:** 0_B no over temperature detected (Reset State) 1_B over temperature detected
CH3_OL	5	r	**Open Load Diagnosis Bit of Channel 3:** 0_B no open load in off detected (Reset State) 1_B open load in off detected
CH3_OC	6	r	**Over Current Diagnosis Bit of Channel 3:** 0_B no over current detected (Reset State) 1_B over current detected

Field	Bits	Type	Description
CH3_OT	7	r	**Over Temperature Diagnosis Bit of Channel 3:** 0_B no over temperature detected (Reset State) 1_B over temperature detected
CH4_OL	8	r	**Open Load Diagnosis Bit of Channel 4:** 0_B no open load in off detected (Reset State) 1_B open load in off detected
CH4_OC	9	r	**Over Current Diagnosis Bit of Channel 4:** 0_B no over current detected (Reset State) 1_B over current detected
CH5_OL	10	r	**Open Load Diagnosis Bit of Channel 5:** 0_B no open load in off detected (Reset State) 1_B open load in off detected
CH5_OC	11	r	**Over Current Diagnosis Bit of Channel 5:** 0_B no over current detected (Reset State) 1_B over current detected
CH45_OT	12	r	**Over Temperature Diagnosis Bit of Channel 4 and 5:** 0_B no over temperature detected (Reset State) 1_B over temperature detected

Stat Register

Status Register (Identifier x10x xxxx xxxx xxxx$_B$) **Reset Value: 0_H**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{R}$/W	AD1	AD0	WD_DIS	WD_TO							ST5	ST4	ST3	ST2	ST1
			r	r							r	r	r	r	r

Field	Bits	Type	Description
ST1	0	r	**Status Bit Channel 1:** 0_B Channel 1 is switched off (Reset State) 1_B Channel 1 is switched on
ST2	1	r	**Status Bit Channel 2:** 0_B Channel 2 is switched off (Reset State) 1_B Channel 2 is switched on
ST3	2	r	**Status Bit Channel 3:** 0_B Channel 3 is switched off (Reset State) 1_B Channel 3 is switched on
ST4	3	r	**Status Bit Channel 4:** 0_B Channel 4 is switched off (Reset State) 1_B Channel 4 is switched on
ST5	4	r	**Status Bit Channel 5:** 0_B Channel 5 is switched off (Reset State) 1_B Channel 5 is switched on

Field	Bits	Type	Description
WD_TO	11	r	**Watchdog Time Out Bit:** 0_B no watchdog time out 1_B watchdog time out occurred
WD_DIS	12	r	**Watchdog Status Bit:** 0_B Watchdog enabled (V_{WD_DIS} = 0V) 1_B Watchdog disabled (V_{WD_DIS} = 5V)

8.2.2 Set and reset of diagnosis register bits

Set of the over current diagnosis bits of channels 1, 3, 4 and 5:

The over current diagnosis bits of channels 1, 3, 4 and 5 are set asynchronously of the internal clock with the output signal of the detection circuit (details see **Chapter 6.1**).

Reset of the over current diagnosis bits of channels 1 and 3:

- Diagnosis register was read out:
  - input pin INx remains high: **no reset** of the over current diagnosis bit, the channel remains switched off
  - input pin INx transition from high to low: the over current diagnosis bit is **reset,** the channel could be switched on again
- Diagnosis register was not read out
  - channel remains **switched off and no reset** of the over current diagnosis bit is done
  - input pin INx is low: with the next read access of the diagnosis register the diagnosis bits are reset

Reset of the over current diagnosis bits of channels 4 and 5:

- Diagnosis register was not read out
  - channel remains **switched off and no reset** of the over current diagnosis bit is done
- Diagnosis register was read out:
  - SPI command register write command is not sent: **no reset** of the over current diagnosis bit, the channel remains switched off
  - SPI command register write command is sent: the over current diagnosis bit is **reset,** the channel will be switched according the status of the control bit

Set and Reset of the over current diagnosis bit of channel 2:

The over current diagnosis register bit for channel 2 is set asynchronously of the internal clock with the output signal of the detection circuit. With this signal the output is switched off and the counter for the off time $t_{oc,off}$ of the repetitive switching cycle starts. After $t_{oc,off}$ the channel will be switched on again. With an remaining over current condition the channel will be switched on repetitively. This internal overcurrent status of the channel is latched internally. The internal over current status is reset in two situations.

- over current condition exists no longer: the internal over current status is reset after the time $t_{oc,St}$
- over current condition remains and the channel is switched off: the internal over current status is reset after the time $t_{oc,off}$

The reset of the over current diagnosis register bit for channel 2 is related to the internal over current status. In **Figure 14** and **Figure 15** the behavior of the diagnosis with temporary and permanent over current condition is drawn.

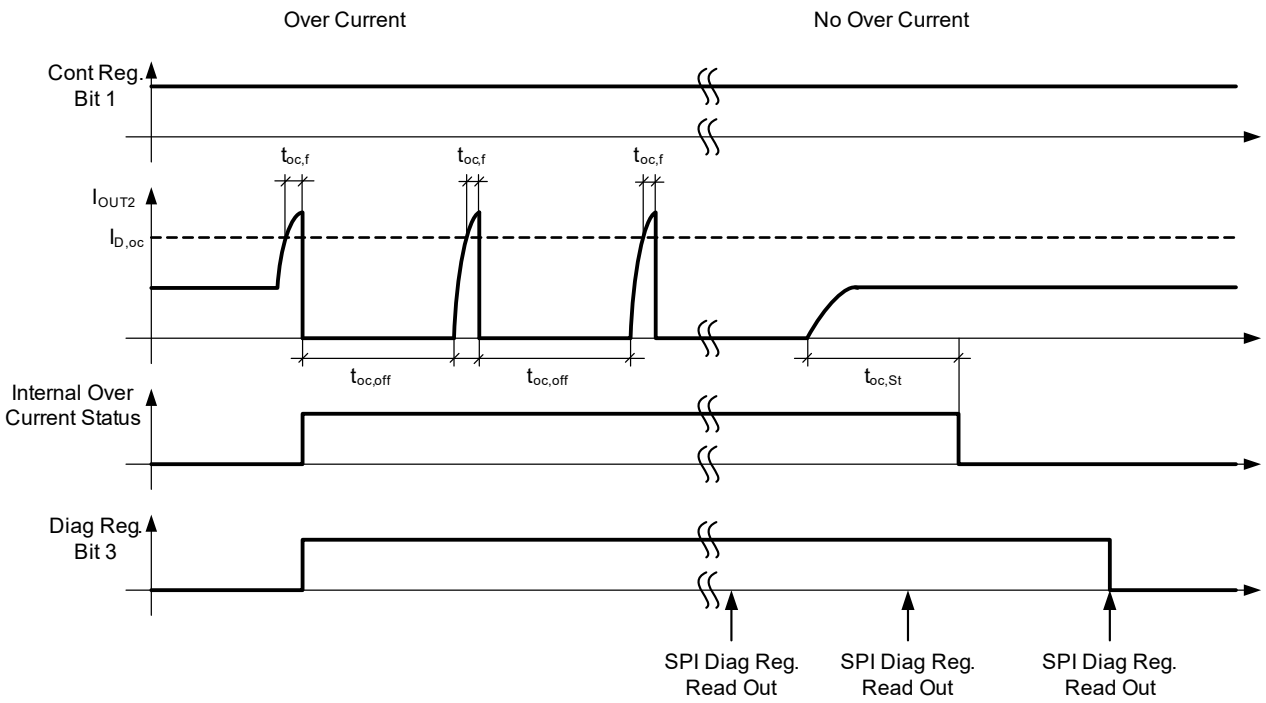


Figure 14 Behavior of diagnosis with temporary over current condition at channel 2

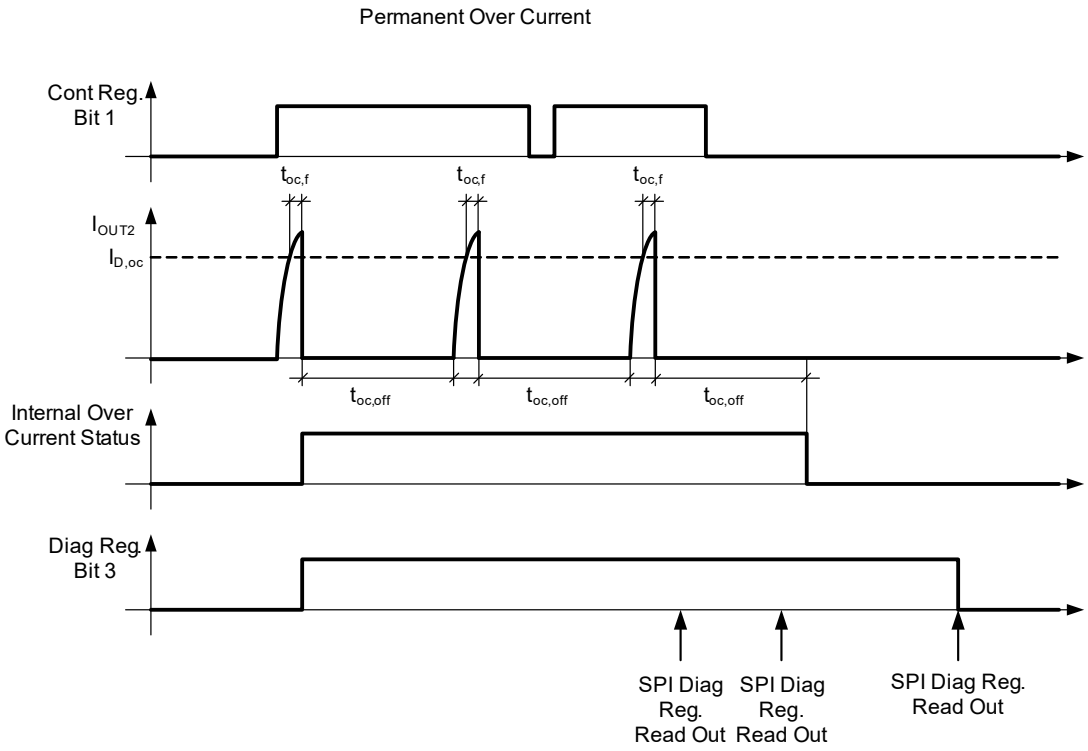


Figure 15 Behavior if diagnosis with permanent over current condition at channel 2

Reset of the over temperature diagnosis bits:

The over temperature diagnosis bits will be reset with read access of the diagnosis register if no over temperature condition is detected.

Reset of the open load in off diagnosis bits:

The open load in off diagnosis bits will be reset with read access of the diagnosis register if no open load condition is detected.

8.3 Electrical characteristics SPI

Table 8 Electrical characteristics: SPI

V_S = 13.5 V, T_j = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input characteristics (CSN, SCLK, SI):							
Low level input voltage	$V_{x,L}$	–	–	1	V		P_8.1.1
High level input voltage	$V_{x,H}$	2	–	–	V		P_8.1.2
Hysteresis	$V_{x,Hys}$	50		250	mV		
Pull up current CSN	$I_{x,pu}$	-25	-50	-100	µA	at V_{IN} = 0 V	P_8.1.3
Pull up current CSN	$I_{x.pu}$	-25	–	–	µA	at V_{IN} = V_{V5DD} - 0.6 V	P_8.1.4
Pull down current SCLK, SI	$I_{x,pu}$	20	50	100	µA	at V_{IN} = V_{V5DD}	P_8.1.5
Pull down current SCLK, SI	$I_{x.pu}$	2.4	–	–	µA	at V_{IN} = 0.6 V	P_8.1.6
Output characteristics (SO):							
Low level output voltage	$V_{So,L}$	–	–	0.4	V	I_x = 100 µA	P_8.2.1
High level output voltage	$V_{SO,H}$	V5DD -0.4	–	–	V	I_x = -100 µA	P_8.2.2
Output high impedance leakage current	$I_{SO,TRI}$	-3	–	3	µA	0 V < V_{SO} < 5 V	P_8.2.3
Timings:							
Lead time	t_1	210	–	–	ns	CSN falling to SCLK rising	P_8.3.1
Lag time	t_2	75	–	–	ns	SCLK falling to CSN rising	P_8.3.2
CSN high time	t_3	550	–	–	ns	CSN rising to CSN falling	P_8.3.3
Period of SCLK	t_4	200	–	–	ns		P_8.3.4
SCLK to CSN set up time	t_5	10	–	–	ns	SCLK falling to CSN falling	P_8.3.5
SCLK low time	t_7	60	–	–	ns		P_8.3.6
CSN to SCLK hold time	t_8	15	–	–	ns	CSN rising to SCLK rising	P_8.3.7
SI set up time	t_9	30	–	–	ns	SI set up time to SCLK falling	P_8.3.8
SI hold up time	t_{10}	30	–	–	ns	SI holdup time after SCLK falling	P_8.3.9
SO enable time	t_{11}	–	–	165	ns	CSN falling to SO active	P_8.3.10
SO valid time	t_{12}	–	–	120	ns	SO data valid after SCLK rising	P_8.3.11
SO disable time	t_{13}	–	–	165	ns	SO high impedance after CSN rising	P_8.3.12
Number of clock pulses while CSN = low		16	–	16	pulses		P_8.3.13

Table 8 Electrical characteristics: SPI (cont'd)

V_S = 13.5 V, T_j = -40°C to +150°C: All voltages with respect to ground. Positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SO rise time	t_{SO_rise}	–	–	75	ns	20% to 80%, C_{load}=1.6 pF	P_8.3.14
SO fall time	t_{SO_fall}	–	–	75	ns	80% to 20% C_{load}=1.6 pF	P_8.3.15

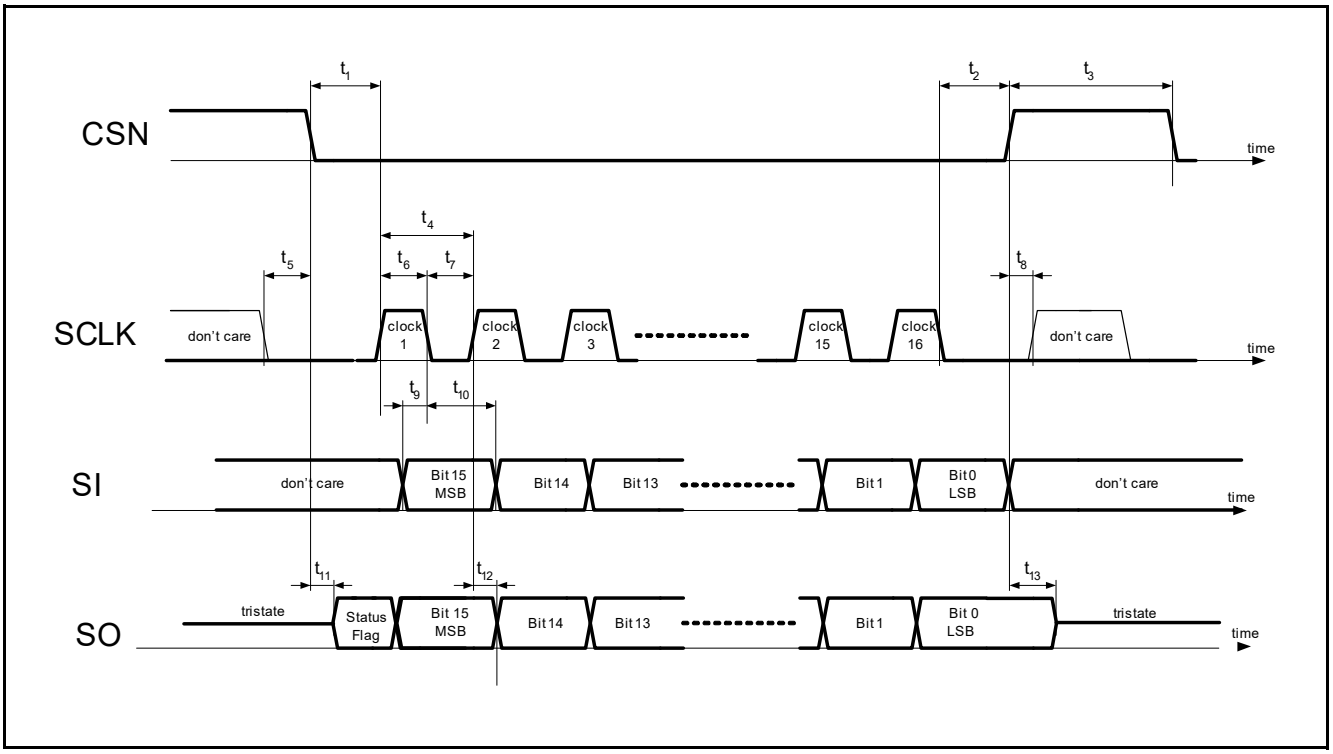


Figure 16 SPI timing diagram

9 K-line

9.1 K-line

The K-line module is a serial link bus interface device designed to provide bi-directional half-duplex communication interfacing. It is designed to interface vehicles via the special ISO K-line and meets the ISO standard 9141. The device's K-line bus driver's output is protected against bus shorts.

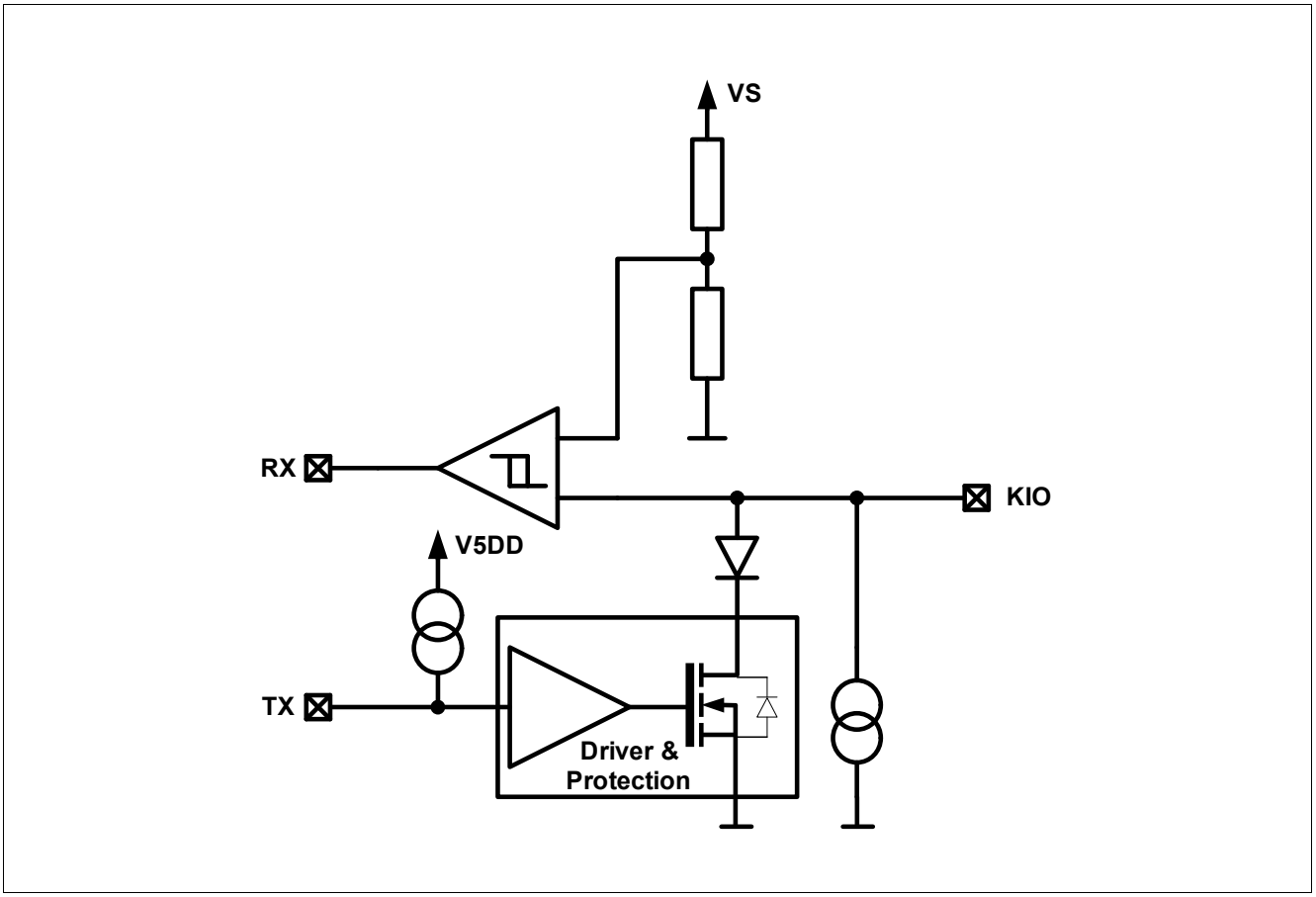


Figure 17 K-line block diagram

9.2 Electrical characteristics K-line

Table 9 Electrical characteristics: K-line

V_S = 13.5 V, T_j = -40°C to +150°C: All voltages with respect to ground.
Positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output RX							
Low level output voltage	$V_{RX,L}$	–	–	0.4	V	I_{RX} = 100 µA	P_9.1.1
High level output voltage	$V_{RX,H}$	V5DD-0.4	–	–	V	I_{RX} = -100 µA	P_9.1.2
Input TX							
Low level input voltage	$V_{TX,L}$	–	–	1	V		P_9.2.1
High level input voltage	$V_{TX,H}$	3.2	–	–	V		P_9.2.2
Hysteresis	$V_{TX,Hys}$	280	500	700	mV		P_9.2.3
Pull up current	I_{PU_L}	-70	-100	-150	µA	at V_{TX} = 0 V	P_9.2.4
Pull up current	I_{PU_L}	-30	–	–	µA	at V_{TX} = V_{V5DD} - 0.6 V	P_9.2.5
K-Line bus driver input/output KIO							
Low level output voltage	$V_{KIO,O,L}$	–	–	1.4	V	TX = low, R_{KIO}= 480 Ω	P_9.3.1
Current limitation	$I_{KIO(lim)}$	40	–	140	mA		P_9.3.2
Low level input voltage	$V_{KIO,I,L}$	–	–	0.4*VS	V		P_9.3.3
High level input voltage	$V_{KIO,I,H}$	0.6*VS	–	–	V		P_9.3.4
Hysteresis	$V_{KIO,I,Hys}$	0.02 *VS	–	0.175 *VS	V		P_9.3.5
Pull down current	$I_{KIO,pd}$	5	10	15	µA		P_9.3.6
Transfer characteristics C_{RX} **= 25 pF;** R_{KIO} **= 540 Ω;** C_{KIO} **≤ 1.3 nF**							
Receive frequency	$f_{KIO,rec}$	–	–	500	kHz	C_{KIO} = 0 pF	P_9.4.1
Transmit frequency	$f_{KIO,tran}$	–	–	100	kHz		P_9.4.2
Delay time KIO -> RX rising edge[1)]	t_{drR}	0.05	–	0.5	µs	$C_{RX,load}$ = 1.6 pF	P_9.4.3
Delay time KIO -> RX falling edge[1)]	t_{dfR}	0.05	–	0.5	µs	$C_{RX,load}$ = 1.6 pF	P_9.4.4
Delay time TX -> KIO rising edge[1)2)]	t_{drT}	0.05	–	0.5	µs	$C_{KIO,load}$ = 1.6 pF	P_9.4.5
Delay time TX -> KIO falling edge[1)]	t_{dfT}	0.05	–	0.5	µs	$C_{KIO,load}$ = 1.6 pF	P_9.4.6

1) For definition see **Figure 18**.

2) Not subject of production test, behavior defined by external devices.

K-line

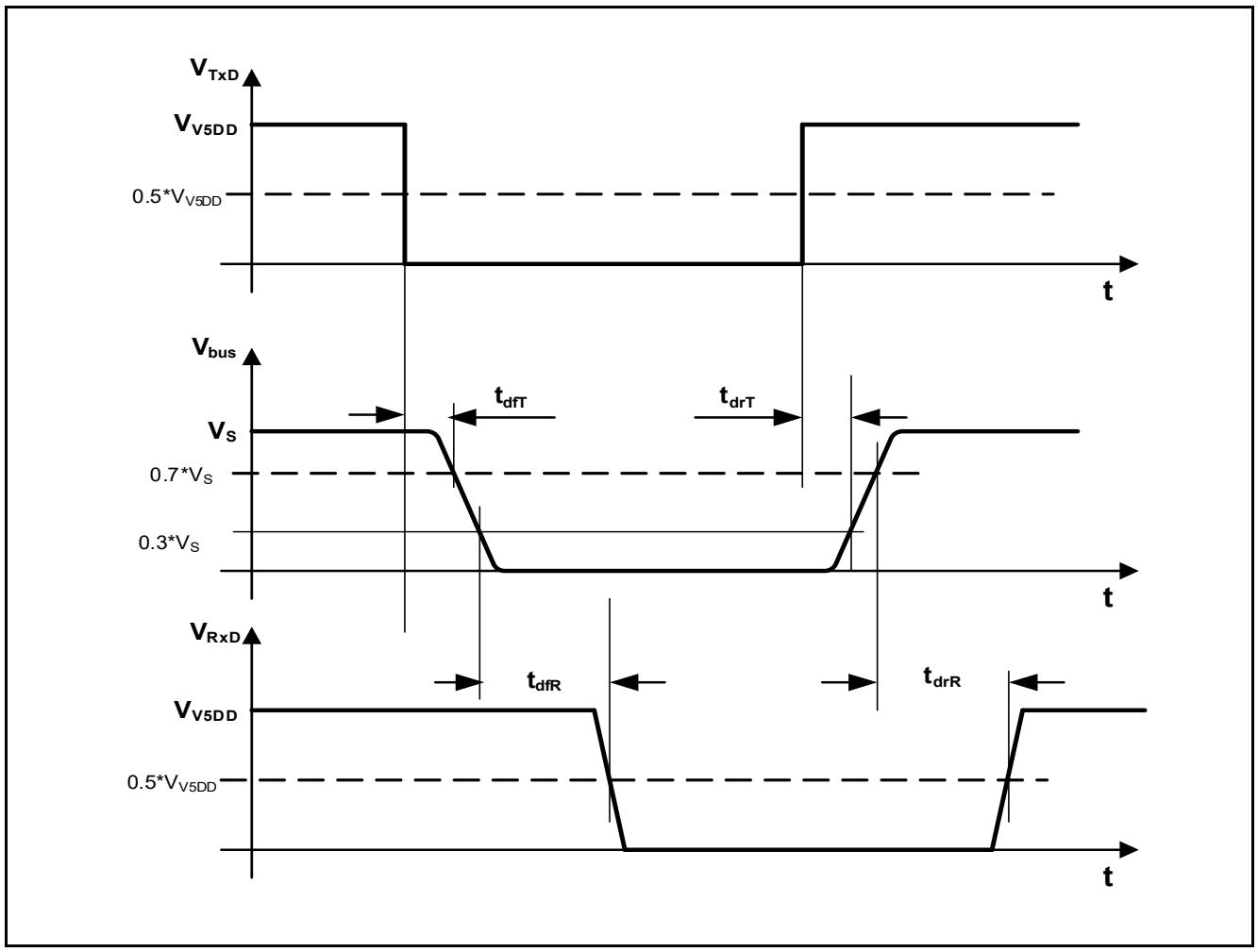


Figure 18 K-line transfer characteristics

10 Package outlines

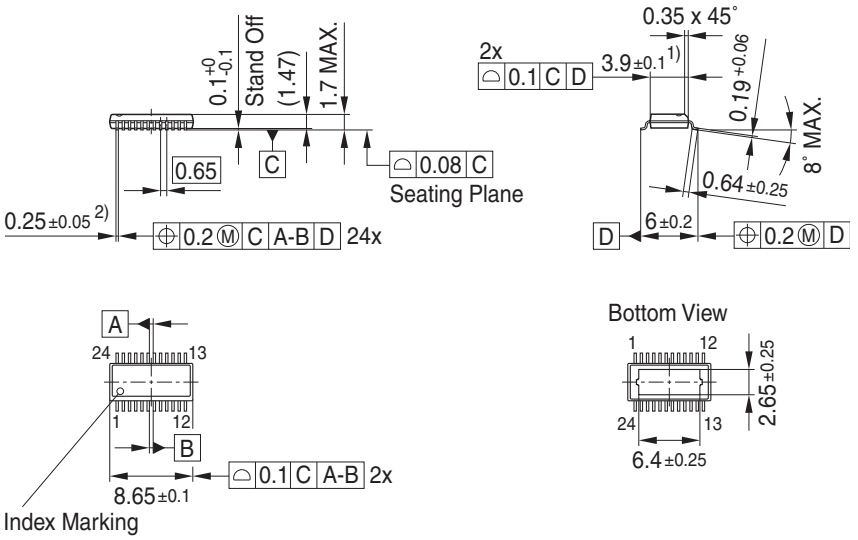


Figure 19 PG-SSOP24

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products, and to be compliant with government regulations, the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

11 Revision history

Revision	Date	Changes
1.0	2012-09-12	Data Sheet.
1.1	2012-12-19	Parameter **“Reset reaction time” on Page 12** increased.
1.2	2016-10-26	Added variant TLE8080-3EM.
		Parameter ”Low Drop Voltage” on Page 11 is spilt in P_5.1.10a and P.5.1.10b.
		Removed “50%” indicator for VCSN signals in **Figure 7**, **Figure 8**, **Figure 9** and **Figure 10**.
		Removed pin “KIO” from P_4.1.5 in **Table 1** as covered by P_4.1.8.
		Added “after a Diagnosis Read has been performed” to description of channel 4 and 5 over current status reset behavior.
		Editorial changes.
1.3	2021-01-15	Parameter updates and improvements: P_4.1.8: Maximum rating of KIO - minimum value reduced. P_4.5.1: V_S functional range increased. P_5.1.1: V_{DD} functional range condition increased. P:_5.1.3: Load regulation improved P:_5.1.4: Line regulation voltage range condition increased. P_5.1.11: Re-defintion of low drop operation, P_5.1.9, P_5.1.10a and P_5.1.10b removed, low drop resistance value added.
		Editorial changes.

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Do you have a question about any aspect of this document?
Email: erratum@infineon.com

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