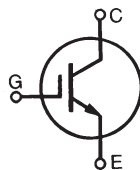


High Voltage IGBT

For Capacitor Discharge Applications

(Electrically Isolated Tab)

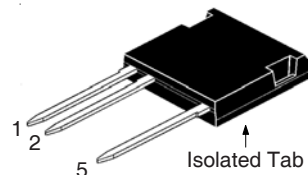
IXGF20N300



$$\begin{aligned} V_{CES} &= 3000V \\ I_{C25} &= 22A \\ V_{CE(sat)} &\leq 3.2V \end{aligned}$$

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^{\circ}C$ to $150^{\circ}C$	3000	V
V_{CGR}	$T_J = 25^{\circ}C$ to $150^{\circ}C$, $R_{GE} = 1M\Omega$	3000	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^{\circ}C$	22	A
I_{C90}	$T_C = 90^{\circ}C$	14	A
I_{CM}	$T_C = 25^{\circ}C$, $V_{GE} = 20V$, 1ms	103	A
SSOA (RBSOA)	$V_{GE} = 20V$, $T_{VJ} = 125^{\circ}C$, $R_G = 10\Omega$ Clamped Inductive Load	$I_{CM} = 200$ @ $0.8 \cdot V_{CES}$	A
P_C	$T_C = 25^{\circ}C$	100	W
T_J		-55 ... +150	$^{\circ}C$
T_{JM}		150	$^{\circ}C$
T_{stg}		-55 ... +150	$^{\circ}C$
T_L	1.6 mm (0.062 in.) from Case for 10s	300	$^{\circ}C$
T_{SOLD}	Plastic Body for 10s	260	$^{\circ}C$
F_C	Mounting Force	20..120/4.5..27	Nm/lb-in.
V_{ISOL}	50/60Hz, 1 Minute	4000	V~
Weight		6	g

ISOPLUS i4-Pak™



1 = Gate
2 = Emitter
5 = Collector

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V Electrical Isolation
- High Peak Current Capability
- Low Saturation Voltage
- Molding Epoxies Meet UL 94 V-0 Flammability Classification

Applications

- Capacitor Discharge
- Pulser Circuits

Advantages

- High Power Density
- Easy to Mount

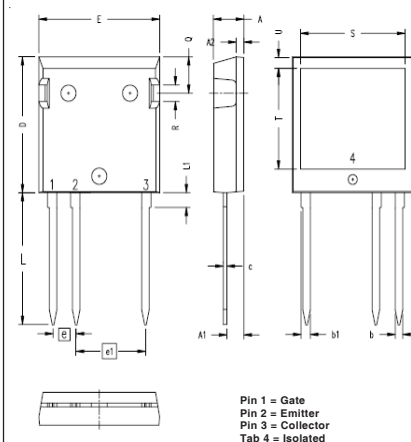
Symbol	Test Conditions ($T_J = 25^{\circ}C$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu A$, $V_{GE} = 0V$	3000		V
$V_{GE(th)}$	$I_C = 250\mu A$, $V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = 0.8 \cdot V_{CES}$, $V_{GE} = 0V$ Note 2, $T_J = 125^{\circ}C$			25 μA 2 mA
I_{GES}	$V_{CE} = 0V$, $V_{GE} = \pm 20V$			± 100 nA
$V_{CE(sat)}$	$I_C = 20A$, $V_{GE} = 15V$, Note 1			3.2 V

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$I_C = 20\text{A}$, $V_{CE} = 10\text{V}$, Note 1	8	12	S
$I_{C(ON)}$	$V_{GE} = 20\text{V}$, $V_{CE} = 20\text{V}$, Note 1		180	A
C_{ies}	$V_{CE} = 25\text{V}$, $V_{GE} = 0\text{V}$, $f = 1\text{MHz}$		1125	pF
C_{oes}			48	pF
C_{res}			16	pF
Q_g	$I_C = 20\text{A}$, $V_{GE} = 15\text{V}$, $V_{CE} = 600\text{V}$		31	nC
Q_{ge}			5.8	nC
Q_{gc}			12	nC
$t_{d(on)}$	Resistive Switching Times $I_C = 20\text{A}$, $V_{GE} = 15\text{V}$ $V_{CE} = 960\text{V}$, $R_G = 10\Omega$		38	ns
t_r			486	ns
$t_{d(off)}$			145	ns
t_f			210	ns
R_{thJC}			0.15	1.25°C/W
R_{thCS}				$^\circ\text{C/W}$
R_{thJA}			30	$^\circ\text{C/W}$

Notes:

1. Pulse test, $t < 300\mu\text{s}$, duty cycle, $d < 2\%$.
2. Device must be heatsunk for high-temperature leakage current measurements to avoid thermal runaway.

ISOPLUS i4-Pak™ (HV) Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.085	1.17	2.16
b	.045	.055	1.14	1.40
b1	.058	.068	1.47	1.73
C	.020	.029	0.51	0.74
D	.819	.840	20.80	21.34
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
e1	.450 BSC		11.43 BSC	
L	.780	.840	19.81	21.34
L1	.083	.102	2.11	2.59
Q	.210	.244	5.33	6.20
R	.100	.180	2.54	4.57
S	.660	.690	16.76	17.53
T	.590	.620	14.99	15.75
U	.065	.080	1.65	2.03

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

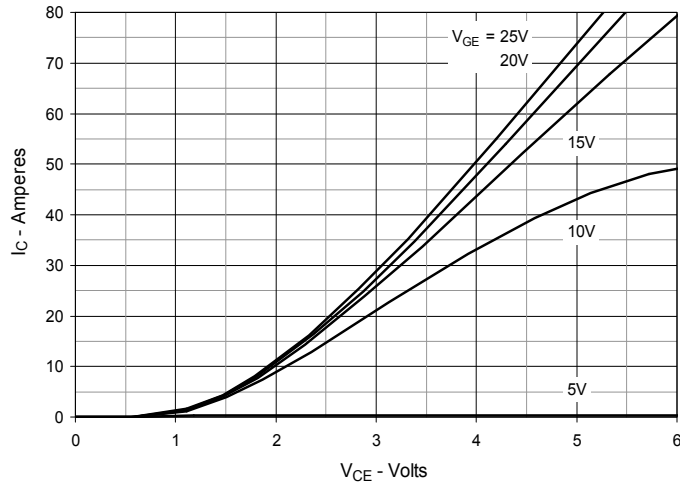
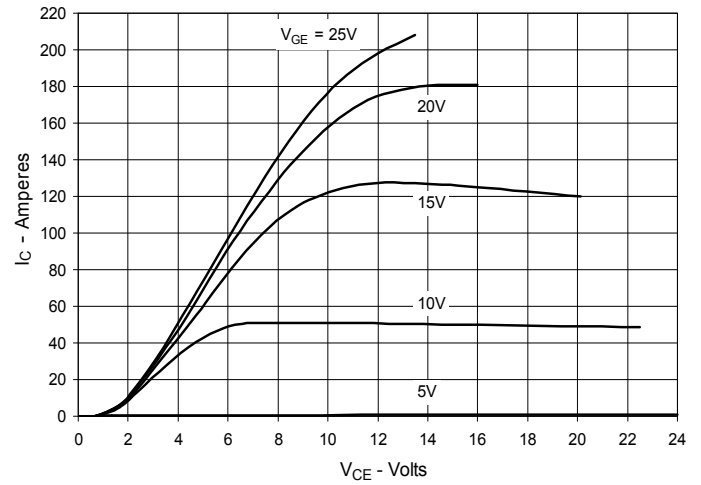
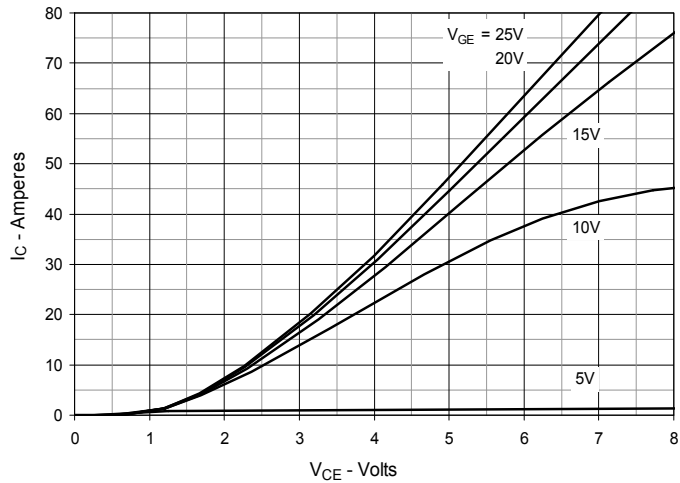
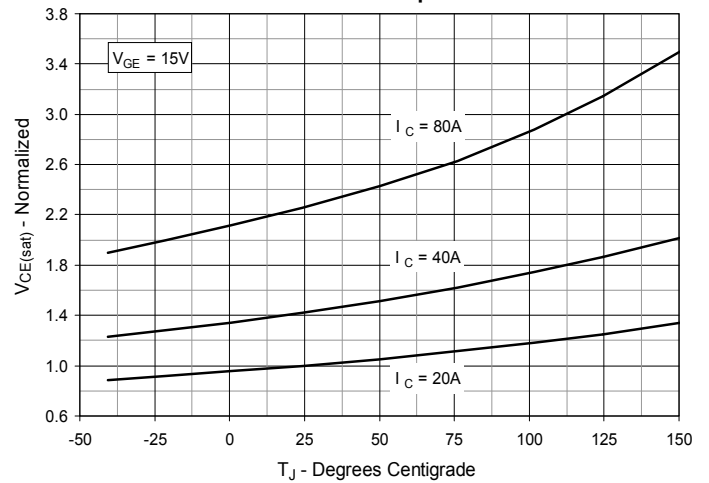
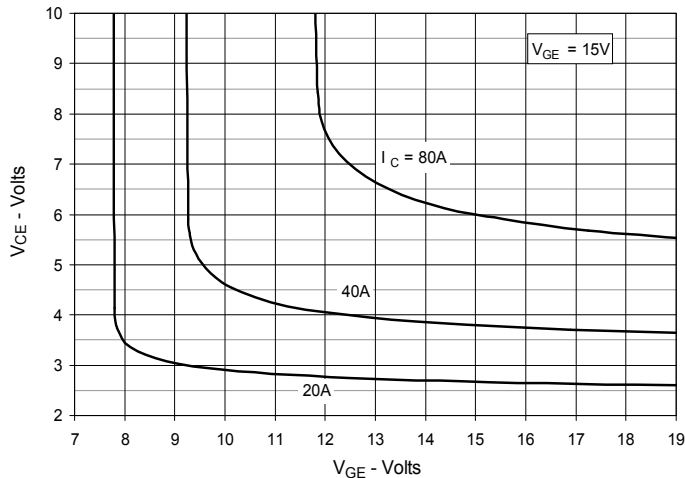
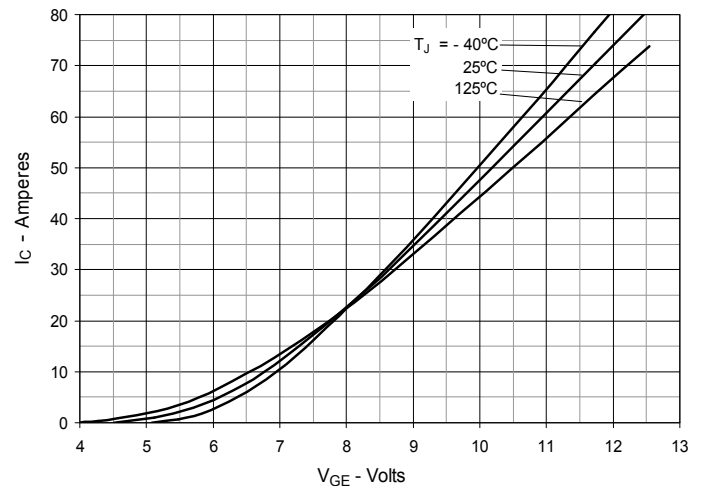
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

Fig. 6. Input Admittance


Fig. 7. Transconductance

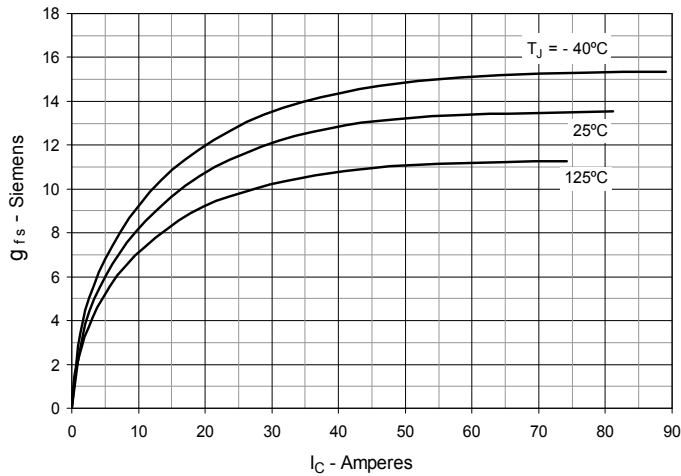


Fig. 8. Gate Charge

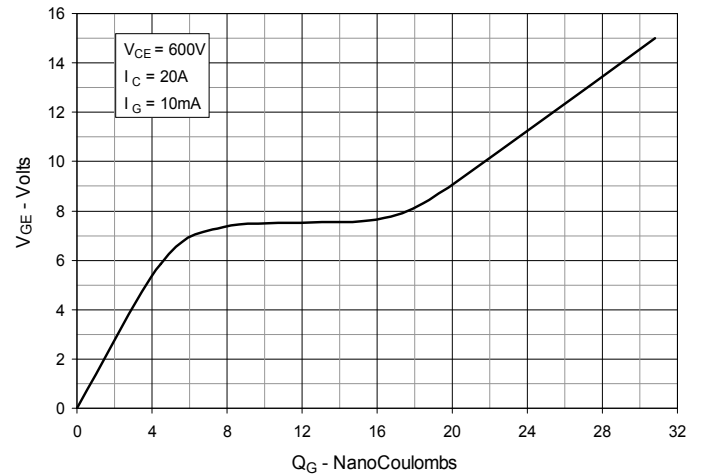


Fig. 9. Reverse-Bias Safe Operating Area

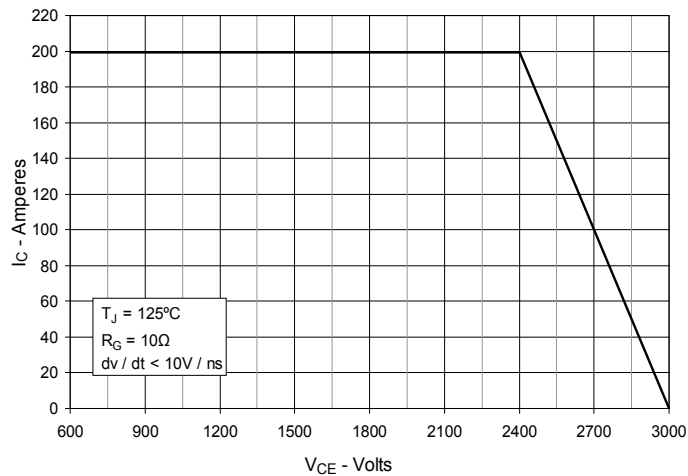


Fig. 10. Capacitance

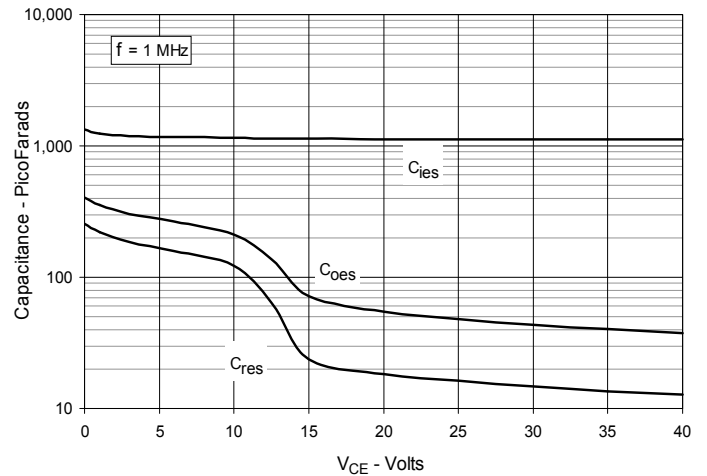
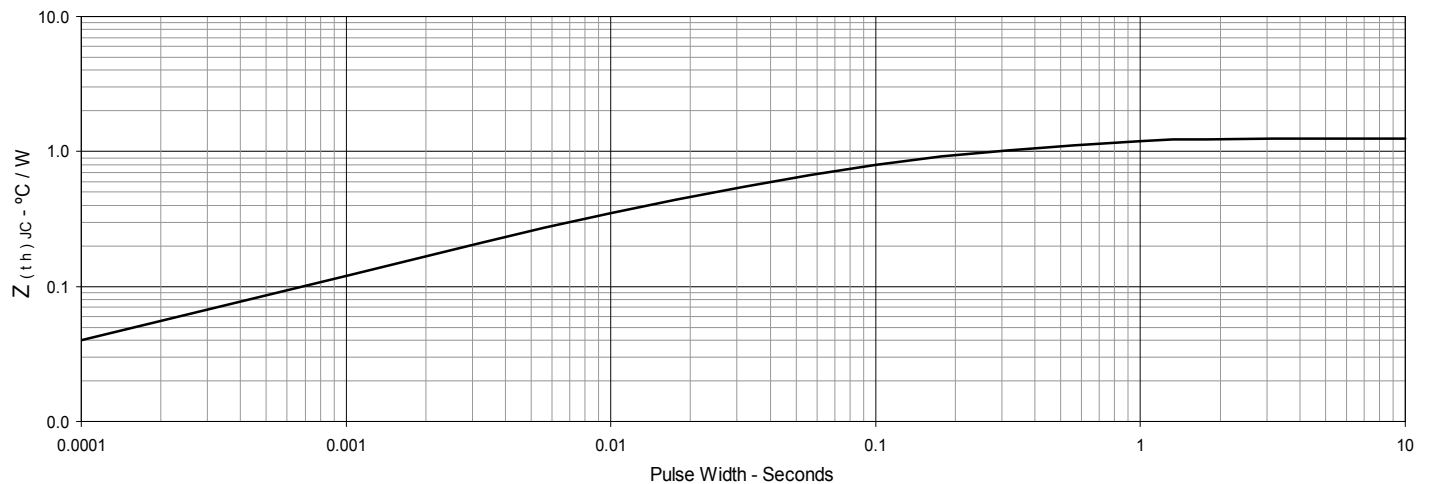


Fig. 11. Maximum Transient Thermal Impedance



IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

Fig. 12. Resistive Turn-on Rise Time vs. Junction Temperature

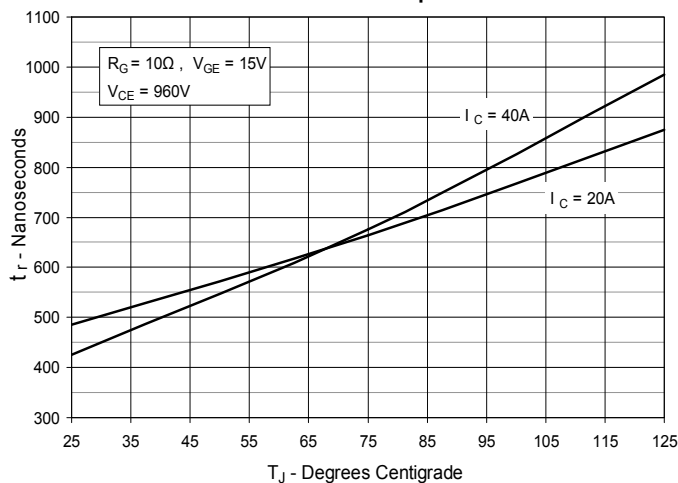


Fig. 13. Resistive Turn-on Rise Time vs. Collector Current

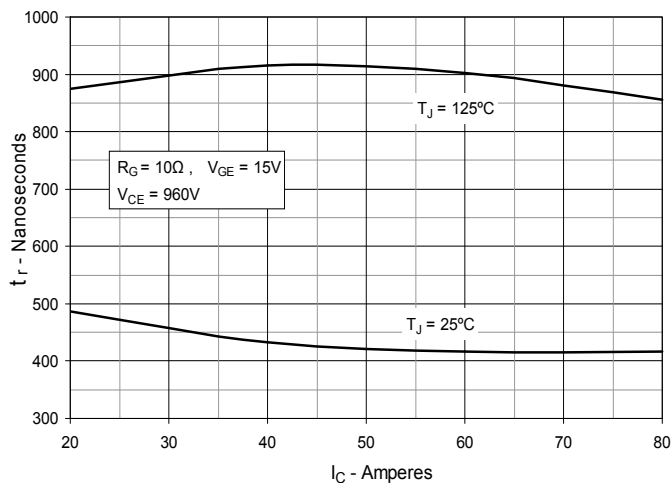


Fig. 14. Resistive Turn-on Switching Times vs. Gate Resistance

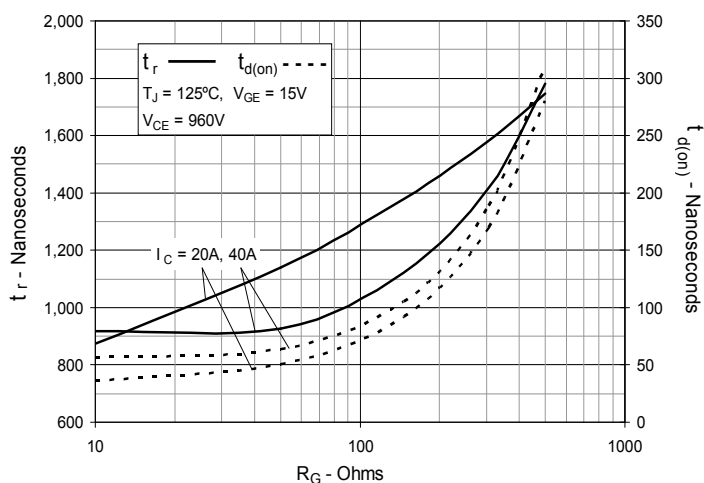


Fig. 15. Resistive Turn-off Switching Times vs. Junction Temperature

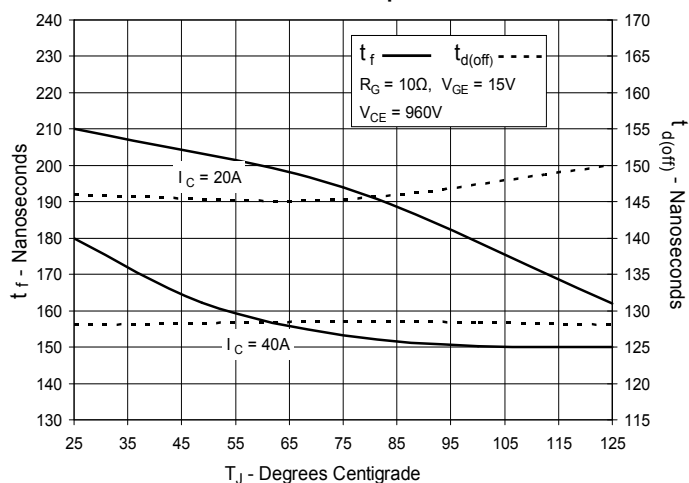


Fig. 16. Resistive Turn-off Switching Times vs. Collector Current

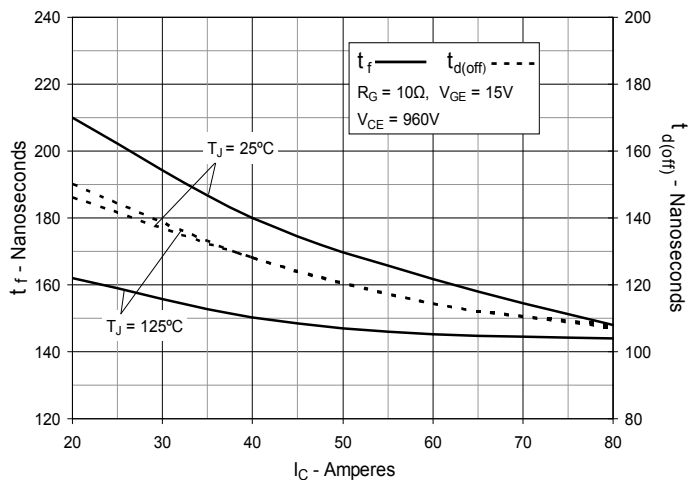
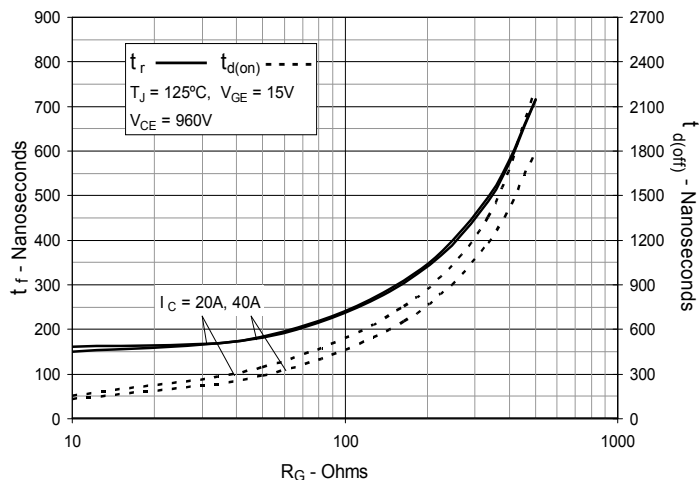


Fig. 17. Resistive Turn-off Switching Times vs. Gate Resistance





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