THCV334-Q

Audio Visual Deserializer with bi-directional transceiver

1. General Description

THCV334-Q video deserializer is designed to support 1080p60 24bit uncompressed video data by V-by-One® HS II Forward Channel (FC) on 100ohm differential STP or 50ohm Coaxial cable between graphic processor and Open-LDI (LVDS) (oLDI) input panel display.

THCV334-Q supports audio.

THCV334-Q supports bi-directional command communication including 2-wire interface and GPIO, which can be controlled and monitored to connect touch panel at local side.

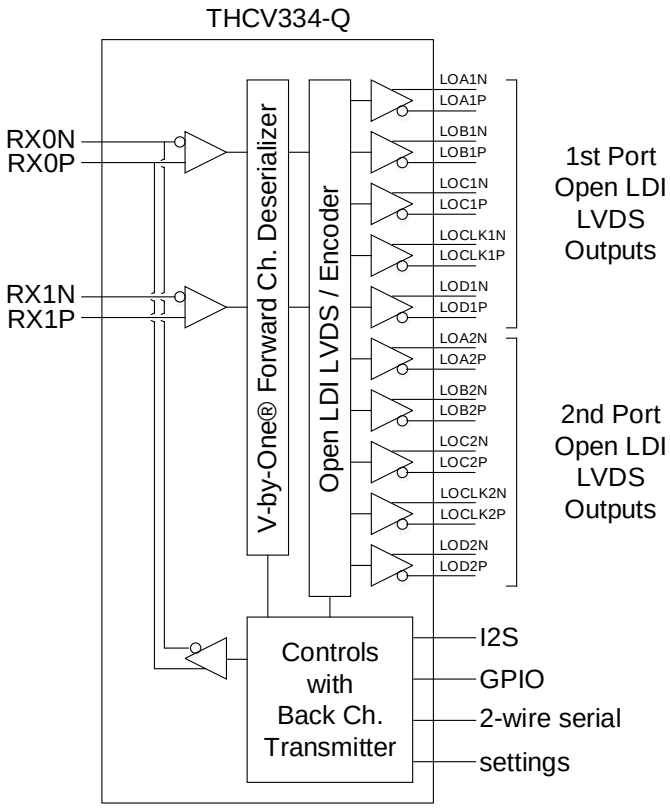
2. Applications

Automotive Infotainment Display
Instrument Cluster Display
Touch Screen Monitor and Panel Display
Security and Surveillance Camera

3. Features

- AEC-Q100 Grade2 (-40 to 105˚C)
- Forward Channel V-by-One® HS II 4Gbps 2lane
- FC to Open-LDI(LVDS) Single 10 to 109MHz
- FC to Open-LDI(LVDS) Dual 50 to 109MHz
- 2xFC to Open-LDI(LVDS) Single 50 to 170MHz
- 2xFC to Open-LDI(LVDS) Dual 50 to 218MHz
- Color depth per pixel:18bit or 24bit
- Back Channel GPIO support up to 120kbps
- 2-wire 1Mbps serial interface bridge function
- Remote side GPIO control and monitoring
- 15 meters of cable transmission
- Wide range IO voltage from 1.71V to 3.465V
- Additional spread spectrum on data stream
- Error Detect and Notification
- 0.5mm pitch QFN64 9x9mm package
- Compliant with RoHS and REACH

4. Block Diagram



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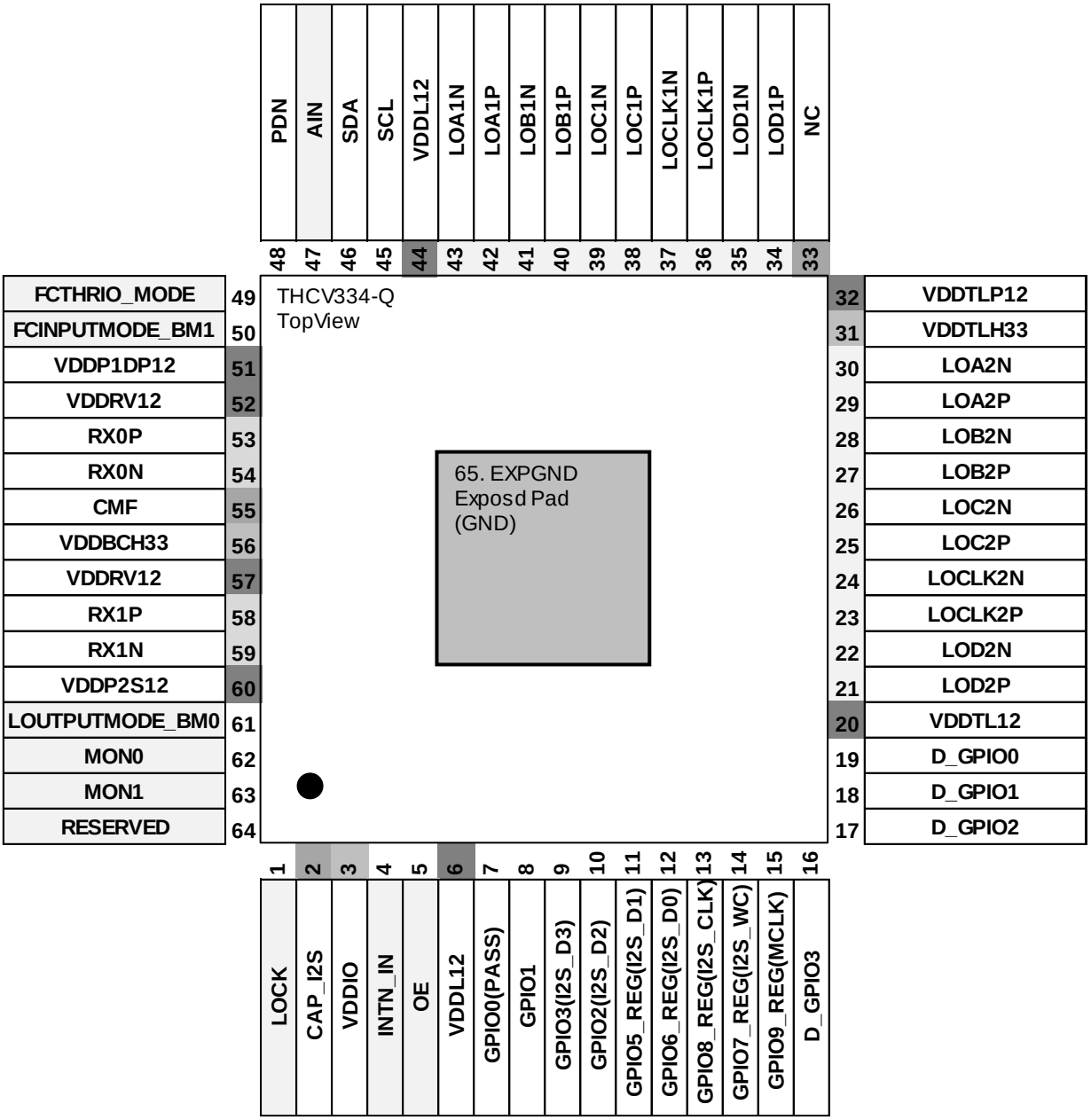
5. Pin Configuration and Functions



Pin Functions

Settings				
Pin Name	Pin#	I/O	PU/PD	Description
RESERVED	64	IL2	-	**Must be tied to GND** 0: GND MUST 1: Not Allowed
FCTHRIO_MODE	49	IL	PD	**SELECT Forward Chanel Through IO MODE** 0 : 8cycle mode (default / audio-video balanced) 1 : 4cycle mode (enhanced audio bandwidth)
FCINPUTMODE_BM1	50	IL	PD	**Forward Ch. Input Mode Select (Base Mode 1)** 0: 1Lane V-by-One® HS II input 1: 2Lane V-by-One® HS II input
LOUTPUTMODE_BM0	61	IL	PD	**oLDI LVDS Output Mode Select (Base Mode 0)** 0: 1Port Single-Link Open-LDI LVDS output 1: 2Port Dual-Link Open-LDI LVDS output
OE	5	IL	PD	**Output Enable** 0: LVDS Output Disable Register Entry Mode. Output is disabled before entry by register access. (oLDI differential Low) 1: LVDS Output Enable Pin Entry Mode. Output is enabled without any register access and can be disabled by register.
PDN	48	IL2	-	**Chip Power Down Negative** 0: Power-Down State (oLDI Hi-Z) 1: Normal Operation
2-Wire Serial Interface				
Pin Name	Pin#	I/O	PU/PD	Description
AIN	47	IL	PD	**Device Address Setting for 2-Wire Serial Interface** 0 : Device Address = 7'h77 (=7'b111_0111) 1 : Device Address = 7'h65 (=7'b110_0101)
SCL	45	B2	-	**2-wire serial I/F Clock Line**
SDA	46	B2	-	**2-wire serial I/F Data Line**

I:VDDIO CMOS Input, IL/IL2:VDDIO CMOS Input (Low speed), O:VDDIO CMOS Output, B/B2:VDDIO CMOS Input and Output,

PU/PD:Pull-Up/Down

LO:Open-LDI (LVDS) Output, VI:V-by-One® Forward Ch. Input and Back Ch. Output, A:Analog, PS:Power Supply

Pin Functions (continued)

I2S Interface				
Pin Name	Pin#	I/O	PU/PD	Description
MCLK	15	O	-	I2S Master Clock output *Shared with GPIO9_REG
I2S_WC	14	O	-	I2S WC(Word Clock) output *Shared with GPIO7_REG
I2S_CLK	13	O	-	I2S Bit Clock output *Shared with GPIO8_REG
I2S_D0	12	O	-	I2S Data output 0 *Shared with GPIO6_REG
I2S_D1	11	O	-	I2S Data output 1 *Shared with GPIO5_REG
I2S_D2	10	O	-	I2S Data output 2 *Shared with GPIO2
I2S_D3	9	O	-	I2S Data output 3 *Shared with GPIO3
Status Monitor				
Pin Name	Pin#	I/O	PU/PD	Description
LOCK	1	O	-	Lock Status Output pin LOCK = 1: PLL acquired lock to the Forward Channel Data Recovered Clock Input LOCK = 0: PLL is unlocked
PASS	7	O	-	Field BET Result Out *Shared with GPIO0
General Purpose I/O				
Pin Name	Pin#	I/O	PU/PD	Description
GPIO0, GPIO1, GPIO2, GPIO3, GPIO5_REG, GPIO6_REG, GPIO7_REG, GPIO8_REG, GPIO9_REG, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3	7, 8, 10, 9, 11, 12, 14, 13, 15, 19, 18, 17, 16	B	-	**General Purpose Input Output**

I:VDDIO CMOS Input, IL:VDDIO CMOS Input (Low speed), O:VDDIO CMOS Output, B:VDDIO CMOS Input and Output, PU/PD:Pull-Up/Down

LO:Open-LDI (LVDS) Output, VI:V-by-One® Forward Ch. Input and Back Ch. Output, A:Analog, PS:Power Supply

Pin Functions (continued)

Interrupt/Error/External Sync				
Pin Name	Pin#	I/O	PU/PD	Description
INTN_IN	4	I	PD	**Interrupt Signal Input** 0: Interrupt State 1: No Interrupt State *polarity is programmable with register

Signal Monitor				
Pin Name	Pin#	I/O	PU/PD	Description
MON0,MON1	62,63	O	PD	**Internal Status Monitor**

V-by-One® HS II Rx				
Pin Name	Pin#	I/O	P-Domain	Description
RX0P, RX0N	53, 54	VI	VDDRV	**V-by-One® HS II Forward Ch. Input** (0lane)
RX1P, RX1N	58, 59	VI	VDDRV	**V-by-One® HS II Forward Ch. Input** (1lane)
LVDS Rx				
Pin Name	Pin#	I/O	P-Domain	Description
LOA1P, LOA1N	42, 43	LO	VDDTL	**LVDS Port1 Output** (Data0 channel)
LOB1P, LOB1N	40, 41	LO	VDDTL	**LVDS Port1 Output** (Data1 channel)
LOC1P, LOC1N	38, 39	LO	VDDTL	**LVDS Port1 Output** (Data2 channel)
LOCLK1P, LOCLK1N	36, 37	LO	VDDTL	**LVDS Port1 Output** (Clock channel)
LOD1P, LOD1N	34, 35	LO	VDDTL	**LVDS Port1 Output** (Data3 channel)
LOA2P, LOA2N	29, 30	LO	VDDTL	**LVDS Port2 Output** (Data0 channel)
LOB2P, LOB2N	27, 28	LO	VDDTL	**LVDS Port2 Output** (Data1 channel)
LOC2P, LOC2N	25, 26	LO	VDDTL	**LVDS Port2 Output** (Data2 channel)
LOCLK2P, LOCLK2N	23, 24	LO	VDDTL	**LVDS Port2 Output** (Clock channel)
LOD2P, LOD2N	21, 22	LO	VDDTL	**LVDS Port2 Output** (Data3 channel)

I:VDDIO CMOS Input, IL:VDDIO CMOS Input (Low speed), O:VDDIO CMOS Output, B:VDDIO CMOS Input and Output, PU/PD:Pull-Up/Down

LO:Open-LDI (LVDS) Output, VI:V-by-One® Forward Ch. Input and Back Ch. Output, A:Analog, PS:Power Supply

Pin Functions (continued)

Analog monitor /				
Pin Name	Pin#	I/O	P-Domain	Description
NC	33	A	-	Not Connected
CAP_I2S	2	A	VDDP2	Recommend to connect with a 0.1uF decoupling capacitor to GND.
CMF	55	A	-	**Common mode filter** LVDS Vcom Out Common mode filter – connect 0.1µF capacitor to GND
Power Line				
Pin Name	Pin#	I/O	P-Domain	Description
VDDIO	3	PS	VDDIO	**Power Supply for LVCMOS I/O (1.8V/3.3V)**
VDDL12	6,44	PS	VDDL	**Power Supply for Digital (1.2V)**
VDDP1DP12	51	PS	VDDP1	**Power Supply for PLL(Data Path) (1.2V)**
VDDP2S12	60	PS	VDDP2	**Power Supply for PLL(I2S) (1.2V)**
VDDRV12	52,57	PS	VDDRV	**Power Supply for V-by-One Rx and Back Channel Analog (1.2V)**
VDDBCH33	56	PS	VDDBCH	**Power Supply for BC LDO (3.3V)**
VDDTL12	20	PS	VDDTL	**Power Supply for LVDS Tx Serializer/Logic (1.2V)**
VDDTLP12	32	PS	VDDTLP	**Power Supply for LVDS Tx PLL/VREF (1.2V)**
VDDTLH33	31	PS	VDDTLH	**Power Supply for LVDS Tx output buffer (3.3V)**
EXPGND	65	PS	VSSEXP	**Exposed Pad Ground**

I:VDDIO CMOS Input, IL:VDDIO CMOS Input (Low speed), O:VDDIO CMOS Output, B:VDDIO CMOS Input and Output, PU/PD:Pull-Up/Down

LO:Open-LDI (LVDS) Output, VI:V-by-One® Forward Ch. Input and Back Ch. Output, A:Analog, PS:Power Supply

6. Specifications

6.1. Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings*

Parameter	min.	typ.	max.	Unit
Supply Voltage (VDDIO,VDDTLH,VDDBCH)	-0.3	-	+4.0	V
Supply Voltage (VDDL,VDDP1,VDDP2,VDDRV,VDDTL,VDDTLP)	-	-	1.6	V
LVCMOS Input Voltage	-0.3	-	VDDIO+0.3	V
LVCMOS Output Voltage	-0.3	-	VDDIO+0.3	V
LVCMOS Bi-directional buffer Input Voltage	-0.3	-	VDDIO+0.3	V
LVCMOS Bi-directional buffer Output Voltage	-0.3	-	VDDIO+0.3	V
LVDS Transmitter Voltage	-0.3	-	VDDTLH+0.3	V
CML Receiver Voltage Back Channel Transmitter Voltage	-0.3	-	VDDRV+0.3	V
Storage Temperature	-55	-	+125	˚C
Junction Temperature	-	-	+125	˚C
Reflow Peak Temperature/time	-	-	+260/10	˚C/sec

* “Absolute Maximum Ratings” are values of safety limit for a device beyond which a device safety cannot be guaranteed.

They do not imply that a device should be operated at these limits. The tables of “Recommended Operating Condition” specify conditions for device operation.

6.2. Electrostatic discharge Ratings

Table 2. Electrostatic discharge (ESD) Ratings

Symbol	Parameter	Condition		Value	Unit
VESD	Electrostatic Discharge	Human Body Model (HBM) on AEC-Q100-002		+/-2000	V
		Charged Device Model (CDM) on AEC-Q100-011		+/-750	
		IEC61000-4-2	Air Discharge	+/-15000	
			Contact Discharge	+/-8000	
		ISO10605	Air Discharge	+/-15000	
			Contact Discharge	+/-8000	

6.3. Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	min.	typ.	max.	Unit
Supply Voltage (VDDIO)	3.135	3.300	3.465	V
	1.89	2.5 / 2.8	3.135	V
	1.71	1.8	1.89	V
Supply Voltage (VDDTLH, VDDBCH)	3.135	3.300	3.465	V
Supply Voltage (VDDL,VDDP1,VDDP2,VDDRV,VDDTL,VDDTLP)	1.14	1.2	1.26	V
Operating Temperature (Ta)	-40	-	105	˚C

6.4. Thermal Information

Table 4. Thermal Information

Symbol	Parameter	Value	Unit
θja	Junction-to-ambient thermal resistance	22.82	˚C/W
θjc(top)	Junction-to-case (top) thermal resistance	11.17	˚C/W
θjb	Junction-to-board thermal resistance	3.06	˚C/W
Ψjt	Junction-to-top characterization parameter	4.56	˚C/W
Ψjb	Junction-to-board characterization parameter	6.88	˚C/W
θjc(bot)	Junction-to-case (bottom) thermal resistance	1.4	˚C/W

6.5. DC Specifications

6.5.1. LVCMOS DC Specifications

Table 5. LVCMOS DC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
IIH	Input Leak Current High	-	-10	-	+10	uA
IIL	Input Leak Current Low	-	-10	-	+10	uA
VIH1	High Level Input Voltage (I, IL and B)	VDDIO=3~3.465V	2.00	-	VDDIO	V
		VDDIO=2~3V	0.70*VDDIO	-	VDDIO	V
		VDDIO=1.71~2V	0.65*VDDIO	-	VDDIO	V
VIL1	Low Level Input Voltage (I, IL and B)	VDDIO=3~3.465V	0	-	0.80	V
		VDDIO=2~3V	0	-	0.30*VDDIO	V
		VDDIO=1.71~2V	0	-	0.35*VDDIO	V
VIH2	High Level Input Voltage (IL2 and B2)	-	0.70*VDDIO	-	VDDIO	V
VIL2	Low Level Input Voltage (IL2 and B2)	-	0	-	0.30*VDDIO	V
VOH	High Level Output Voltage	IOH=1mA	VDDIO-0.45		VDDIO	V
VOL	Low Level Output Voltage	IOL=1mA	0	-	0.45	V

6.5.2. CML Forward Channel Receiver DC Specifications

Table 6. CML Forward Channel (FC) Receiver DC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
VRTH	CML Differential Input High Threshold	-	-	-	50	mV
VRTL	CML Differential Input Low Threshold	-	-50	-	-	mV
IRIH	CML Input Leak Current High	PDN=L RXP/N=VDDRV	-	-	85	uA
IRIL	CML Input Leak Current Low	PDN=L RXP/N=GND	-	-	163	uA
IRRIH	CML Input Current High	RXP/N=VDDRV	1.5	-	5	mA
IRRIL	CML Input Current Low	RXP/N=GND	-35	-	-15	mA
RRIN	CML Differential Input Resistance	-	80	100	120	ohm

6.5.3. Open-LDI LVDS Transmitter DC Specifications

Table 7. Open-LDI (oLDI) LVDS Transmitter DC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
VROD	LVDS Differential Mode Output Voltage(Normal Swing)	RL=100 Ω , R_VODSEL=d'0111(default)	250	350	450	mV
	LVDS Differential Mode Output Voltage(Reduced Swing)	RL=100Ω, R_VODSEL=d'0010	140	200	300	mV
ΔVROD	Change in VROD between Complementary Output States	RL=100Ω	-	-	35	mV
VROC	LVDS Common Mode Output Voltage	RL=100Ω	1.125	1.25	1.375	V
ΔVROC	Change in VROC between Complementary Output States	RL=100Ω	-	-	35	mV
IROS	LVDS Output Short Circuit Current	RLxn+/-=0 (x=A~F,CLK, n=0,1)	- 135	-	-55	mA
IROZ	LVDS Output TRI-STATE Current	PDN=L, RLxN+/-=0, VDDTLH (x=A~F,CLK, n=0,1)	-	-	±10	uA

6.6. AC Specifications

6.6.1. General AC Specifications

Table 8. General AC Specifications (1/3)

Symbol	Parameter	Condition	min.	typ.	max.	Unit
tDL_V2V_1	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Single-Link oLDI output FC_THRIO: 4cycle mode 1/TRCIP=85MHz	331*TRCIP	341*TRCIP	351*TRCIP +10	ns
tDL_V2V_2	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Single-Link oLDI output FC_THRIO: 8cycle mode 1/TRCIP=85MHz	367*TRCIP	377*TRCIP	387*TRCIP +10	ns
tDL_V2V_3	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Single CML FC output Des: Single CML FC input / Dual-Link oLDI output FC_THRIO: 4cycle mode 1/TRCIP=85MHz	171*TRCIP	181*TRCIP	191*TRCIP +10	ns
tDL_V2V_4	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Single CML FC output Des: Single CML FC input / Dual-Link oLDI output FC_THRIO: 8cycle mode 1/TRCIP=85MHz	180*TRCIP	190*TRCIP	200*TRCIP +10	ns
tDL_V2V_5	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Single CML FC output Des: Single CML FC input / Single-Link oLDI output FC_THRIO: 4cycle mode 1/TRCIP=85MHz	227*TRCIP	237*TRCIP	247*TRCIP +10	ns
tDL_V2V_6	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Single CML FC output Des: Single CML FC input / Single-Link oLDI output FC_THRIO: 8cycle mode 1/TRCIP=85MHz	244*TRCIP	254*TRCIP	264*TRCIP +10	ns
tDL_V2V_7	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Dual-Link oLDI output FC_THRIO: Off 1/TRCIP=85MHz	260*TRCIP	270*TRCIP	280*TRCIP +10	ns

*Serializer above table is THCV333-Q. Deserializer above table is THCV334-Q.

Table 9. General AC Specifications (2/3)

Symbol	Parameter	Condition	min.	typ.	max.	Unit
tDL_V2V_8	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Single-Link oLDI output FC_THRIO: 8cycle mode Low Freq mode: x2mode 1/TRCIP=85MHz	245*TRCIP	255*TRCIP	265*TRCIP +10	ns
tDL_V2V_9	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Single CML FC output Des: Single CML FC input / Dual-Link oLDI output FC_THRIO: 8cycle mode Low Freq mode: x2mode 1/TRCIP=85MHz	149*TRCIP	159*TRCIP	169*TRCIP +10	ns
tDL_V2V_10	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Dual-Link oLDI output FC_THRIO: 4cycle mode Low Freq mode: x2mode 1/TRCIP=85MHz	175*TRCIP	185*TRCIP	195*TRCIP +10	ns
tDL_V2V_11	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Dual-Link oLDI output FC_THRIO: 8cycle mode Low Freq mode: x2mode 1/TRCIP=85MHz	180*TRCIP	190*TRCIP	200*TRCIP +10	ns
tDL_V2V_12	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Single-Link oLDI output FC_THRIO: 4cycle mode Low Freq mode: x4mode 1/TRCIP=85MHz	172*TRCIP	182*TRCIP	192*TRCIP +10	ns
tDL_V2V_13	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Single-Link oLDI output FC_THRIO: 8cycle mode Low Freq mode: x4mode 1/TRCIP=85MHz	180*TRCIP	190*TRCIP	200*TRCIP +10	ns
tDL_V2V_14	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Dual-Link oLDI output FC_THRIO: 8cycle mode Low Freq mode: x4mode 1/TRCIP=85MHz	150*TRCIP	160*TRCIP	170*TRCIP +10	ns

*Serializer above table is THCV333-Q. Deserializer above table is THCV334-Q.

Table 10. General AC Specifications (3/3)

Symbol	Parameter	Condition	min.	typ.	max.	Unit
tDL_A2A	Data Latency Audio from Serializer input to Deserializer output	Ser. I2S_WC input to Des. I2S_WC output 1/TRCIP=91.5MHz	106*TTFC BIT*30	116*TTFC BIT*30	126*TTFC BIT*30+10	ns
tDL_GPI2FC 2GPO	Data Latency Through GPIO from Serializer GPI to Deserializer GPO	FC THRIO_MODE=8cycle, FC Through GPIO=8bit 1/TRCIP=91.5MHz	75*TTFCBI T*30	85*TTFCBI T*30	95*TTFCBI T*30+10	ns
tDL_GPI2BC 2GPO	Data Latency Through GPIO from Deserializer GPI to Serializer GPO	BC Through GPIO=8bit 1/TRCIP=91.5MHz	367*TTFC BIT*30	527*TTFC BIT*30	687*TTFC BIT*30+10	ns
tDL_2WIRE WRITE2FC2 REM2WIRE	Data Latency 2-wire remote write from Serializer input to Deserializer output	FC THRIO_MODE=8cycle, 1/TRCIP=91.5MHz	262*TTFC BIT*30	282*TTFC BIT*30	302*TTFC BIT*30+10	ns
tDL_2WIRE WRITEACK2 BC2LOCAL2 WIRE	Data Latency 2-wire remote ACK from Deserializer input to Serializer output	FC THRIO_MODE=8cycle, 1/TRCIP=91.5MHz	736*TTFC BIT*30	1136*TTFC BIT*30	1536*TTF CBIT*30 +10	ns
tDL_2WIRE READ2FC2 REM2WIRE	Data Latency 2-wire remote read from Serializer input to Deserializer output	FC THRIO_MODE=8cycle, 1/TRCIP=91.5MHz	240*TTFC BIT*30	260*TTFC BIT*30	280*TTFC BIT*30+10	ns
tDL_2WIRE READBACK 2BC2LOCAL 2WIRE	Data Latency 2-wire remote read from Deserializer input to Serializer output	FC THRIO_MODE=8cycle, 1/TRCIP=91.5MHz	1302*TTFC BIT*30	1502*TTF CBIT*30	1702*TTF CBIT*30 +10	ns
tDL_INTIN2I NTN	Data Latency Interrupt from Deserializer INTN_IN to Serializer INTN	FC THRIO_MODE=8cycle, 1/TRCIP=91.5MHz	1470*TTFC BIT*30	2170*TTF CBIT*30	2870*TTF CBIT*30 +10	ns

*Serializer above table is THCV333-Q. Deserializer above table is THCV334-Q.

6.6.2. Open-LDI LVDS Transmitter AC Specifications

Table 11. Open-LDI (oLDI) LVDS Transmitter AC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
TTCOP	LOCLKxP/N Period	-	5.88	TTCOP	100	ns
FOLDIOUT	LOCLKxP/N Frequency per port		10		170	MHz
UI	LOyxP/N data bit Period	-	-	TTCOP/7	-	-
TLVT	oLDI LVDS Transition Time	-	-	0.6	1.5	ns
|TSKEW|	oLDI LVDS Data Output Skew for Single Link	FOLDIOUT =170MHz	-	-	150	ps
	oLDI LVDS Data Output Skew for Dual Link	FOLDIOUT =85MHz	-	-	185	ps
		FOLDIOUT =116MHz	-	-	185	ps
		FOLDIOUT =133.3MHz	-	-	205	ps
TTOP1	oLDI Output Data Position0	-	-|TSKEW|	0	+|TSKEW|	-
TTOP0	oLDI Output Data Position1	-	1/7 TTCOP -|TSKEW|	1/7 TTCOP	1/7 TTCOP +|TSKEW|	-
TTOP6	oLDI Output Data Position2	-	2/7 TTCOP -|TSKEW|	2/7 TTCOP	2/7 TTCOP +|TSKEW|	-
TTOP5	oLDI Output Data Position3	-	3/7 TTCOP -|TSKEW|	3/7 TTCOP	3/7 TTCOP +|TSKEW|	-
TTOP4	oLDI Output Data Position4	-	4/7 TTCOP -|TSKEW|	4/7 TTCOP	4/7 TTCOP +|TSKEW|	-
TTOP3	oLDI Output Data Position5	-	5/7 TTCOP -|TSKEW|	5/7 TTCOP	5/7 TTCOP +|TSKEW|	-
TTOP2	oLDI Output Data Position6	-	6/7 TTCOP -|TSKEW|	6/7 TTCOP	6/7 TTCOP +|TSKEW|	-
TTCH	oLDI LVDS clock H	-	-	TTCOP * 4/7	-	-
TTCL	oLDI LVDS clock L	-	-	TTCOP * 3/7	-	-
TTOSK	oLDI clock skew between LOCLK1P/N and LOCLK2P/N	-	-	-	70	ps

6.6.3. CML Forward Channel Receiver AC Specifications

Table 12. CML Forward Channel (FC) Receiver AC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
TRFCBIT	Unit Interval	-	250 (4Gbps)	-	666.7 (1.5Gbps)	ps
FRFC	Forward Channel Data-Rate	-	1.5	-	4.0	Gbps
TRISK_INTRA	Intra Pair Skew Tolerance	-	-	-	0.3	UI
TRISK_INTER	Inter Pair Skew Tolerance from Lane0 input to Lane1 input	-	-30	-	30	UI
Δmod	Spread Spectrum Clock Amplitude Tolerance	30kHz modulation Center Spread	-0.5	-	0.5	%

6.6.4. CML Back Channel Transmitter AC Specifications

Table 13. CML Back Channel Transmitter AC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
TRBCBIT	RXxP/N output each bit Period Back Channel (Unit Interval)	-	37.5 (26.7Mbps)	TRFCBIT *150	100 (10Mbps)	ns

6.6.5. 2-wire serial Interface AC Specifications

Table 14. 2-wire serial Interface AC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
t_{OSC}	Cycle of internal oscillator clock	-	10.4	12.5	15.7	ns
F_{scl}	SCL clock frequency	-	-	-	1000	kHz
t_{LOW}	LOW period of the SCL clock	-	0.5	-	-	us
t_{HIGH}	HIGH period of the SCL clock	-	0.26	-	-	us
$t_{HD;STA}$	hold time START condition	-	0.26	-	-	us
$t_{SH;STA}$	set-up time for a repeated START condition	-	0.26	-	-	us
$t_{HD;DAT}$	Data hold time (input)	-	0	-	-	ns
$t_{SU;DAT}$	Data setup time (input)	-	50	-	-	ns
t_r	rise time of both SDA and SCL signals	-	-	-	120	ns
t_f	fall time of both SDA and SCL signals	pull-up:2.5kohm bus cap:400pF	-	-	120	ns
$t_{SU;STO}$	set-up time for STOP condition	-	0.26	-	-	us
t_{BUF}	Bus free time between a STOP and START condition	-	0.5	-	-	us
$t_{VD;DAT}$	Data valid time	-	-	-	0.45	us
$t_{VD;ACK}$	Data valid acknowledge time	-	-	-	0.45	us
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	-	-	-	50	ns
t_{PDS}	Required wait time from PDN high to START condition	-	500	-	-	us

6.6.6. Power On and Re-Lock Sequence AC Specifications

Table 15. Power On Sequence AC Specifications

symbol	discription	min	typ	max	unit
t11	3.3V to VDDIO	0	0	-	us
t12	VDDIO to 1.2V	0	0	-	us
t2	Internal Pow er On Reset	1	-	-	us
t3	PDN Pin ReleaseTime	-	any	-	us
t5	OSC EN to CLKOUT output delay	4.99	-	8.75	us
t6	Register Access Enable from tOSC start after Reset Release	80	100	120	us
t10	FCBC CX Link Up Time	-	-	10	ms
t15	FC Rx LockTime	-	0.5	1	ms
t16	FNPLL Lock Time	-	500	1000	1/F(PFD) Cycle
t17	FNPLL Lock Flag Filter	-	-	any	tosc cycle
t18	Open-LDI LVDS PLL Lock Time	-	0.5	1	ms
t910	LOCKN=High to LVDS stop	-	-	10	us

6.6.7. AC Specifications Timing Diagrams

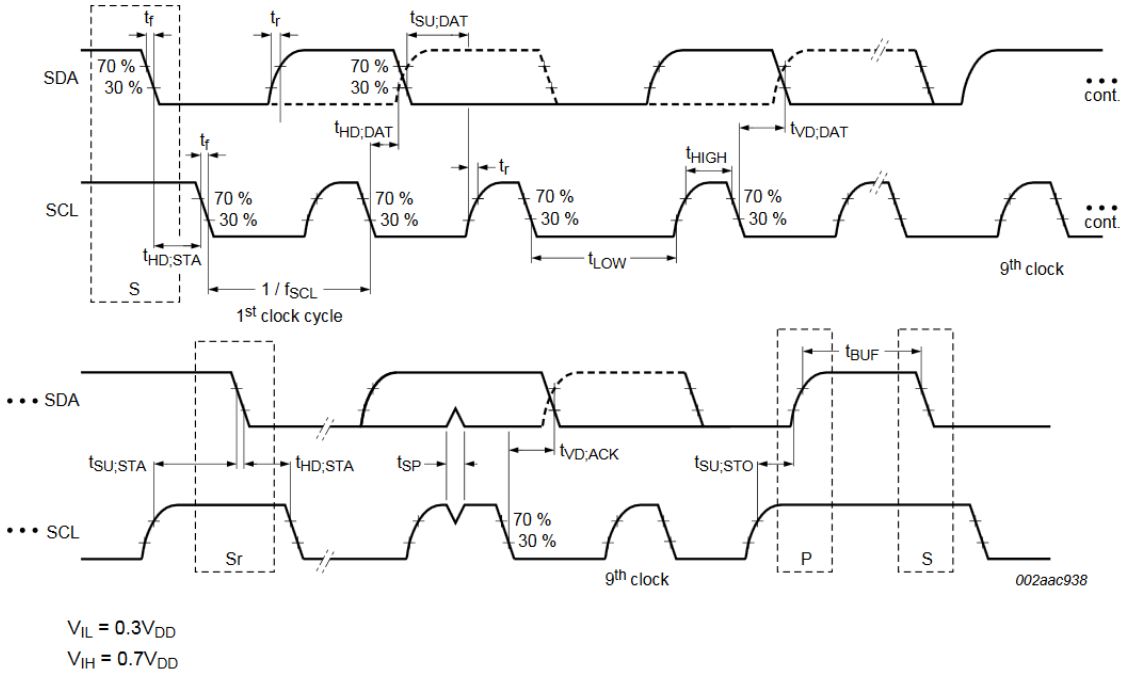


Figure 1. 2-wire serial Interface AC timing

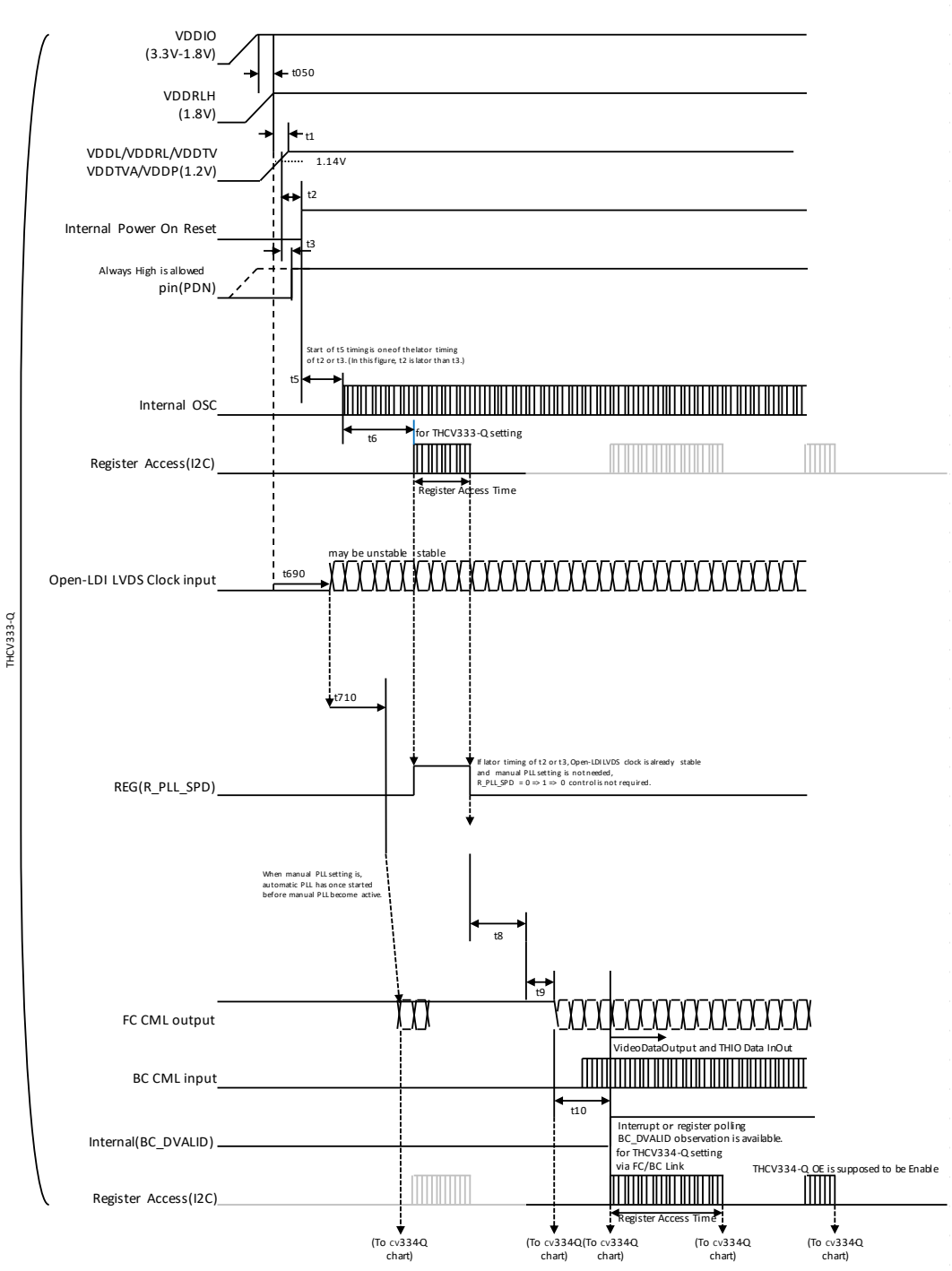


Figure 2. THCV333-Q Power On Sequence Register Entry

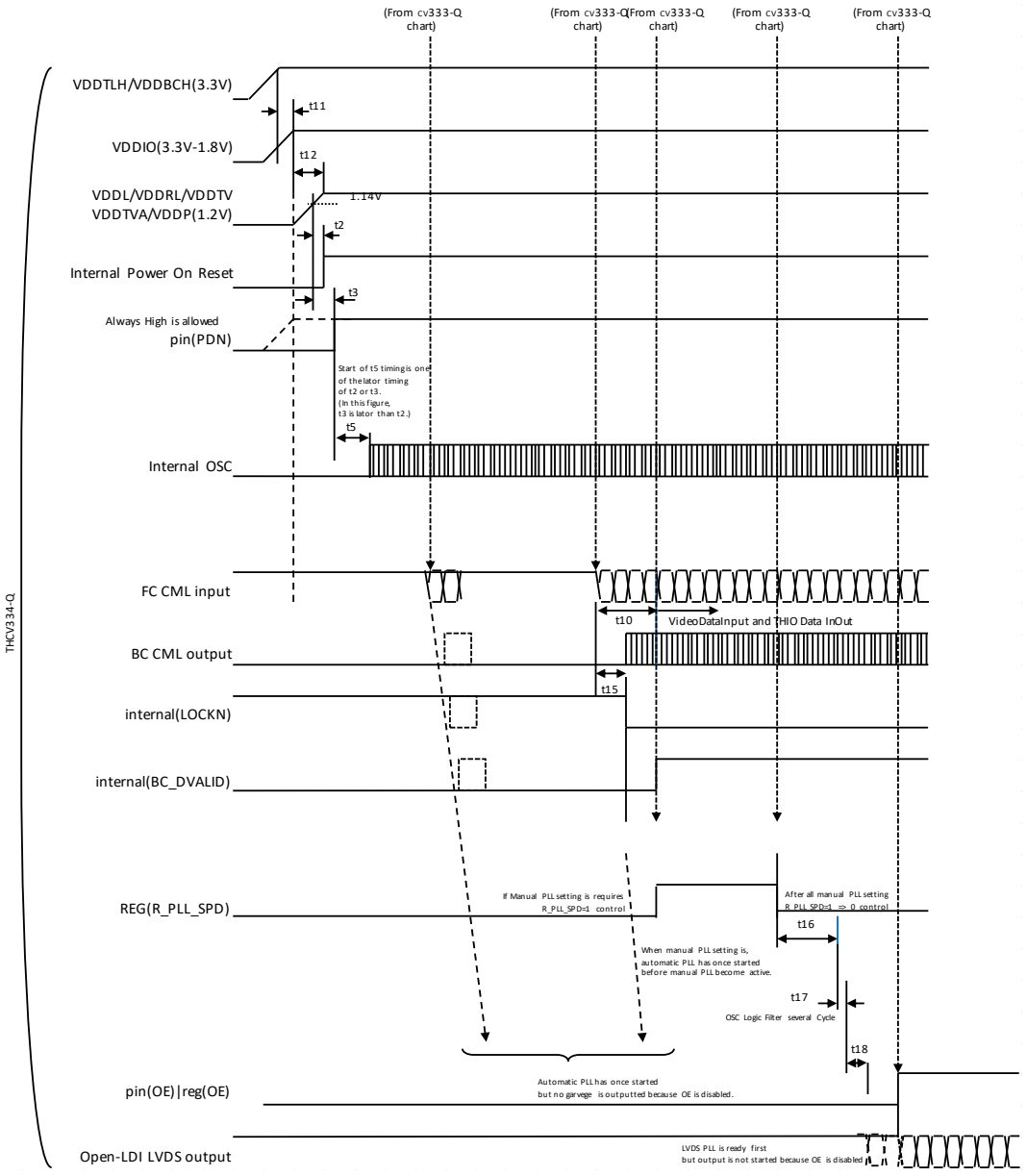


Figure 3. THCV334-Q Power On Sequence Register Entry

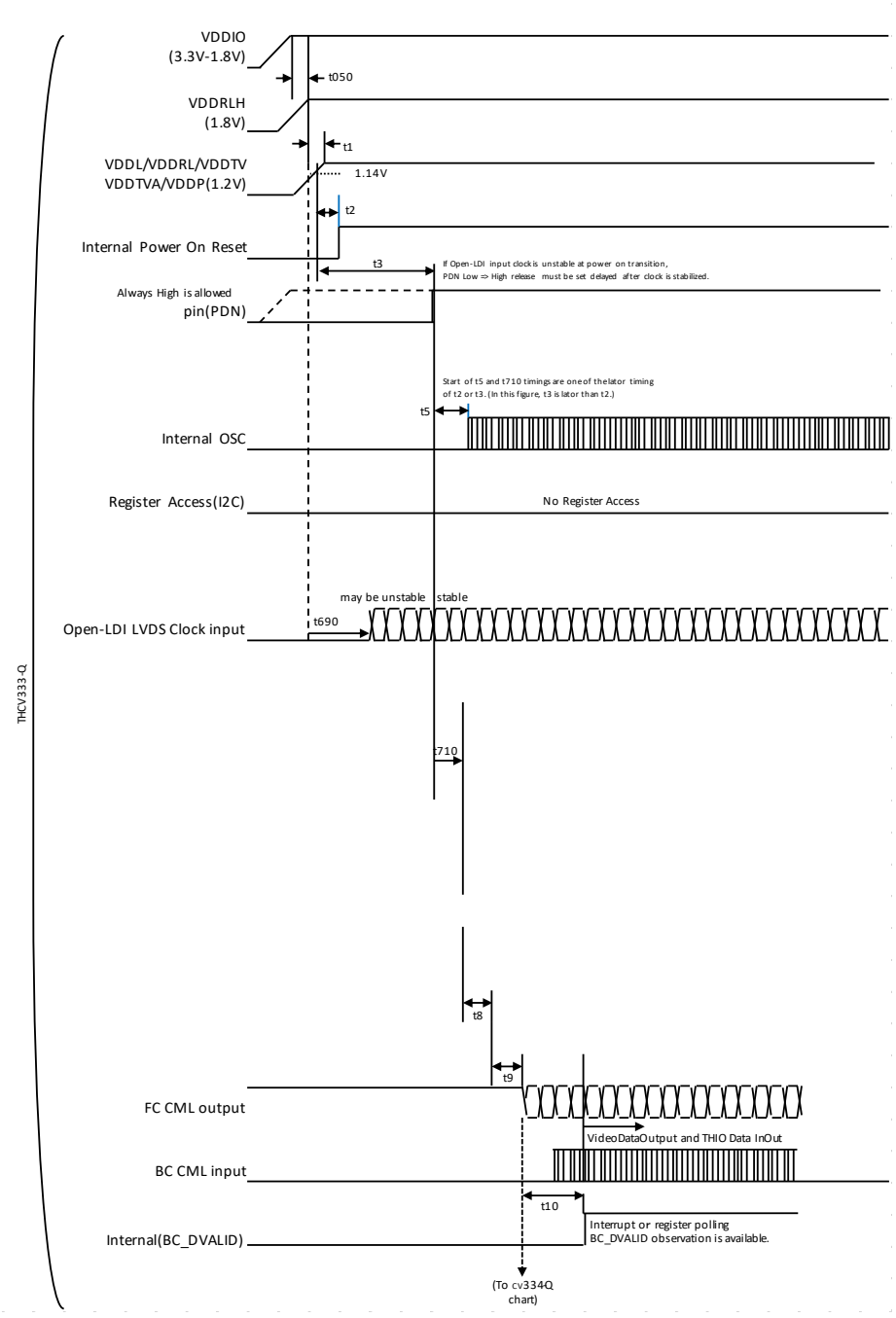


Figure 4. THCV333-Q Power On Sequence Pin Entry

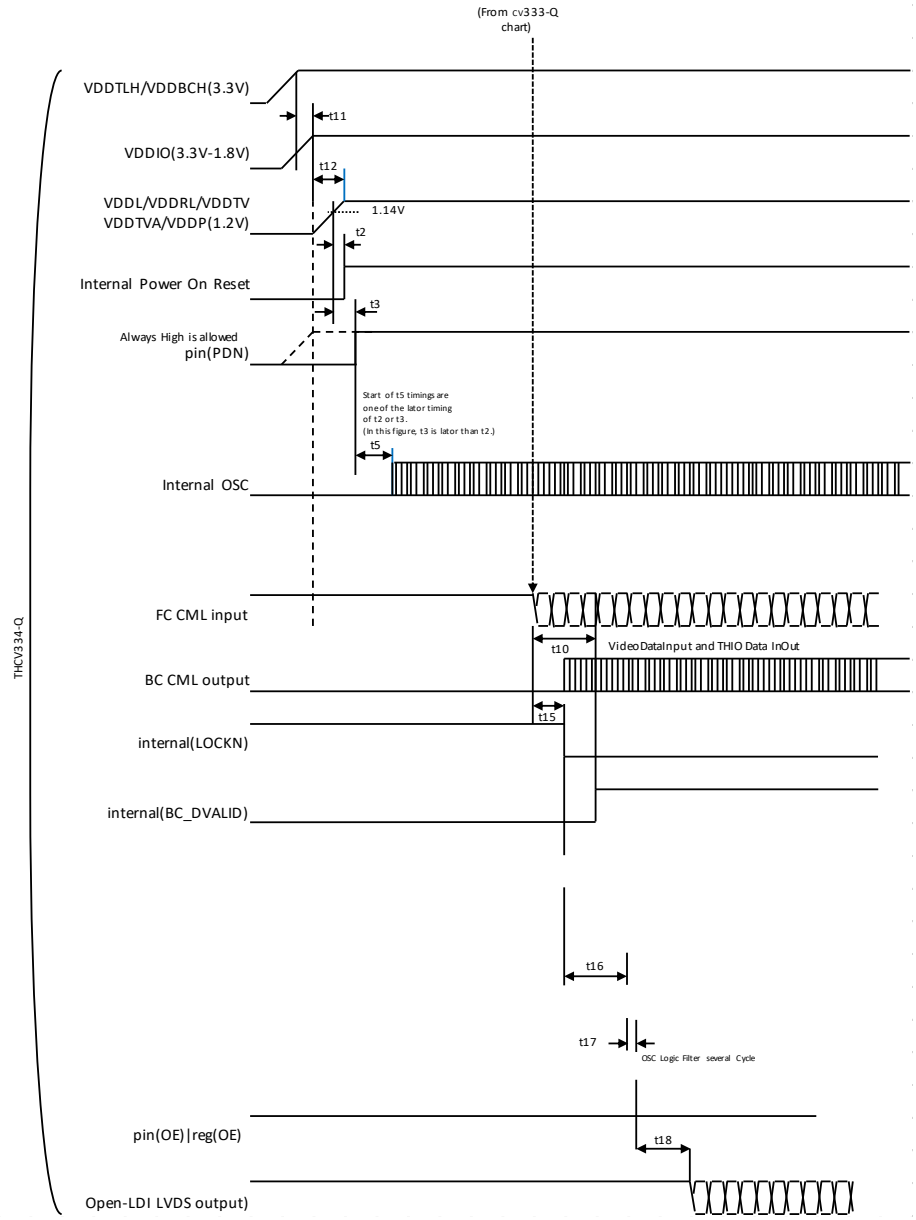


Figure 5. THCV334-Q Power On Sequence Pin Entry

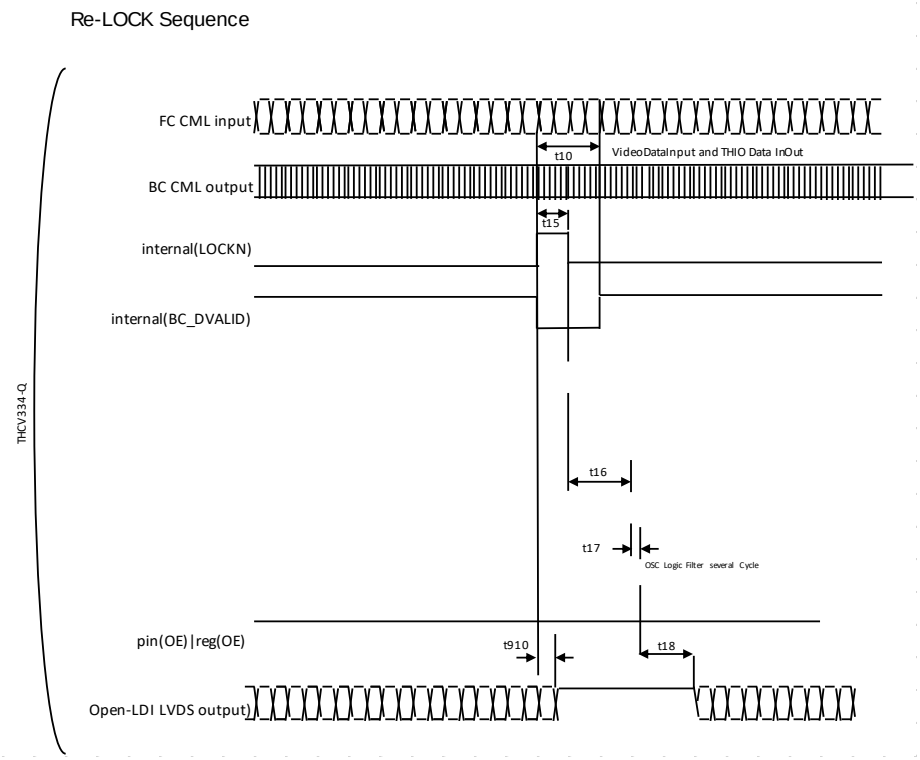


Figure 6. THCV334-Q Re-LOCK Sequence

6.7. Consumption Current

Table 16. Consumption Current at Power Down

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICCS33	Power Down Supply Current	PDN=0, VDDIO=3.465V	-	0.01	0.3	mA
ICCS12		PDN=0, VDDRLH=1.26V	-	5	40	mA

Table 17. Consumption Current of VDDH

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IRCCWIO_33_1	VDDIO=3.3V	No Audio, No GPIO	-	0.1	0.2	mA
IRCCWIO_33_2		I2S Audio 48kHz 16bit stereo MCLK=12.288MHz, No GPIO	-	3.0	3.2	mA
IRCCWIO_33_3		No Audio, GPIO UART 115200bps Tx/Rx and FC to PWM 20kHz 99%	-	0.1	0.2	mA
IRCCWIO_33_4		I2S Audio 48kHz 16bit stereo MCLK=12.288MHz, GPIO UART 115200bps Tx/Rx and FC to PWM 20kHz 99%	-	3.0	3.2	mA
IRCCWIO_18_1	VDDIO=1.8V	No Audio, No GPIO	-	0.05	0.1	mA
IRCCWTLH_18_2A	VDDTLH=3.3V	85MHz x oLDI Single-Link		27.2	27.8	mA
IRCCWTLH_18_2B		42.5MHz x oLDI Dual-Link	-	51.4	52.7	mA
IRCCWTLH_18_4B		75MHz x oLDI Dual-Link	-	52.2	53.5	mA
IRCCWTLH_18_8A		170MHz x oLDI Single-Link	-	28.5	29.4	mA
IRCCWTLH_18_9		109MHzxoLDI Dual-Link(218MHz)	-	52.7	54.3	mA

Table 18. Consumption Current of VDD12

Symbol	port.in#	port.out#	video format	input	output	min.	typ.	max.	Unit
IRCCW12_1	1	1	640x480p60 RGB888	1.72Gbps x1lane	25MHz x oLDI Single-Link	-	87.7	120.1	mA
IRCCW12_2A	1	1	1920x720p60(1) RGB888	3Gbps x1lane	85MHz x oLDI Single-Link	-	126.3	160.9	mA
IRCCW12_2B	1	2	1920x720p60(1) RGB888	3Gbps x1lane	42.5MHzxoLDI Dual-Link(85MHz)	-	110.0	149.3	mA
IRCCW12_3A	1	1	1920x720p60(2) RGB888	3.75Gbps x1lane	109MHz x oLDI Single-Link	-	148.5	184.6	mA
IRCCW12_3B	1	2	1920x720p60(2) RGB888	3.75Gbps x1lane	54.5MHzxoLDI Dual-Link	-	130.3	169.9	mA
IRCCW12_4A	2	1	1920x1080p60(1) RGB888	2.6Gbps x2lane	150MHz x oLDI Single-Link	-	208.0	249.4	mA
IRCCW12_4B	2	2	1920x1080p60(1) RGB888	2.6Gbps x2lane	75MHz x oLDI Dual-Link(150MHz)	-	183.5	227.9	mA
IRCCW12_8A	2	1	2880x720p60 RGB888	3Gbps x2lane	170MHz x oLDI Single-Link	-	227.5	269.8	mA
IRCCW12_8B	2	2	2880x720p60 RGB888	3Gbps x2lane	85MHz x oLDI Dual-Link(170MHz)	-	200.6	245.1	mA
IRCCW12_9	2	2	3840x720p60 RGB888	3.75Gbps x2lane	109MHzxoLDI Dual-Link(218MHz)	-	244.4	290.0	mA

Condition: Checkerboard Pattern

7. Detailed Description

7.1. Overview

The THCV334-Q receives a 24-bit video and several control symbol over single or dual serial V-by-One® HS II pairs operating at up to 4Gbps line rate in 1-lane V-by-One® HS II mode and 4 Gbps per lane in 2-lane V-by-One® HS II mode. The THCV334-Q converts this stream into a single or dual Open-LDI (LVDS) Interface (4 LVDS data channels + 1 LVDS clock, or 8 LVDS data channels + 2 LVDS clocks). The V-by-One® HS II serial stream contains an embedded clock, video control signals, and the DC-balanced video data and audio data which enhance signal quality to support AC coupling.

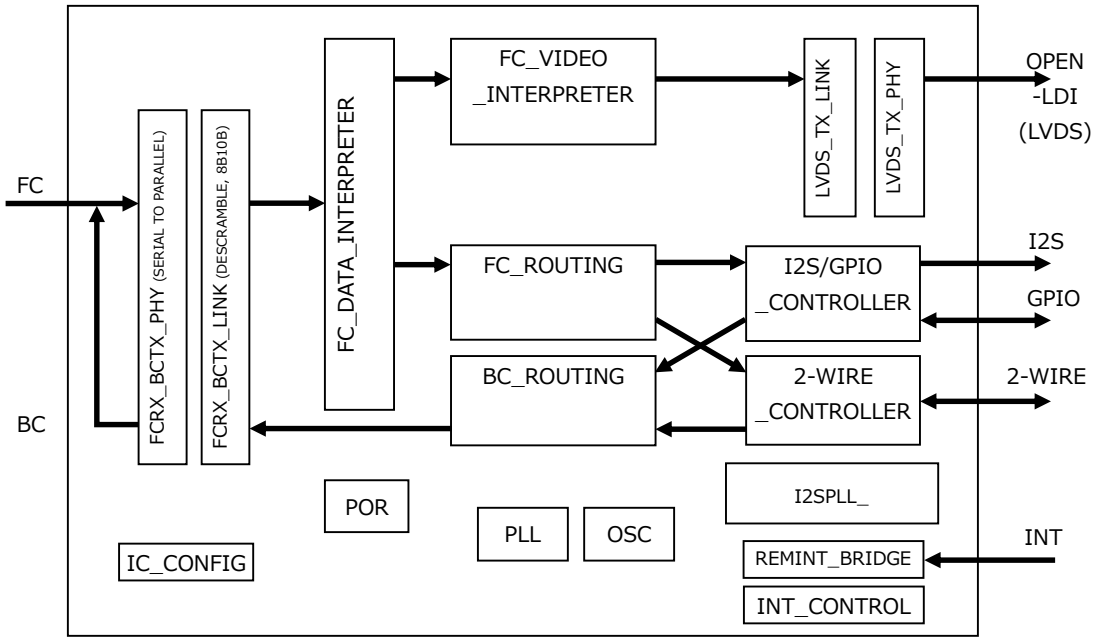
The THCV334-Q is is intended for use with the THCV333-Q serializer.

The THCV334-Q deserializer attains lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The deserializer also synchronizes to the serializer, delivering true automatic plug and lock performance. It can lock to the incoming serial stream. The deserializer recovers the clock and data by extracting the embedded clock information, validating then deserializing the incoming data stream.

The THCV334-Q deserializer incorporates an 2-wire serial interface. The 2-wire serial interface allows programming of serializer or deserializer devices from a local host controller. The devices also incorporate a bidirectional control channel (BCC) that allows communication between serializer/deserializer as well as remote 2-wire slave devices.

The bidirectional control channel (BCC) is implemented through embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge 2-wire serial transactions across the serial link from one 2-wire serial bus to another.

7.2. Functional Block Diagram



7.3. Feature Description

7.3.1. High-Speed Forward Channel Data Transfer

The High-Speed Forward Channel (FC) is composed of 30 bits of data containing RGB data, sync signals, 2-wire interface, GPIOs, and I2S audio transmitted from serializer to deserializer. The serial stream mostly contains RGB data, sync signals and CRC information, while once in determined cycle time by FCTHRIO_MODE it contains 2-wire interface, GPIOs and I2S audio. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled.

The device supports Open LDI (LVDS) clocks in the range of 10 MHz to 109 MHz over one lane, or 50 MHz to 218 MHz over two lanes. The V-by-One® HS II serial stream rate is 4 Gbps maximum (1.5 Gbps minimum).

[Data-rate.FCin)] = Input Data-rate on Forward Channel (FC) per lane
[PCLK.input] = Pixel clock input on V-by-One® HS II per lane
[FClaneNum] = V-by-One® HS II Forward Channel input Lane number selected by pin setting
[oLDIportNum] = Open-LDI output port number selected by pin setting
[THRIOrate] = 8/7 (when FCTHRIO_MODE=0 selected by pin setting as 8cycle mode)
4/3 (when FCTHRIO_MODE=1 selected by pin setting as 4cycle mode)
[LowFreqMode] = x1 or x2 or x4 selected by register setting
[PCLK.input] = [Data-rate.FC)] / (3 x 8 x 10/8)
[PCLK.oLDIout)] = Pixel clock output on Open-LDI per port = [F(oLDIout)]
[PCLK.oLDIout)] = [PCLK.input] x {[FClaneNum] / [oLDIportNum]} x {1/[THRIOrate]} x {1/[LowFreqMode]}
[PCLK.oLDIout.total] = Total Pixel clock output on oLDI = [F(oLDIout.total)] = [F(oLDIout)] x [oLDIportNum]

The THCV334-Q requires internal settings to be adjusted according to the PCLK (FOLDIOUT) from Open-LDI per port. See the table below for details.

PCLK (FOLDIOUT)		
Item	10MHz to 25MHz	25MHz to 170MHz
PLL (0x0271 to 0x0278)	See 7.3.20 section	Auto (Default)

PCLK (FOLDIOUT)		
Item	10MHz to 30MHz	30MHz to 170MHz
R_LFEN (0x0504 bit[0])	0x1	0x0 (Default)

7.3.2. Back Channel Data Transfer

The Backward Channel (BC) provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as serial frames. The back channel control data is transferred over both serial links along with the high-speed forward data with DC balance coding. This architecture provides a backward path across the serial link together with a high-speed forward channel. The back channel contains the 2-wire interface, CRC and GPIO information with 10 ~ 26.7 Mbps line rate (configured by the compatible serializer).

[Data-rate.BCout)] = Output Data-rate on Backward Channel (BC)

[Data-rate.BCout)] = [Data-rate.FCin)] / 150

7.3.3. BCC Port Register Access

The THCV334-Q contains one upstream ports.

The THCV334-Q and counterpart compatible serializer have independent 2-wire slave address respectively. They require independent setting transaction.

7.3.4. Oscillator Output

The deserializer provides an optional LOCLK[2:1]N/P output when the input clock (serial stream) has been lost. This is based on an internal oscillator and may be controlled from register.

7.3.5. Clock and Output Status

When PDN is driven HIGH, the CDR PLL begins locking to the serial input and LOCK is tri-state or LOW. After the deserializer completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the LVDS outputs. The state of the LVDS outputs is based on the OE pin setting.

7.3.6. LVCMOS VDDIO Option

VDDIO offer compatibility with external system interface signals.

Note:When configuring the VDDIO power supplies, all the single-ended data and control input pins for device must scale together with the same operating VDDIO levels.

7.3.7. Power Down (PDN)

The deserializer has a PDN input pin to ENABLE or POWER DOWN the device. This pin can be controlled by the host or through the VDDIO, where VDDIO = 3 V to 3.6 V or VDD33. To save power, disable the link when the display is not needed (PDN = LOW). When the pin is driven by the host, make sure to release it after VDD33 and VDDIO have reached final levels; no external components are required.

7.3.8. Interrupt Pin — Functional Description and Usage (INTN_IN)

The INTN_IN pin is an active low interrupt input pin. This interrupt signal, when configured, propagates to the paired serializer. Consult the appropriate serializer data sheet for details of how to configure this interrupt functionality.

1. On the Serializer, set remote INTN_IN interrupt Enable
2. Deserializer INTN _IN pin is set LOW by some downstream
3. Serializer pulls INTN pin LOW. The signal is active LOW, so a LOW indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read Interrupt source indicator register.
5. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving the Deserializer INT N _IN . This would be when the downstream device releases the INT N _IN pin on the Deserializer. The system is now ready to return to step (2) at next falling edge of INT N.
6. A wrote to Interrupt clear will clear the interrupt at the Serializer, releasing INTN

7.3.9. General-Purpose I/O (GPIO)

7.3.9.1. GPIO[3:0] Configuration

In normal operation, GPIO[3:0] may be used as general purpose IOs in either forward channel (outputs) or back channel (inputs) mode. GPIO modes may be configured from the registers.

7.3.9.2. D_GPIO[3:0] Configuration

In normal operation, D_GPIO[3:0] may be used as general purpose IOs in either forward channel (outputs) or back channel (inputs) mode. GPIO modes may be configured from the registers.

7.3.9.3. GPIO_REG[9:5] Configuration

GPIO_REG[9:5] are register only GPIOs and may be programmed as outputs or read as inputs through local register bits only. Where applicable, these bits are shared with I2S pins and will override I2S input if enabled into GPIO_REG mode.

NOTE : Local GPIO value may be configured and read either through local register access, or remote register access through the Bidirectional Control Channel.

7.3.10. General Protocol Communication

7.3.10.1. SPI Communication

SPI Communication can be configured by utilizing GPIO function.

SPI data rates are not symmetrical for the two modes of operation. Data over the forward channel can be sent much faster than data over the reverse channel. The SPI Control Channel can operate in a high-speed when writing data only by FC, but must operate at lower frequencies when reading data by FC, BC, and BCC.

NOTE: SPI cannot be used to access Serializer / Deserializer registers.

7.3.10.2. UART Communication

UART Communication can be configured by utilizing GPIO function.

7.3.10.3. PWM Bridge

PWM Bridge can be configured by utilizing GPIO function. Data over the forward channel can be sent much faster than data over the reverse channel.

7.3.11. Family Compatibility

This V-by-One® HS II serializer is not backward compatible to the THCV23x nor THCV24x series.

7.3.12. Adaptive Equalizer

The V-by-One® HS II receiver inputs incorporate an adaptive equalizer (AEQ) to compensate for signal degradation from the communications channel and interconnect components. Each RX port signal path continuously monitors cable characteristics for long-term cable aging and temperature changes. The AEQ is primarily intended to adapt and compensate for channel losses over the lifetime of a cable installed in an automobile. The AEQ attempts to optimize the equalization setting of the RX receiver. This adaption includes compensating insertion loss from temperature effects and aging degradation due to bending and flexion. To determine the maximum cable reach, factors that affect signal integrity such as jitter, skew, inter-symbol interference (ISI), crosstalk, and so forth, must also be considered.

The equalization configuration programmed in registers. Adaptive or manual control is selectable.

The equalization status selected by Adaptive Equalizer can be monitored in registers.

7.3.12.1. Transmission Distance

When designing the transmission channel, consider the total insertion loss of all components in the signal path between a serializer and a deserializer. An example of the transmission channel connects from a V-by-One® HS II serializer (SER) to a deserializer would consist of a serializer PCB, two or more connectors, one or more cables, and a deserializer PCB.

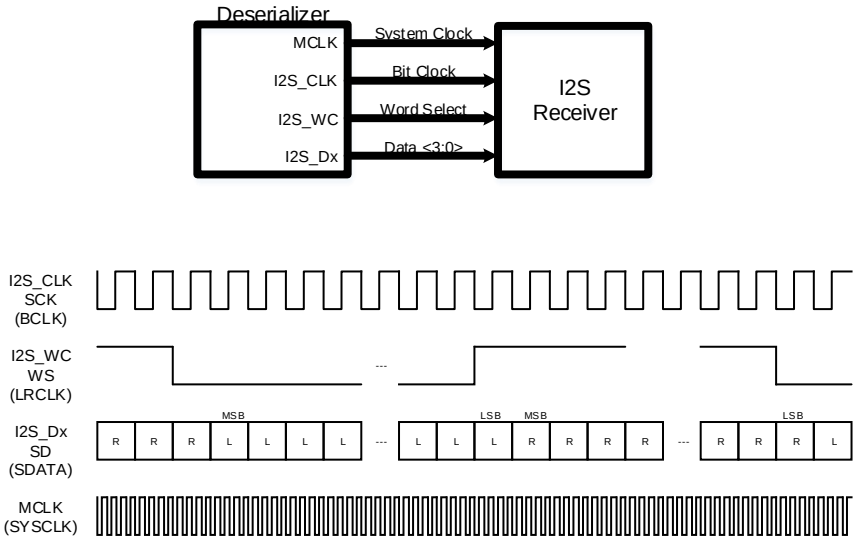
The attenuation increases with cable length and frequency. The trace length of the PCB has very small contribution to the differential insertion loss of the transmission channel.

PCLK (MHz) with FCTHRIO_MODE=0	V-by-One® HS II LINE RATE (Gbps)	NYQUIST FREQUENCY (GHz)	(Informative) CHANNEL ATTENUATION (dB)	(Informative) TYPICAL CABLE LENGTH (m)
45	1.54	0.77	-20	15
75	2.57	1.29	-17	12
85	2.91	1.46	-15	10
94	3.22	1.61	-12	7
96	3.29	1.65	-9	5
109	3.74	1.87	-5	3
150	2.57	1.29	-17	12 (2xFC)
170	2.91	1.46	-15	10 (2xFC)
188	3.22	1.61	-12	7 (2xFC)
192	3.29	1.65	-9	5 (2xFC)
218	3.74	1.87	-5	3 (2xFC)

7.3.13. Audio Modes

7.3.13.1. I2S Audio Interface

The THCV334-Q deserializer features six I2S output pins that, when paired with a compatible serializer supports 7.1 High-Definition (HD) Surround Sound audio applications. The bit clock (I2S_CLK) supports frequencies restricted by FC PCLK. Four I2S data outputs transport two channels of I2S-formatted digital audio each, with each channel delineated by the word select (I2S_WC) output.



7.3.13.2. I2S MCLK

The deserializer has an I2S Master Clock Output (MCLK). The MCLK frequencies can be set by register. MCLK maximum frequency must be below 25MHz.

SAMPLE RATE fs (kHz)	I2S DATA WORD SIZE(bit)	I2S CLK (MHz)	MCLK OUTPUT SAMPLING	MCLK OUTPUT (MHz)
32	16	1.024	192	6.144
32	16	1.024	256	8.192
44.1	16	1.4112	192	8.4672
44.1	16	1.4112	256	11.2896
48	16	1.536	192	9.216
48	16	1.536	256	12.288
96	16	3.072	192	18.432
96	16	3.072	256	24.576
32	24	1.536	192	6.144
32	24	1.536	256	8.192
44.1	24	2.1168	192	8.4672
44.1	24	2.1168	256	11.2896
48	24	2.304	192	9.216
48	24	2.304	256	12.288
32	32	2.048	256	8.192
44.1	32	2.8224	256	11.2896
48	32	3.072	256	12.288

7.3.14. Data Transfer Speed

Symbol	Parameter	Condition	formula	unit
fSMPL _GPI2BC	Digitize Sampling Rate Through GPIO from GPI to BC	y=GPIO_CNT_REGS.SMPNUM=4or8 (active GPIOs)	fSMPL_GPI2BC =1/{20*y*(30*TRFCBIT)}	(sample /second)
fSMPL _INTB_IN2BC	Digitize Sampling Rate Interrupt from INTB_IN to BC	-	fSMPL_INTB_IN2BC =1/[1280*(30*TRFCBIT)]	(sample /second)

7.3.15. Link Status Monitor

The THCV334-Q deserializer have several Link Status Monitor functions like below.

2-wire interface unique ID

Forward Channel V-by-One® HS II Rx monitor (including CRC)

I2S MCLK PLL status monitor

In addition, Open-LDI LVDS Tx output source CRC status code can be embedded into dedicated output data mapping location. CRC code can be checked at specially designed counterpart Rx.

7.3.16. Internal Pattern Generation

The THCV334-Q deserializer provides an internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode but with clock input, the test pattern will be displayed even if no data input is applied.

7.3.17. Internal Status Monitoring output

Internal status signal can be monitored as external MON0/MON1 pin output by register setting.

7.3.18. Output Spread Spectrum

Spread Spectrum Clock Generation (SSCG) modulation is available to apply on Open-LDI output.

SSCG modulated input and internal additional SSCG modulation are not available at the same time.

$$[PCLK.oLDIout]|_{no\ SSCG} \times \frac{(100 - |[R\_SPREAD]|)}{100} < [PCLK.oLDIout]|_{SSCG.CenterSpread} < [PCLK.oLDIout]|_{no\ SSCG} \times \frac{(100 + |[R\_SPREAD]|)}{100}$$

$$[PCLK.oLDIout]|_{no\ SSCG} \times \frac{(100 - |[R\_SPREAD]|)}{100} < [PCLK.oLDIout]|_{SSCG.DownSpread} < [PCLK.oLDIout]|_{no\ SSCG}$$

7.3.19. IO digital filter

Digital filters are prepared for IOs. GPIO digital filter can be arranged by register setting. SCL, SDA, and PDN, several VDDIO CMOS Input (Low speed) pins have also prepared digital filters with fixed tOSC x8 cycle filter setting behavior.

7.3.20. PLL manual operation for Low Frequency PCLK (OLDIOUT) output between 10MHz to 25MHz

For typical operation, PLL manual setting is not required for normal operation. When PCLK (OLDIOUT) is between 10MHz to 25MHz, PLL manual setting is required.

For PLL manual setting, PLL_SPD is supposed to be set 1 (PLL Power down) from default value 0 before PLL manual parameters setting and re-activation (PLL power on) and start of normal operation.

PLL Setting	PCLK (FOLDIOUT)	
	10MHz to 20MHz	20MHz to 25MHz
0x0271	0x07	0x07
0x0272	0x00	0x00
0x0273	0x37	0x37
0x0274	0x20	0x20
0x0276	0x00	0x00
0x0277	0x67	0x37
0x0278	0x01	0x01
-	Register set1	Register set2

For PLL manual setting, PLL_SPD is supposed to be set 1 (PLL Power down) from default value 0 before PLL manual parameters setting and re-activation (PLL power on) and start of normal operation.

Set Register for Serializer part as necessary

Link up

cmd: write devaddr: 0x77 regaddr: 0x0000 val: 0x01 //PLL Power down

Set Register set1 or 2

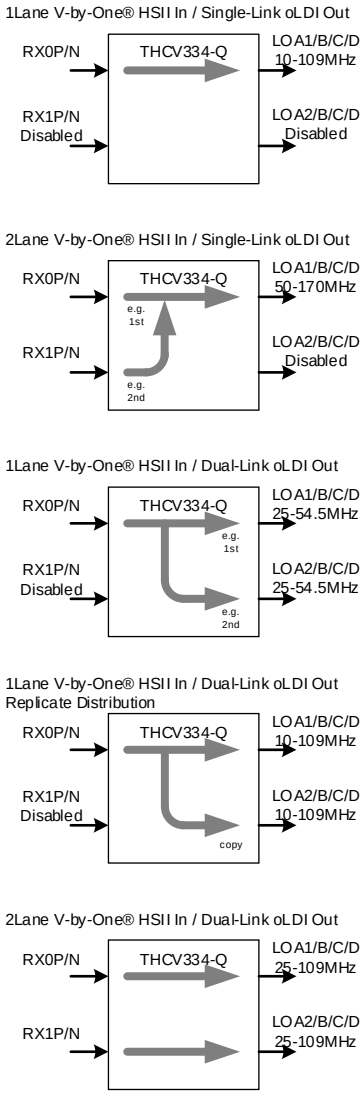
cmd: write devaddr: 0x77 regaddr: 0x0000 val: 0x00 //PLL Power on

cmd: write devaddr: 0x77 regaddr: 0x0504 val: 0x01 // R_LFEN

7.4. Device Functional Modes

7.4.1. Mode Select Configuration Settings (BASEMODE[1:0])

Configuration of the device may be done via the FCINPUTMODE_BM1 / LOUTPUTMODE_BM 0 ,BASEMODE [1:0] input pins, or via the configuration registers.



7.4.1.1. 1-Lane V-by-One® HS II input, Single Link Open-LDI Output Operation

1-Lane V-by-One® HS II input, Single Link Open-LDI Output mode supports frequency up to 109MHz for 24-bit video when paired with the compatible serializer.

7.4.1.2. 2-Lane V-by-One® HS II input, Single Link Open-LDI Output Operation

2-Lane V-by-One® HS II input, Single Link Open-LDI Output mode supports frequency up to 170MHz for 24-bit video when paired with the compatible serializer. This allows support for full 1080p video.

7.4.1.3. 1-Lane V-by-One® HS II input, Dual Link Open-LDI Output Operation

1-Lane V-by-One® HS II input, Dual Link Open-LDI Output mode supports frequency up to 109MHz for 24-bit video when paired with the compatible serializer.

7.4.1.4. 1-Lane V-by-One® HS II input, Dual Link Open-LDI Output Replicate Distribution

In this mode, the same video (up to 109MHz, 24-bit color) is delivered to each Open-LDI ports.

7.4.1.5. 2-Lane V-by-One® HS II input, Dual Link Open-LDI Output Operation

2-Lane V-by-One® HS II input, Dual Link Open-LDI Output mode, the deserializer receives a single video stream of alternating pixels on two downstream links. The compatible serializer must be capable of sending the dual stream video. This mode is capable of supporting an Open LDI clock frequency of up to 218MHz, with each V-by-One® HS II Rx port running at one-half the frequency. This allows support for full 1080p video.

7.4.2. Low Frequency mode

Low Frequency mode support speeded-up Forward Channel data-rate x2 or x4 in order to support the situation in which Open-LDI output frequency is too low to excess minimum data-rate of Forward Channel by the use of normal speed. For usage of Low Frequency mode, counterpart V-by-One® HS II transmitter must have installed Low Frequency mode format encoder.

7.4.3. Open-LDI Output Frame and Color Bit Mapping Select

The THCV334-Q can be configured to accept 24-bit color (8-bit RGB) with several mapping schemes. Each unit corresponds to a single pixel clock (PCLK) cycle. The Open-LDI LVDS clock output to CLK± follows a 4:3 duty cycle scheme, with each 28-bit pixel frame starting with two LVDS bit clock periods high, three low, and ending with two high. The mapping scheme is controlled by Register.

Open-LDI LVDS JEIDA 8bit Format

CLK

	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A1/2 ch	G2	R7	R6	R5	R4	R3	R2
B1/2 ch	B3	B2	G7	G6	G5	G4	G3
C1/2 ch	DE	VS	HS	B7	B6	B5	B4
D1/2 ch	-	B1	B0	G1	G0	R1	R0

Open-LDI LVDS VESA 8bit Format

CLK

	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A1/2 ch	G0	R5	R4	R3	R2	R1	R0
B1/2 ch	B1	B0	G5	G4	G3	G2	G1
C1/2 ch	DE	VS	HS	B5	B4	B3	B2
D1/2 ch	-	B7	B6	G7	G6	R7	R6

MIPI DPI THC63LVD827-Q Conversion Format

CLK

	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A1 ch	R2	R1	R0	G7	G6	G5	G4
B1 ch	-	-	R7	R6	R5	R4	R3
C1 ch	DE	VS	HS	-	-	-	-
D1 ch	-	-	-	-	-	-	-

	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A2 ch	B6	B5	B4	B3	B2	B1	B0
B2 ch	-	-	G3	G2	G1	G0	B7
C2 ch	DE	VS	HS	-	-	-	-
D2 ch	-	-	-	-	-	-	-

FCB-EV Single Pixel Link External Sync Format

CLK

SONY.S	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A1 ch	Y6	Y5	Y4	Y3	Y2	Y1	Y0
B1 ch	-	-	-	DE	VS	HS	Y7
C1 ch	-	C5	C4	C3	C2	C1	C0
D1 ch	-	-	-	-	-	C6	C7

FCB-EV Single Pixel Link Internal Sync Format

CLK

SONY.S	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A1 ch	Y6	Y5	Y4	Y3	Y2	Y1	Y0
B1 ch	-	-	-	-	-	-	Y7
C1 ch	-	C5	C4	C3	C2	C1	C0
D1 ch	-	-	-	-	-	C6	C7

FCB-EV Dual Pixel Link External Sync Format

CLK

SONY.D	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A1/2 ch	Y6	Y5	Y4	Y3	Y2	Y1	Y0
B1/2 ch	-	-	-	-	VS	HS	Y7
C1/2 ch	DE	C5	C4	C3	C2	C1	C0
D1/2 ch	-	-	-	-	-	C6	C7

FCB-EV Dual Pixel Link Internal Sync Format

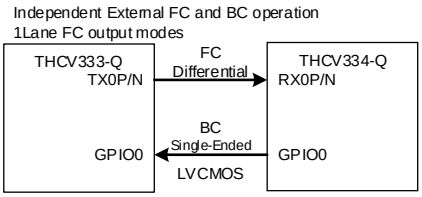
CLK

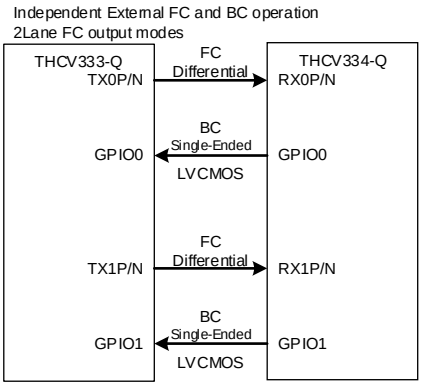
SONY.D	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A1/2 ch	Y6	Y5	Y4	Y3	Y2	Y1	Y0
B1/2 ch	-	-	-	-	-	-	Y7
C1/2 ch	-	C5	C4	C3	C2	C1	C0
D1/2 ch	-	-	-	-	-	C6	C7

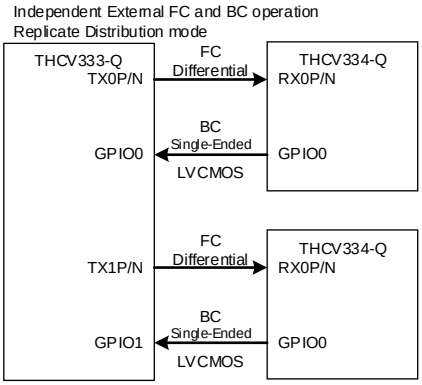
7.4.4. Independent External FC and BC operation mode

BCC operation can be separated in Independent External FC and BC mode. Register EXTBC control can enable separated BC. GPIO0/1 pins operate as external outputs.

cmd: write devaddr: 0x77 regaddr: 0x010A val: 0x01 // VbyOneHSII BCC external input select



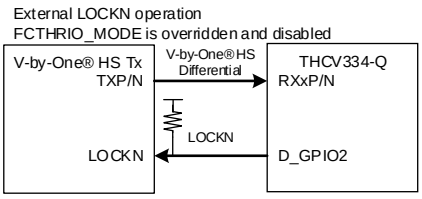




7.4.5. V-by-One® HS external LOCKN mode

V-by-One® HS behavior, in which FCTHRIO is disabled, is connectable to standard V-by-One® HS product with external LOCKN connection.

V-by-One® HS LOCKN outputs for respective lanes, Lane0 and Lane1, are output separately, which may require external care on PCB.



cmd: write devaddr: 0x77 regaddr: 0x0C31 val: 0x01 //D_GPIO2 open-drain output mode

cmd: write devaddr: 0x77 regaddr: 0x1C0D val: 0x5D //D_GPIO2 LOCKN0 output

cmd: write devaddr: 0x77 regaddr: 0x0101 val: 0x12 //Through IO Disable

cmd: write devaddr: 0x77 regaddr: 0x010A val: 0x01 //without BC

7.5. Spread Spectrum Tolerance

Forward Channel accommodate Spread Spectrum Clock Generation (SSCG) modulation.

Spread Spectrum Clock Generation (SSCG) modulation is available to apply on Open-LDI LVDS output.

Maximum available modulation frequency and modulation rate is 30kHz +/-0.5% center spread profile.

7.6. Programming

7.6.1. Serial Control Bus

This deserializer may also be configured by the use of a 2-wire interface serial control bus or BCC function from compatible counterpart serializer. Multiple devices may share the serial control bus (multiple device addresses supported). The device address (2-wire slave address) is set by AIN pin or register setting.

THCV334-Q has 2-wire serial master and slave function. BCC function of THCV334-Q realize 2-wire serial interface remote bridge from remote 2-wire serial master with BCC compatible counterpart serializer to THCV334-Q itself or local 2-wire slave device.

7.6.2. Serial slave device ID

AIN pin determines 2-wire slave Device ID setting.

Note: When BCC Master side remote access to THCV334-Q, the serial slave ID is in the BCC Master are followed.

7.6.3. Serial Read/Write access to local Register

HOST MPU can directly access THCV334-Q local register by 2-wire serial I/F.

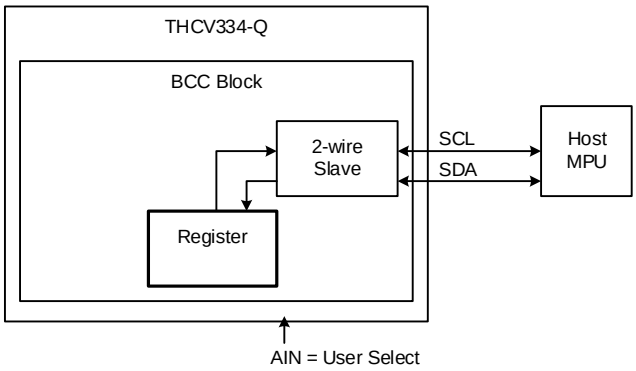


Figure 7. Host to local register access configuration

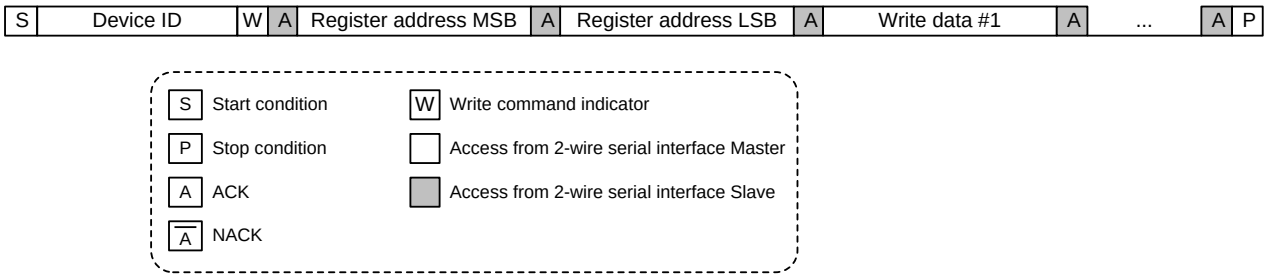


Figure 8. Serial I/F write to local register protocol

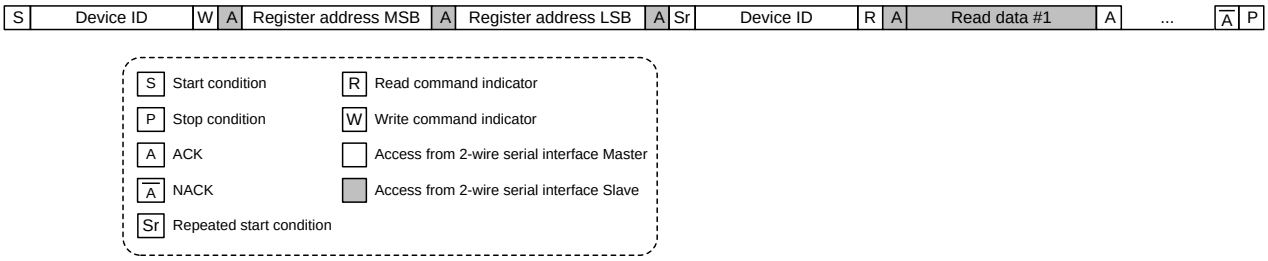


Figure 9. Serial I/F read to local register protocol

7.6.4. Bi-directional Control Channel bus

THCV334-Q has Bi-directional Control Channel (BCC) which enables bi-directional transmission of 2-wire serial interface signals, GPIO signals and also HTPDN/LOCKN signals for FC. THCV334-Q is BCC Slave and connectable to BCC Master device such as THCV333-Q.

THCV334-Q has 2-wire serial master block and can connect to 2-wire serial slave devices. Remote side HOST MPU, which is connected to BCC Master device, can access register of BCC Master device, BCC Slave device and 2-wire serial slave devices connected to BCC Slave device. While THCV334-Q has also 2-wire serial slave block and can connect to local MCU as Multi-Master coexistence.

7.6.4.1. BCC 2-wire Pass Through mode with divided write/read mode

THCV334-Q processing protocol “Divided write/read” scheme divides 2-wire commands into determined data Byte groups. Each data Byte groups are sent separately on remote side. Burst write/read access target Sub-Address (Word-Address) is interpreted so that subsequent Sub-Address (Word-Address) from 2nd group is automatically and properly incremented. The detailed operation follows the settings on the BCC Master (Serializer) side.
Must be set the same mode with the BCC Master (Serializer) side.
cmd: write devaddr: 0x77 regaddr: 0x0B6A val: 0x00 //Default

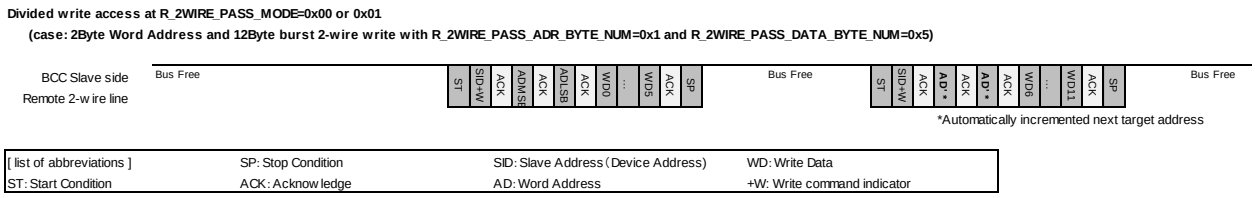


Figure 10. 2-wire Pass Through Divided mode BCC Slave command write scheme

7.6.4.2. BCC 2-wire Pass Through mode with non-divided write/read mode

THCV334-Q processing protocol “Non-divided write/read” scheme divides 2-wire commands into determined data Byte groups. However burst write/read access target Sub-Address (Word-Address) is NOT incremented, the access complete including SCL Low period.

cmd: write devaddr: 0x77 regaddr: 0x0B6A val: 0x01 //Non-divided write/read mode enable

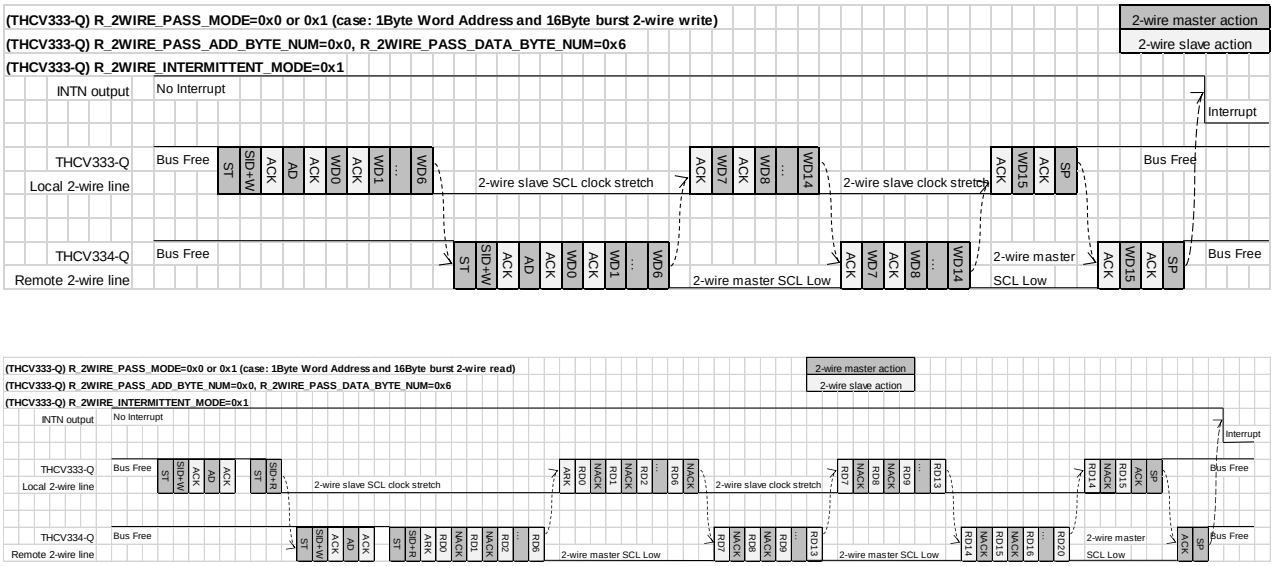


Figure 11. 2-wire Pass Through Non-divided mode BCC Slave command write/read scheme

7.6.5. Restrictions on Multi-Master Coexistence Operation

Only one 2-wire interface transaction should be active at any time across the Bidirectional Control Channel. If Multi-Master coexistence are required, some method of transferring control initiative and avoidance of control collision between 2-wire interface masters at local and remote should be implemented.

7.7. Register Maps

Register regions are sectioned as below.

Register address		
Start	End	Description
0x0000	0x00FF	RST_control
0x0100	0x01FF	MODE_of_operation_control
0x0200	0x02FF	CLK_and_PLL_control
0x0500	0x05FF	LVDS_TX_control
0x0600	0x067F	FC_V-by-OneHSII_control
0x0680	0x06FF	PATTERN_GENarator
0x0700	0x07FF	PATTERN_CHecKer
0x0900	0x0AFF	FCRX_BCTX_LINK_control
0x0B00	0x0BFF	I2C_control
0x0C00	0x0CFF	I2SGPIO_control
0x0D00	0x0DFF	I2SPLL_control
0x1000	0x10FF	FCRXLANE0_control
0x1100	0x11FF	FCRXLANE1_control
0x1200	0x12FF	CHECKSUM
0x1300	0x13FF	INTN_interrupt_control
0x1700	0x17FF	FC_THRIO_control
0x1C00	0x1CFF	Extra_control

NOTE

Any registers, which are not explained in this Register Maps, must be left untouched (No write nor read are allowed.) as default.

Any reserved registers, which are explained in this Register Maps and its all bits of the register address is reserved, must be left untouched (No write nor read are allowed.) as default.

Any reserved bits, which are explained in this Register Maps and remained bits other than the reserved bits in the same address is available function bits, according to the instruction of function bits, reserved bits can be write or read as 1 Byte unit access of 2-wire communication.

Any Read Only registers, whose “R/W” classification column is “R” in this Register Maps, are prohibited to be written by Write access.

Address	bit	Register Name	width	R/W	Init	Description
0x0000	[7:2]	reserved	6	-	-	-
	[1]	I2SPLL_SPD	1	R/W	1'h0	I2S PLL Power down 0x0: Power on 0x1: Power down
	[0]	PLL_SPD	1	R/W	1'h0	PLL Power down 0x0: Power on 0x1: Power down When changing PLL settings in Manual mode, need to power down once.
0x0001	[7:0]	reserved	8	-	-	-
0x0002	[7:0]	reserved	8	-	-	-
0x0003	[7:0]	reserved	8	-	-	-
0x0004	[7:0]	reserved	8	-	-	-
0x0005	[7:0]	reserved	8	-	-	-
0x0006	[7:0]	reserved	8	-	-	-
0x0007	[7:0]	reserved	8	-	-	-
0x0008	[7:0]	reserved	8	-	-	-
0x000B	[7:0]	reserved	8	-	-	-
0x000C	[7:0]	reserved	8	-	-	-
0x000D	[7:0]	reserved	8	-	-	-
0x000E	[7:0]	reserved	8	-	-	-
0x000F	[7:0]	KEY	8	R/W	1'h0	Power down registers access Enable 0x77: Enable (0x0000 - 0x000E registers are able to set) Other: Disable
0x0010	[7:0]	reserved	8	-	-	-
0x0011	[7:0]	reserved	8	-	-	-
0x0012	[7:0]	reserved	8	-	-	-
0x0013	[7:0]	reserved	8	-	-	-
0x0014	[7:0]	reserved	8	-	-	-
0x0015	[7:0]	reserved	8	-	-	-
0x0016	[7:0]	reserved	8	-	-	-
0x0017	[7:0]	reserved	8	-	-	-
0x0018	[7:0]	reserved	8	-	-	-
0x0019	[7:0]	reserved	8	-	-	-
0x001A	[7:2]	reserved	6	-	-	-
	[1]	PLZLOCK_EN	1	R/W	1'h1	PLL Lock signal select 0x0: Disable PLL Lock signal 0x1: Enable PLL Lock signal
	[0]	RXLOCKN_EN	1	R/W	1'h1	VbyOneHSII RX Lock signal select 0x0: Disable VbyOneHSII RX Lock signal 0x1: Enable VbyOneHSII RX Lock signal When using internal OSC clock for PATGEN enable, should be set 0x0.
0x001B	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0020	[7:1]	reserved	7	-	-	-
	[0]	CMN_SRST	1	WC	1'h0	All Register clear 0x1: Reset and automatic clear
0x0021	[7:5]	reserved	3	-	-	-
	[4]	FCTXPDX_MON	1	R	1'h0	VbyOneHSII FC TX Power down Status Monitor 0x1: Power on, 0x0: Power down
	[3:2]	FCRXPDX_MON	2	R	2'h0	VbyOneHSII FC RX Power down Status Monitor [3]: Lane1 0x1: Power on, 0x0: Power down [2]: Lane0 0x1: Power on, 0x0: Power down
	[1]	I2SLLPDX_MON	1	R	1'h0	I2S PLL Power down Status Monitor 0x1: Power on, 0x0: Power down
	[0]	FPLLPDX_MON	1	R	1'h0	PLL Power down Status Monitor 0x1: Power on, 0x0: Power down
0x0022	[7:6]	reserved	2	-	-	-
	[5:4]	BCBUFPDX_MON	2	R	2'h0	VbyOneHSII BC Buffer Power down Status Monitor [5]: Lane1 0x1: Power on, 0x0: Power down [4]: Lane0 0x1: Power on, 0x0: Power down
	[3:2]	BCBIASPDX_MON	2	R	2'h0	VbyOneHSII BC Bias Power down Status Monitor [3]: Lane1 0x1: Power on, 0x0: Power down [2]: Lane0 0x1: Power on, 0x0: Power down
	[1:0]	BCLDOPDX_MON	2	R	2'h0	VbyOneHSII BC LDO Power down Status Monitor [1]: Lane1 0x1: Power on, 0x0: Power down [0]: Lane0 0x1: Power on, 0x0: Power down
0x0023	[7:6]	FIFO_FCTXRSTX_MON	2	R	2'h0	VbyOneHSII FC TX FIFO Reset Status Monitor [7]: Lane1 0x1: Reset release , 0x0: Reset [6]: Lane0 0x1: Reset release , 0x0: Reset
	[5:4]	FCTXRSTX_MON	2	R	2'h0	VbyOneHSII FC TX Reset Status Monitor [5]: Lane1 0x1: Reset release , 0x0: Reset [4]: Lane0 0x1: Reset release , 0x0: Reset
	[3:2]	FIFO_FCRXRSTX_MON	2	R	2'h0	VbyOneHSII FC RX FIFO Reset Status Monitor [7]: Lane1 0x1: Reset release , 0x0: Reset [6]: Lane0 0x1: Reset release , 0x0: Reset
	[1:0]	FCRXRSTX_MON	2	R	2'h0	VbyOneHSII FC RX Reset Status Monitor [5]: Lane1 0x1: Reset release , 0x0: Reset [4]: Lane0 0x1: Reset release , 0x0: Reset
0x0024	[7:6]	reserved	2	-	-	-
	[5]	I2CBRSTX_MON	1	R	1'h0	BCC 2-wire Reset Status Monitor 0x1: Reset release , 0x0: Reset
	[4]	I2SGPIO_RSTX_MON	1	R	1'h0	I2S Reset Status Monitor 0x1: Reset release , 0x0: Reset
	[3]	APBRSTX_MON	1	R	1'h0	APB Reset Status Monitor 0x1: Reset release , 0x0: Reset
	[2]	OSCRSTX_MON	1	R	1'h0	Internal OSC Reset Status Monitor 0x1: Reset release , 0x0: Reset
	[1:0]	BCRSTX_MON	2	R	2'h0	VbyOneHSII BC Reset Status Monitor [1]: Lane1 0x1: Reset release , 0x0: Reset [0]: Lane0 0x1: Reset release , 0x0: Reset
0x0025	[7]	reserved	1	-	-	-
	[6]	VRZ1_LOCKN_MON	1	R	1'h0	VbyOneHSII LOCKN status monitor for lane1 0x1: Unlock, 0x0: Lock
	[5]	VRZ0_LOCKN_MON	1	R	1'h0	VbyOneHSII LOCKN status monitor for lane0 0x1: Unlock, 0x0: Lock
	[4]	reserved	1	-	-	-
	[3]	reserved	1	-	-	-
	[2]	reserved	1	-	-	-
	[1]	PLL_PD_MON	1	R	1'h0	PLL Power down status monitor 0x1: Power down, 0x0: Power on
	[0]	UNSTABLE_DET_MON	1	R	1'h0	Unstable detector status monitor 0x1: Detect unstable, 0x0: Not detect unstable
0x0026	[7:0]	reserved	8	-	-	-
0x0027	[7:0]	reserved	8	-	-	-
0x0028	[7:0]	reserved	8	-	-	-
0x0029	[7:0]	reserved	8	-	-	-
0x002A	[7:0]	reserved	8	-	-	-
0x002B	[7:0]	reserved	8	-	-	-
0x002C	[7:0]	reserved	8	-	-	-
0x002D	[7:0]	reserved	8	-	-	-
0x002E	[7:0]	reserved	8	-	-	-
0x002F	[7:0]	reserved	8	-	-	-
0x0030	[7:0]	GBL_SRST	8	R/W	8'h0	Global Reset 0x00: Normal operation 0xAA: Logic Reset. All registers return to the initial values. This register also returns to 0x00. Others: reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0100	[7:5]	reserved	3	-	-	-
	[4]	BASEMODE_OVERRIDE	1	R/W	1'h0	BASEMODE override enable. Can overridee the BM0/1 pin settings. 0x0: disable 0x1: enable
	[3:2]	reserved	2	-	-	-
	[1:0]	BASEMODE_REG	2	R/W	2'h0	<this regiseter is valid only when 0x0100[4]=1> BASEMODE setting 0x0: Single VbyOneHSII input, Single LVDS output mode 0x1: Single VbyOneHSII input, Dual LVDS output mode 0x2: Dual VbyOneHSII input, Single LVDS output mode 0x3: Dual VbyOneHSII input, Dual LVDS output mode
0x0101	[7:5]	reserved	3	-	-	-
	[4]	FCTHRIO_MODE_OVERRIDE	1	R/W	1'h0	FCTHRIO MODE override enable. Can overridee the FCTHRIO_MODE pin setting. 0x0: disable 0x1: enable
	[3:2]	reserved	2	-	-	-
	[1]	FCTHRIO_MODE_DISABLE	1	R/W	1'h0	<this regiseter is valid only when 0x0101[4]=1> FCTHRIO disable setting. To connect with VbyOneHS Serializer may set disable. 0x0: enable 0x1: disable
	[0]	FCTHRIO_MODE_REG	1	R/W	1'h0	<this regiseter is valid only when 0x0101[4]=1> FCTHRIO MODE setting 0x0: 8cycle mode 0x1: 4cycle mode Need to set the same mode with Serializer.
0x0102	[7:2]	reserved	6	-	-	-
	[1:0]	DUPLICATE_REG	2	R/W	2'h0	Low frequency mode select. This register is used when the VbyOneHSII FC rate is too slow to meet the specification or to increase the sampling rate of the control signal. This setting should be the same value with attached Serializer. 0x0: FC data rate x1 mode 0x1: FC data rate x2 mode 0x2: FC data rate x4 mode 0x3: Reserved
0x0103	[7:1]	reserved	7	-	-	-
	[0]	HIGHFREQIN_REG	1	R/W	1'h1	VbyOneHSII clock frequency select 0x0: Set when [PCLK.input] clock frequency 25MHz to 60MHz 0x1: Set when [PCLK.input] clock frequency 60MHz to 133.3MHz
0x0104	[7:1]	reserved	7	-	-	-
	[0]	LVDSBITMODE_REG	1	R/W	1'h0	LVDS bit mode select 0x0: 8bit mode 0x1: 6bit mode
0x0105	[7:1]	reserved	7	-	-	-
	[0]	DISTMODE_REG	1	R/W	1'h0	LVDS Distribution output mode select 0x0: Distribution output mode disable 0x1: Distribute LVDS output mode enable
0x0107	[7:0]	reserved	8	-	-	-
0x0108	[7:1]	reserved	7	-	-	-
	[0]	TXLSWAP_REG	1	R/W	1'h0	LVDS output port swap enable setting 0x0: Disable 0x1: Swaps LVDS output port
0x0109	[7:1]	reserved	7	-	-	-
	[0]	OE	1	R/W	1'h0	LVDS output enable select. This register is valid when OE pin set 0(Register entry mode). 0x0: Output disable 0x1: Output enable
0x010A	[7:1]	reserved	7	-	-	-
	[0]	EXTBC_EN_REG	1	R/W	1'h0	VbyOneHSII BCC external output select. It also should be set enable when connect to VbyOneHS protocol Serializer. 0x0: Disable, Normal operation. 0x1: Enable
0x010B	[7:0]	reserved	8	-	-	-
0x010C	[7:0]	reserved	8	-	-	-
0x010D	[7:0]	reserved	8	-	-	-
0x010E	[7:0]	reserved	8	-	-	-
0x010F	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0110	[7:0]	reserved	8	-	-	-
0x0111	[7:0]	reserved	8	-	-	-
0x0112	[7:0]	reserved	8	-	-	-
0x0113	[7:0]	reserved	8	-	-	-
0x0114	[7:0]	reserved	8	-	-	-
0x0115	[7:0]	reserved	8	-	-	-
0x0116	[7:0]	reserved	8	-	-	-
0x0117	[7:0]	reserved	8	-	-	-
0x0121	[7:1]	reserved	7	-	-	-
	[0]	DES_RXAEQEN	1	R/W	1'h1	VbyOneHSII Adaptive CTLC Equalizer Setting 0x0: Static Equalizer Mode. The strength is set by 0x0122 [2:0]. 0x1: Adaptive CTLC Equalizer Mode for Strength Control.
0x0122	[7:3]	reserved	5	-	-	-
	[2:0]	DES_RXLEQCTLC	3	R/W	3'h0	<this regiseter is valid only when 0x0121[0]=0> VbyOneHSII CTLC Equalizer strength Control setting 0x0 (0b000): peak gain level0 (the weakest) 0x1 (0b001): peak gain level1 0x3 (0b011): peak gain level2 0x2 (0b010): peak gain level3 0x6 (0b110): peak gain level4 0x7 (0b111): peak gain level5 0x5 (0b101): peak gain level6 0x4 (0b100): peak gain level7 (the strongest)
0x0123	[7:3]	reserved	5	-	-	-
	[2:0]	DES_RXLEQCTLR	3	R/W	3'h5	VbyOneHSII CTLR Equalizer strength Control setting 0x0 (0b000): peak gain level0 (the weakest) 0x1 (0b001): peak gain level1 0x3 (0b011): peak gain level2 0x2 (0b010): peak gain level3 0x6 (0b110): peak gain level4 0x7 (0b111): peak gain level5 0x5 (0b101): peak gain level6 0x4 (0b100): peak gain level7 (the strongest)
0x0124	[7:0]	reserved	8	-	-	-
0x0125	[7:1]	reserved	7	-	-	-
	[0]	DES_RXFLIP	1	R/W	1'h0	VbyOneHSII P/N swap enable setting 0x0: Disable, 0x1: Swaps VbyOneHSII input P/N
0x0126	[7:0]	reserved	8	-	-	-
0x0127	[7:0]	reserved	8	-	-	-
0x0128	[7]	reserved	1	-	-	-
	[6:4]	LEQOC_0	3	R	3'h0	<this regiseter is valid only when 0x0121[0]=0> VbyOneHSII CTLC Equalizer strength Control Observation for Lane0 0x0 (0b000): peak gain level0 (the weakest) 0x1 (0b001): peak gain level1 0x3 (0b011): peak gain level2 0x2 (0b010): peak gain level3 0x6 (0b110): peak gain level4 0x7 (0b111): peak gain level5 0x5 (0b101): peak gain level6 0x4 (0b100): peak gain level7 (the strongest)
	[3]	reserved	1	-	-	-
	[2:0]	reserved	3	-	-	-
0x0129	[7]	reserved	1	-	-	-
	[6:4]	LEQOC_1	3	R	3'h0	<this regiseter is valid only when 0x0121[0]=0> VbyOneHSII CTLC Equalizer strength Control Observation for Lane1 0x0 (0b000): peak gain level0 (the weakest) 0x1 (0b001): peak gain level1 0x3 (0b011): peak gain level2 0x2 (0b010): peak gain level3 0x6 (0b110): peak gain level4 0x7 (0b111): peak gain level5 0x5 (0b101): peak gain level6 0x4 (0b100): peak gain level7 (the strongest)
	[3]	reserved	1	-	-	-
	[2:0]	reserved	3	-	-	-
0x012A	[7:1]	reserved	7	-	-	-
	[0]	EN	1	R/W	1'h0	VbyOneHSII LOCK Status output select for LOCK pin. FC RX Lock signal may be output. 0x0: Hi-Z, 0x1: Output LOCK status

Address	bit	Register Name	width	R/W	Init	Description
0x0140	[7:4]	reserved	4	-	-	-
	[3]	TL12UN_EN	1	R/W	1'h0	VDDTL 1.2V power supply monitor enable setting. Under voltage fault can be detected. The detection result can be output as an Interrupt. 0x0: Disable, 0x1: Enable
	[2]	TL12UP_EN	1	R/W	1'h0	VDDTL 1.2V power supply monitor enable setting. High voltage fault can be detected. The detection result can be output as an Interrupt. 0x0: Disable, 0x1: Enable
	[1]	L12UP_EN	1	R/W	1'h0	VDDL 1.2V power supply monitor enable setting. High voltage fault can be detected. The detection result can be output as an Interrupt. 0x0: Disable, 0x1: Enable
	[0]	IO33UN_EN	1	R/W	1'h0	VDDIO 3.3V power supply monitor enable setting. Under voltage fault can be detected. The detection result can be output as an Interrupt. 0x0: Disable, 0x1: Enable
0x0141	[7]	AIN_PE	1	R/W	1'h1	AIN pin pull-down select setting 0x0: disable 0x1: enable
	[6]	FCTHRIO_MODE_PE	1	R/W	1'h1	FCTHRIO_MODE pin pull-down select setting 0x0: disable 0x1: enable
	[5]	BASEMODE1_PE	1	R/W	1'h1	FCOUTPUTMODE_BM1 pin pull-down select setting 0x0: disable 0x1: enable
	[4]	BASEMODE0_PE	1	R/W	1'h1	LINPUTMODE_BM0 pin pull-down select setting 0x0: disable 0x1: enable
	[3]	MON1_PE	1	R/W	1'h1	MON1 pin pull-down select setting 0x0: disable 0x1: enable
	[2]	MON0_PE	1	R/W	1'h1	MON0 pin pull-down select setting 0x0: disable 0x1: enable
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x0142	[7:4]	reserved	4	-	-	-
	[3]	OE_PE	1	R/W	1'h1	OE pin pull-down select setting 0x0: disable 0x1: enable
	[2]	LOCK_PE	1	R/W	1'h1	LOCK pin pull-down select setting 0x0: disable 0x1: enable
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x0143	[7:2]	reserved	6	-	-	-
	[2]	INTN_IN_PE	1	R/W	1'h1	INTN_IN pin pull-down select setting 0x0: disable 0x1: enable
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x0144	[7:0]	reserved	8	-	-	-
0x01F0	[7:0]	ID0	8	R	8'h74	ID code "t"
0x01F1	[7:0]	ID1	8	R	8'h68	ID code "h"
0x01F2	[7:0]	ID2	8	R	8'h63	ID code "c"
0x01F3	[7:0]	ID3	8	R	8'h76	ID code "v"
0x01F4	[7:0]	ID4	8	R	8'h33	ID code "3"
0x01F5	[7:0]	ID5	8	R	8'h33	ID code "3"
0x01F6	[7:0]	ID6	8	R	8'h34	ID code "4"
0x01F7	[7:0]	ID7	8	R	8'h00	ID code " "

Address	bit	Register Name	width	R/W	Init	Description
0x0250	[7:5]	reserved	3	-	-	-
	[4:0]	CDET_EN	5	R/W	5'h0	Clock Frequency Detector enable. This register can detect the internal clock frequency using the internal oscillator or the VbyOneHSIII clock. It can also detect when the clock frequency crosses above or below a set value. 0x0: Disable, 0x1: Enable [0]: VbyOneHSII FC Lane0 clock [1]: VbyOneHSII FC Lane1 clock [2]: LVDS TX clock [3]: Internal oscillator clock by VbyOneHSII FC Lane0 clock [4]: Reserved [0][1][2] are detected by internal oscillator [3] is detected by LVDS RX clock. It's necessary the stable lock.
0x0260	[7:0]	TGETCNT0_1	8	R	7'h0	<this regiseter is valid only when 0x0250[0]=1> VbyOneHSII FC Lane0 clock frequency counter [15:8] TRFCBIT * 30 = PCLK.input ~ MEASURE_VALUE0 * tosc / TGETCNT0[15:0] MEASURE_VALUE0 = 480 as default when it is unchanged.
0x0261	[7:0]	TGETCNT0_0	8	R	7'h0	<this regiseter is valid only when 0x0250[0]=1> VbyOneHSII FC Lane0 clock frequency counter [7:0]
0x0262	[7:0]	TGETCNT1_1	8	R	7'h0	<this regiseter is valid only when 0x0250[1]=1> VbyOneHSII FC Lane1 clock frequency counter [15:8] TRFCBIT * 30 = PCLK.input ~ MEASURE_VALUE1 * tosc / TGETCNT0[15:0] MEASURE_VALUE1 = 480 as default when it is unchanged.
0x0263	[7:0]	TGETCNT1_0	8	R	7'h0	<this regiseter is valid only when 0x0250[1]=1> VbyOneHSII FC Lane1 clock frequency counter [7:0]
0x0264	[7:0]	TGETCNT2_1	8	R	7'h0	<this regiseter is valid only when 0x0250[2]=1> VbyOneHSII clock frequency counter [15:8] TTCOP ~ MEASURE_VALUE2 * tosc / TGETCNT2[15:0] MEASURE_VALUE2 = 480 as default when it is unchanged.
0x0265	[7:0]	TGETCNT2_0	8	R	7'h0	<this regiseter is valid only when 0x0250[2]=1> VbyOneHSII clock frequency counter [7:0]
0x0266	[7:0]	TGETCNT3_1	8	R	7'h0	<this regiseter is valid only when 0x0250[3]=1> Internal oscillator clock frequency counter [15:8] tOSC ~ MEASURE_VALUE3 * PCLK.input / TGETCNT3[15:0] MEASURE_VALUE3 = 480 as default when it is unchanged.
0x0267	[7:0]	TGETCNT3_0	8	R	7'h0	<this regiseter is valid only when 0x0250[3]=1> Internal oscillator clock frequency counter [7:0]
0x0268	[7:0]	reserved	8	-	-	-
0x0269	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0270	[7:0]	reserved	8	-	-	-
0x0271	[7:6]	reserved	2	-	-	-
	[5:0]	REFDIV	6	R/W	6'h3	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0272	[7:4]	reserved	4	-	-	-
	[3:0]	INTIN_1	4	R/W	4'h0	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0273	[7:0]	INTIN_0	8	R/W	8'h18	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0274	[7:0]	FRACIN_2	8	R/W	8'h0	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0275	[7:0]	FRACIN_1	8	R/W	8'h0	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0276	[7:0]	FRACIN_0	8	R/W	8'h0	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0277	[7]	reserved	1	-	-	-
	[6:4]	POSTDIV2	3	R/W	3'h1	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
	[3]	reserved	1	-	-	-
	[2:0]	POSTDIV1	3	R/W	3'h7	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0278	[7:1]	reserved	7	-	-	-
	[0]	DIRECTMODE	1	R/W	1'h0	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0280	[7:4]	reserved	4	-	-	-
	[3:0]	DIVVAL	4	R/W	4'hC	<this regiseter is valid only when 0x0283[0]=0> SSCG modulation frequency setting. Must be not set 0x0. FMOD = PCLK / (DIVVAL*128) ≦ 30kHz
0x0281	[7:5]	reserved	3	-	-	-
	[4:0]	SPREAD	5	R/W	5'h3	<this regiseter is valid only when 0x0283[0]=0> SSCG modulation depth select setting 0x0: 0% 0x1: 0.1% 0x2: 0.2% 0x3: 0.3% 0x4: 0.4% 0x5: 0.5% others: Reserved
0x0282	[7:1]	reserved	7	-	-	-
	[0]	DOWNSPREAD	1	R/W	1'h0	<this regiseter is valid only when 0x0283[0]=0> Spread mode select setting 0x0: Center Spread 0x1: Down Spread
0x0283	[7:1]	reserved	7	-	-	-
	[0]	DISABLE_SSCG	1	R/W	1'h1	SSCG enable setting 0x0: Enable 0x1: Disable

Address	bit	Register Name	width	R/W	Init	Description
0x0500	[7:0]	reserved	8	-	-	-
0x0501	[7:0]	reserved	8	-	-	-
0x0502	[7:0]	reserved	8	-	-	-
0x0503	[7:0]	reserved	8	-	-	-
0x0504	[7:1]	reserved	7	-	-	-
	[0]	R_LFEN	1	R/W	1'h0	LVDS TX Low Frequency mode setting 0x0: 30MHz to 150MHz 0x1: 10MHz to 30MHz
0x0505	[7:0]	reserved	8	-	-	-
0x0506	[7:0]	reserved	8	-	-	-
0x0507	[7:0]	reserved	8	-	-	-
0x0508	[7:0]	reserved	8	-	-	-
0x0509	[7:0]	reserved	8	-	-	-
0x050A	[7:4]	reserved	4	-	-	-
	[3:0]	R_VODSEL	4	R/W	4'h7	Open-LDI (LVDS) Tx VOD Swing Setting R_VODSEL=d'0111:350mV(Typ.) R_VODSEL=d'0010:200mV(Typ.)
0x050B	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0600	[7:0]	reserved	8	-	-	-
0x0601	[7:0]	reserved	8	-	-	-
0x0602	[7:0]	reserved	8	-	-	-
0x0603	[7:0]	reserved	8	-	-	-
0x0604	[7:0]	reserved	8	-	-	-
0x0605	[7:0]	reserved	8	-	-	-
0x0606	[7:0]	reserved	8	-	-	-
0x0607	[7:0]	reserved	8	-	-	-
0x0608	[7:1]	reserved	7	-	-	-
	[0]	CRC_CHECK_EN	1	R/W	1'h0	VbyOneHSII FC CRC check enable 0 : disable / 1 : enable
0x0609	[7:0]	reserved	8	-	-	-
0x060A	[7:0]	CRC_ERR_COUNT0_0	8	R	8'h0	VbyOneHSII FC CRC Error counter MSB for lane0.
0x060B	[7:0]	CRC_ERR_COUNT0_1	8	R	8'h0	VbyOneHSII FC CRC Error counter LSB for lane0.
0x060C	[7:0]	CRC_ERR_COUNT1_0	8	R	8'h0	VbyOneHSII FC CRC Error counter MSB for lane1.
0x060D	[7:0]	CRC_ERR_COUNT1_1	8	R	8'h0	VbyOneHSII FC CRC Error counter LSB for lane1.
0x060E	[7:2]	reserved	6	-	-	-
	[1]	CRC_ERR_COUNT_CLEAR1	1	W	-	VbyOneHSII FC CRC Error counter clear for lane1. 0x1: clear
	[0]	CRC_ERR_COUNT_CLEAR0	1	W	-	VbyOneHSII FC CRC Error counter clear for lane0. 0x1: clear
0x060F	[7:0]	reserved	8	-	-	-
0x0610	[7:0]	reserved	8	-	-	-
0x0611	[7:0]	reserved	8	-	-	-
0x0612	[7:0]	reserved	8	-	-	-
0x0613	[7:0]	reserved	8	-	-	-
0x0614	[7:0]	reserved	8	-	-	-
0x0615	[7:0]	reserved	8	-	-	-
0x0616	[7:0]	reserved	8	-	-	-
0x0617	[7:0]	reserved	8	-	-	-
0x0618	[7:0]	reserved	8	-	-	-
0x0619	[7:0]	reserved	8	-	-	-
0x061A	[7:0]	reserved	8	-	-	-
0x061B	[7:0]	reserved	8	-	-	-
0x061C	[7:0]	reserved	8	-	-	-
0x061D	[7:0]	reserved	8	-	-	-
0x061E	[7:0]	reserved	8	-	-	-
0x061F	[7:0]	reserved	8	-	-	-
0x0620	[7:0]	reserved	8	-	-	-
0x0621	[7:0]	reserved	8	-	-	-
0x0622	[7:4]	reserved	4	-	-	-
	[3]	FCB_EV_BLANK_DATA	1	R/W	1'h0	<this regiseter is valid only when 0x0622[2:0]=0x3, 0x4, 0x5 or 0x6> 0x0: Y/C = 0x10/0x80 mode 0x1: Y/C = 0x00/0x00 mode
	[2:0]	LVDS_FORMAT	3	R/W	3'h0	LVDS color format setting 0x0 : JEIDA format 0x1 : VESA format 0x2 : Reserved 0x3 : FCB-EV Single External Sync0 0x4 : FCB-EV Single Internal Sync0 0x5 : FCB-EV Dual External Sync 0x6 : FCB-EV Dual Internal Sync Others : Reserved
0x0623	[7:3]	reserved	5	-	-	-
	[2]	SYNC_POL_HS	1	R/W	1'h0	HSYNC polarity setting 0x0: Low Active, 0x1: High Active
	[1]	SYNC_POL_VS	1	R/W	1'h0	VSYNC polarity setting 0x0: Low Active, 0x1: High Active
	[0]	SYNC_POL_DE	1	R/W	1'h1	DE polarity setting 0x0: Low Active, 0x1: High Active
0x0624	[7:0]	reserved	8	-	-	-
0x0625	[7:0]	reserved	8	-	-	-
0x0626	[7:0]	reserved	8	-	-	-
0x0627	[7:0]	reserved	8	-	-	-
0x0628	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0680	[7:1]	reserved	7	-	-	-
	[0]	PATGENEN	1	R/W	1'h0	Pattern Generator Enable setting. 0x0: Disable, 0x1: Enable If use internal OSC clock, need to check 0x001A and 0x1C11 registers.
0x0681	[7:1]	reserved	7	-	-	-
	[0]	LANESEL	1	R/W	1'h0	Pattern Generator lane setting. 0x0: Set when VbyOneHS RX is Single link. 0x1: Set when VbyOneHS RX is Dual link.
0x0682	[7:4]	reserved	4	-	-	-
	[3:0]	HACTIVE_UPPER	4	R/W	4'h7	H active period [11:8]. ([pixel])
0x0683	[7:0]	HACTIVE_LOWER	8	R/W	8'h80	H active period [7:0]. ([pixel]). Default value is 1920 pixels.
0x0684	[7:3]	reserved	5	-	-	-
	[2:0]	VACTIVE_UPPER	3	R/W	3'h4	V active period [10:8]. ([line])
0x0685	[7:0]	VACTIVE_LOWER	8	R/W	8'h38	V active period [7:0]. ([line]). Default value is 1080 lines. If this setting is odd value, will automatically add 1 lines.
0x0686	[7:4]	reserved	4	-	-	-
	[3:0]	HBLANK_UPPER	4	R/W	4'h1	H blank period [11:8]. ([pixel])
0x0687	[7:0]	HBLANK_LOWER	8	R/W	8'h18	H blank period [7:0]. ([pixel]). Default value is 280 pixels.
0x0688	[7:2]	reserved	6	-	-	-
	[1:0]	VBLANK_UPPER	2	R/W	2'h0	V blank period [9:8]. ([line])
0x0689	[7:0]	VBLANK_LOWER	8	R/W	8'h2D	V blank period [7:0]. ([line]). Default value is 45 lines.
0x068A	[7:1]	reserved	7	-	-	-
	[0]	HSYNCWIDTH_UPPER	1	R/W	1'h0	H active pluse width [8]. ([pixel])
0x068B	[7:0]	HSYNCWIDTH_LOWER	8	R/W	8'h2C	H active pluse width [7:0]. ([pixel]). Default value is 44 pixels.
0x068C	[7:0]	VSYNCWIDTH	8	R/W	8'h5	V active pluse width [7:0]. ([line]). Default value is 5 lines.
0x068D	[7:1]	reserved	7	-	-	-
	[0]	HBACKPORCH_UPPER	1	R/W	1'h0	H back portch period [8]. ([pixel])
0x068E	[7:0]	HBACKPORCH_LOWER	8	R/W	8'h94	H back portch period [7:0]. ([pixel]). Default value is 148 pixels.
0x068F	[7]	reserved	1	-	-	-
	[6:0]	VBACKPORCH	7	R/W	7'h24	V back porch period [6:0]. ([line]). Default value is 36 lines.
0x0690	[7:0]	reserved	8	-	-	-
0x0691	[7:0]	reserved	8	-	-	-
0x0692	[7:0]	reserved	8	-	-	-
0x0693	[7:0]	reserved	8	-	-	-
0x0694	[7:0]	reserved	8	-	-	-
0x0695	[7:0]	reserved	8	-	-	-
0x0696	[7:1]	reserved	7	-	-	-
	[0]	HSYNCDIS	1	R/W	1'h0	Generate HSYNC setting 0x0: Generate Hsync 0x1: Not generate Hsync
0x0697	[7:5]	reserved	3	-	-	-
	[4]	VSYNCPOL	1	R/W	1'h1	VSYNC polality setting 0x0: Active low, idle high. 0x1: Active high, idle low.
	[3:1]	reserved	3	-	-	-
	[0]	HSYNCPOL	1	R/W	1'h1	HSYNC polality setting 0x0: Active low, idle high. 0x1: Active high, idle low.
0x0698	[7:6]	reserved	2	-	-	-
	[5:0]	PATGEN_PTN	6	R/W	6'hB	Pattern select setting. 0x0: Automatic pattern switching repetition from 0x1 to 0x5. 0x1: White Raster 0x2: Black Raster 0x3: Red Raster 0x4: Green Raster 0x5: Blue Raster 0xF: Black Raster 0x21: PRBS7 Others: Reserved
0x0699	[7:0]	GS_SEL_R	8	R/W	8'hFF	Gradient Setting for Red. This register effects to the Raster, Color Bars and Dot Pattern. 00:Black <=> FF:Red
0x069A	[7:0]	GS_SEL_G	8	R/W	8'hFF	Gradient Setting for Green. This register effects to the Raster, Color Bars and Dot Pattern. 00:Black <=> FF:Green
0x069B	[7:0]	GS_SEL_B	8	R/W	8'hFF	Gradient Setting for Blue. This register effects to the Raster, Color Bars and Dot Pattern. 00:Black <=> FF:Blue

Address	bit	Register Name	width	R/W	Init	Description
0x0700	[7:1]	reserved	7	-	-	-
	[0]	PATCHKEN	1	R/W	1'h0	Pattern Checker Enable setting. 0x0: Disable, 0x1: Enable
0x0701	[7:1]	reserved	7	-	-	-
	[0]	LANESEL	1	R/W	1'h0	Pattern Checker lane setting. 0x0: Set when VbyOne® HS II RX is Single link. 0x1: Set when VbyOne® HS II RX is Dual link.
0x0702	[7:0]	reserved	8	-	-	-
0x0703	[7:0]	reserved	8	-	-	-
0x0704	[7:0]	reserved	8	-	-	-
0x0705	[7:0]	reserved	8	-	-	-
0x0706	[7:0]	reserved	8	-	-	-
0x0707	[7:0]	reserved	8	-	-	-
0x0708	[7:0]	reserved	8	-	-	-
0x0709	[7:0]	reserved	8	-	-	-
0x070A	[7:0]	reserved	8	-	-	-
0x070B	[7:0]	reserved	8	-	-	-
0x070C	[7:0]	reserved	8	-	-	-
0x070D	[7:0]	reserved	8	-	-	-
0x070E	[7:0]	reserved	8	-	-	-
0x070F	[7:0]	reserved	8	-	-	-
0x0710	[7:0]	reserved	8	-	-	-
0x0711	[7:0]	reserved	8	-	-	-
0x0712	[7:0]	reserved	8	-	-	-
0x0713	[7:0]	reserved	8	-	-	-
0x0714	[7:0]	reserved	8	-	-	-
0x0715	[7:0]	reserved	8	-	-	-
0x0716	[7:6]	reserved	2	-	-	-
	[5:0]	PATCHK_PTN	6	R/W	6'hB	Pattern select setting. 0x0: Automatic pattern switching repetition from 0x1 to 0x5. 0x1: White Raster 0x2: Black Raster 0x3: Red Raster 0x4: Green Raster 0x5: Blue Raster 0xF: Black Raster 0x21: PRBS7 Others: Reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0720	[7:0]	reserved	8	-	-	-
0x0721	[7:0]	reserved	8	-	-	-
0x0722	[7:0]	reserved	8	-	-	-
0x0723	[7:0]	reserved	8	-	-	-
0x0724	[7:0]	reserved	8	-	-	-
0x0725	[7:0]	reserved	8	-	-	-
0x0726	[7:0]	reserved	8	-	-	-
0x0727	[7:0]	reserved	8	-	-	-
0x0728	[7:0]	reserved	8	-	-	-
0x0729	[7:1]	reserved	7	-	-	-
	[0]	CMP_VALID	1	R	-	Pattern Checker Valid Indicator. 0x0: Not Valid, 0x1: Valid
0x072A	[7:0]	CMP_ERR_LAT0	8	R	-	Pattern Checker Result0 (Sync, etc.) 0x00: No Error, others: Error exists.
0x072B	[7:6]	reserved	2	-	-	-
	[5:0]	CMP_ERR_LAT1	6	R	-	Pattern Checker Result1 (Sync, RGB, etc.) 0x00: No Error, others: Error exists.
0x072C	[7:0]	CMP_ERR_LAT_CLR0	8	R/W	-	Pattern Checker Result0 Clear by 2steps of Write action Step1 Write 0x00 => Step2 Write 0xFF : CMP_ERR_LAT0 is cleared.
0x072D	[7:6]	reserved	2	-	-	-
	[5:0]	CMP_ERR_LAT_CLR1	6	R/W		Pattern Checker Result0 Clear by 2steps of Write action Step1 Write 0x00 => Step2 Write 0x3F : CMP_ERR_LAT1 is cleared.
0x072E	[7:0]	reserved	8	-	-	-
0x072F	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0900	[7:0]	reserved	8	-	-	-
0x0901	[7:0]	reserved	8	-	-	-
0x0902	[7:0]	reserved	8	-	-	-
0x0903	[7:1]	reserved	7	-	-	-
	[0]	MODESEL_L0	1	R/W	1'h0	VbyOneHSII FC RX operation mode select for lane0. Configures by cabling. 0x0: Differential (STP), 0x1: Single end (Coaxial)
0x0904	[7:0]	reserved	8	-	-	-
0x0905	[7:0]	reserved	8	-	-	-
0x0906	[7:0]	reserved	8	-	-	-
0x0907	[7:0]	reserved	8	-	-	-
0x0908	[7:0]	reserved	8	-	-	-
0x0909	[7:0]	reserved	8	-	-	-
0x090A	[7:0]	reserved	8	-	-	-
0x090B	[7:0]	reserved	8	-	-	-
0x090C	[7:0]	reserved	8	-	-	-
0x0910	[7:0]	reserved	8	-	-	-
0x0A00	[7:0]	reserved	8	-	-	-
0x0A01	[7:0]	reserved	8	-	-	-
0x0A02	[7:0]	reserved	8	-	-	-
0x0A03	[7:1]	reserved	7	-	-	-
	[0]	MODESEL_L1	1	R/W	1'h0	VbyOneHSII FC RX operation mode select for lane1. Configures by cabling. 0x0: Differential (STP), 0x1: Single end (Coaxial)
0x0A05	[7:0]	reserved	8	-	-	-
0x0A06	[7:0]	reserved	8	-	-	-
0x0A07	[7:0]	reserved	8	-	-	-
0x0A08	[7:0]	reserved	8	-	-	-
0x0A09	[7:0]	reserved	8	-	-	-
0x0A0A	[7:0]	reserved	8	-	-	-
0x0A0B	[7:0]	reserved	8	-	-	-
0x0A0C	[7:0]	reserved	8	-	-	-
0x0A0D	[7:0]	reserved	8	-	-	-
0x0A0E	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0B60	[7:0]	reserved	8	-	-	-
0x0B61	[7:0]	reserved	8	-	-	-
0x0B64	[7:0]	R_2WIRE_HW	8	R/W	7'h06	2 wire controller SCL High width setting {16×{R_I2C_SCL_HW<7:0>+1}+11}×tOSC [ns] Default 2 wire frequensy is 325.2[kHz] by typical tOSC (12.5ns).
0x0B65	[7:0]	R_2WIRE_LW	8	R/W	7'h06	2 wire controller SCL Low width setting {16×{R_I2C_SCL_LW<7:0>+1}+11}×tOSC [ns]
0x0B68	[7:0]	reserved	8	-	-	-
0x0B69	[7:0]	reserved	8	-	-	-
0x0B6A	[7:1]	reserved	7	-	-	-
	[0]	R_2WIRE_INTERMITTENT_MODE	1	R/W	1'h0	BCC 2-wire Non-divided write/read mode enable. Must be set the same mode with the BCC Master (Serializer) side. 0x0: Disable 0x1: Enable
0x0B6F	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0C00	[7:6]	reserved	2	-	-	-
	[5]	GPIO0_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C00[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	GPIO0_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C00[2:0]=0x1, 0x7> GPIO0 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO0_MODE	3	R/W	3'h0	GPIO0 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output GPIO0_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to GPIO0_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs.
0x0C01	[7:6]	reserved	2	-	-	-
	[5]	GPIO1_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C01[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	GPIO1_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C01[2:0]=0x1, 0x7> GPIO1 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO1_MODE	3	R/W	3'h0	GPIO1 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output GPIO1_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to GPIO1_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs.
0x0C02	[7:6]	reserved	2	-	-	-
	[5]	GPIO2_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C02[2:0]=0x0, 0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	GPIO2_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C02[2:0]=0x1, 0x7> GPIO2 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO2_MODE	3	R/W	3'h2	GPIO2 I/O Mode setting. 0x0: I2S_D2 output mode 0x1: Programable GPO (To output GPIO2_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to GPIO2_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs.
0x0C03	[7:6]	reserved	2	-	-	-
	[5]	GPIO3_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C03[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	GPIO3_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C03[2:0]=0x1, 0x7> GPIO3 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO3_MODE	3	R/W	3'h2	GPIO3 I/O Mode setting. 0x0: I2S_D3 output mode 0x1: Programable GPO (To output GPIO3_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to GPIO3_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs.

Address	bit	Register Name	width	R/W	Init	Description
0x0C04	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	GPIO5_REG_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C04[2:0]=0x1> GPIO5_REG output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO5_REG_MODE	3	R/W	3'h2	GPIO5_REG I/O Mode setting. 0x0: I2S_D1 output mode 0x1: Programable GPO (To output GPIO5_REG_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI Others: Reserved
0x0C05	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	GPIO6_REG_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C05[2:0]=0x1> GPIO6_REG output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO6_REG_MODE	3	R/W	3'h2	GPIO6_REG I/O Mode setting. 0x0: I2S_D0 output mode 0x1: Programable GPO (To output GPIO6_REG_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI Others: Reserved
0x0C06	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	GPIO7_REG_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C06[2:0]=0x1> GPIO7_REG output data slect. 0x0: Low output 0x1: High output
	[2:0]	GPIO7_REG_MODE	3	R/W	3'h2	GPIO7_REG I/O Mode setting. 0x0: I2S_WC output mode 0x1: Programable GPO (To output GPIO7_REG_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI Others: Reserved
0x0C07	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	GPIO8_REG_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C07[2:0]=0x1> GPIO8_REG output data slect. 0x0: Low output 0x1: High output
	[2:0]	GPIO8_REG_MODE	3	R/W	3'h2	GPIO8_REG I/O Mode setting. 0x0: I2S_CLK output mode 0x1: Programable GPO (To output GPIO8_REG_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI Others: Reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0C08	[7:6]	reserved	2	-	-	-
	[5]	D_GPIO0_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C08[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	D_GPIO0_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C08[2:0]=0x1, 0x7> D_GPIO0 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	D_GPIO0_MODE	3	R/W	3'h0	D_GPIO0 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output D_GPIO0_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO0_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs.
0x0C09	[7:6]	reserved	2	-	-	-
	[5]	D_GPIO1_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C09[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	D_GPIO1_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C09[2:0]=0x1, 0x7> D_GPIO1 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	D_GPIO1_MODE	3	R/W	3'h0	D_GPIO1 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output D_GPIO1_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO1_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs.
0x0C0A	[7:6]	reserved	2	-	-	-
	[5]	D_GPIO2_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C0A[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	D_GPIO2_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C0A[2:0]=0x1, 0x7> D_GPIO2 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	D_GPIO2_MODE	3	R/W	3'h0	D_GPIO2 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output D_GPIO2_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO2_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs.
0x0C0B	[7:6]	reserved	2	-	-	-
	[5]	D_GPIO3_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C0B[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	D_GPIO3_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C0B[2:0]=0x1, 0x7> D_GPIO3 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	D_GPIO3_MODE	3	R/W	3'h0	D_GPIO3 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output D_GPIO3_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO3_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs.

Address	bit	Register Name	width	R/W	Init	Description
0x0C0C	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	GPIO9_REG_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C0C[2:0]=0x1> GPIO9_REG output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO9_REG_MODE	3	R/W	3'h2	GPIO7_REG I/O Mode setting. 0x0: MCLK output mode 0x1: Programable GPO (To output GPIO9_REG_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI Others: Reserved
0x0C0D	[7:1]	reserved	7	-	-	-
	[0]	GPIO0_IMON	1	R	1'h0	GPIO0 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C0E	[7:1]	reserved	7	-	-	-
	[0]	GPIO1_IMON	1	R	1'h0	GPIO1 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C0F	[7:1]	reserved	7	-	-	-
	[0]	GPIO2_IMON	1	R	1'h0	GPIO2 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C10	[7:1]	reserved	7	-	-	-
	[0]	GPIO3_IMON	1	R	1'h0	GPIO3 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C11	[7:1]	reserved	7	-	-	-
	[0]	GPIO5_REG_IMON	1	R	1'h0	GPIO5_REG Input Monitor Register 0x0: Low input, 0x01: High input
0x0C12	[7:1]	reserved	7	-	-	-
	[0]	GPIO6_REG_IMON	1	R	1'h0	GPIO6_REG Input Monitor Register 0x0: Low input, 0x01: High input
0x0C13	[7:1]	reserved	7	-	-	-
	[0]	GPIO7_REG_IMON	1	R	1'h0	GPIO7_REG Input Monitor Register 0x0: Low input, 0x01: High input
0x0C14	[7:1]	reserved	7	-	-	-
	[0]	GPIO8_REG_IMON	1	R	1'h0	GPIO8_REG Input Monitor Register 0x0: Low input, 0x01: High input
0x0C15	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO0_IMON	1	R	1'h0	D_GPIO0 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C16	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO1_IMON	1	R	1'h0	D_GPIO1 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C17	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO2_IMON	1	R	1'h0	D_GPIO2 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C18	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO3_IMON	1	R	1'h0	D_GPIO3 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C19	[7:1]	reserved	7	-	-	-
	[0]	GPIO9_REG_IMON	1	R	1'h0	GPIO9_REG Input Monitor Register 0x0: Low input, 0x01: High input
0x0C1A	[7:0]	reserved	8	-	-	-
0x0C1B	[7:0]	reserved	8	-	-	-
0x0C1C	[7:0]	reserved	8	-	-	-
0x0C1D	[7:0]	reserved	8	-	-	-
0x0C1E	[7:0]	reserved	8	-	-	-
0x0C1F	[7:0]	reserved	8	-	-	-
0x0C20	[7:0]	reserved	8	-	-	-
0x0C21	[7:0]	reserved	8	-	-	-
0x0C22	[7:0]	reserved	8	-	-	-
0x0C23	[7:0]	reserved	8	-	-	-
0x0C24	[7:0]	reserved	8	-	-	-
0x0C25	[7:0]	reserved	8	-	-	-
0x0C26	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0C27	[7:1]	reserved	7	-	-	-
	[0]	GPIO0_OD_MODE	1	R/W	1'h0	GPIO0 output buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C28	[7:1]	reserved	7	-	-	-
	[0]	GPIO1_OD_MODE	1	R/W	1'h0	GPIO1 output buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C29	[7:1]	reserved	7	-	-	-
	[0]	GPIO2_OD_MODE	1	R/W	1'h0	GPIO2 output buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C2A	[7:1]	reserved	7	-	-	-
	[0]	GPIO3_OD_MODE	1	R/W	1'h0	GPIO3 output buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C2B	[7:1]	reserved	7	-	-	-
	[0]	GPIO5_REG_OD_MODE	1	R/W	1'h0	GPIO5_REG output buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C2C	[7:1]	reserved	7	-	-	-
	[0]	GPIO6_REG_OD_MODE	1	R/W	1'h0	GPIO6_REG output buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C2D	[7:1]	reserved	7	-	-	-
	[0]	GPIO7_REG_OD_MODE	1	R/W	1'h0	GPIO7_REG output buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C2E	[7:1]	reserved	7	-	-	-
	[0]	GPIO8_REG_OD_MODE	1	R/W	1'h0	GPIO8_REG output buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C2F	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO0_OD_MODE	1	R/W	1'h0	D_GPIO0 output buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C30	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO1_OD_MODE	1	R/W	1'h0	D_GPIO1 output buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C31	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO2_OD_MODE	1	R/W	1'h0	D_GPIO2 output buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C32	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO3_OD_MODE	1	R/W	1'h0	D_GPIO3 output buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C33	[7:1]	reserved	7	-	-	-
	[0]	GPIO9_REG_OD_MODE	1	R/W	1'h0	GPIO9_REG output buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C34	[7:0]	reserved	8	-	-	-
0x0C35	[7:0]	reserved	8	-	-	-
0x0C36	[7:0]	reserved	8	-	-	-
0x0C37	[7:0]	reserved	8	-	-	-
0x0C38	[7:0]	reserved	8	-	-	-
0x0C39	[7:0]	reserved	8	-	-	-
0x0C3A	[7:0]	reserved	8	-	-	-
0x0C3B	[7:0]	reserved	8	-	-	-
0x0C3C	[7:0]	reserved	8	-	-	-
0x0C3D	[7:1]	reserved	7	-	-	-
	[0]	SMP_NUM_FIXMODE	1	R/W	1'h1	BCC Through GPIO select 0x0: Flexible, depending on SMP_GPIOx. 0x1: Fixed, depending on SMP_NUM.

Address	bit	Register Name	width	R/W	Init	Description
0x0C3E	[7:1]	reserved	7	-	-	-
	[0]	SMP_NUM	1	R/W	1'h1	BCC Through GPIO select (When SMP_NUM_FIXMODE=0x1 Fixed.) 0x0: Enable GPIO0-3 only. Sampling rate will be double but disable D_GPIO0-3. 0x1: Enable GPIO0-3 and D_GPIO0-3.
0x0C3F	[7:4]	SMP_GPIO7	4	R/W	4'h0	GPIO_ENCOUT[7] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[7] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[7] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[7] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[7] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[7] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[7] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[7] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[7] output others:reserved
	[3:0]	SMP_GPIO6	4	R/W	4'h0	GPIO_ENCOUT[6] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[6] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[6] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[6] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[6] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[6] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[6] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[6] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[6] output others:reserved
0x0C40	[7:4]	SMP_GPIO5	4	R/W	4'h0	GPIO_ENCOUT[5] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[5] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[5] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[5] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[5] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[5] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[5] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[5] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[5] output others:reserved
	[3:0]	SMP_GPIO4	4	R/W	4'h0	GPIO_ENCOUT[4] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[4] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[4] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[4] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[4] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[4] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[4] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[4] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[4] output others:reserved
0x0C41	[7:4]	SMP_GPIO3	4	R/W	4'h0	GPIO_ENCOUT[3] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[3] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[3] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[3] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[3] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[3] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[3] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[3] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[3] output others:reserved
	[3:0]	SMP_GPIO2	4	R/W	4'h0	GPIO_ENCOUT[2] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[2] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[2] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[2] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[2] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[2] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[2] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[2] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[2] output others:reserved
0x0C42	[7:4]	SMP_GPIO1	4	R/W	4'h0	GPIO_ENCOUT[1] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[1] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[1] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[1] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[1] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[1] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[1] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[1] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[1] output others:reserved
	[3:0]	SMP_GPIO0	4	R/W	4'h0	GPIO_ENCOUT[0] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[0] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[0] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[0] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[0] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[0] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[0] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[0] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[0] output others:reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0C43	[7:4]	DESMP_GPIO7	4	R/W	4'h0	GPIO_DECIN[7] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[7] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[7] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[7] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[7] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[7] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[7] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[7] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[7] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO6	4	R/W	4'h0	GPIO_DECIN[6] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[6] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[6] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[6] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[6] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[6] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[6] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[6] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[6] is Decodeded to D_GPIO3 output others:reserved
0x0C44	[7:4]	DESMP_GPIO5	4	R/W	4'h0	GPIO_DECIN[5] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[5] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[5] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[5] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[5] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[5] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[5] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[5] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[5] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO4	4	R/W	4'h0	GPIO_DECIN[4] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[4] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[4] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[4] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[4] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[4] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[4] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[4] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[4] is Decodeded to D_GPIO3 output others:reserved
0x0C45	[7:4]	DESMP_GPIO3	4	R/W	4'h0	GPIO_DECIN[3] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[3] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[3] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[3] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[3] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[3] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[3] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[3] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[3] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO2	4	R/W	4'h0	GPIO_DECIN[2] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[2] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[2] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[2] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[2] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[2] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[2] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[2] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[2] is Decodeded to D_GPIO3 output others:reserved
0x0C46	[7:4]	DESMP_GPIO1	4	R/W	4'h0	GPIO_DECIN[1] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[1] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[1] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[1] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[1] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[1] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[1] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[1] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[1] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO0	4	R/W	4'h0	GPIO_DECIN[0] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[0] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[0] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[0] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[0] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[0] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[0] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[0] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[0] is Decodeded to D_GPIO3 output others:reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0C47	[7:5]	reserved	3	-	-	-
	[4]	ERR8B10B_ERRDET_EN	1	R/W	1'h0	FC 8B10B Error Detection Enable 0x0: Disable, 0x01: Enable
	[3]	WDTEN_ERRDET_EN	1	R/W	1'h0	BC WDT Error Detection Enable 0x0: Disable, 0x01: Enable
	[2]	MC_ERRDET_EN	1	R/W	1'h1	BC Manchester Code Error Detection Enable 0x0: Disable, 0x01: Enable
	[1]	LOCK_ERRDET_EN	1	R/W	1'h1	FC and BC Lock Error Detection Enable 0x0: Disable, 0x01: Enable
	[0]	CRC_ERRDET_EN	1	R/W	1'h1	FC and BC CRC Error Detection Enable 0x0: Disable, 0x01: Enable
0x0C48	[7:0]	reserved	8	-	-	-
0x0C49	[7:0]	reserved	8	-	-	-
0x0C4A	[7:0]	reserved	8	-	-	-
0x0C4B	[7:0]	reserved	8	-	-	-
0x0C4C	[7:0]	reserved	8	-	-	-
0x0C4D	[7:0]	reserved	8	-	-	-
0x0C4E	[7:0]	reserved	8	-	-	-
0x0C4F	[7:0]	reserved	8	-	-	-
0x0C50	[7:0]	reserved	8	-	-	-
0x0C51	[7:0]	reserved	8	-	-	-
0x0C52	[7:0]	reserved	8	-	-	-
0x0C53	[7:0]	reserved	8	-	-	-
0x0C54	[7:0]	reserved	8	-	-	-
0x0C55	[7:0]	reserved	8	-	-	-
0x0C56	[7:5]	reserved	3	-	-	-
	[4:0]	GPIO_PULLDOWN_UPPER	5	R/W	5'h0	GPIO Pull down setting-1. 0x0: Disable, 0x1: Enable [4]: GPIO9_REG [3]: D_GPIO3 [2]: D_GPIO2 [1]: D_GPIO1 [0]: D_GPIO0
0x0C57	[7:0]	GPIO_PULLDOWN_LOWER	8	R/W	8'h0	GPIO Pull down setting-2. 0x0: Disable, 0x1: Enable [7]: GPIO8_REG [6]: GPIO7_REG [5]: GPIO6_REG [4]: GPIO5_REG [3]: GPIO3 [2]: GPIO2 [1]: GPIO1 [0]: GPIO0

Address	bit	Register Name	width	R/W	Init	Description
0x0D00	[7:3]	reserved	5	-	-	-
	[2:1]	BITWIDTH	2	R/W	2'h0	Audio I2S bit width setting. 0x0: 16bit 0x1: 24bit 0x2: 32bit 0x3: Reserved
	[0]	SMP	1	R/W	1'h0	Audio I2S sampling parameter. This register and BITWIDTH setting determine the ratio (MCLK/I2S_CLK) 0x0: 192 0x1: 256 MCLK[MHz] = I2S_CLK*SMP/(BITWIDTH*2)
0x0D01	[7:0]	reserved	8	-	-	-
0x0D02	[7:0]	reserved	8	-	-	-
0x0D03	[7:0]	reserved	8	-	-	-
0x0D04	[7:0]	reserved	8	-	-	-
0x0D05	[7:0]	reserved	8	-	-	-
0x0D06	[7:0]	reserved	8	-	-	-
0x0D07	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1000	[7:1]	reserved	7	-	-	-
	[0]	EMENP_REG	1	R/W	1'h0	FC Lane0 Eye Monitor Enable sampling 0x0: Disable, 0x1: Enable
0x1001	[7]	reserved	1	-	-	-
	[6:0]	EM_PH_REG	7	R/W	7'h0	FC Lane0 Eye Monitor Sampler Phase Control (0~5UI, 1/16UI step) 000_0000 : 0/80 * 5UI 000_0001 : 1/80 * 5UI 101_0000 : 80/80 * 5UI
0x1002	[7:5]	reserved	3	-	-	-
	[4:0]	EM_VTH_REG	5	R/W	5'h0	FC Lane0 Eye Monitor Sampler Threshold Voltage Control (±105mV (7mV Step), MSB is Signed Polarity) 0_0000 : + 0 * 7mV 0_0001 : + 1 * 7mV 0_1111 : + 15 * 7mV 1_1111 : - 15 * 7mV
0x1003	[7:0]	reserved	8	-	-	-
0x1004	[7:0]	reserved	8	-	-	-
0x1005	[7:0]	reserved	8	-	-	-
0x1006	[7:1]	reserved	7	-	-	-
	[0]	EMSTART_REG	1	W	1'h0	FC Lane0 Eye Monitor SUM Start Trigger 0x0: wait(default), 0x1: Start
0x1007	[7:1]	reserved	7	-	-	-
	[0]	EMSTOP_REG	1	W	1'h0	FC Lane0 Eye Monitor SUM Stop at FreeRun 0x0: continue(default), 0x1: Stop
0x1008	[7:3]	reserved	5	-	-	-
	[2:0]	EM_VTH_REG	3	R/W	3'h0	FC Lane0 Eye Monitor Error Value SUM Number of Times Select (Any change during FC Lane0 Eye Monitor execution is prohibited.) 000 : 1024 001 : 8192 010 : 65536 011 : 524288 Others : FreeRun depending on EMSTOP_REG
0x1009	[7:1]	reserved	7	-	-	-
	[0]	EMDONE_REG	1	R	1'h0	FC Lane0 Eye Monitor Error SUM Complete Flag 1 : Eye Monitor Finish 0 : Eye Monitor caluclation
0x100A	[7:0]	EMERRSUM_REG_0	8	R	8'h0	FC Lane0 Eye monitor Error Value SUM Output ([7:0]) EMERRSUM [20:0] : Error Value SUM Output EMERRSUM[21] : OverFlowFlag
0x100B	[7:0]	EMERRSUM_REG_1	8	-	-	FC Lane0 Eye monitor Error Value SUM Output ([15:8])
0x100C	[7:6]	reserved	2	-	-	-
	[5:0]	EMERRSUM_REG_2	6			FC Lane0 Eye monitor Error Value SUM Output ([21:16])
0x100D	[7:0]	reserved	8	-	-	-
0x100E	[7:0]	reserved	8	-	-	-
0x100F	[7:0]	reserved	8	-	-	-
0x1010	[7:0]	reserved	8	-	-	-
0x1011	[7:0]	reserved	8	-	-	-
0x1012	[7:0]	reserved	8	-	-	-
0x1013	[7:0]	reserved	8	-	-	-
0x1014	[7:0]	reserved	8	-	-	-
0x1015	[7:0]	reserved	8	-	-	-
0x1016	[7:0]	reserved	8	-	-	-
0x1017	[7:0]	reserved	8	-	-	-
0x1018	[7:0]	reserved	8	-	-	-
0x1019	[7:0]	reserved	8	-	-	-
0x101A	[7:0]	reserved	8	-	-	-
0x101B	[7:0]	reserved	8	-	-	-
0x101C	[7:0]	reserved	8	-	-	-
0x101D	[7:0]	reserved	8	-	-	-
0x101E	[7:0]	reserved	8	-	-	-
0x101F	[7:0]	reserved	8	-	-	-
0x1020	[7:0]	reserved	8	-	-	-
0x1021	[7:0]	reserved	8	-	-	-
0x1022	[7:0]	reserved	8	-	-	-
0x1023	[7:0]	reserved	8	-	-	-
0x1024	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1100	[7:1]	reserved	7	-	-	-
	[0]	EMENP_REG	1	R/W	1'h0	FC Lane1 Eye Monitor Enable sampling 0x0: Disable, 0x1: Enable
0x1101	[7]	reserved	1	-	-	-
	[6:0]	EM_PH_REG	7	R/W	7'h0	FC Lane1 Eye Monitor Sampler Phase Control (0~5UI, 1/16UI step) 000_0000 : 0/80 * 5UI 000_0001 : 1/80 * 5UI 101_0000 : 80/80 * 5UI
0x1102	[7:5]	reserved	3	-	-	-
	[4:0]	EM_VTH_REG	5	R/W	5'h0	FC Lane1 Eye Monitor Sampler Threshold Voltage Control (±105mV (7mV Step), MSB is Signed Polarity) 0_0000 : + 0 * 7mV 0_0001 : + 1 * 7mV 0_1111 : + 15 * 7mV 1_1111 : - 15 * 7mV
0x1103	[7:0]	reserved	8	-	-	-
0x1104	[7:0]	reserved	8	-	-	-
0x1105	[7:0]	reserved	8	-	-	-
0x1106	[7:1]	reserved	7	-	-	-
	[0]	EMSTART_REG	1	W	1'h0	FC Lane1 Eye Monitor SUM Start Trigger 0x0: wait(default), 0x1: Start
0x1107	[7:1]	reserved	7	-	-	-
	[0]	EMSTOP_REG	1	W	1'h0	FC Lane1 Eye Monitor SUM Stop at FreeRun 0x0: continue(default), 0x1: Stop
0x1108	[7:3]	reserved	5	-	-	-
	[2:0]	EM_VTH_REG	3	R/W	3'h0	FC Lane1 Eye Monitor Error Value SUM Number of Times Select (Any change during FC Lane1 Eye Monitor execution is prohibited.) 000 : 1024 001 : 8192 010 : 65536 011 : 524288 Others : FreeRun depending on EMSTOP_REG
0x1109	[7:1]	reserved	7	-	-	-
	[0]	EMDONE_REG	1	R	1'h0	FC Lane1 Eye Monitor Error SUM Complete Flag 1 : Eye Monitor Finish 0 : Eye Monitor caluclation
0x110A	[7:0]	EMERRSUM_REG_0	8	R	8'h0	FC Lane1 Eye monitor Error Value SUM Output ([7:0]) EMERRSUM [20:0] : Error Value SUM Output EMERRSUM[21] : OverFlowFlag
0x110B	[7:0]	EMERRSUM_REG_1	8	-	-	FC Lane1 Eye monitor Error Value SUM Output ([15:8])
0x110C	[7:6]	reserved	2	-	-	-
	[5:0]	EMERRSUM_REG_2	6			FC Lane1 Eye monitor Error Value SUM Output ([21:16])
0x110D	[7:0]	reserved	8	-	-	-
0x110E	[7:0]	reserved	8	-	-	-
0x110F	[7:0]	reserved	8	-	-	-
0x1110	[7:0]	reserved	8	-	-	-
0x1111	[7:0]	reserved	8	-	-	-
0x1112	[7:0]	reserved	8	-	-	-
0x1113	[7:0]	reserved	8	-	-	-
0x1114	[7:0]	reserved	8	-	-	-
0x1115	[7:0]	reserved	8	-	-	-
0x1116	[7:0]	reserved	8	-	-	-
0x1117	[7:0]	reserved	8	-	-	-
0x1118	[7:0]	reserved	8	-	-	-
0x1119	[7:0]	reserved	8	-	-	-
0x111A	[7:0]	reserved	8	-	-	-
0x111B	[7:0]	reserved	8	-	-	-
0x111C	[7:0]	reserved	8	-	-	-
0x111D	[7:0]	reserved	8	-	-	-
0x111E	[7:0]	reserved	8	-	-	-
0x111F	[7:0]	reserved	8	-	-	-
0x1120	[7:0]	reserved	8	-	-	-
0x1121	[7:0]	reserved	8	-	-	-
0x1122	[7:0]	reserved	8	-	-	-
0x1123	[7:0]	reserved	8	-	-	-
0x1124	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1200	[7:1]	reserved	7	-	-	-
	[0]	CLR	1	W	-	Checksum clear 0x1: clear
0x1201	[7:1]	reserved	7	-	-	-
	[0]	EN	1	R/W	1'h0	Checksum Enable 0x0: Disable, 0x1: Enable
0x1202	[7:0]	TIMER	8	R/W	8'h0	Checksum diagnosis interval setting. 1024 x 64 x (N+THIMER[7:0]) x OSC cycle Valid 820us ~ 210ms when OSC is typical value
0x1203	[7:0]	VAL	8	R/W	8'h9C	Checksum calculation pass/fail target setting
0x1204	[7:0]	RES	8	R	8'h0	Checksum calculation result
0x1210	[7:0]	reserved	8	-	-	-
0x1211	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1300	[7:3]	reserved	5	-	-	-
	[2]	INTN_IN_BYPASS	1	R/W	1'h1	INTN_IN pin input select. INTN_IN pin will propagate the status to INTN_REM on the Serializer when set 0x1. 0x0: Interrupt 0x1: Propagate the attached VbyOneHSII Serializer
	[1:0]	INTN_IN_MODE	2	R/W	2'h0	INTN_IN pin input mode select 0x0: Low Active 0x1: High Active 0x2: Disable 0x3: Reserved
0x1301	[7:0]	INTN_IN_FILT_RANGE	8	R/W	8'd48	INTN_IN input Filter Range 0x0: Disable Others: INTN_IN_FILT_RANGE * tosc is pulse filter threshold.
0x1302	[7:0]	reserved	8	-	-	-
0x1303	[7:2]	reserved	6	-	-	-
	[1]	INTN_M_CLEAR	1	W	-	Mask all clear. Interrupt Mask settings will be disable. 0x1: clear
	[0]	INTN_S_CLEAR	1	W	-	Interrupt all clear. Interrupt statuses will be clear. 0x1: clear

Address	bit	Register Name	width	R/W	Init	Description
0x1310	[7:1]	reserved	7	-	-	-
	[0]	INTN_LOCK	1	R/W1C	1'h0	PLL Lock Detect 0x0: No interrupt, 0x1: Interrupt
0x1311	[7]	INTN_ERR_OSCOUTU	1	R/W1C	1'h0	Internal OSC Clockout Upper Error 0x0: No interrupt, 0x1: Interrupt
	[6]	INTN_ERR_OSCOUTL	1	R/W1C	1'h0	Internal OSC Clockout Low er Error 0x0: No interrupt, 0x1: Interrupt
	[5]	INTN_ERR_PLLOUTU	1	R/W1C	1'h0	PLL Clock Upper Error 0x0: No interrupt, 0x1: Interrupt
	[4]	INTN_ERR_PLLOUTL	1	R/W1C	1'h0	PLL Clock Low er Error 0x0: No interrupt, 0x1: Interrupt
	[3]	INTN_ERR_RX1CHU	1	R/W1C	1'h0	VbyOneHSII RX Clock for lane1 Upper Error 0x0: No interrupt, 0x1: Interrupt
	[2]	INTN_ERR_RX1CHL	1	R/W1C	1'h0	VbyOneHSII RX Clock for lane1 Lower Error 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_ERR_RX0CHU	1	R/W1C	1'h0	VbyOneHSII RX Clock for lane0 Upper Error 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_RX0CHL	1	R/W1C	1'h0	VbyOneHSII RX Clock for lane0 Lower Error 0x0: No interrupt, 0x1: Interrupt
0x1312	[7:0]	reserved	8	-	-	-
0x1313	[7:5]	reserved	3	-	-	-
	[4]	INTN_ERR_VSYNCWIDTH	1	R/W1C	1'h0	LVDS Domain PATCHK VSYNCWIDTH Error 0x0: No interrupt, 0x1: Interrupt
	[3:2]	reserved	2	-	-	-
	[1]	INTN_ERR_VACTIVE	1	R/W1C	1'h0	LVDS Domain PATCHK VACTIVE Error 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_VTOTAL	1	R/W1C	1'h0	LVDS Domain PATCHK VTOTAL Error 0x0: No interrupt, 0x1: Interrupt
0x1314	[7:2]	reserved	6	-	-	-
	[1]	INTN_ERR_HFRONTPORCH	1	R/W1C	1'h0	LVDS Domain PATCHK HFRONTPORCH Error 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_HBLANK	1	R/W1C	1'h0	LVDS Domain PATCHK HBLANK Error 0x0: No interrupt, 0x1: Interrupt
0x1315	[7:5]	reserved	3	-	-	-
	[4]	INTN_ERR_VSYNCWIDTH_FC	1	R/W1C	1'h0	FC Domain PATCHK VSYNCWIDTH Error 0x0: No interrupt, 0x1: Interrupt
	[3:2]	reserved	2	-	-	-
	[1]	INTN_ERR_VACTIVE_FC	1	R/W1C	1'h0	FC Domain PATCHK VACTIVE Error 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_VTOTAL_FC	1	R/W1C	1'h0	FC Domain PATCHK VTOTAL Error 0x0: No interrupt, 0x1: Interrupt
0x1316	[7:2]	reserved	6	-	-	-
	[1]	INTN_ERR_HFRONTPORCH_FC	1	R/W1C	1'h0	FC Domain PATCHK HFRONTPORCH Error 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_HBLANK_FC	1	R/W1C	1'h0	FC Domain PATCHK HBLANK Error 0x0: No interrupt, 0x1: Interrupt

Address	bit	Register Name	width	R/W	Init	Description
0x1317	[7:3]	reserved	5	-	-	-
	[2]	INTN_FIFO_ERR_PARITY1	1	R/W1C	1'h0	VbyOneHSII FC RX FIFO Parity Error1 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_FIFO_ERR_PARITY0	1	R/W1C	1'h0	VbyOneHSII FC RX FIFO Parity Error0 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_FIFO_ERR	1	R/W1C	1'h0	VbyOneHSII FC RX FIFO Error 0x0: No interrupt, 0x1: Interrupt
0x1318	[7:2]	reserved	6	-	-	-
	[1]	INTN_FC_VIDEO_CRC_ERR_L1	1	R/W1C	1'h0	VbyOneHSII FC Video CRC Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_FC_VIDEO_CRC_ERR_L0	1	R/W1C	1'h0	VbyOneHSII FC Video CRC Error for lane0 0x0: No interrupt, 0x1: Interrupt
0x1319	[7:2]	reserved	6	-	-	-
	[1]	INTN_ERR_WDT_TIMEOUT	1	R/W1C	1'h0	WDT Timeout Error 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_MASTER_NOACK_DET	1	R/W1C	1'h0	Master no ACK Detect Error 0x0: No interrupt, 0x1: Interrupt
0x131A	[7:1]	reserved	7	-	-	-
	[0]	INTN_ERR	1	R/W1C	1'h0	Register CheckSum Error 0x0: No interrupt, 0x1: Interrupt
0x131B	[7:2]	reserved	6	-	-	-
	[1]	INTN_ERR_ECC_ROM1	1	R/W1C	1'h0	Memory ECC Error for ROM 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_ECC_ROM0	1	R/W1C	1'h0	Memory ECC Error for ROM 0x0: No interrupt, 0x1: Interrupt
0x131C	[7:3]	reserved	5	-	-	-
	[2]	INTN_WRITE_ERR	1	R/W1C	1'h0	Ring Buffer Write Error 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_FC_THRIO_CRC_ERR_VCLK	1	R/W1C	1'h0	VCLK domain VbyOneHSII FC THRIO CRC Error 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_FC_THRIO_CRC_ERR_OCLK	1	R/W1C	1'h0	OCLK domain VbyOneHSII FC THRIO CRC Error 0x0: No interrupt, 0x1: Interrupt
0x131D	[7:1]	reserved	7	-	-	-
	[0]	INTN_ERR_FC	1	R/W1C	1'h0	FC Error 0x0: No interrupt, 0x1: Interrupt
0x131E	[7:1]	reserved	7	-	-	-
	[0]	INTN_ERR_FC	1	R/W1C	1'h0	FC Error 0x0: No interrupt, 0x1: Interrupt
0x131F	[7:1]	reserved	7	-	-	-
	[0]	INTN_IN	1	R/W1C	1'h0	INTN_IN 0x0: No interrupt, 0x1: Interrupt
0x1320	[7:0]	reserved	8	-	-	-
0x1321	[7:0]	reserved	8	-	-	-
0x1322	[7:0]	reserved	8	-	-	-
0x1323	[7:0]	reserved	8	-	-	-
0x1324	[7:0]	reserved	8	-	-	-
0x1325	[7:0]	reserved	8	-	-	-
0x1326	[7:0]	reserved	8	-	-	-
0x1327	[7:0]	reserved	8	-	-	-
0x1328	[7:0]	reserved	8	-	-	-
0x1329	[7:0]	reserved	8	-	-	-
0x132A	[7:0]	reserved	8	-	-	-
0x132B	[7:0]	reserved	8	-	-	-
0x132C	[7:0]	reserved	8	-	-	-
0x132D	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1350	[7:1]	reserved	7	-	-	-
	[0]	INTN_LOCK_M	1	R/W1C	1'h0	PLL Lock Detect Mask 0x0: No interrupt, 0x1: Interrupt
0x1351	[7]	INTN_ERR_OSCOUTU_M	1	R/W1C	1'h0	Internal OSC Clockout Upper Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[6]	INTN_ERR_OSCOUTL_M	1	R/W1C	1'h0	Internal OSC Clockout Low er Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[5]	INTN_ERR_PLLOUTU_M	1	R/W1C	1'h0	PLL Clock Upper Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[4]	INTN_ERR_PLLOUTL_M	1	R/W1C	1'h0	PLL Clock Low er Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[3]	INTN_ERR_RX1CHU_M	1	R/W1C	1'h0	VbyOneHSII RX Clock for lane1 Upper Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[2]	INTN_ERR_RX1CHL_M	1	R/W1C	1'h0	VbyOneHSII RX Clock for lane1 Lower Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[1]	INTN_ERR_RX0CHU_M	1	R/W1C	1'h0	VbyOneHSII RX Clock for lane0 Upper Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[0]	INTN_ERR_RX0CHL_M	1	R/W1C	1'h0	VbyOneHSII RX Clock for lane0 Lower Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
0x1352	[7:0]	reserved	8	-	-	-
0x1353	[7:5]	reserved	3	-	-	-
	[4]	INTN_ERR_VSYNCWIDTH_M	1	R/W1C	1'h0	LVDS Domain PATCHK VSYNCWIDTH Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[3:2]	reserved	2	-	-	-
	[1]	INTN_ERR_VACTIVE_M	1	R/W1C	1'h0	LVDS Domain PATCHK VACTIVE Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[0]	INTN_ERR_VTOTAL_M	1	R/W1C	1'h0	LVDS Domain PATCHK VTOTAL Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
0x1354	[7:2]	reserved	6	-	-	-
	[1]	INTN_ERR_HFRONTPORCH_M	1	R/W1C	1'h0	LVDS Domain PATCHK HFRONTPORCH Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[0]	INTN_ERR_HBLANK_M	1	R/W1C	1'h0	LVDS Domain PATCHK HBLANK Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
0x1355	[7:5]	reserved	3	-	-	-
	[4]	INTN_ERR_VSYNCWIDTH_FC_M	1	R/W1C	1'h0	FC Domain PATCHK VSYNCWIDTH Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[3:2]	reserved	2	-	-	-
	[1]	INTN_ERR_VACTIVE_FC_M	1	R/W1C	1'h0	FC Domain PATCHK VACTIVE Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[0]	INTN_ERR_VTOTAL_FC_M	1	R/W1C	1'h0	FC Domain PATCHK VTOTAL Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
0x1356	[7:2]	reserved	6	-	-	-
	[1]	INTN_ERR_HFRONTPORCH_FC_M	1	R/W1C	1'h0	FC Domain PATCHK HFRONTPORCH Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[0]	INTN_ERR_HBLANK_FC_M	1	R/W1C	1'h0	FC Domain PATCHK HBLANK Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor

Address	bit	Register Name	width	R/W	Init	Description
0x1357	[7:3]	reserved	5	-	-	-
	[2]	INTN_FIFO_ERR_PARITY1_M	1	R/W1C	1'h0	VbyOneHSII FC RX FIFO Parity Error1 Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[1]	INTN_FIFO_ERR_PARITY0_M	1	R/W1C	1'h0	VbyOneHSII FC RX FIFO Parity Error0 Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[0]	INTN_FIFO_ERR_M	1	R/W1C	1'h0	VbyOneHSII FC RX FIFO Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
0x1358	[7:2]	reserved	6	-	-	-
	[1]	INTN_FC_VIDEO_CRC_ERR_L1_M	1	R/W1C	1'h0	VbyOneHSII FC Video CRC Error for lane1 Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[0]	INTN_FC_VIDEO_CRC_ERR_L0_M	1	R/W1C	1'h0	VbyOneHSII FC Video CRC Error for lane0 Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
0x1359	[7:2]	reserved	6	-	-	-
	[1]	INTN_ERR_WDT_TIMEOUT_M	1	R/W1C	1'h0	WDT Timeout Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[0]	INTN_ERR_MASTER_NOACK_DET_M	1	R/W1C	1'h0	Master no ACK Detect Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
0x135A	[7:1]	reserved	7	-	-	-
	[0]	INTN_ERR_M	1	R/W1C	1'h0	Register CheckSum Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
0x135B	[7:2]	reserved	6	-	-	-
	[1]	INTN_ERR_ECC_ROM1_M	1	R/W1C	1'h0	Memory ECC Error for ROM Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[0]	INTN_ERR_ECC_ROM0_M	1	R/W1C	1'h0	Memory ECC Error for ROM Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
0x135C	[7:3]	reserved	5	-	-	-
	[2]	INTN_WRITE_ERR_M	1	R/W1C	1'h0	Ring Buffer Write Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[1]	INTN_FC_THRIO_CRC_ERR_VCLK_M	1	R/W1C	1'h0	VCLK domain VbyOneHSII FC THRIO CRC Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
	[0]	INTN_FC_THRIO_CRC_ERR_OCLK_M	1	R/W1C	1'h0	OCLK domain VbyOneHSII FC THRIO CRC Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
0x135D	[7:1]	reserved	7	-	-	-
	[0]	INTN_ERR_FC_M	1	R/W1C	1'h0	FC Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
0x135E	[7:1]	reserved	7	-	-	-
	[0]	INTN_ERR_FC_M	1	R/W1C	1'h0	FC Error Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
0x135F	[7:1]	reserved	7	-	-	-
	[0]	INTN_IN_M	1	R/W1C	1'h0	INTN_IN Mask 0x0: Apply interrupt fuctor to the attached Serializer, 0x1: Mask interrupt fuctor
0x1360	[7:0]	reserved	8	-	-	-
0x1361	[7:0]	reserved	8	-	-	-
0x1362	[7:0]	reserved	8	-	-	-
0x1363	[7:0]	reserved	8	-	-	-
0x1364	[7:0]	reserved	8	-	-	-
0x1365	[7:0]	reserved	8	-	-	-
0x1366	[7:0]	reserved	8	-	-	-
0x1367	[7:0]	reserved	8	-	-	-
0x1368	[7:0]	reserved	8	-	-	-
0x1369	[7:0]	reserved	8	-	-	-
0x136A	[7:0]	reserved	8	-	-	-
0x136B	[7:0]	reserved	8	-	-	-
0x136C	[7:0]	reserved	8	-	-	-
0x136D	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1730	[7:0]	THRIO_ERROR_COUNT_UPPER	8	R	8'h0	VbyOneHSII FC THRIO CRC Error count (MSB). Count limit is 16'hFFFF and stop.
0x1731	[7:0]	THRIO_ERROR_COUNT_LOWER	8	R	8'h0	VbyOneHSII FC THRIO CRC Error count (LSB) Count limit is 16'hFFFF and stop.
0x1732	[7:1]	reserved	7	-	-	-
	[0]	THRIO_ERROR_CLEAR	1	R/W	1'h0	VbyOneHSII FC THRIO CRC Error count clear 0x1: Clear CRC Error count
0x1733	[7:0]	reserved	8	-	-	-
0x1734	[7:0]	reserved	8	-	-	-
0x1735	[7:0]	reserved	8	-	-	-
0x1736	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1C00	[7]	reserved	1	-	-	-
	[6:0]	MON0	7	R/W	7'h0	MON0 pin debug output select. See MONitor configuration table.
0x1C01	[7]	reserved	1	-	-	-
	[6:0]	MON1	7	R/W	7'h0	MON1 pin debug output select. See MONitor configuration table.
0x1C02	[7:0]	EXTRA_GPIO0_IOSEL	8	R/W	8'h0	GPIO0 pin extra/internal clock output select. 0x00: Normal operation 0x11: Internal OSC clock output 0x12: VbyOneHSII BC Clock output 0x13: LVDS TX Pixel Clock output 0x14: VbyOneHSII FC RX Pixel Clock for lane0 output 0x15: VbyOneHSII FC RX Pixel Clock for lane1 output Others: reserved
0x1C03	[7:0]	EXTRA_GPIO1_IOSEL	8	R/W	8'h0	GPIO1 pin extra/internal clock output select. 0x00: Normal operation 0x11: Internal OSC clock output 0x12: VbyOneHSII BC Clock output 0x13: LVDS TX Pixel Clock output 0x14: VbyOneHSII FC RX Pixel Clock for lane0 output 0x15: VbyOneHSII FC RX Pixel Clock for lane1 output Others: reserved
0x1C04	[7:0]	EXTRA_GPIO2_IOSEL	8	R/W	8'h0	GPIO2 pin extra/internal clock output select. 0x00: Normal operation 0x11: Internal OSC clock output 0x12: VbyOneHSII BC Clock output 0x13: LVDS TX Pixel Clock output 0x14: VbyOneHSII FC RX Pixel Clock for lane0 output 0x15: VbyOneHSII FC RX Pixel Clock for lane1 output Others: reserved
0x1C05	[7:0]	EXTRA_GPIO3_IOSEL	8	R/W	8'h0	GPIO3 pin extra/internal clock output select. 0x00: Normal operation 0x11: Internal OSC clock output 0x12: VbyOneHSII BC Clock output 0x13: LVDS TX Pixel Clock output 0x14: VbyOneHSII FC RX Pixel Clock for lane0 output 0x15: VbyOneHSII FC RX Pixel Clock for lane1 output Others: reserved
0x1C06	[7:0]	EXTRA_GPIO5_REG_IOSEL	8	R/W	8'h0	GPIO5_REG pin extra/internal signal output select. 0x00: Normal operation 0x72: VbyOneHSII LOCKN signal for lane1 output Others: reserved
0x1C07	[7:0]	reserved	8	-	-	-
0x1C08	[7:0]	reserved	8	-	-	-
0x1C09	[7:0]	reserved	8	-	-	-
0x1C0A	[7:0]	reserved	8	-	-	-
0x1C0B	[7:0]	reserved	8	-	-	-
0x1C0C	[7:0]	reserved	8	-	-	-
0x1C0D	[7:0]	EXTRA_D_GPIO2_IOSEL	8	R/W	8'h0	D_GPIO2 pin extra/internal signal output select. 0x00: Normal operation 0x5D: VbyOneHSII LOCKN signal for lane0 output Others: reserved
0x1C0E	[7:0]	reserved	8	-	-	-
0x1C0F	[7:0]	reserved	8	-	-	-
0x1C10	[7:0]	reserved	8	-	-	-
0x1C11	[7:6]	reserved	2	-	-	-
	[5:4]	TUNING_RXCLK_SEL	2	R/W	2'h0	VbyOneHSII FC RX Clock select. When use PATGEN by internal OSC clock, should be set 0x3. 0x0: Normal operation 0x3: Internal OSC Clock. Others: reserved
	[3:2]	reserved	2	-	-	-
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x1C12	[7:0]	reserved	8	-	-	-
0x1C13	[7:0]	reserved	8	-	-	-
0x1C14	[7:0]	reserved	8	-	-	-
0x1C15	[7:0]	reserved	8	-	-	-
0x1C16	[7:0]	TUNING_EN	8	R/W	8'h0	Tuning Registers access enable 0x22: Enable, 0x1C11 to 0x1C15 are able to set Others: Disable

Table 19. MONitor configuration table

MON0/1[7:0]	Error signal	Description
0x00	Disable	Hi-z, Pull-down
0x01	Low fix	-
0x02	High fix	-
0x03	CLK_TOP.TXCLK	LVDS TX PCLK
0x04	CLK_TOP.RX0CLK	VbyOneHSII Des PCLK for lane0
0x05	CLK_TOP.RX1CLK	VbyOneHSII Des PCLK for lane1
0x06	FCRX_BCTX_LINK_0.VSYNC	VbyOneHSII Des VSYNC for lane0 *
0x07	FCRX_BCTX_LINK_0.HSYNC	VbyOneHSII Des HSYNC for lane0 *
0x08	FCRX_BCTX_LINK_0.DE	VbyOneHSII Des DE for lane0
0x09	FCRX_BCTX_LINK_1.VSYNC	VbyOneHSII Des VSYNC for lane1 *
0x0A	FCRX_BCTX_LINK_1.HSYNC	VbyOneHSII Des HSYNC for lane1 *
0x0B	FCRX_BCTX_LINK_1.DE	VbyOneHSII Des DE for lane1
0x0C	Reserved	-
0x0D	FC_V_DTOP.LVDS_D0_O[0]	LVDS LOA1[0]
0x0E	FC_V_DTOP.LVDS_D0_O[1]	LVDS LOA1[1]
0x0F	FC_V_DTOP.LVDS_D0_O[2]	LVDS LOA1[2]
0x10	FC_V_DTOP.LVDS_D0_O[3]	LVDS LOA1[3]
0x11	FC_V_DTOP.LVDS_D0_O[4]	LVDS LOA1[4]
0x12	FC_V_DTOP.LVDS_D0_O[5]	LVDS LOA1[5]
0x13	FC_V_DTOP.LVDS_D0_O[6]	LVDS LOA1[6]
0x14	FC_V_DTOP.LVDS_D0_O[7]	LVDS LOB1[0]
0x15	FC_V_DTOP.LVDS_D0_O[8]	LVDS LOB1[1]
0x16	FC_V_DTOP.LVDS_D0_O[9]	LVDS LOB1[2]
0x17	FC_V_DTOP.LVDS_D0_O[10]	LVDS LOB1[3]
0x18	FC_V_DTOP.LVDS_D0_O[11]	LVDS LOB1[4]
0x19	FC_V_DTOP.LVDS_D0_O[12]	LVDS LOB1[5]
0x1A	FC_V_DTOP.LVDS_D0_O[13]	LVDS LOB1[6]
0x1B	FC_V_DTOP.LVDS_D0_O[14]	LVDS LOC1[0]
0x1C	FC_V_DTOP.LVDS_D0_O[15]	LVDS LOC1[1]
0x1D	FC_V_DTOP.LVDS_D0_O[16]	LVDS LOC1[2]
0x1E	FC_V_DTOP.LVDS_D0_O[17]	LVDS LOC1[3]
0x1F	FC_V_DTOP.LVDS_D0_O[18]	LVDS LOC1[4]
0x20	FC_V_DTOP.LVDS_D0_O[19]	LVDS LOC1[5]
0x21	FC_V_DTOP.LVDS_D0_O[20]	LVDS LOC1[6]
0x22	FC_V_DTOP.LVDS_D0_O[21]	LVDS LOD1[0]
0x23	FC_V_DTOP.LVDS_D0_O[22]	LVDS LOD1[1]
0x24	FC_V_DTOP.LVDS_D0_O[23]	LVDS LOD1[2]
0x25	FC_V_DTOP.LVDS_D0_O[24]	LVDS LOD1[3]
0x26	FC_V_DTOP.LVDS_D0_O[25]	LVDS LOD1[4]
0x27	FC_V_DTOP.LVDS_D0_O[26]	LVDS LOD1[5]
0x28	FC_V_DTOP.LVDS_D0_O[27]	LVDS LOD1[6]
0x29	FC_V_DTOP.LVDS_D1_O[0]	LVDS LOA2[0]
0x2A	FC_V_DTOP.LVDS_D1_O[1]	LVDS LOA2[1]
0x2B	FC_V_DTOP.LVDS_D1_O[2]	LVDS LOA2[2]
0x2C	FC_V_DTOP.LVDS_D1_O[3]	LVDS LOA2[3]
0x2D	FC_V_DTOP.LVDS_D1_O[4]	LVDS LOA2[4]
0x2E	FC_V_DTOP.LVDS_D1_O[5]	LVDS LOA2[5]
0x2F	FC_V_DTOP.LVDS_D1_O[6]	LVDS LOA2[6]
0x30	FC_V_DTOP.LVDS_D1_O[7]	LVDS LOB2[0]
0x31	FC_V_DTOP.LVDS_D1_O[8]	LVDS LOB2[1]
0x32	FC_V_DTOP.LVDS_D1_O[9]	LVDS LOB2[2]
0x33	FC_V_DTOP.LVDS_D1_O[10]	LVDS LOB2[3]
0x34	FC_V_DTOP.LVDS_D1_O[11]	LVDS LOB2[4]
0x35	FC_V_DTOP.LVDS_D1_O[12]	LVDS LOB2[5]
0x36	FC_V_DTOP.LVDS_D1_O[13]	LVDS LOB2[6]
0x37	FC_V_DTOP.LVDS_D1_O[14]	LVDS LOC2[0]
0x38	FC_V_DTOP.LVDS_D1_O[15]	LVDS LOC2[1]
0x39	FC_V_DTOP.LVDS_D1_O[16]	LVDS LOC2[2]
0x3A	FC_V_DTOP.LVDS_D1_O[17]	LVDS LOC2[3]
0x3B	FC_V_DTOP.LVDS_D1_O[18]	LVDS LOC2[4]
0x3C	FC_V_DTOP.LVDS_D1_O[19]	LVDS LOC2[5]
0x3D	FC_V_DTOP.LVDS_D1_O[20]	LVDS LOC2[6]
0x3E	FC_V_DTOP.LVDS_D1_O[21]	LVDS LOD2[0]
0x3F	FC_V_DTOP.LVDS_D1_O[22]	LVDS LOD2[1]
0x40	FC_V_DTOP.LVDS_D1_O[23]	LVDS LOD2[2]
0x41	FC_V_DTOP.LVDS_D1_O[24]	LVDS LOD2[3]
0x42	FC_V_DTOP.LVDS_D1_O[25]	LVDS LOD2[4]
0x43	FC_V_DTOP.LVDS_D1_O[26]	LVDS LOD2[5]
0x44	FC_V_DTOP.LVDS_D1_O[27]	LVDS LOD2[6]

*H/VSYNC signal do not match the output H/VSYNC signals because they are encoded.

8. Application and Implementation

NOTE

Information in the following applications sections is not part of the THine component specification, and THine does not warrant its accuracy or completeness. THine's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1. Applications Information

V-by-One® HSII behavior is connectable to THCV333-Q.

V-by-One® HS behavior, in which FCTHRIO is disabled, is connectable to standard V-by-One® HS product with external LOCKN connection.

8.2. Typical Applications

8.2.1. Design Requirements

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme.

For applications utilizing single-ended 50Ω coaxial cable, the unused data pins should be terminated with a 50Ω resistor.

8.2.2. Detailed Design Procedure

8.2.2.1. High-Speed Interconnect Guidelines

- ☐ Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer. (Refer to figure below.)
- ☐ PCB traces for high-speed signals must be single-ended micorstirp lines or coupled microstrip lines whose differential characteristic impedance is 100Ω.
- ☐ Minimize the distance between traces of a differential pair (S1) to maximize common mode rejection and coupling effect which works to reduce EMI(Electro-Magnetic Interference).
- ☐ Route differential signal traces symmetrically.
- ☐ Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity.
- ☐ Mismatch among impedances of PCB traces, connectors, or cables also caused reflection, limiting the bandwidth of the high-speed channels.
- ☐ Using common-mode filter on differential traces is desirable to reduce EMI. Pay attention on data-rate driven noise. For example, if data-rate is 1.5Gbps, common mode choke coil of 1.5GHz common mode impedance is desired to be high, while 1.5GHz differential impedance is low.

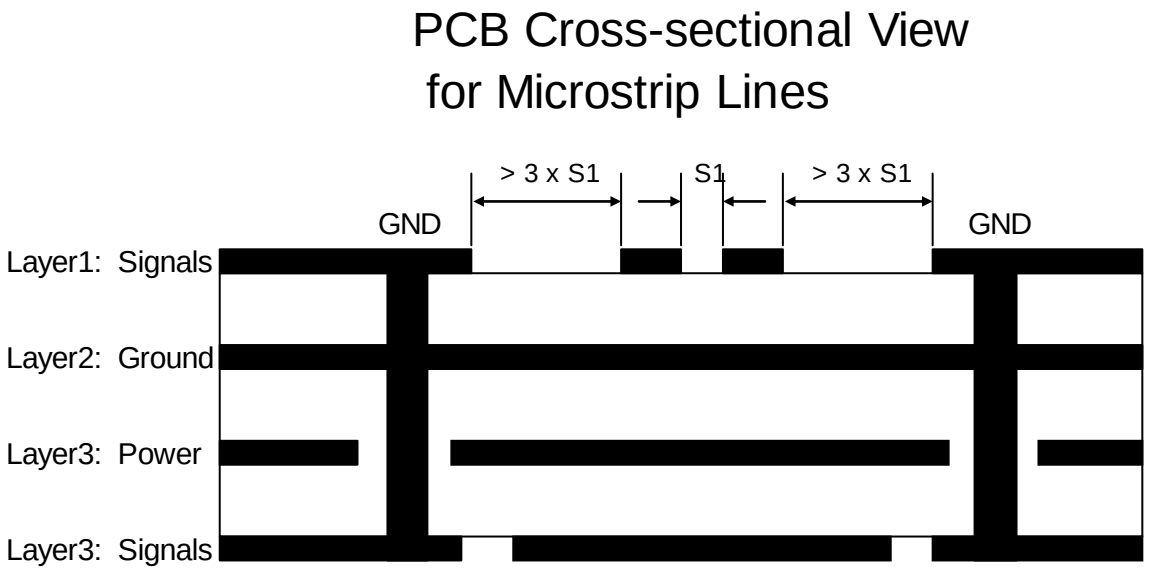


Figure 1 PCB cross-sectional view

9. Power Supply Recommendations

9.1. Power-Up Requirements and PDN Pin

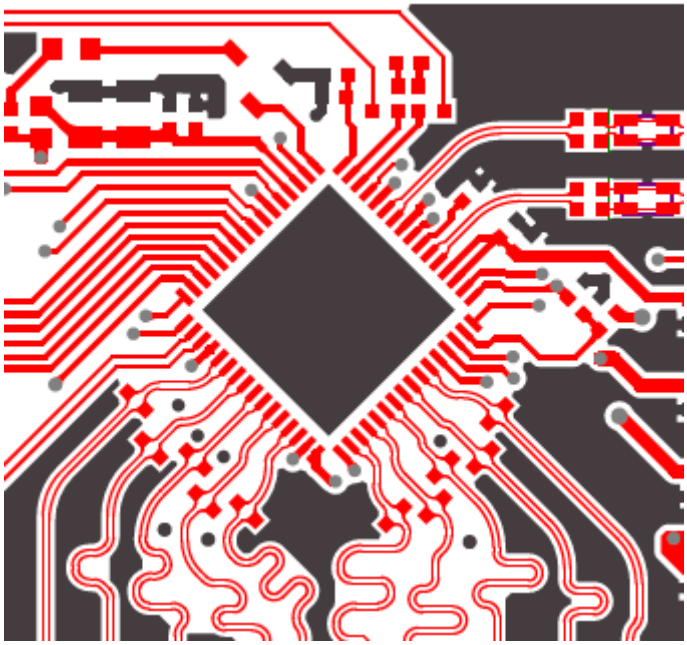
Please refer to 6.6.6. Power On and Re-Lock Sequence AC Specifications.

10. Layout

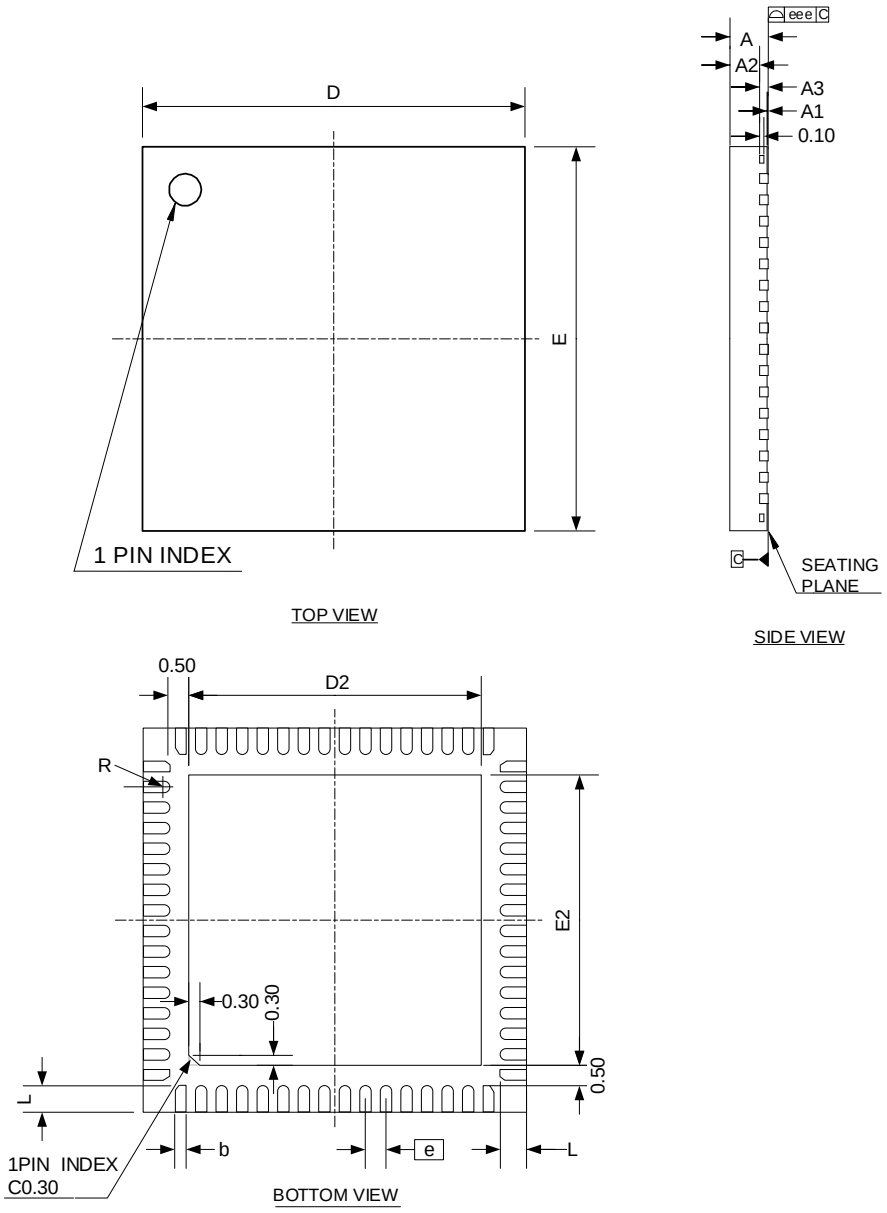
10.1. Layout Guidelines

Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer.

10.2. Layout Example



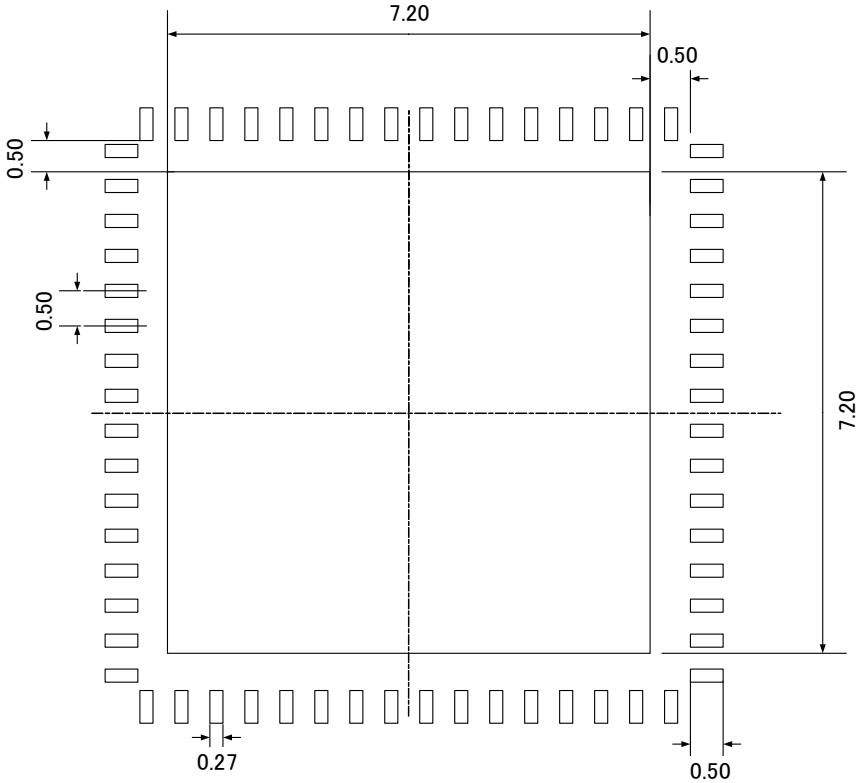
11. Package



Unit: mm

Symbol	Items	Min.	Nom.	Max.
A	Mounting Height	-	-	0.90
A1	Standoff	0.00	-	0.05
A2	-	-	0.65	0.70
A3	-		(0.20)	
b	Terminal Width	0.18	0.25	0.30
D	Body Length		9.00 BSC	
D2	Exposed Length	7.10	7.20	7.30
E	Body Width		9.00 BSC	
E2	Exposed Width	7.10	7.20	7.30
L	-	0.30	0.40	0.50
e	Pitch		0.50 BSC	
R	-	0.09	-	-
eee	Coplanarity		0.08	

12. Land Pattern



TOP VIEW

Unit: mm

LAND PATTERN EXMPLE

(Note)

Please carefully consider your SMT conditions (Material of substrate, Solder Composition, Reflow Condition and so on), and adjusts the Land Pattern at your own risk.

13. Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. THine Electronics, Inc. ("THine") is not responsible for possible errors and omissions in this material. Please note even if errors or omissions should be found in this material, THine may not be able to correct them immediately.

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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently fail-safe design principles such as redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.

7. This product may be permanently damaged and suffer from performance degradation or loss of mechanical functionality if subjected to electrostatic charge exceeding capacity of the ESD (Electrostatic Discharge) protection circuitry. Safety earth ground must be provided to anything in contact with the product, including any operator, floor, tester and soldering iron.

8. Please note that this product is not designed to be radiation-proof.

9. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.

10. This product must be stored according to storage method which is specified in this specifications. THine accepts no liability whatsoever for any damage or loss caused to the user due to any storage not according to above-mentioned method.

11. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act in Japan and the Export Administration Regulations in the United States of America on export or transit of this product. This product is prohibited for the purpose of developing military modernization, including the development of weapons of mass destruction (WMD), and the purpose of violating human rights.

12. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses. THine accepts no liability whatsoever for any damage or loss caused to the user due to use under a condition exceeding the limiting values.

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