

# Silicon Carbide (SiC) Schottky Diode – EliteSiC, 6 A, 650 V, D1, DPAK

## FFSD0665A

### Description

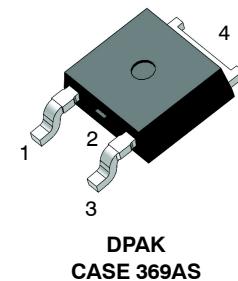
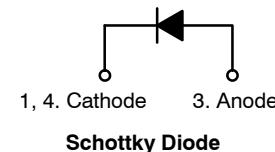
Silicon Carbide (SiC) Schottky Diodes use a completely new technology that provides superior switching performance and higher reliability compared to Silicon. No reverse recovery current, temperature independent switching characteristics, and excellent thermal performance sets Silicon Carbide as the next generation of power semiconductor. System benefits include highest efficiency, faster operating frequency, increased power density, reduced EMI, and reduced system size and cost.

### Features

- Max Junction Temperature 175°C
- Avalanche Rated 36 mJ
- High Surge Current Capacity
- Positive Temperature Coefficient
- Ease of Paralleling
- No Reverse Recovery/No Forward Recovery
- This Device is Pb-Free, Halogen Free/BFR Free and RoHS Compliant

### Applications

- General Purpose
- SMPS, Solar Inverter, UPS
- Power Switching Circuits



### MARKING DIAGRAM



A = Assembly Plant Code  
YWW = Date Code (Year & Week)  
ZZ = Lot Code  
FFSD0665A = Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# FFSD0665A

**Table 1. ABSOLUTE MAXIMUM RATINGS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter		FFSD0665A	Unit	
$V_{RRM}$	Peak Repetitive Reverse Voltage		650	V	
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)		36	mJ	
$I_F$	Continuous Rectified Forward Current @ $T_C < 159^\circ\text{C}$		6	A	
	Continuous Rectified Forward Current @ $T_C < 135^\circ\text{C}$		11		
$I_{F,Max}$	Non-Repetitive Peak Forward Surge Current		$T_C = 25^\circ\text{C}, 10 \mu\text{s}$	430	A
			$T_C = 150^\circ\text{C}, 10 \mu\text{s}$	415	A
$I_{F,SM}$	Non-Repetitive Forward Surge Current		Half-Sine Pulse, $t_p = 8.3 \text{ ms}$	42	A
$I_{F,RM}$	Repetitive Forward Surge Current		Half-Sine Pulse, $t_p = 8.3 \text{ ms}$	24	A
$P_{tot}$	Power Dissipation		$T_C = 25^\circ\text{C}$	89	W
			$T_C = 150^\circ\text{C}$	15	W
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +175		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1.  $E_{AS}$  of 36 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.5 \text{ mH}$ ,  $I_{AS} = 12 \text{ A}$ ,  $V = 50 \text{ V}$ .

**Table 2. THERMAL CHARACTERISTICS**

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	1.7	°C/W

**Table 3. OPERATING CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_F$	Forward Voltage	$I_F = 6 \text{ A}, T_C = 25^\circ\text{C}$	-	1.50	1.75	V
		$I_F = 6 \text{ A}, T_C = 125^\circ\text{C}$	-	1.6	2.0	
		$I_F = 6 \text{ A}, T_C = 175^\circ\text{C}$	-	1.72	2.4	
$I_R$	Reverse Current	$V_R = 650 \text{ V}, T_C = 25^\circ\text{C}$	-	-	200	μA
		$V_R = 650 \text{ V}, T_C = 125^\circ\text{C}$	-	-	400	
		$V_R = 650 \text{ V}, T_C = 175^\circ\text{C}$	-	-	600	
$Q_C$	Total Capacitive Charge	$V = 400 \text{ V}$	-	22	-	nC
$C$	Total Capacitance	$V_R = 1 \text{ V}, f = 100 \text{ kHz}$	-	361	-	pF
		$V_R = 200 \text{ V}, f = 100 \text{ kHz}$	-	41	-	
		$V_R = 400 \text{ V}, f = 100 \text{ kHz}$	-	32	-	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## PART MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method	Reel Size <sup>†</sup>	Tape Width	Quantity
FFSD0665A	FFSD0665A	DPAK	N/A	13"	N/A	2500 Units

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

**TYPICAL CHARACTERISTICS**  
( $T_J = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)

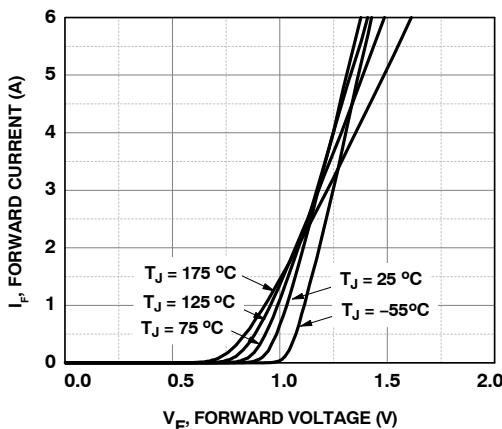


Figure 1. Forward Characteristics

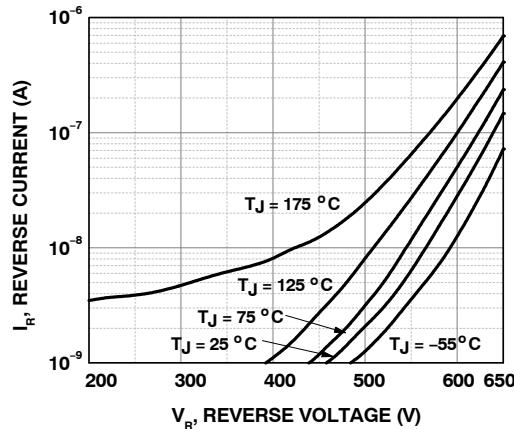


Figure 2. Reverse Characteristics

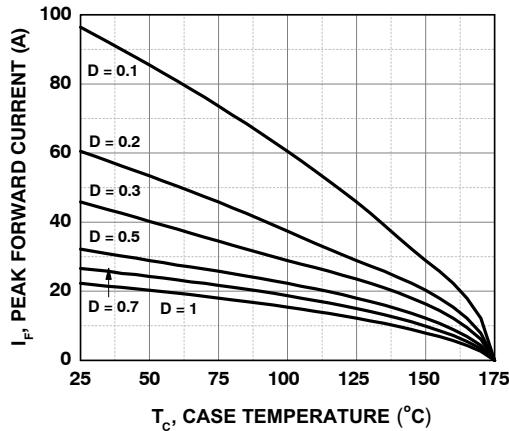


Figure 3. Current Derating

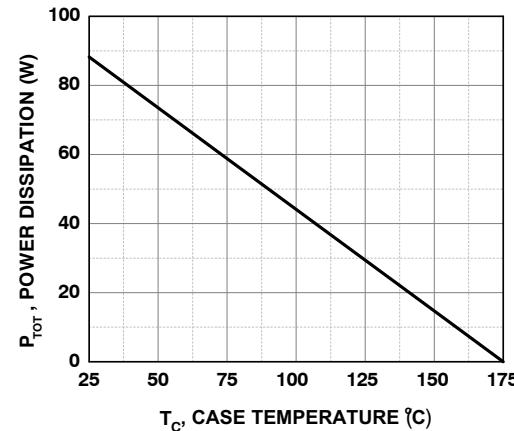


Figure 4. Power Derating

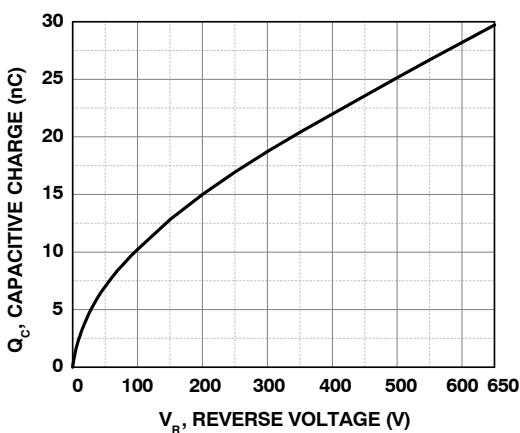


Figure 5. Capacitive Charge vs. Reverse Voltage

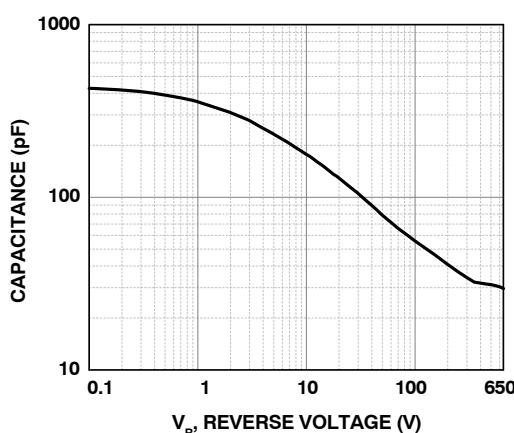


Figure 6. Capacitance vs. Reverse Voltage

# FFSD0665A

## TYPICAL CHARACTERISTICS (CONTINUED)

( $T_J = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)

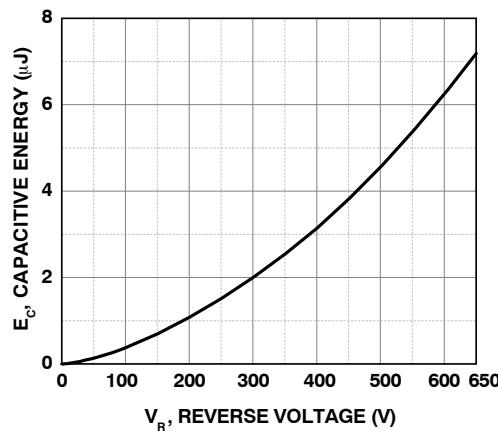


Figure 7. Capacitance Stored Energy

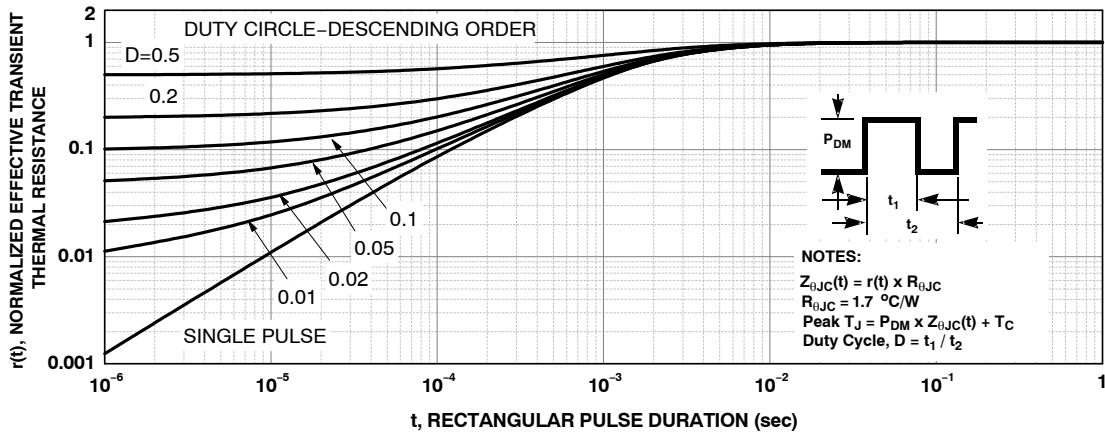


Figure 8. Junction-to-Case Transient Thermal Response Curve

## TEST CIRCUIT AND WAVEFORMS

$L = 0.5 \text{ mH}$   
 $R < 0.1 \Omega$   
 $V_{DD} = 50 \text{ V}$   
 $EAVL = 1/2LI_2 [V_{R(AVL)} / (V_{R(AVL)} - V_{DD})]$   
 $Q1 = \text{IGBT } (BV_{CES} > \text{DUT } V_{R(AVL)})$

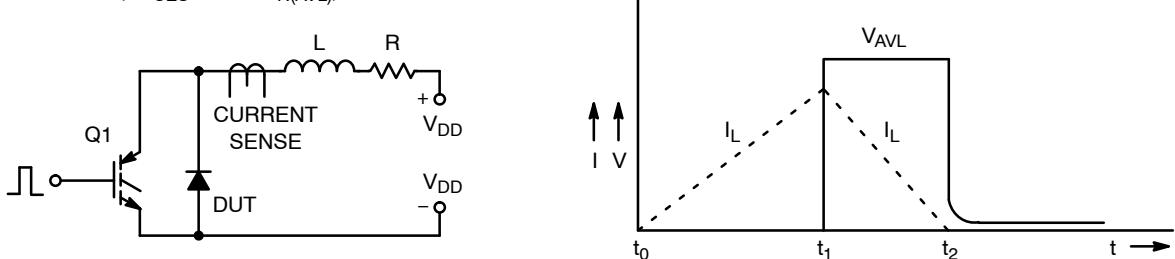
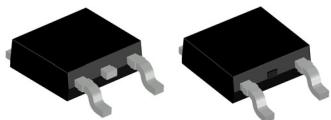
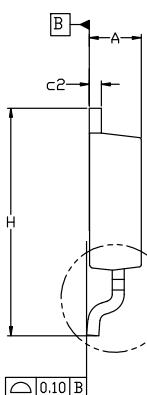
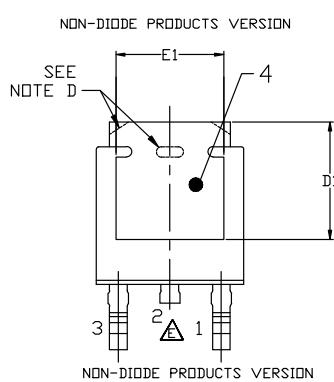
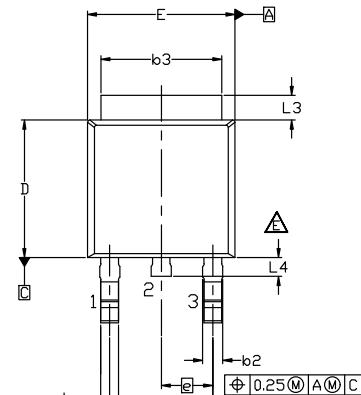


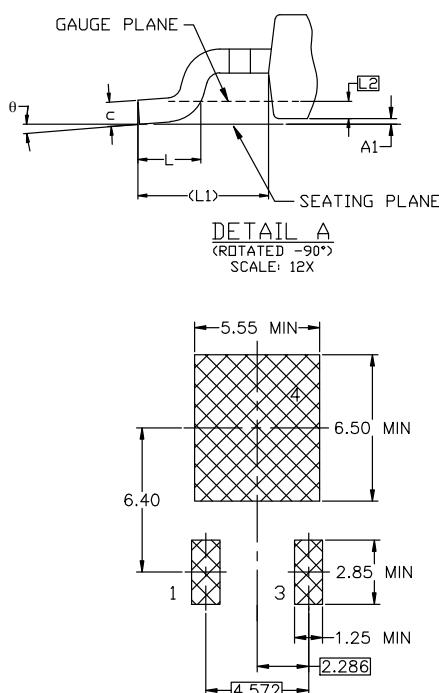
Figure 9. Unclamped Inductive Switching Test Circuit & Waveform


**DPAK3 6.10x6.54x2.29, 4.57P**  
CASE 369AS  
ISSUE B

DATE 20 DEC 2023



NOTES: UNLESS OTHERWISE SPECIFIED  
A) THIS PACKAGE CONFORMS TO JEDEC, TD-252,  
ISSUE F, VARIATION AA.  
B) ALL DIMENSIONS ARE IN MILLIMETERS.  
C) DIMENSIONING AND TOLERANCING PER  
ASME Y14.5M-2018.  
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED  
CORNERS OR EDGE PROTRUSION.  
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY  
STUB WITHOUT CENTER LEAD.  
F) DIMENSIONS ARE EXCLUSIVE OF BURRS,  
MOLD FLASH AND TIE BAR EXTRUSIONS.  
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD  
TD228P991X239-3N.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	—	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	—	—
E	6.35	6.54	6.73
E1	4.32	—	—
e	2.286	BSC	
e1	4.572	BSC	
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90	REF	
L2	0.51	BSC	
L3	0.89	1.08	1.27
L4	—	—	1.02
θ	0°	—	10°

## LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR  
PB-FREE STRATEGY AND SOLDERING DETAILS,  
PLEASE DOWNLOAD THE ON SEMICONDUCTOR  
SOLDERING AND MOUNTING TECHNIQUES  
REFERENCE MANUAL, SOLDERRM/D.

**GENERIC  
MARKING DIAGRAM\***


XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

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