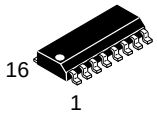
# 5 V ECL 1:4 Clock Distribution Chip

# MC10EL15, MC100EL15




**SOIC−16**
**D SUFFIX**
**CASE 751B−05**

## Description

The MC10EL/100EL15 is a low skew 1:4 clock distribution chip designed explicitly for low skew clock distribution applications. The $V_{BB}$ pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to $V_{BB}$ as a switching reference voltage. $V_{BB}$ may also rebias AC coupled inputs. When used, decouple $V_{BB}$ and $V_{CC}$ via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, $V_{BB}$ should be left open.

The EL15 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pulldown resistor) the SEL pin will select the differential clock input.

The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

The 100 series contains temperature compensation.

## Features

- 50 ps Output-to-Output Skew
- Synchronous Enable/Disable
- Multiplexed Clock Input
- PECL Mode Operating Range:
  - $V_{CC}$ = 4.2 V to 5.7 V with $V_{EE}$ = 0 V
- NECL Mode Operating Range:
  - $V_{CC}$ = 0 V with $V_{EE}$ = −4.2 V to −5.7 V
- Internal Input Pulldown Resistors on CLKs, SCLK, SEL, and $\overline{EN}$
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

## MARKING DIAGRAMS*







A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC100EL15DG | SOIC−16 (Pb-Free) | 48 Units/Tube |
| MC100EL15DR2G | SOIC−16 (Pb-Free) | 2500 / Tape & Reel |

**DISCONTINUED** (Note 1)

| | | |
|---|---|---|
| MC10EL15DR2G | SOIC−16 (Pb-Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

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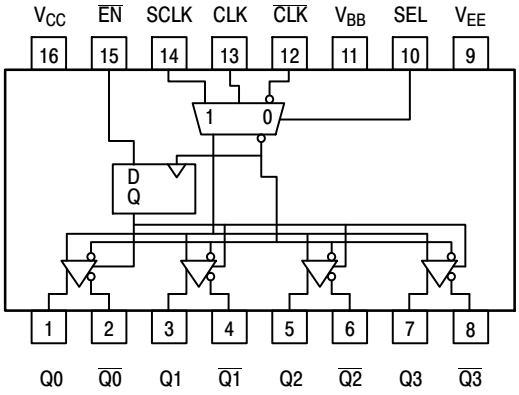



**Figure 1. Logic Diagram and Pinout Assignment**

**Table 1. PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| CLK, $\overline{CLK}$ | ECL Diff Clock Inputs |
| SCLK | ECL Scan Clock Input |
| $\overline{EN}$ | ECL Sync Enable |
| SEL | ECL Clock Select Input |
| $Q_{0-3}$, $\overline{Q_{0-3}}$ | ECL Diff Clock Outputs |
| $V_{BB}$ | Reference Voltage Output |
| $V_{CC}$ | Positive Supply |
| $V_{EE}$ | Negative Supply |

**Table 2. FUNCTION TABLE**

| CLK* | SCLK* | SEL* | $\overline{EN}$* | Q |
|---|---|---|---|---|
| L | X | L | L | L |
| H | X | L | L | H |
| X | L | H | L | L |
| X | H | H | L | H |
| X | X | X | H | L(1) |

*Pins will default low when left open.
1. On next negative transition of CLK or SCLK

**Table 3. ATTRIBUTES**

| Characteristics | Value |
|---|---|
| Internal Input Pulldown Resistor | 75 kΩ |
| Internal Input Pullup Resistor | N/A |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | <br>> 1 kV<br>> 100 V<br>2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Level 1 |
| Flammability Rating<br>Oxygen Index: 28 to 34 | <br>UL 94 V−0 @ 0.125 in |
| Transistor Count | 103 |
| Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.



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**Table 4. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | PECL Mode Power Supply | $V_{EE}$ = 0 V | | 8 | V |
| $V_{EE}$ | NECL Mode Power Supply | $V_{CC}$ = 0 V | | −8 | V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA |
| $V_I$ | PECL Mode Input Voltage<br>NECL Mode Input Voltage | $V_{EE}$ = 0 V<br>$V_{CC}$ = 0 V | $V_I \le V_{CC}$<br>$V_I \ge V_{EE}$ | 6<br>−6 | V |
| $I_{BB}$ | $V_{BB}$ Sink/Source | | | ± 0.5 | mA |
| $T_A$ | Operating Temperature Range | | | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction-to-Ambient) | 0 lfpm<br>500 lfpm | SOIC−16 | 130<br>75 | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction-to-Case) | Standard Board | SOIC−16 | 33 to 36 | °C/W |
| $T_{sol}$ | Wave Solder (Pb-Free) | <2 to 3 sec @ 260°C | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 5. 10EL SERIES PECL DC CHARACTERISTICS** ($V_{CC}$ = 5.0 V; $V_{EE}$ = 0.0 V (Note 1))

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Power Supply Current | | 25 | 35 | | 25 | 35 | | 25 | 35 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 3920 | 4010 | 4110 | 4020 | 4105 | 4190 | 4090 | 4185 | 4280 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 3050 | 3200 | 3350 | 3050 | 3210 | 3370 | 3050 | 3227 | 3405 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 3770 | | 4110 | 3870 | | 4190 | 3940 | | 4280 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 3050 | | 3500 | 3050 | | 3520 | 3050 | | 3555 | mV |
| $V_{BB}$ | Output Voltage Reference | 3.57 | | 3.7 | 3.65 | | 3.75 | 3.69 | | 3.81 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3) | 2.5 | | 4.6 | 2.5 | | 4.6 | 2.5 | | 4.6 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.3 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.06 V / −0.5 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP}$min and 1 V.



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**Table 6. 10EL SERIES NECL DC CHARACTERISTICS** ($V_{CC}$ = 0 V; $V_{EE}$ = −5.0 V (Note 1))

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Power Supply Current | | 25 | 35 | | 25 | 35 | | 25 | 35 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | −1080 | −990 | −890 | −980 | −895 | −810 | −910 | −815 | −720 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | −1950 | −1800 | −1650 | −1950 | −1790 | −1630 | −1950 | −1773 | −1595 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | −1230 | | −890 | −1130 | | −810 | −1060 | | −720 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | −1950 | | −1500 | −1950 | | −1480 | −1950 | | −1445 | mV |
| $V_{BB}$ | Output Voltage Reference | −1.43 | | −1.30 | −1.35 | | −1.25 | −1.31 | | −1.19 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3) | −2.5 | | −0.4 | −2.5 | | −0.4 | −2.5 | | −0.4 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.3 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.06 V / −0.5 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP}$min and 1 V.

**Table 7. 100EL SERIES PECL DC CHARACTERISTICS** ($V_{CC}$ = 5.0 V; $V_{EE}$ = 0.0 V (Note 1))

| | | −40°C | | | 25°C | | | 85°C | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Characteristic** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| $I_{EE}$ | Power Supply Current | | 25 | 35 | | 25 | 35 | | 25 | 38 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | 3915 | 3995 | 4120 | 3975 | 4045 | 4120 | 3975 | 4050 | 4120 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | 3170 | 3305 | 3445 | 3190 | 3295 | 3380 | 3190 | 3295 | 3380 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | 3835 | | 4120 | 3835 | | 4120 | 3835 | | 4120 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | 3190 | | 3525 | 3190 | | 3525 | 3190 | | 3525 | mV |
| $V_{BB}$ | Output Voltage Reference | 3.62 | | 3.74 | 3.62 | | 3.74 | 3.62 | | 3.74 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3) | 2.5 | | 4.6 | 2.5 | | 4.6 | 2.5 | | 4.6 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.8 V / −0.5 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP}$min and 1 V.



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**Table 8. 100EL SERIES NECL DC CHARACTERISTICS** ($V_{CC}$ = 0 V; $V_{EE}$ = −5.0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{EE}$ | Power Supply Current | | 25 | 35 | | 25 | 35 | | 25 | 38 | mA |
| $V_{OH}$ | Output HIGH Voltage (Note 2) | −1085 | −1005 | −880 | −1025 | −955 | −880 | −1025 | −955 | −880 | mV |
| $V_{OL}$ | Output LOW Voltage (Note 2) | −1830 | −1695 | −1555 | −1810 | −1705 | −1620 | −1810 | −1705 | −1620 | mV |
| $V_{IH}$ | Input HIGH Voltage (Single-Ended) | −1165 | | −880 | −1165 | | −880 | −1165 | | −880 | mV |
| $V_{IL}$ | Input LOW Voltage (Single-Ended) | −1810 | | −1475 | −1810 | | −1475 | −1810 | | −1475 | mV |
| $V_{BB}$ | Output Voltage Reference | −1.38 | | −1.26 | −1.38 | | −1.26 | −1.38 | | −1.26 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential) (Note 3) | −2.5 | | −0.4 | −2.5 | | −0.4 | −2.5 | | −0.4 | V |
| $I_{IH}$ | Input HIGH Current | | | 150 | | | 150 | | | 150 | μA |
| $I_{IL}$ | Input LOW Current | 0.5 | | | 0.5 | | | 0.5 | | | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. Input and output parameters vary 1:1 with $V_{CC}$. $V_{EE}$ can vary +0.8 V / −0.5 V.
2. Outputs are terminated through a 50 Ω resistor to $V_{CC}$ − 2.0 V.
3. $V_{IHCMR}$ min varies 1:1 with $V_{EE}$, $V_{IHCMR}$ max varies 1:1 with $V_{CC}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between $V_{PP}$min and 1 V.

**Table 9. AC CHARACTERISTICS** ($V_{CC}$ = 5.0 V; $V_{EE}$ = 0.0 V or $V_{CC}$= 0 V; $V_{EE}$ = −5.0 V (Note 1))

| Symbol | Characteristic | −40°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $f_{MAX}$ | Maximum Toggle Frequency | | | | | 1.25 | | | | | GHz |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>CLK to Q (Diff)<br>CLK to Q (SE)<br>SCLK to Q | 460<br>410<br>410 | | 660<br>710<br>710 | 470<br>420<br>420 | | 670<br>720<br>720 | 500<br>450<br>470 | | 700<br>750<br>750 | ps |
| $t_{SKEW}$ | Part-to-Part Skew<br>Within-Device Skew (Note 2) | | | 200<br>50 | | | 200<br>50 | | | 200<br>50 | ps |
| $t_{JITTER}$ | Random Clock Jitter (RMS) | | | | | 2.6 | | | | | ps |
| $t_S$ | Setup Time $\overline{EN}$ | 150 | | | 150 | | | 150 | | | ps |
| $t_H$ | Hold Time $\overline{EN}$ | 400 | | | 400 | | | 400 | | | ps |
| $V_{PP}$ | Input Swing (Note 3) | 150 | | 1000 | 150 | | 1000 | 150 | | 1000 | mV |
| $t_r$<br>$t_f$ | Output Rise/Fall Times Q<br>(20% − 80%) | 325 | | 575 | 325 | | 575 | 325 | | 575 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

1. 10 Series: $V_{EE}$ can vary +0.06 V / −0.5 V.
   100 Series: $V_{EE}$ can vary +0.8 V / −0.5 V.
2. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.
3. $V_{PP}$(min) is minimum input swing for which AC parameters guaranteed. The device has a DC gain of ≈ 40.



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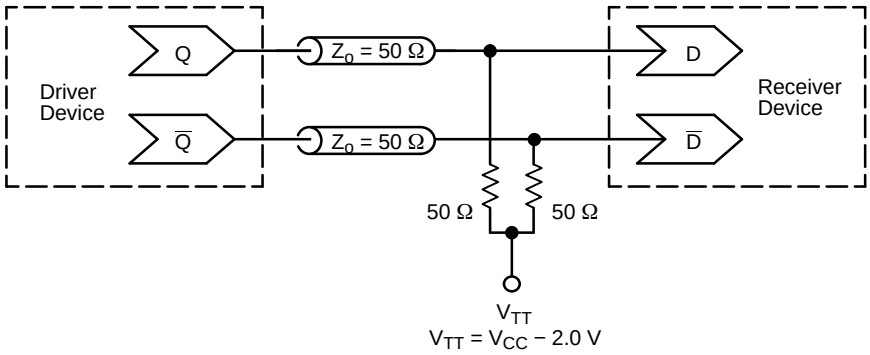



**Figure 2. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)**

### Resource Reference of Application Notes

**AN1405/D** − ECL Clock Distribution Techniques

**AN1406/D** − Designing with PECL (ECL at +5.0 V)

**AN1503/D** − ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** − Metastability and the ECLinPS Family

**AN1568/D** − Interfacing Between LVDS and ECL

**AN1672/D** − The ECL Translator Guide

**AND8001/D** − Odd Number Counters Design

**AND8002/D** − Marking and Date Codes

**AND8020/D** − Termination of ECL Logic Devices

**AND8066/D** − Interfacing with ECLinPS

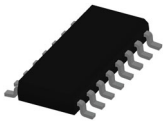
**AND8090/D** − AC Characteristics of ECL Devices

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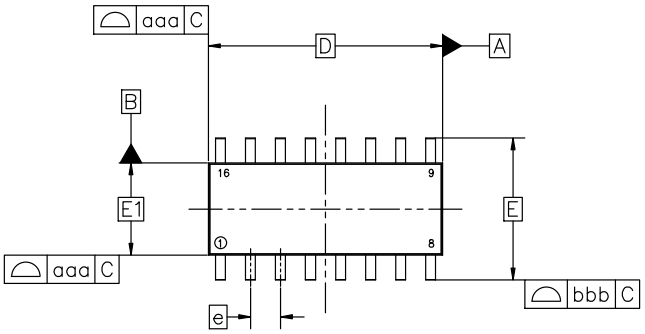
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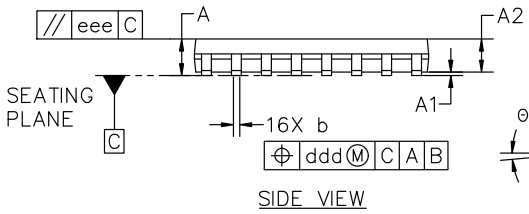
**SOIC−16 9.90x3.90x1.37 1.27P**
CASE 751B
ISSUE M

DATE 18 OCT 2024

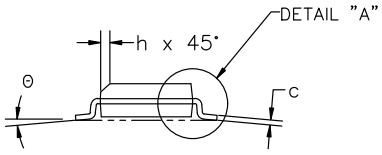
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



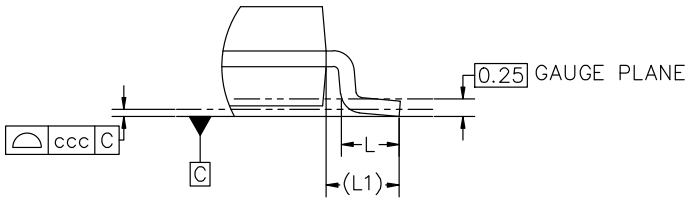

TOP VIEW




SIDE VIEW

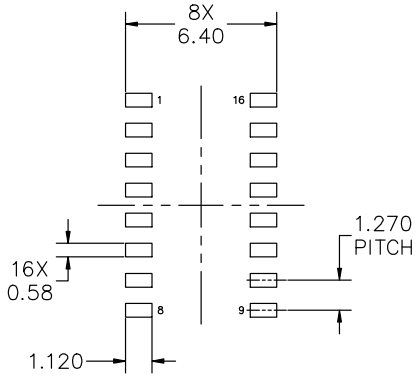



END VIEW




DETAIL "A"
Scale 3:1

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 1.35 | 1.55 | 1.75 |
| A1 | 0.10 | 0.18 | 0.25 |
| A2 | 1.25 | 1.37 | 1.50 |
| b | 0.35 | 0.42 | 0.49 |
| c | 0.19 | 0.22 | 0.25 |
| D | 9.90 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27 BSC | | |
| h | 0.25 | −−− | 0.50 |
| L | 0.40 | 0.83 | 1.25 |
| L1 | 1.05 REF | | |
| Θ | 0° | −−− | 7° |
| TOLERANCE OF FORM AND POSITION | | | |
| aaa | 0.10 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.25 | | |
| eee | 0.10 | | |




RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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| **DESCRIPTION:** | **SOIC−16 9.90X3.90X1.37 1.27P** | | **PAGE 1 OF 2** |

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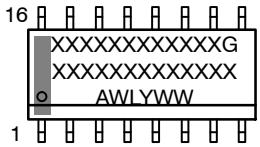


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CASE 751B
ISSUE M

DATE 18 OCT 2024

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

| | |
|---|---|
| PIN 1. | COLLECTOR |
| 2. | BASE |
| 3. | EMITTER |
| 4. | NO CONNECTION |
| 5. | EMITTER |
| 6. | BASE |
| 7. | COLLECTOR |
| 8. | COLLECTOR |
| 9. | BASE |
| 10. | EMITTER |
| 11. | NO CONNECTION |
| 12. | EMITTER |
| 13. | BASE |
| 14. | COLLECTOR |
| 15. | EMITTER |
| 16. | COLLECTOR |

STYLE 2:

| | |
|---|---|
| PIN 1. | CATHODE |
| 2. | ANODE |
| 3. | NO CONNECTION |
| 4. | CATHODE |
| 5. | CATHODE |
| 6. | NO CONNECTION |
| 7. | ANODE |
| 8. | CATHODE |
| 9. | CATHODE |
| 10. | ANODE |
| 11. | NO CONNECTION |
| 12. | CATHODE |
| 13. | CATHODE |
| 14. | NO CONNECTION |
| 15. | ANODE |
| 16. | CATHODE |

STYLE 3:

| | |
|---|---|
| PIN 1. | COLLECTOR, DYE #1 |
| 2. | BASE, #1 |
| 3. | EMITTER, #1 |
| 4. | COLLECTOR, #1 |
| 5. | COLLECTOR, #2 |
| 6. | BASE, #2 |
| 7. | EMITTER, #2 |
| 8. | COLLECTOR, #2 |
| 9. | COLLECTOR, #3 |
| 10. | BASE, #3 |
| 11. | EMITTER, #3 |
| 12. | COLLECTOR, #3 |
| 13. | COLLECTOR, #4 |
| 14. | BASE, #4 |
| 15. | EMITTER, #4 |
| 16. | COLLECTOR, #4 |

STYLE 4:

| | |
|---|---|
| PIN 1. | COLLECTOR, DYE #1 |
| 2. | COLLECTOR, #1 |
| 3. | COLLECTOR, #2 |
| 4. | COLLECTOR, #2 |
| 5. | COLLECTOR, #3 |
| 6. | COLLECTOR, #3 |
| 7. | COLLECTOR, #4 |
| 8. | COLLECTOR, #4 |
| 9. | BASE, #4 |
| 10. | EMITTER, #4 |
| 11. | BASE, #3 |
| 12. | EMITTER, #3 |
| 13. | BASE, #2 |
| 14. | EMITTER, #2 |
| 15. | BASE, #1 |
| 16. | EMITTER, #1 |

STYLE 5:

| | |
|---|---|
| PIN 1. | DRAIN, DYE #1 |
| 2. | DRAIN, #1 |
| 3. | DRAIN, #2 |
| 4. | DRAIN, #2 |
| 5. | DRAIN, #3 |
| 6. | DRAIN, #3 |
| 7. | DRAIN, #4 |
| 8. | DRAIN, #4 |
| 9. | GATE, #4 |
| 10. | SOURCE, #4 |
| 11. | GATE, #3 |
| 12. | SOURCE, #3 |
| 13. | GATE, #2 |
| 14. | SOURCE, #2 |
| 15. | GATE, #1 |
| 16. | SOURCE, #1 |

STYLE 6:

| | |
|---|---|
| PIN 1. | CATHODE |
| 2. | CATHODE |
| 3. | CATHODE |
| 4. | CATHODE |
| 5. | CATHODE |
| 6. | CATHODE |
| 7. | CATHODE |
| 8. | CATHODE |
| 9. | ANODE |
| 10. | ANODE |
| 11. | ANODE |
| 12. | ANODE |
| 13. | ANODE |
| 14. | ANODE |
| 15. | ANODE |
| 16. | ANODE |

STYLE 7:

| | |
|---|---|
| PIN 1. | SOURCE N-CH |
| 2. | COMMON DRAIN (OUTPUT) |
| 3. | COMMON DRAIN (OUTPUT) |
| 4. | GATE P-CH |
| 5. | COMMON DRAIN (OUTPUT) |
| 6. | COMMON DRAIN (OUTPUT) |
| 7. | COMMON DRAIN (OUTPUT) |
| 8. | SOURCE P-CH |
| 9. | SOURCE P-CH |
| 10. | COMMON DRAIN (OUTPUT) |
| 11. | COMMON DRAIN (OUTPUT) |
| 12. | COMMON DRAIN (OUTPUT) |
| 13. | GATE N-CH |
| 14. | COMMON DRAIN (OUTPUT) |
| 15. | COMMON DRAIN (OUTPUT) |
| 16. | SOURCE N-CH |




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