

FDMS015N04B

N-Channel PowerTrench® MOSFET

40 V, 100 A, 1.5 mΩ

Features

- $R_{DS(on)} = 1.13 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 50 \text{ A}$
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant

Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advance PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Synchronous Rectification for A/C Server
- Battery Protection Circuit
- Motor Drives and Renewable Power Supplies



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDMS015N04B	Unit
V_{DSS}	Drain to Source Voltage	40	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	A
		- Continuous ($T_A = 25^\circ\text{C}$) (Note 1a)	
I_{DM}	Drain Current	- Pulsed (Note 2)	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 3)	mJ
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	W
		($T_A = 25^\circ\text{C}$) (Note 1a)	W
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDMS015N04B	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS015N04B	FDMS015N04B	Power 56	13 "	12 mm	3000 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
--------	-----------	-----------------	------	------	------	------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	40	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	37	-	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\ \text{V}$, $V_{GS} = 0\ \text{V}$	-	-	1	μA
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	-	-	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 50\ \text{A}$	-	1.3	1.5	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\ \text{V}$, $I_D = 50\ \text{A}$	-	71	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$	-	6560	8725	pF
C_{oss}	Output Capacitance	$f = 1\ \text{MHz}$	-	2795	3720	pF
C_{rss}	Reverse Transfer Capacitance		-	162	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$	-	3896	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V		-	91	118	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DS} = 20\ \text{V}$, $I_D = 50\ \text{A}$	-	26	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$	-	9	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	16	-	nC
ESR	Equivalent Series Resistance	$f = 1\ \text{MHz}$	-	1.4	-	Ω

Switching Characteristics

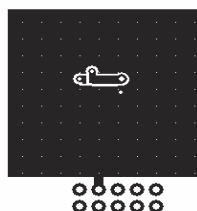
$t_{d(on)}$	Turn-On Delay Time	$V_{DS} = 20\ \text{V}$, $I_D = 50\ \text{A}$	-	34	78	ns
t_r	Turn-On Rise Time	$V_{GS} = 10\ \text{V}$, $R_G = 4.7\ \Omega$	-	24	58	ns
$t_{d(off)}$	Turn-Off Delay Time		-	71	152	ns
t_f	Turn-Off Fall Time	(Note 4)	-	26	62	ns

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	100	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	400	A
V_{SD}	Drain to Source Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_{SD} = 50\ \text{A}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\ \text{V}$, $I_{SD} = 50\ \text{A}$	-	78	-	ns
Q_{rr}	Reverse Recovery Charge	$di_F/dt = 100\ \text{A}/\mu\text{s}$	-	90	-	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50\ ^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



b. $125\ ^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Repetitive rating: pulse-width limited by maximum junction temperature.
3. $L = 3\ \text{mH}$, $I_{AS} = 18.72\ \text{A}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

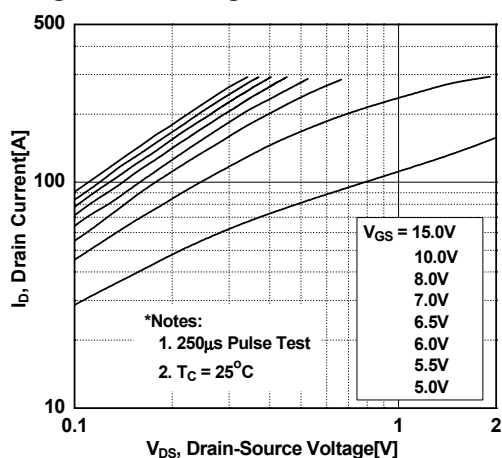


Figure 2. Transfer Characteristics

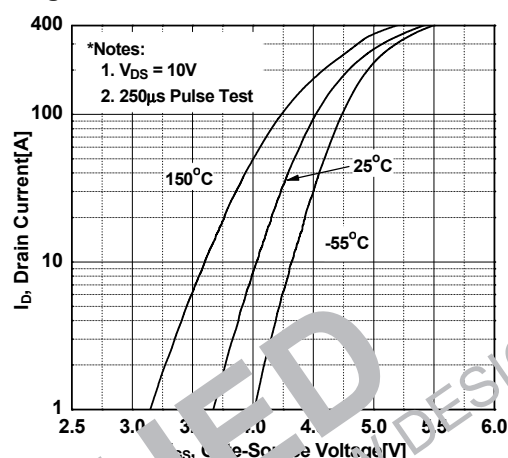


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

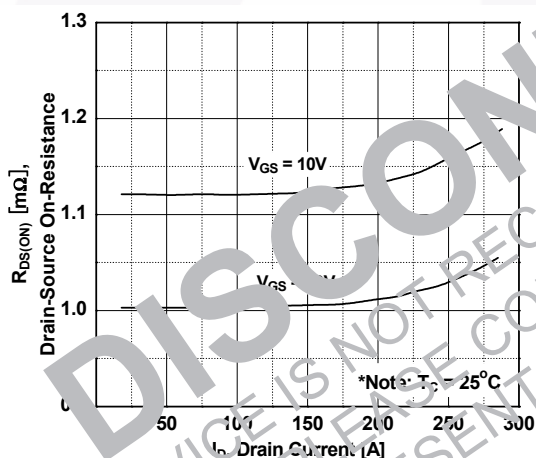


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

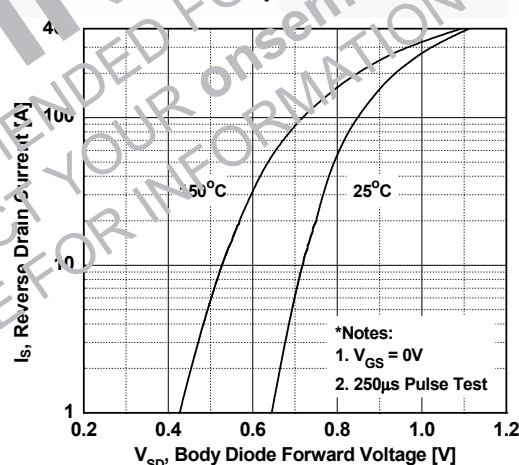


Figure 5. Capacitance Characteristics

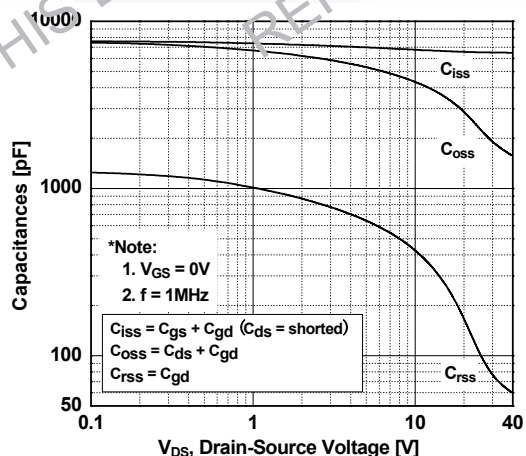
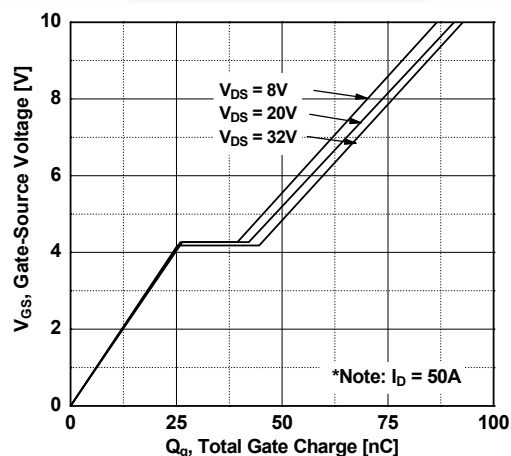


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

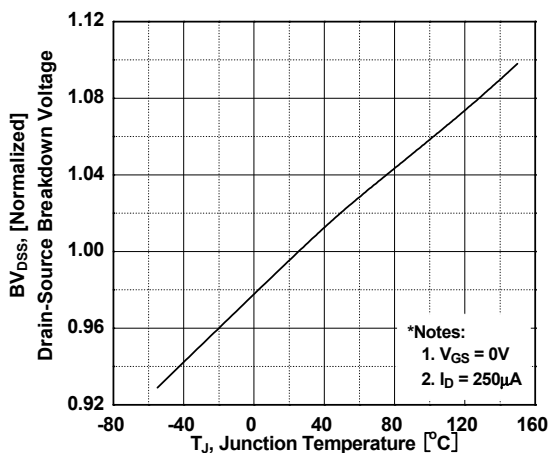


Figure 8. On-Resistance Variation vs. Temperature

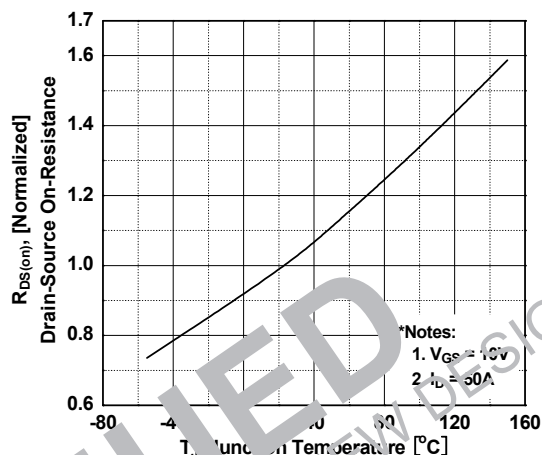


Figure 9. Maximum Safe Operating Area

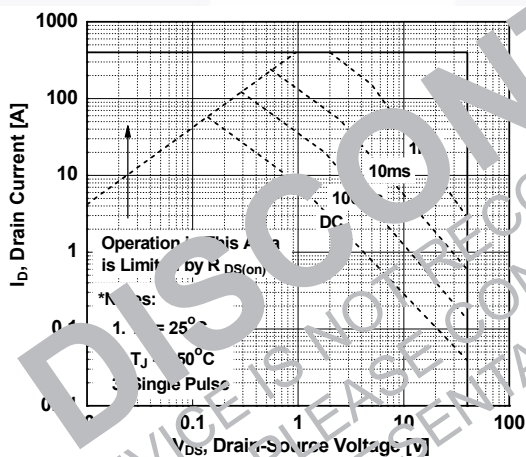


Figure 10. Maximum Drain Current vs. Case Temperature

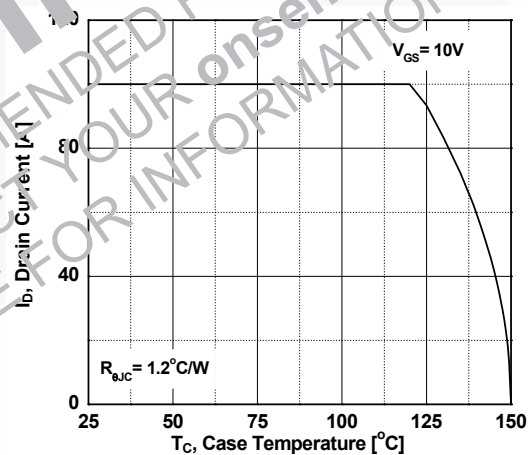


Figure 11. E_oss vs. Drain to Source Voltage

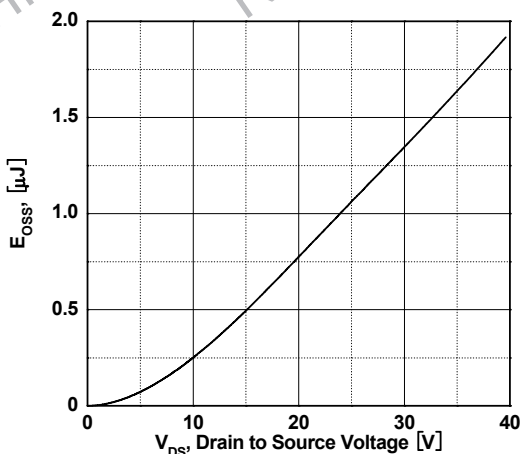
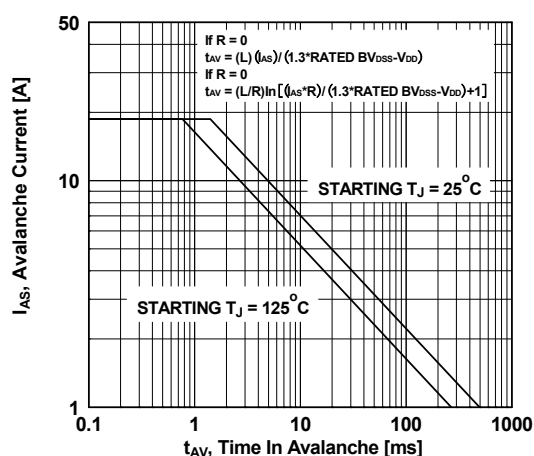
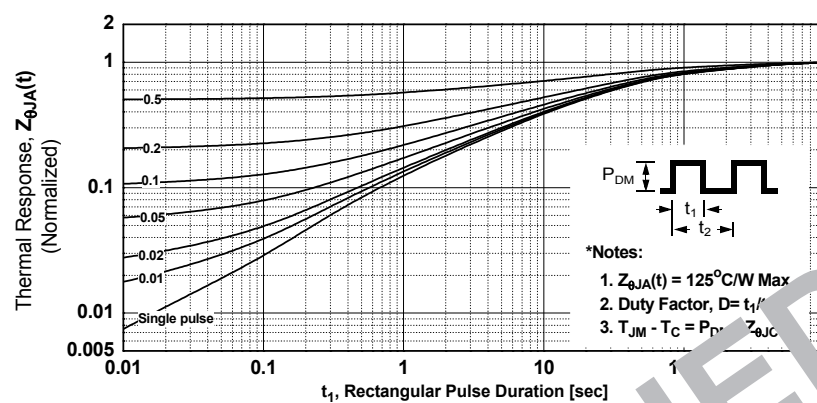


Figure 12. Unclamped Inductive Switching Capability



Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve



DISCONTINUED

THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
 PLEASE CONTACT YOUR onsemi
 REPRESENTATIVE FOR INFORMATION

Figure 14. Gate Charge Test Circuit & Waveform

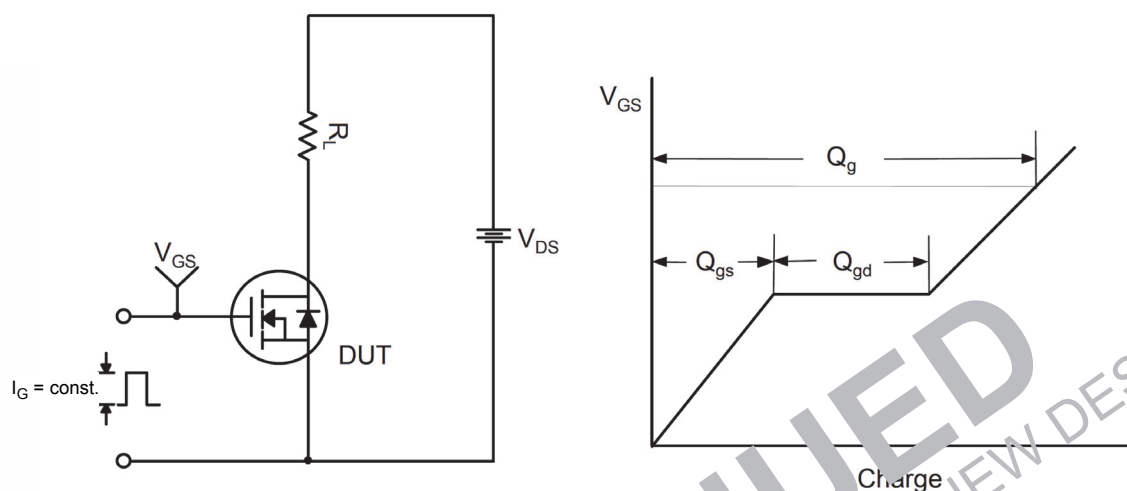


Figure 15. Resistive Switching Test Circuit & Waveforms

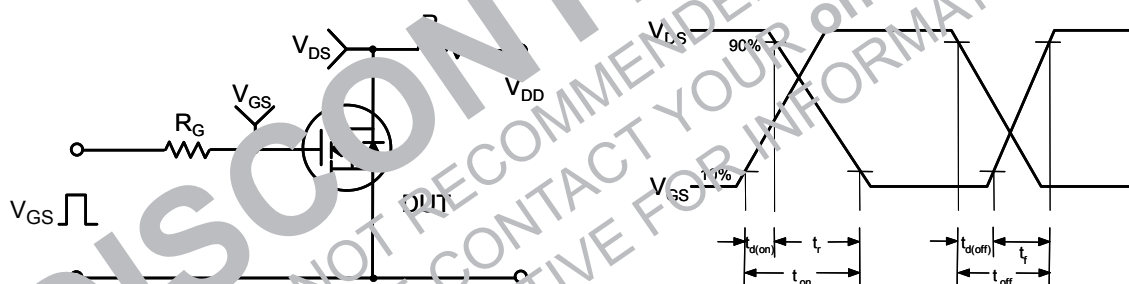


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

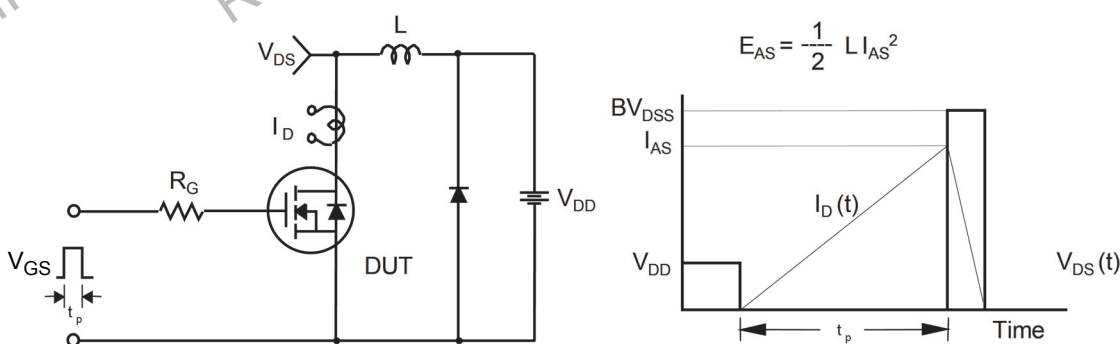
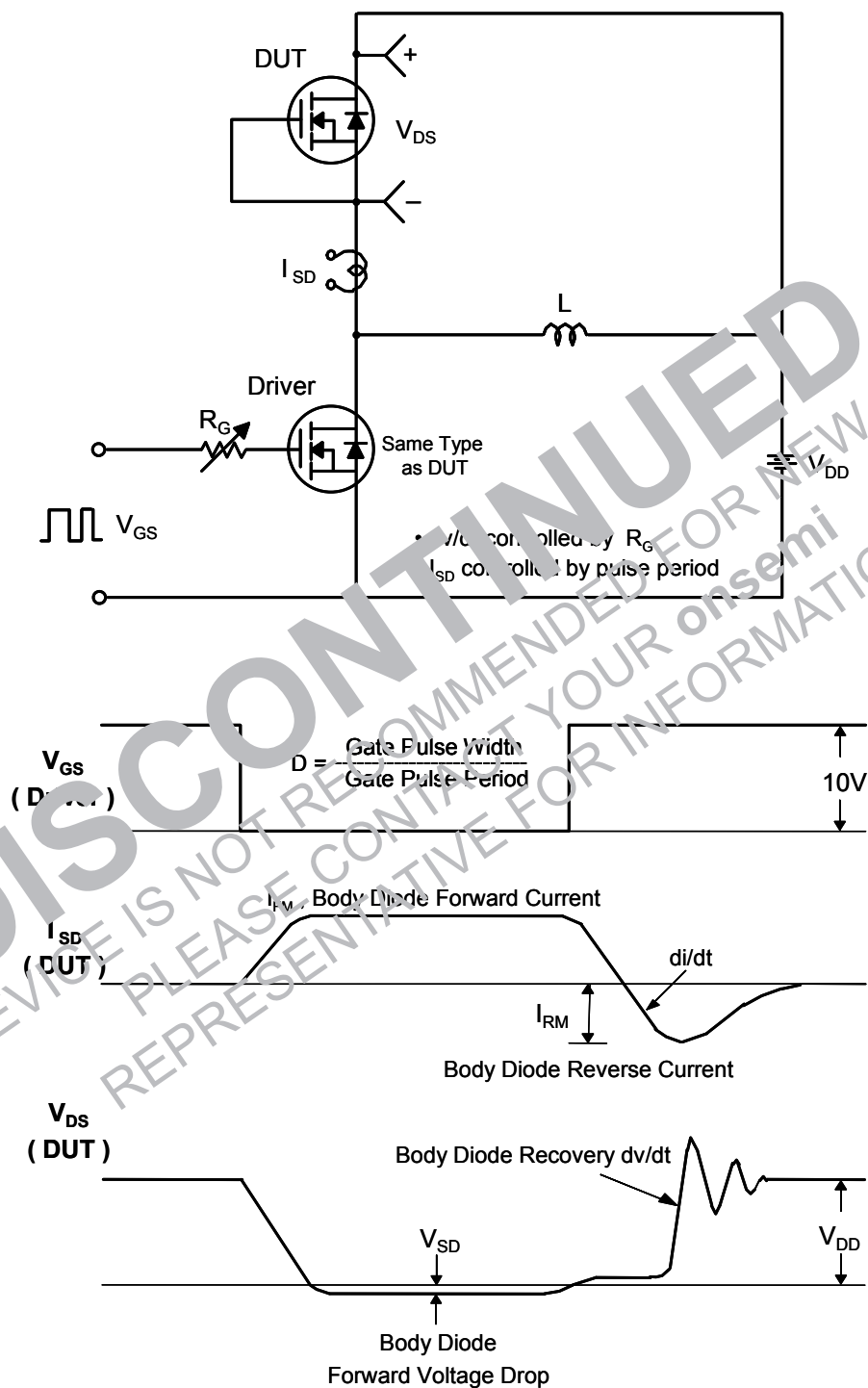
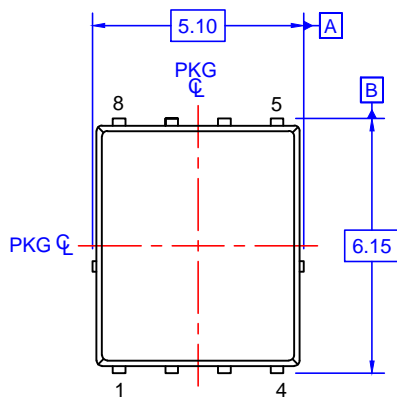


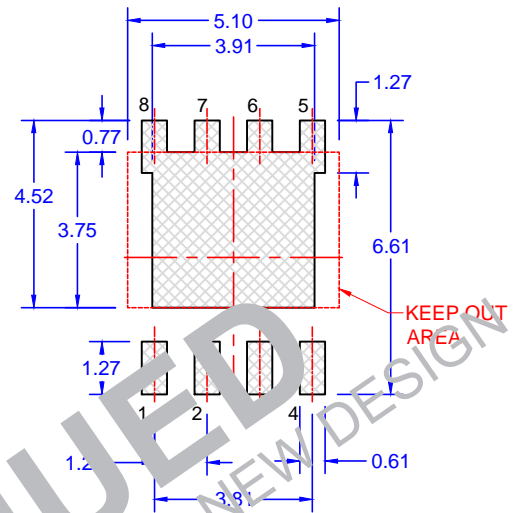
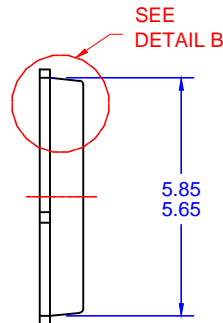
Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms



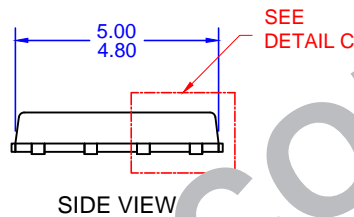
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE A



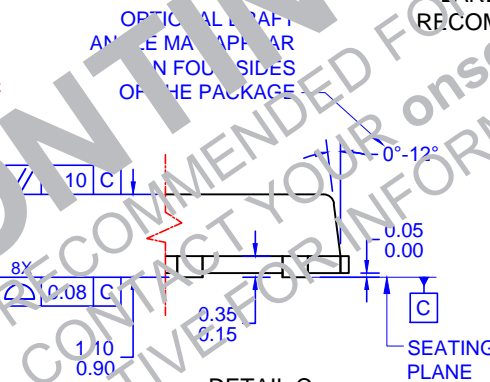
TOP VIEW



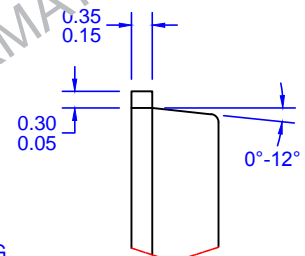
LAND PATTERN
RECOMMENDATION



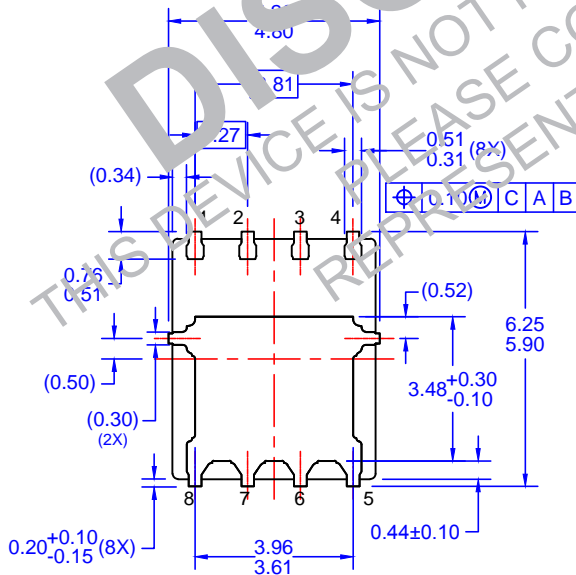
SIDE VIEW



DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW


NOTES: UNLESS OTHERWISE SPECIFIED

- PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
- DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

ON Semiconductor



DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative