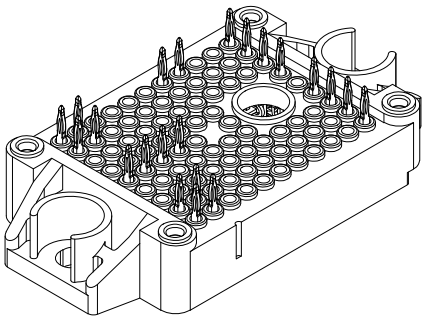
Silicon Carbide (SiC) Module – 30 mohm SiC M3S MOSFET, 1200 V, 4-PACK Full Bridge Topology, F1 Package

Product Preview

NXH030F120M3F1PTG



PIM22 33.8x42.5 (PRESS FIT)
CASE 180HL

The NXH030F120M3F1PTG is a power module containing 30 mΩ/1200 V SiC MOSFET full−bridge and a thermistor with Al_2O_3 DBC in an F1 package.

Features

- 30 mΩ /1200 V M3S SiC MOSFET Full−Bridge
- Al_2O_3 DBC
- Thermistor
- Options with Pre−Applied Thermal Interface Material (TIM) and without Pre−Applied TIM
- Options with Solderable Pins and Press−Fit Pins
- These Devices are Pb−Free, Halide Free and are RoHS Compliant

Typical Applications

- Solar Inverter
- Uninterruptible Power Supplies
- Electric Vehicle Charging Stations
- Industrial Power

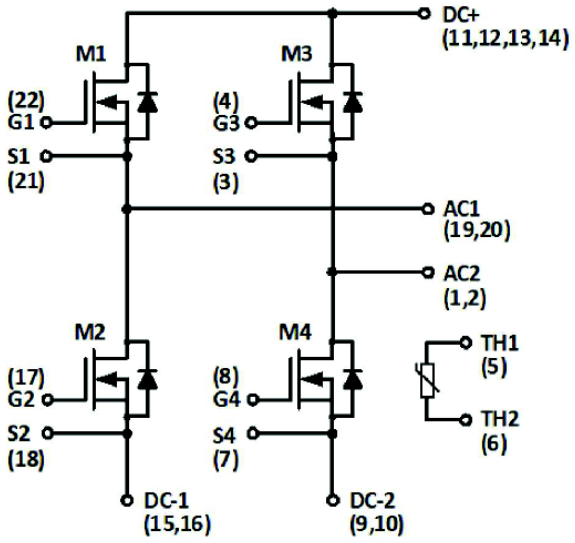


Figure 1. NXH030F120M3F1PTG Schematic Diagram

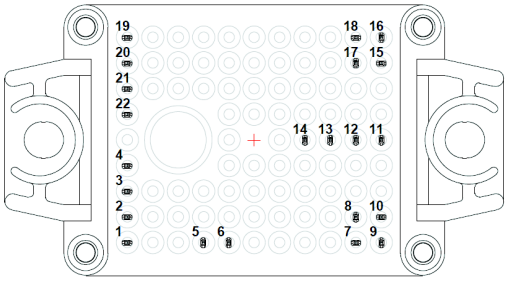
This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

MARKING DIAGRAM



NXH030F120M3F1PTG = Specific Device Code
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

PIN CONNECTIONS



See Pin Function Description for pin names

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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PIN FUNCTION DESCRIPTION

Pin	Name	Description
1	AC2	Center point of full bridge 2
2	AC2	Center point of full bridge 2
3	S3	M3 Kelvin Source (High Side switch)
4	G3	M3 Gate (High Side switch)
5	TH1	Thermistor Connection 1
6	TH2	Thermistor Connection 2
7	S4	M4 Kelvin Source (Low side switch)
8	G4	M4 Gate (Low side switch)
9	DC−2	DC Negative Bus connection
10	DC−2	DC Negative Bus connection
11	DC+	DC Positive Bus connection
12	DC+	DC Positive Bus connection
13	DC+	DC Positive Bus connection
14	DC+	DC Positive Bus connection
15	DC−1	DC Negative Bus connection
16	DC−1	DC Negative Bus connection
17	G2	M2 Gate (Low side switch)
18	S2	M2 Kelvin Source (Low side switch)
19	AC1	Center point of full bridge 1
20	AC1	Center point of full bridge 1
21	S1	M1 Kelvin Source (High side switch)
22	G1	M1 Gate (High side switch)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
SiC MOSFET			
Drain−Source Voltage	V_{DSS}	1200	V
Gate−Source Voltage	V_{GS}	+22/−10	V
Continuous Drain Current @ T_C = 80°C (T_J = 175°C)	I_D	38	A
Pulsed Drain Current (T_J = 175°C)	I_{Dpulse}	115	A
Maximum Power Dissipation (T_J = 175°C)	P_{tot}	100	W
Minimum Operating Junction Temperature	T_{JMIN}	−40	°C
Maximum Operating Junction Temperature	T_{JMAX}	175	°C
THERMAL PROPERTIES			
Storage Temperature Range	T_{stg}	−40 to 150	°C
INSULATION PROPERTIES			
Isolation Test Voltage, t = 1 s, 60 Hz	V_{is}	4800	V_{RMS}
Creepage Distance		12.7	mm
CTI		600	
Substrate Ceramic Material		Al_2O_3	
Substrate Ceramic Material Thickness		0.32	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.

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RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Module Operating Junction Temperature	T_J	−40	150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
SiC MOSFET CHARACTERISTICS						
Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 1200 V, T_J = 25°C	I_{DSS}	–	–	100	μA
Drain−Source On Resistance	V_{GS} = 18 V, I_D = 30 A, T_J = 25°C	$R_{DS(ON)}$	–	30.6	38.5	mΩ
	V_{GS} = 18 V, I_D = 30 A, T_J = 125°C		–	51.1	–	
	V_{GS} = 18 V, I_D = 30 A, T_J = 150°C		–	59.3	–	
	V_{GS} = 18 V, I_D = 30 A, T_J = 175°C		–	68.2	–	
Gate−Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 15 mA	$V_{GS(TH)}$	2.04	2.6	4.4	V
Recommended Gate Voltage		V_{GOP}	−3	–	+18	V
Gate−to−Source Leakage Current	V_{GS} = +22/−10 V, V_{DS} = 0 V	I_{GSS}	–	–	±1	μA
Input Capacitance	V_{GS} = 0 V, f = 1 Mhz, V_{DS} = 800 V	C_{ISS}	–	2246	–	pF
Reverse Transfer Capacitance		C_{RSS}	–	12.1	–	
Output Capacitance		C_{OSS}	–	156	–	
Total Gate Charge	V_{GS} = −3/18 V, V_{DS} = 800 V, I_D = 30 A	$Q_{G(TOTAL)}$	–	110	–	nC
Gate−Source Charge		Q_{GS}	–	19	–	
Gate−Drain Charge		Q_{GD}	–	30	–	
Internal Gate Resistance	f = 1 MHz	R_{GINT}	–	3.3	–	Ω
Turn−on Delay Time	T_J = 25°C, V_{DS} = 800 V, I_D = 30 A, V_{GS} = −3 V/18 V, R_G = 4.7 Ω	$t_{d(on)}$	–	40.4	–	ns
Rise Time		t_r	–	9	–	
Turn−off Delay Time		$t_{d(off)}$	–	109.5	–	
Fall Time		t_f	–	9.3	–	
Turn−on Switching Loss per Pulse		E_{ON}	–	520	–	μJ
Turn off Switching Loss per Pulse		E_{OFF}	–	80	–	
Turn−on Delay Time	T_J = 150°C, V_{DS} = 800 V, I_D = 30 A, V_{GS} = −3 V/18 V, R_G = 4.7 Ω	$t_{d(on)}$	–	39.9	–	ns
Rise Time		t_r	–	6.8	–	
Turn−off Delay Time		$t_{d(off)}$	–	118.1	–	
Fall Time		t_f	–	8.7	–	
Turn−on Switching Loss per Pulse		E_{ON}	–	750	–	μJ
Turn off Switching Loss per Pulse		E_{OFF}	–	96	–	
Diode Forward Voltage	V_{GS} = −3 V, I_{SD} = 30 A, T_J = 25°C	V_{SD}	–	4.67	6	V
	V_{GS} = −3 V, I_{SD} = 30 A, T_J = 125°C		–	4.45	–	
	V_{GS} = −3 V, I_{SD} = 30 A, T_J = 150°C		–	4.4	–	
Thermal Resistance − Chip−to−Case	M1, M2	R_{thJC}	–	0.95	–	°C/W
Thermal Resistance − Chip−to−Heatsink		R_{thJH}	–	1.54	–	°C/W

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ELECTRICAL CHARACTERISTICS (continued) (T_J = 25 °C unless otherwise noted)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
THERMISTOR CHARACTERISTICS						
Nominal Resistance	T = 25°C	R_{25}	–	5	–	kΩ
	T = 100°C	R_{100}	–	493	–	Ω
	T = 150°C	R_{150}	–	159.5	–	Ω
Deviation of R_{100}	T = 100°C	ΔR/R	−5	–	5	%
Power Dissipation – Recommended Limit	0.15 mA, Non−self−heating Effect	P_D	–	0.1	–	mW
Power Dissipation – Absolute Maximum	5 mA	P_D	–	34.2	–	mW
Power Dissipation Constant			–	1.4	–	mW/K
B−value	B (25/50), tolerance ±2%		–	3375	–	K
B−value	B (25/100), tolerance ±2%		–	3436	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ORDERING INFORMATION

Orderable Part Number	Marking	Package	Shipping
NXH030F120M3F1PTG	NXH030F120M3F1PTG	F1FULLBR: Case 180HL Press−fit Pins with pre−applied thermal interface material (TIM) (Pb−Free and Halide−Free)	28 Units / Blister Tray

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TYPICAL CHARACTERISTICS M1/M2 SIC MOSFET CHARACTERISTIC

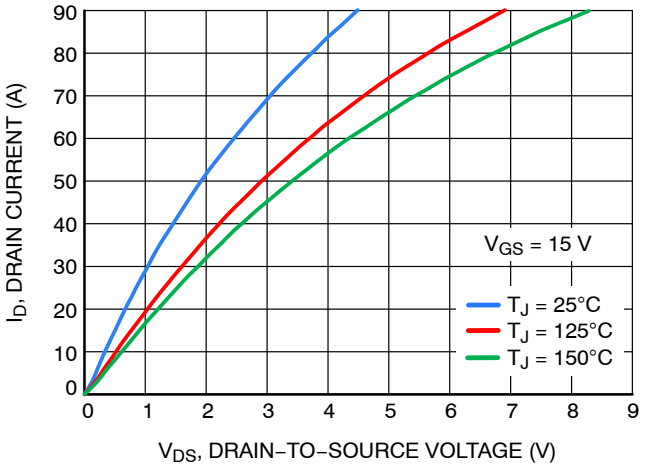


Figure 2. MOSFET Typical Output Characteristic V_{GS} = 15 V

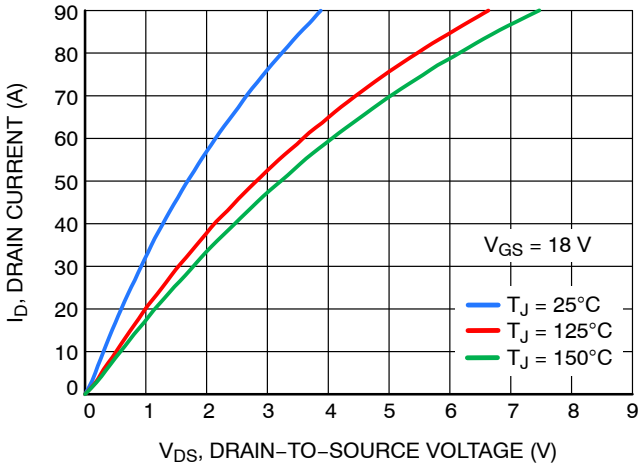


Figure 3. MOSFET Typical Output Characteristic V_{GS} = 18 V

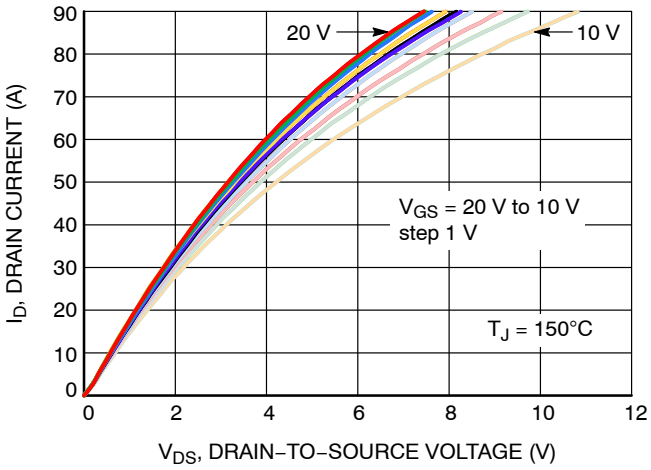


Figure 4. MOSFET Typical Output Characteristic V_{GS} = var.

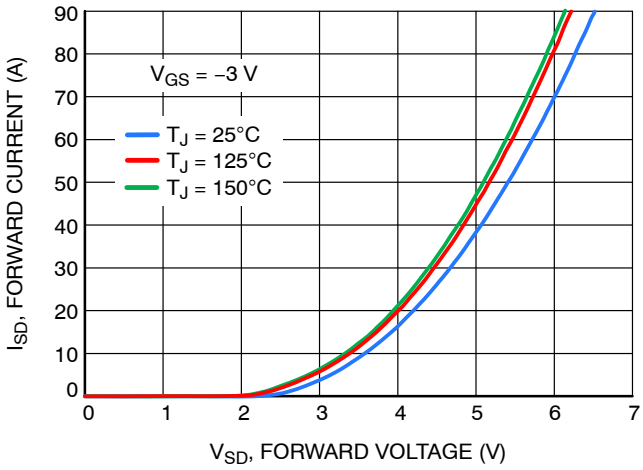


Figure 5. Body Diode Forward Characteristic

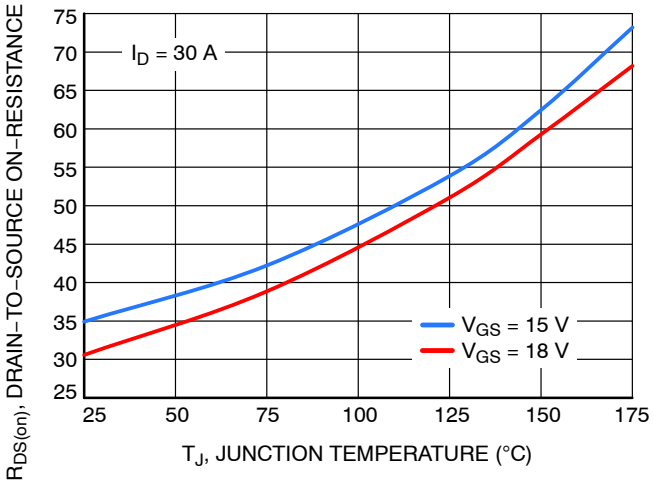


Figure 6. RDS(ON) Drain−to−Source ON Resistance vs. Junction Temperature

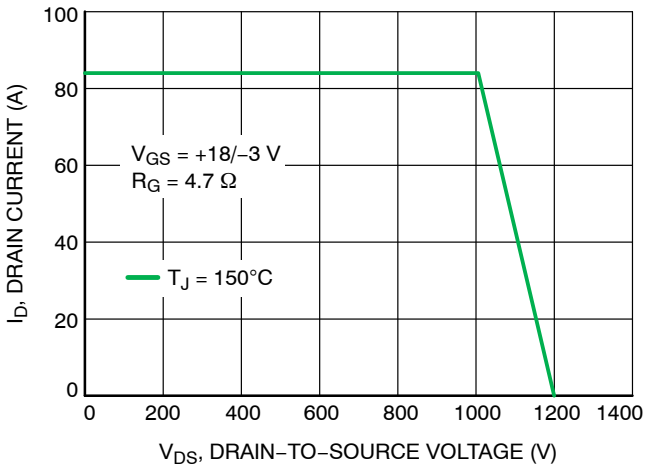


Figure 7. Reverse Bias Safe Operating Area (RBSOA)

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TYPICAL CHARACTERISTICS M1/M2 SIC MOSFET CHARACTERISTIC

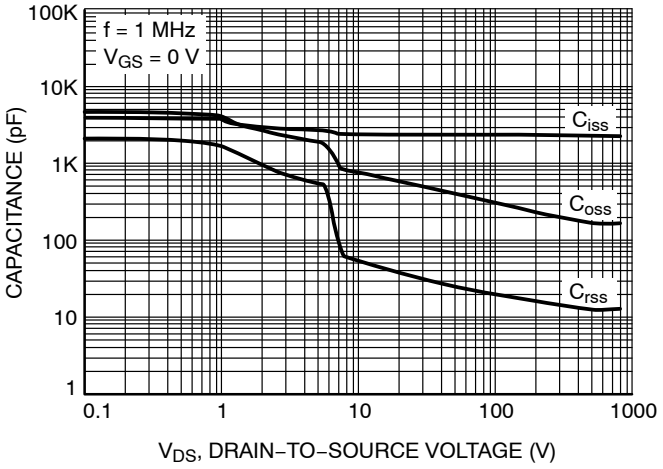


Figure 8. Capacitance vs. Drain−to−Source Voltage

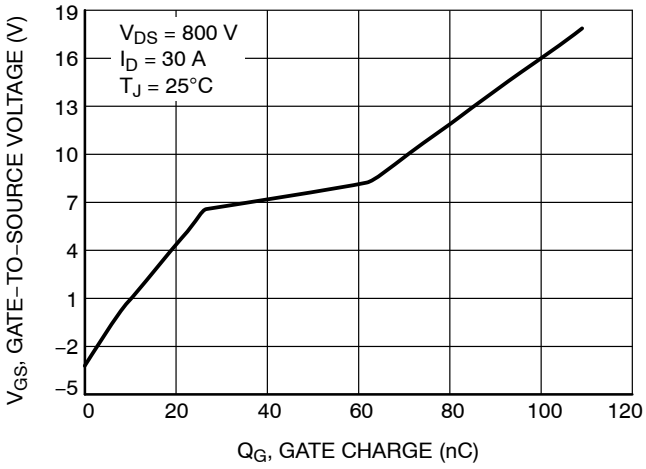


Figure 9. Gate−to−Source Voltage vs. Gate Charge

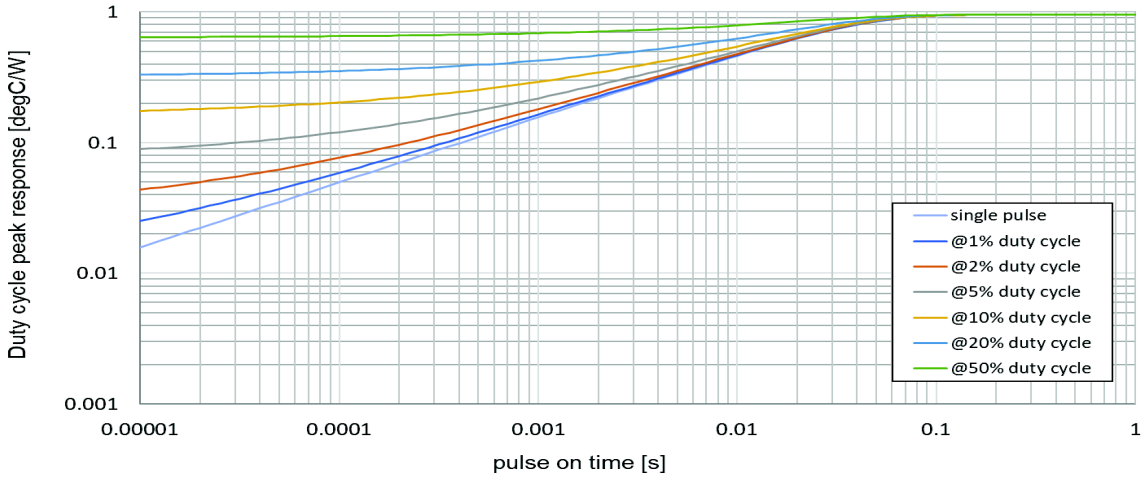


Figure 10. Duty Cycle vs. Junction−to−Case Transient Thermal Impedance

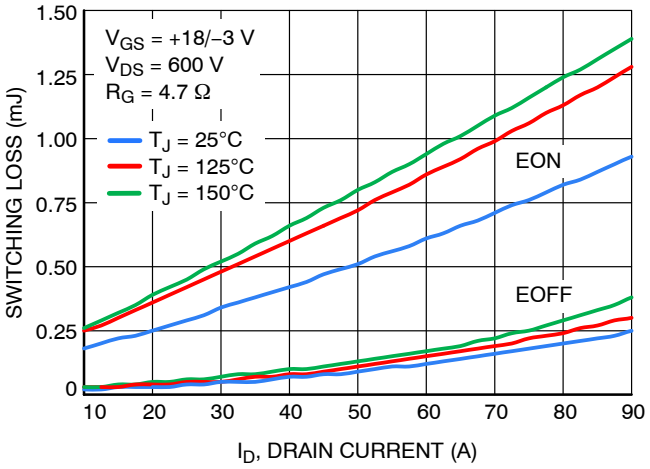


Figure 11. Switching Loss vs. Drain Current V_{DS} = 600 V

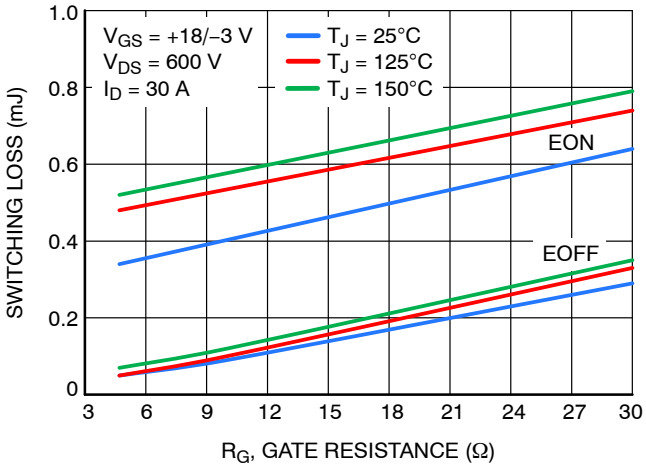


Figure 12. Switching Loss vs. Gate Resistance V_{DS} = 600 V

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TYPICAL CHARACTERISTICS M1/M2 SIC MOSFET CHARACTERISTIC

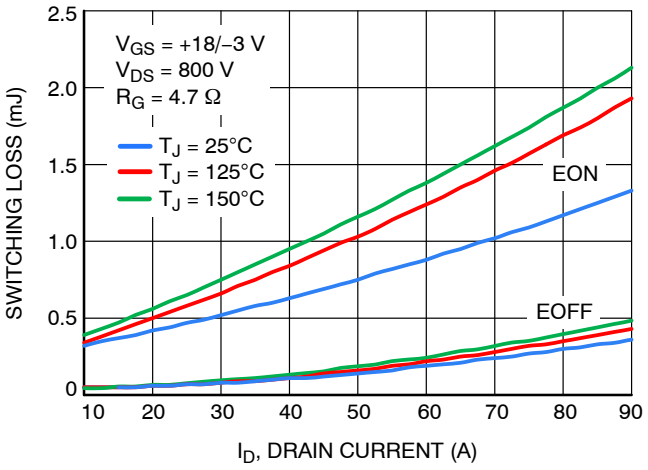


Figure 13. Switching Loss vs. Drain Current V_{DS} = 800 V

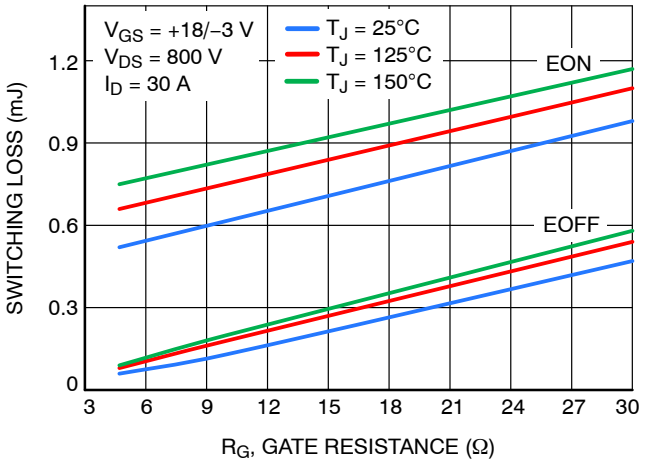


Figure 14. Switching Loss vs. Gate Resistance V_{DS} = 800 V

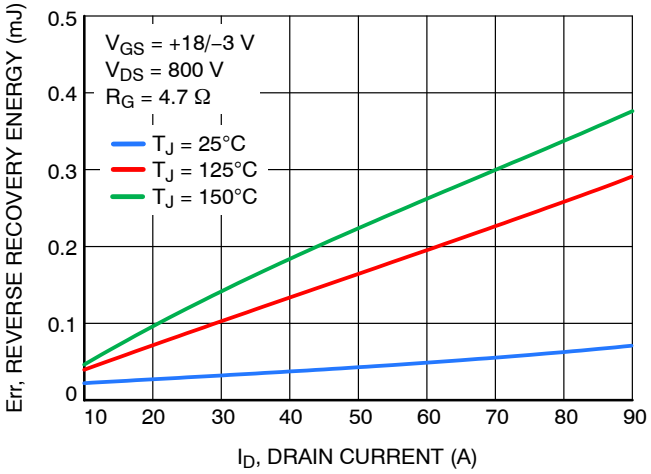


Figure 15. Reverse Recovery Energy vs. Drain Current V_{DS} = 800 V

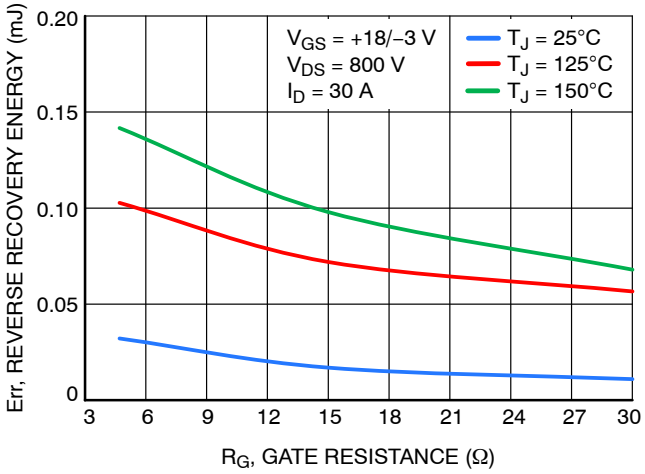


Figure 16. Reverse Recovery Energy vs. Gate Resistance V_{DS} = 800 V

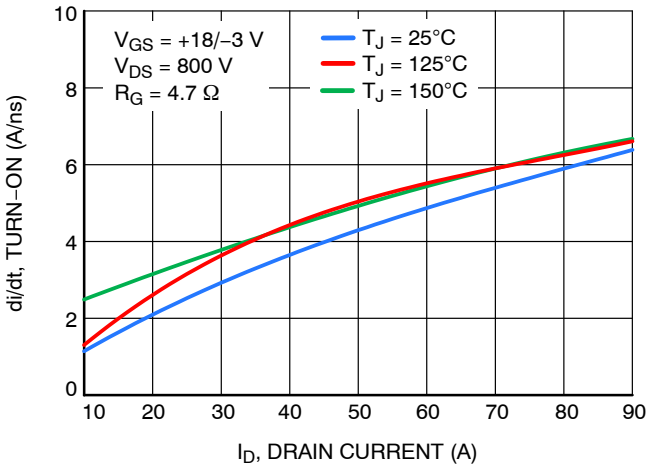


Figure 17. di/dt Turn ON vs. Drain Current V_{DS} = 800 V

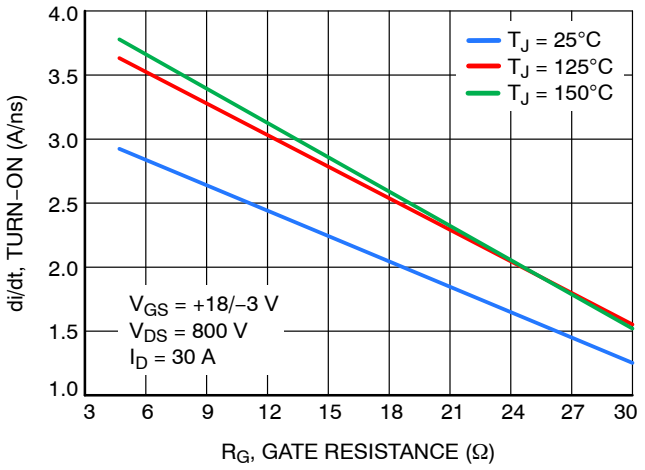


Figure 18. di/dt Turn ON vs. Gate Resistance V_{DS} = 800 V

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TYPICAL CHARACTERISTICS M1/M2 SIC MOSFET CHARACTERISTIC

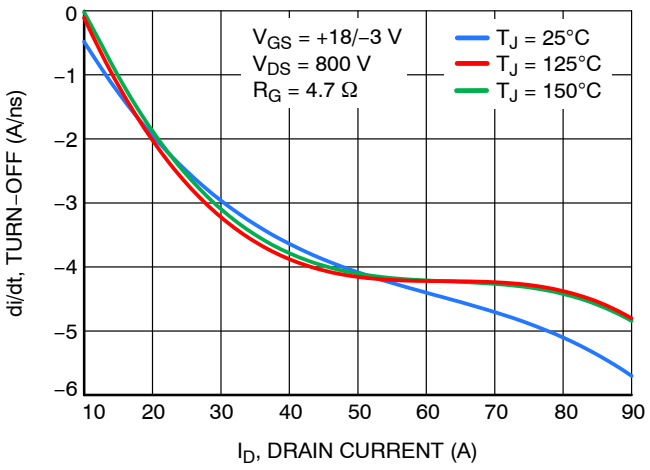


Figure 19. di/dt Turn OFF vs. Drain Current
V_{DS} = 800 V

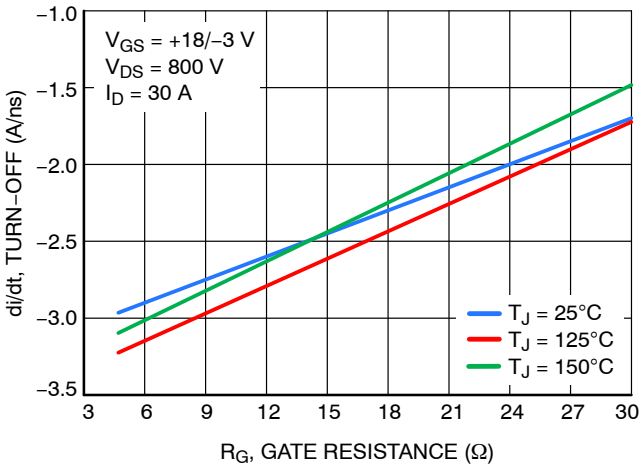


Figure 20. di/dt Turn OFF vs. Gate Resistance
V_{DS} = 800 V

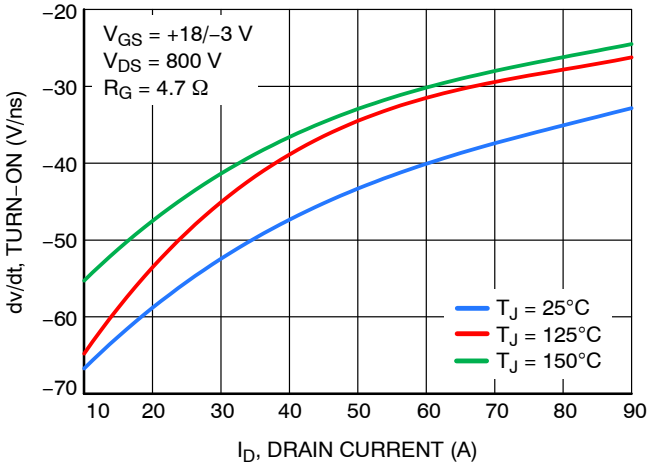


Figure 21. dv/dt Turn ON vs. Drain Current
V_{DS} = 800 V

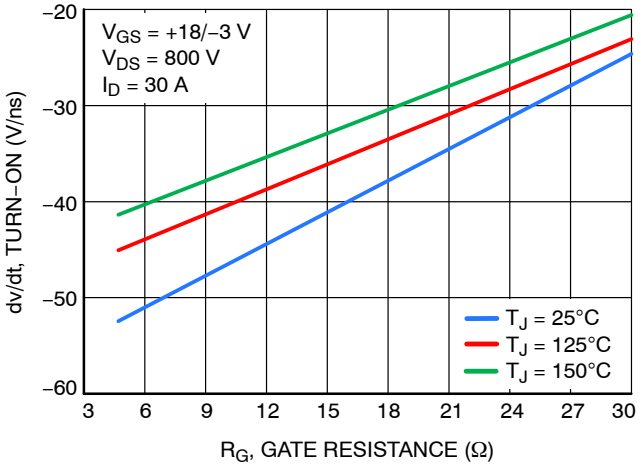


Figure 22. dv/dt Turn ON vs. Gate Resistance
V_{DS} = 800 V

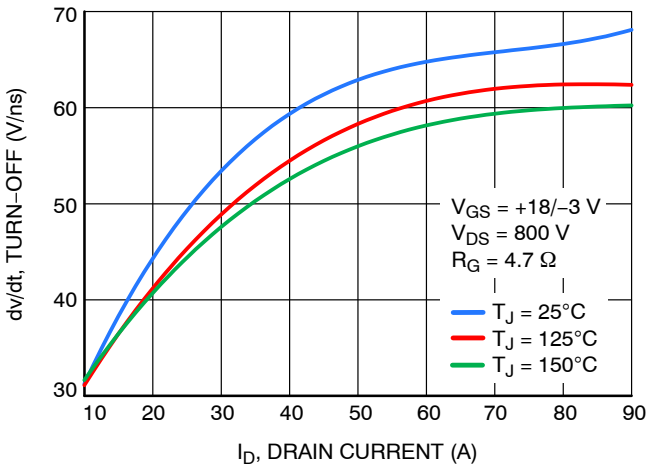


Figure 23. dv/dt Turn OFF vs. Drain Current
V_{DS} = 800 V

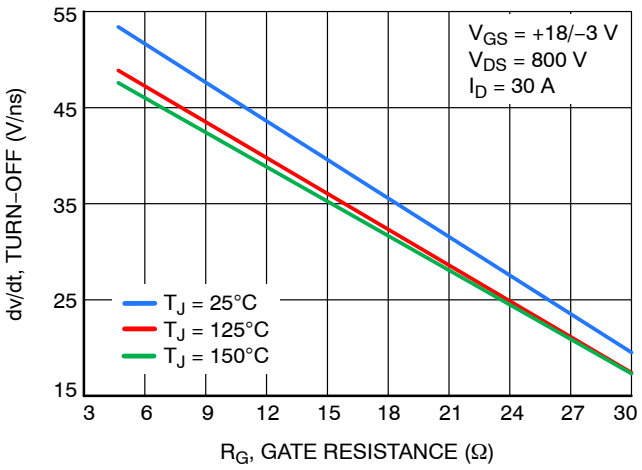


Figure 24. dv/dt Turn OFF vs. Gate Resistance
V_{DS} = 800 V

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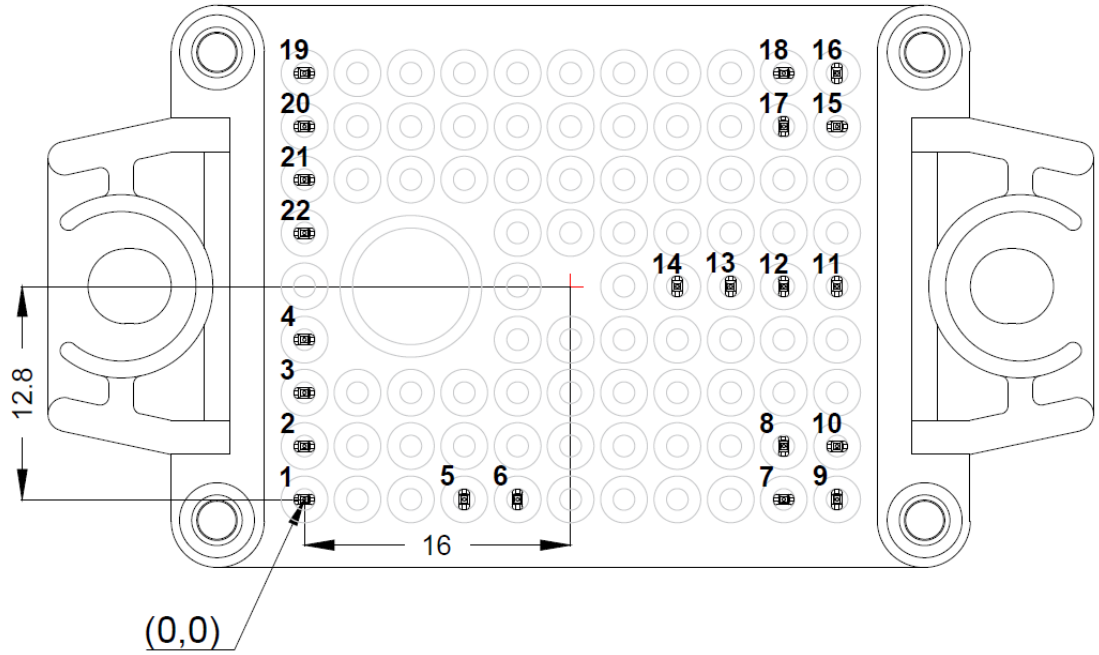
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Table 1. CAUER NETWORKS

Cauer Element #	Rth (K/W)	Cth (Ws/K)
1	0.0008598	0.0006888
2	0.0060273	0.0001577
3	0.0131590	0.0002630
4	0.0651160	0.0013257
5	0.1977800	0.0040903
6	0.3716200	0.0208140
7	0.1618000	0.5875200

PIN POSITION INFORMATION

scale = 2.5 : 1

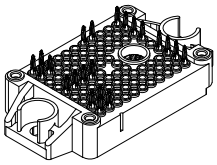


Pin position

Pin #	X	Y	Function	Pin #	X	Y	Function
1	0	0	AC2	12	28.8	12.8	DC+
2	0	3.2	AC2	13	25.6	12.8	DC+
3	0	6.4	S3	14	22.4	12.8	DC+
4	0	9.6	G3	15	32	22.4	DC-1
5	9.6	0	TH1	16	32	25.6	DC-1
6	12.8	0	TH2	17	28.8	22.4	G2
7	28.8	0	S4	18	28.8	25.6	S2
8	28.8	3.2	G4	19	0	25.6	AC1
9	32	0	DC-2	20	0	22.4	AC1
10	32	3.2	DC-2	21	0	19.2	S1
11	32	12.8	DC+	22	0	16	G1

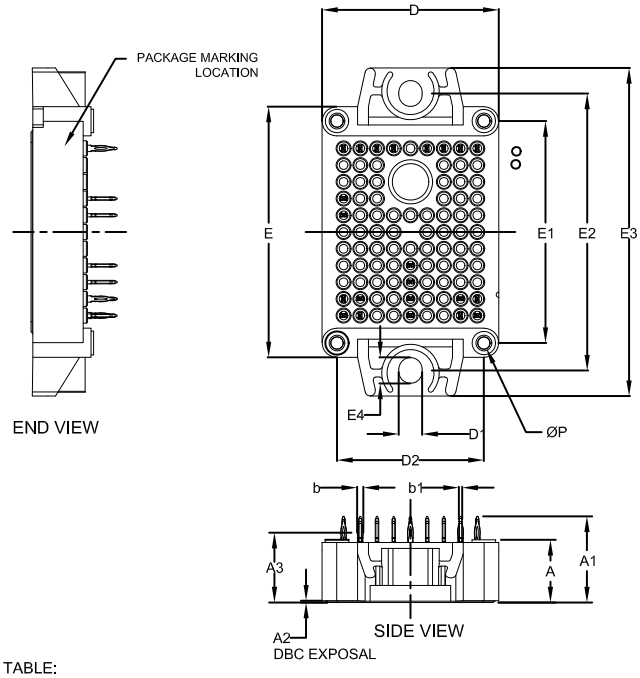
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PIM22 33.80x42.50x10.00
CASE 180HL
ISSUE O

DATE 29 AUG 2023

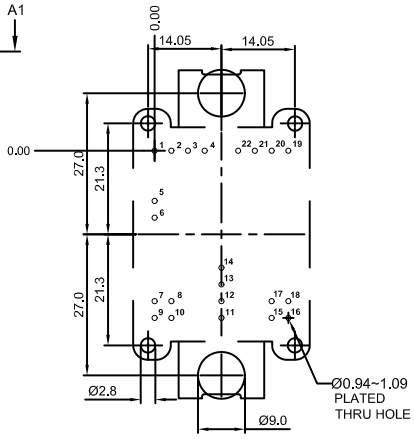


NOTES:
1. CONTROLLING DIMENSION: MILLIMETERS
2. PIN POSITION TOLERANCE IS ± 0.4mm
3. PRESS FIT PIN

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.65	12.00	12.35
A1	16.00	16.50	17.00
A2	0.00	0.35	0.60
A3	12.85	13.35	13.85
b	1.15	1.20	1.25
b1	0.59	0.64	0.69
D	33.50	33.80	34.10
D1	4.40	4.50	4.60
D2	27.95	28.10	28.25
E	47.70	48.00	48.30
E1	42.35	42.50	42.65
E2	52.90	53.00	53.10
E3	62.30	62.80	63.30
E4	4.90	5.00	5.10
P	2.20	2.30	2.40

PIN POSITION TABLE:

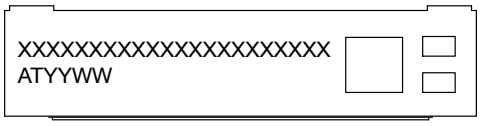
Pin	X	Y	Function	Pin	X	Y	Function
1	0	0	AC2	12	28.8	12.8	DC+
2	0	3.2	AC2	13	25.6	12.8	DC+
3	0	6.4	S3	14	22.4	12.8	DC+
4	0	9.6	G3	15	32	22.4	DC-1
5	9.6	0	TH1	16	32	25.6	DC-1
6	12.8	0	TH2	17	28.8	22.4	G2
7	28.8	0	S4	18	28.8	25.6	S2
8	28.8	3.2	G4	19	0	25.6	AC1
9	32	0	DC-2	20	0	22.4	AC1
10	32	3.2	DC-2	21	0	19.2	S1
11	32	12.8	DC+	22	0	16	G1



RECOMMENDED
MOUNTING PATTERN

* For additional Information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
AT = Assembly & Test Site Code
YYWW = Year and Work Week Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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