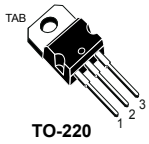
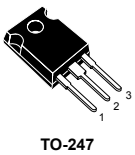
STP36N60M6, STW36N60M6

Datasheet

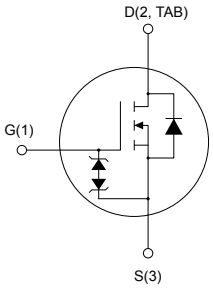
N-channel 600 V, 85 mΩ typ., 30 A MDmesh M6 Power MOSFETs in a TO-220 and TO-247 packages



TO-220



TO-247



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STPOWER

Product status links
STP36N60M6
STW36N60M6

Product summary	
Order code	**STP36N60M6**
Marking	36N60M6
Package	TO-220
Packing	Tube
Order code	**STW36N60M6**
Marking	36N60M6
Package	TO-247
Packing	Tube

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP36N60M6	600 V	99 mΩ	30 A
STW36N60M6			

- Reduced switching losses
- Lower $R_{DS(on)}$ per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

The new MDmesh M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	30	A
	Drain current (continuous) at T_C = 100 °C	19	
I_{DM}(1)	Drain current (pulsed)	102	A
P_{TOT}	Total power dissipation at T_C = 25 °C	208	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 30 A, di/dt ≤ 400 A/µs, V_{DS} (peak) < $V_{(BR)DSS}$, V_{DD} = 400 V.*
3. *V_{DD} ≤ 480 V.*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220	TO-247	
R_{thJC}	Thermal resistance, junction-to-case	0.6		°C/W
R_{thJA}	Thermal resistance junction-to-ambient	62.5	50	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max.)	5	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	750	mJ

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2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600	-	-	V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V	-	-	1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)	-	-	100	
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V	-	-	±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	I_D = 15 A, V_{GS} = 10 V	-	85	99	mΩ

1. *Specified by design, not tested in production.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1960	-	pF
C_{oss}	Output capacitance		-	93	-	pF
C_{rss}	Reverse transfer capacitance		-	6	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	332	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	1.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 30 A, V_{GS} = 0 to 10 V (see the Figure 16. Test circuit for gate charge behavior)	-	44.3	-	nC
Q_{gs}	Gate-source charge		-	10.1	-	nC
Q_{gd}	Gate-drain charge		-	25	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 15 A, R_G = 4.7 Ω, V_{GS} = 10 V (see the Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	15.2	-	ns
t_r	Rise time		-	5.3	-	ns
$t_{d(off)}$	Turn-off delay time		-	50.2	-	ns
t_f	Fall time		-	7.3	-	ns

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Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	-	30	A
I_{SDM}(1)	Source-drain current (pulsed)		-	-	102	A
V_{SD}(2)	Forward on voltage	I_{SD} = 30 A, V_{GS} = 0 V	-	-	1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 30 A, di/dt = 100 A/µs,	-	340	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V	-	5.3	-	µC
I_{RRM}	Reverse recovery current	(see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	31	-	A
t_{rr}	Reverse recovery time	I_{SD} = 30 A, di/dt = 100 A/µs,	-	430	-	ns
Q_{rr}	Reverse recovery charge	V_{DD} = 60 V, T_J = 150 °C	-	7.7	-	µC
I_{RRM}	Reverse recovery current	(see the Figure 17. Test circuit for inductive load switching and diode recovery times)	-	36	-	A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

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2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220

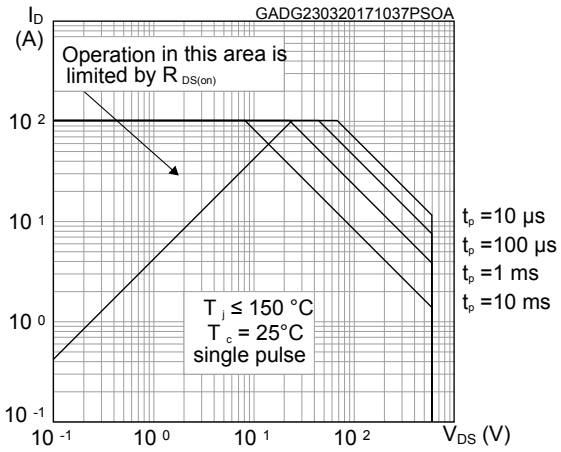

Figure 2. Normalized transient thermal impedance for TO-220

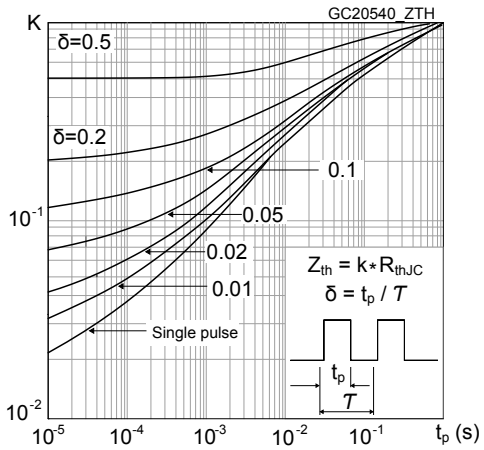

Figure 3. Safe operating area for TO-247

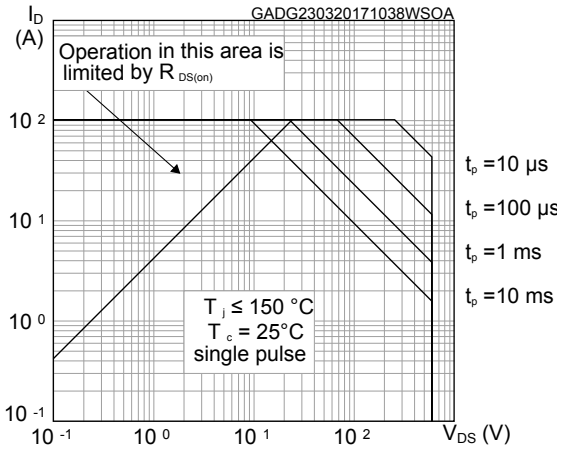

Figure 4. Normalized transient thermal impedance for TO-247

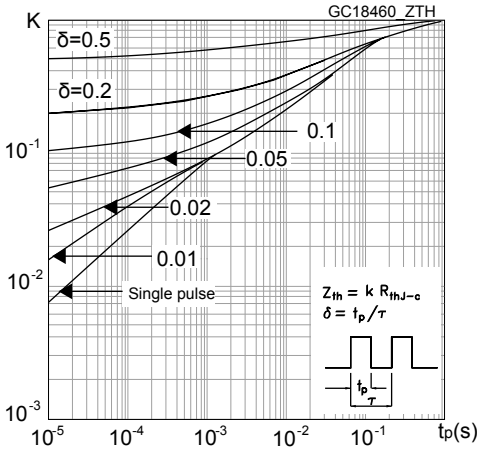

Figure 5. Typical output characteristics

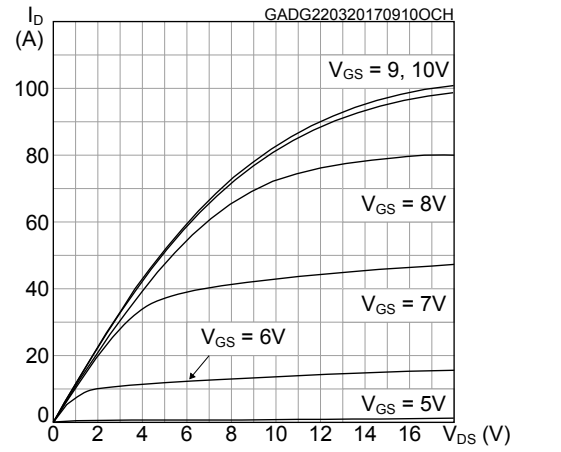

Figure 6. Typical transfer characteristics

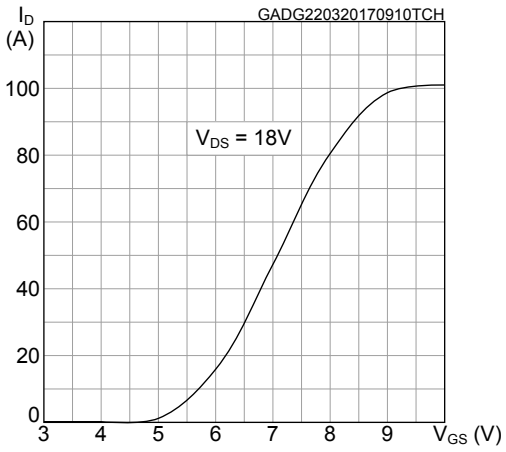

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Figure 7. Typical gate charge characteristics

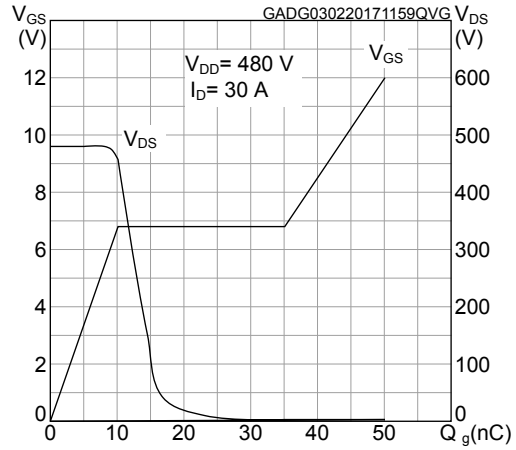

Figure 8. Typical drain-source on-resistance

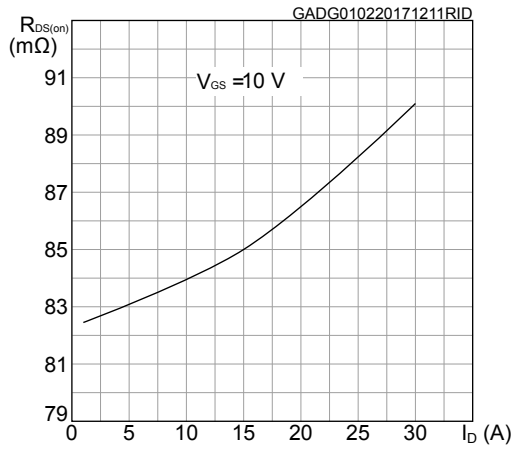

Figure 9. Typical capacitance characteristics

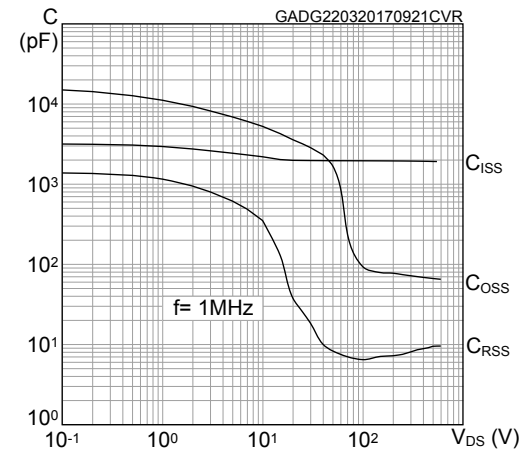

Figure 10. Normalized gate threshold vs temperature

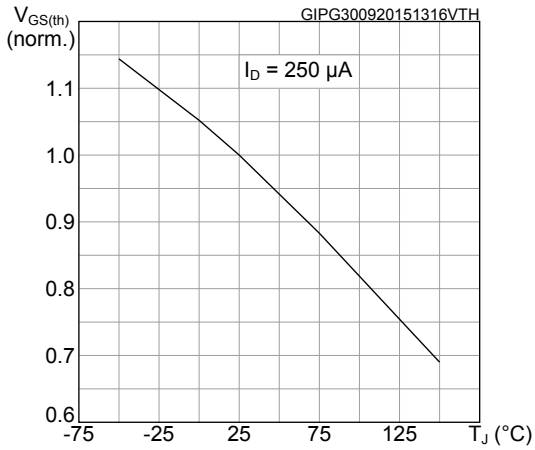

Figure 11. Normalized on-resistance vs temperature

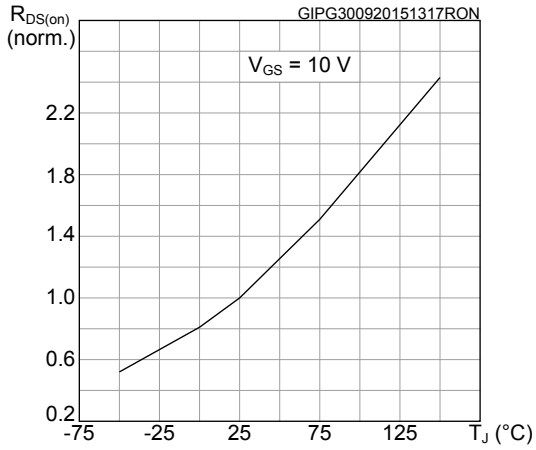

Figure 12. Normalized breakdown voltage vs temperature

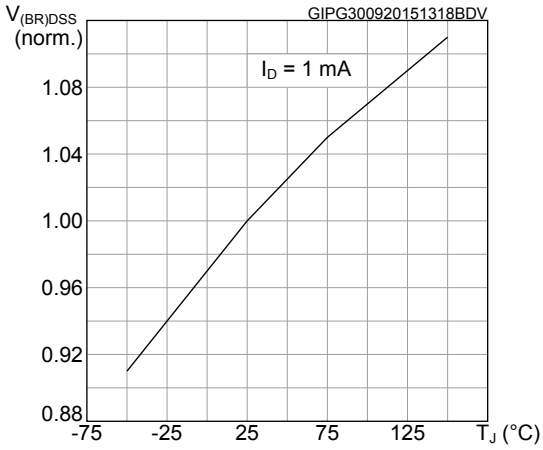

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Figure 13. Typical output capacitance stored energy

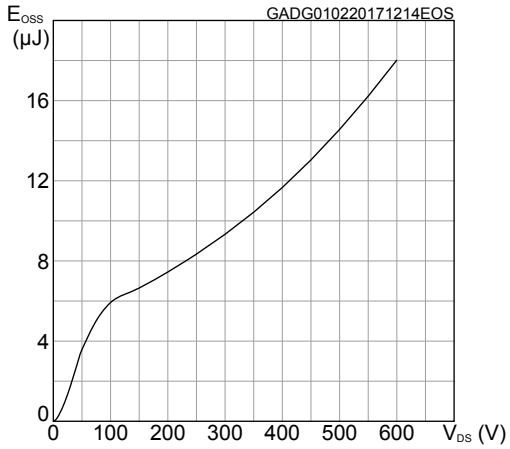
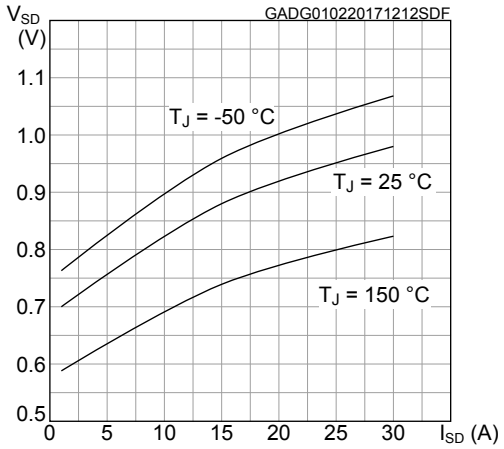


Figure 14. Typical reverse diode forward characteristics



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3 Test circuits

Figure 15. Test circuit for resistive load switching times

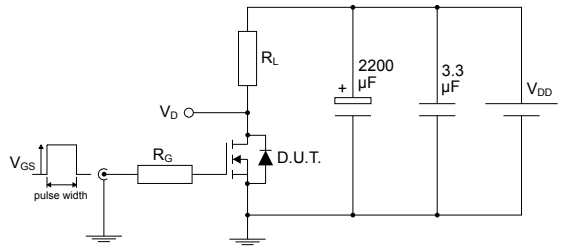

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Figure 16. Test circuit for gate charge behavior

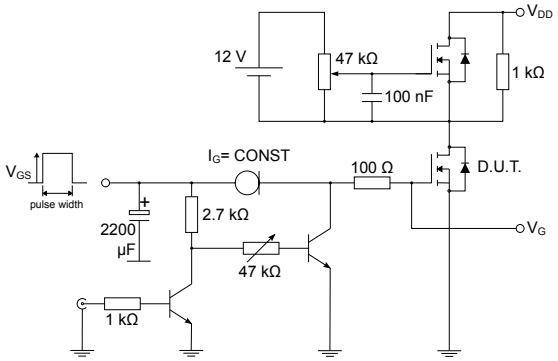

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Figure 17. Test circuit for inductive load switching and diode recovery times

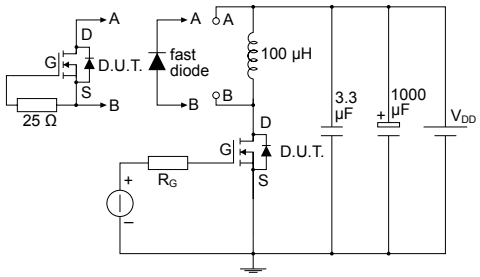

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Figure 18. Unclamped inductive load test circuit

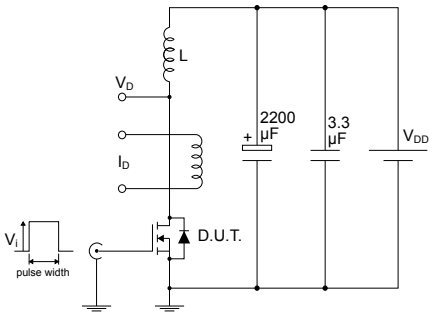

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Figure 19. Unclamped inductive waveform

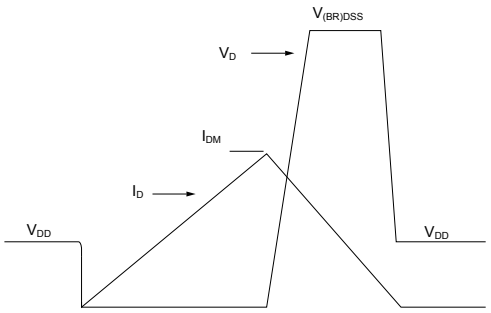

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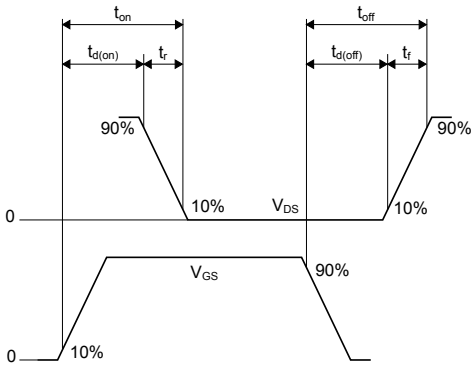
Figure 20. Switching time waveform



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4 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220 type A package information

Figure 21. TO-220 type A package outline

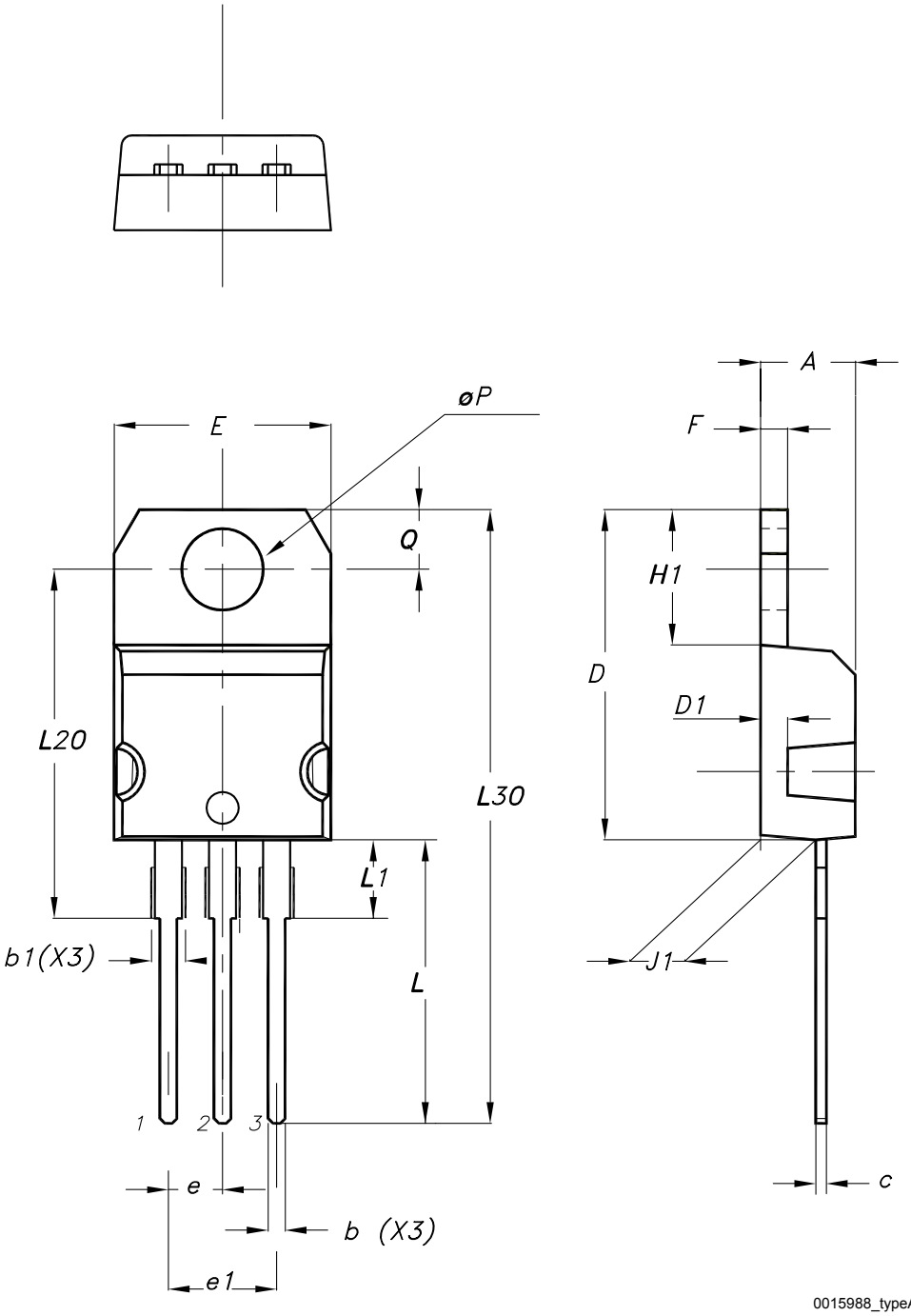

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Table 8. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

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4.2 TO-247 package information

Figure 22. **TO-247 package outline**

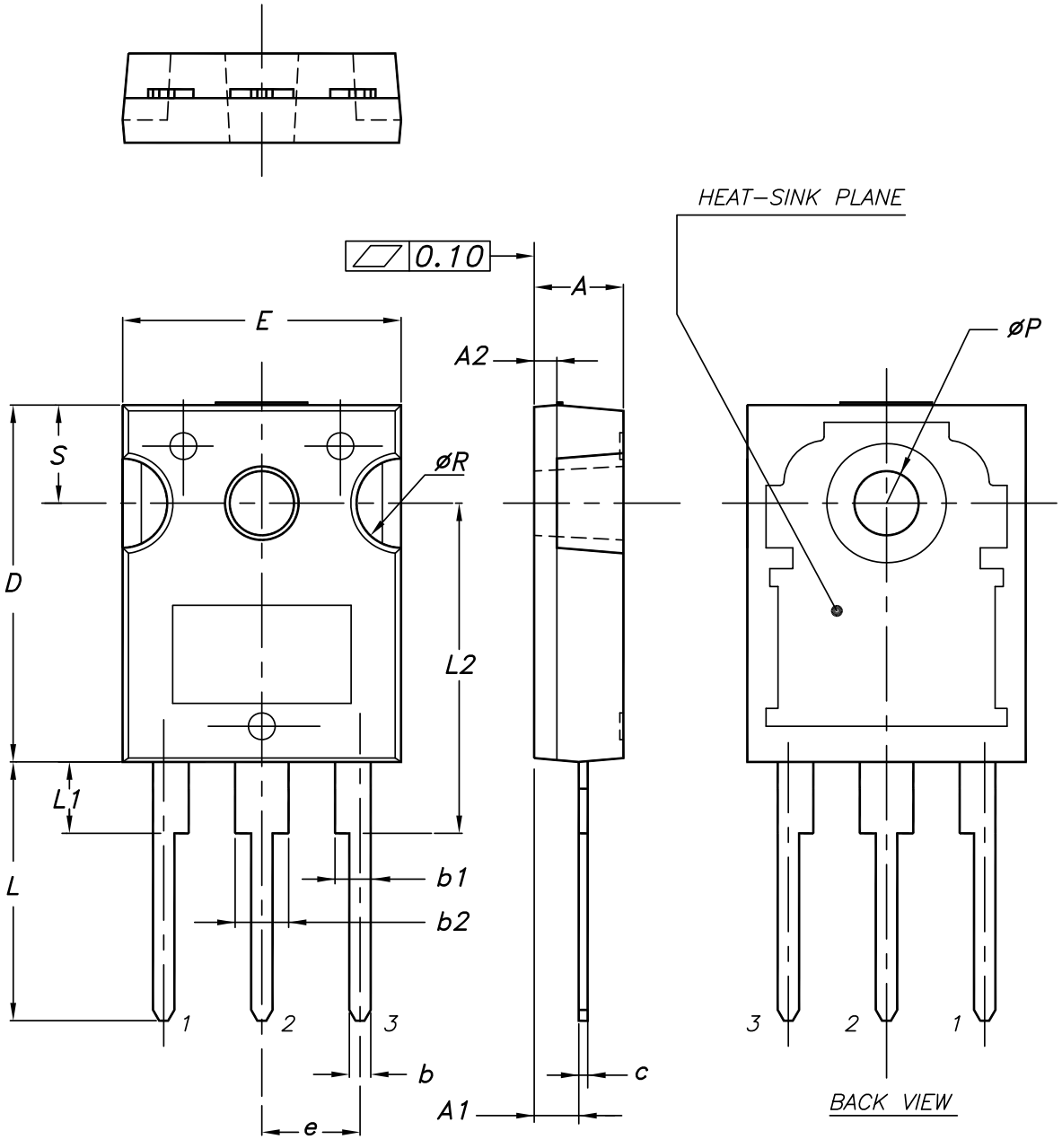

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Table 9. **TO-247 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
A2		1.27	
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

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Revision history

Table 10. **Document revision history**

Date	Version	Changes
06-Oct-2015	1	First release.
14-Oct-2015	2	Updated: V_{DD} value in *Table 8: "Source drain diode"*. Minor text changes.
27-Mar-2017	3	Updated *Table 2: "Absolute maximum ratings"*. Updated *Section 2: "Electrical characteristics"*. Updated *Section 4: "Package information"*. Minor text changes.
13-Jan-2026	4	Updated Section 4: Package information. Minor text changes.

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