REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add RHA data and radiation features. Change I_{CCH}, I_{CCL}, t_{OSLH}, and t_{OSHL} limits in table I. Add new output rise and fall time tests to table I. Modify figure 4 to include the new t_{RISE} and t_{FALL} tests. Update the boilerplate to remove classes B and S, and to reflect the changes required by MIL-PRF-38535. Editorial changes throughout. - TVN	03-02-12	Thomas M. Hess
B	Add radiation hardness assurance level F. - jak	03-09-22	Thomas M. Hess
C	Update boilerplate paragraphs to the current MIL-PRF-38535 requirements. - LTG	10-03-25	Thomas M. Hess
D	Add new device type 02 and SEP test limits in table IB. Add case outline X for device type 02 in section 1.2.4. Correct truth table in figure 2. - MAA	10-10-18	Thomas M. Hess

REV																				
SHEET																				
REV	D	D	D	D	D															
SHEET	15	16	17	18	19															

REV STATUS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Thomas J. Ricciuti

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
93-12-08

REVISION LEVEL
D

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, 1-TO-8 MINIMUM SKEW CLOCK DRIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-92174**

SHEET 1 OF 19

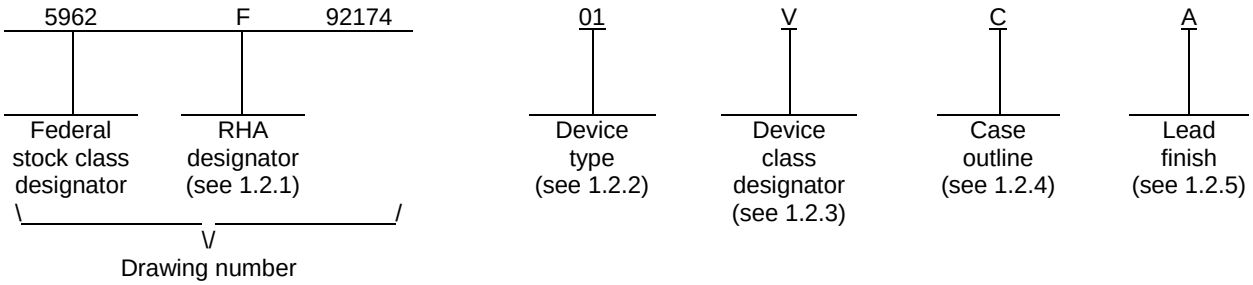
DSCC FORM 2233
APR 97

5962-E378-10

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54AC2525	1-to-8 minimum skew clock driver
02	AC2525	Radiation hardness, 1-to-8 minimum skew clock driver

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
X	CDFP3-F14	14	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC}) for device type 01	-0.5 V dc to +6.0 V dc
Supply voltage range (V_{CC}) for device type 02	-0.5 V dc to +7.0 V dc
Input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
Output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
DC input diode current (I_{IK}) (-0.5 V ≤ V_{IN} ≤ V_{CC} + 0.5 V)	±20 mA
DC output diode current (I_{OK}) (-0.5 V ≤ V_{OUT} ≤ V_{CC} + 0.5 V)	±20 mA
DC output current (I_{OUT}) (per output pin)	±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) (per pin)	±400 mA
Maximum power dissipation (P_D)	500 mW
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C 4/

1.4 Recommended operating conditions. 2/ 3/ 5/

Supply voltage range (V_{CC}):	
For device type 01	+3.0 V dc to +5.5 V dc
For device type 02	+2.0 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL}):	
at V_{CC} = 2.0 V dc (for device type 02 only)	0.61 V dc
at V_{CC} = 3.0 V dc	0.90 V dc
at V_{CC} = 3.6 V dc	1.08 V dc
at V_{CC} = 4.5 V dc	1.35 V dc
at V_{CC} = 5.5 V dc	1.65 V dc
Minimum high level input voltage (V_{IH}):	
at V_{CC} = 2.0 V dc (for device type 02 only)	1.4 V dc
at V_{CC} = 3.0 V dc	2.10 V dc
at V_{CC} = 3.6 V dc	2.52 V dc
at V_{CC} = 4.5 V dc	3.15 V dc
at V_{CC} = 5.5 V dc	3.85 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Minimum Input edge rate ($\Delta v/\Delta t$) (V_{IN} from 30% to 70% of V_{CC})	125 mV/ns
Maximum high level output current (I_{OH}):	
at V_{CC} = 3.0 V dc and 3.6 V dc	-12 mA
at V_{CC} = 4.5 V dc and 5.5 V dc	-24 mA
Maximum low level output current (I_{OL}):	
at V_{CC} = 3.0 V dc and 3.6 V dc	+12 mA
at V_{CC} = 4.5 V dc and 5.5 V dc	+24 mA

1.5 Radiation features.

Device type 01:	
Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	300 Krads (Si)
No Single Event Latch-up (SEL) at effective LET	≤ 100 MeV-cm^2/mg
Device type 02:	
Maximum total dose available (dose rate = 50 – 300 rads (Si)/s)	300 Krads (Si)
No Single Event Latch-up (SEL) at effective LET	≤ 110 MeV-cm^2/mg

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1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

5/ Operation from 2.0 V dc to 3.0 V dc are provided for compatibility with data retention and battery back up systems. Data retention implies no input transitions and no stored data loss with the following conditions: V_{IH} ≥ 70% of V_{CC}, V_{IL} ≤ 30% of V_{CC}, V_{OH} ≥ 70% of V_{CC} at –20 μA, V_{OL} ≤ 30% of V_{CC} at 20 μA.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from: ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXXX and 54/74ACTXXXXX Advanced High-Speed CMOS Devices.

EIA/JEDEC Standard No. 78 - IC Latch-Up Test.

(Copies of these documents are available online at http://www.jedec.org or from Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DLA Land and Maritime-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 37 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device type and device class 4/	V_{CC}	Group A subgroups	Limits 5/		Unit
							Min	Max	
High level output voltage 3006	V_{OH1}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10\ V$ $V_{IL} = 0.90\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$		All All	3.0 V	1, 2, 3	2.9		V
	V_{OH2}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$ $V_{IL} = 1.35\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$		All All	4.5 V	1, 2, 3	4.4		
	V_{OH3} 6/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$, $V_{IL} = 1.65\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$		All All	5.5 V	1, 2, 3	5.4		
			M, D, P, L, R, F	01, 02 V		1	5.4		
	V_{OH4}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10\ V$ $V_{IL} = 0.90\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -12\ mA$		All All	3.0 V	1, 2, 3	2.4		
	V_{OH5} 6/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$, $V_{IL} = 1.35\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$		All All	4.5 V	1, 2, 3	3.7		
			M, D, P, L, R, F	01, 02 V		1	3.7		
	V_{OH6}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$ $V_{IL} = 1.65\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -24\ mA$		All All	5.5 V	1, 2, 3	4.7		
	V_{OH7} 6/ 7/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$, $V_{IL} = 1.65\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ mA$		All All	5.5 V	1, 2, 3	3.85		
			M, D, P, L, R, F	01, 02 V		1	3.85		

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type and device class 4/	V_{CC}	Group A subgroups	Limits 5/		Unit
						Min	Max	
Low level output voltage 3007	V_{OL1}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10\ V$, $V_{IL} = 0.90\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ \mu A$	All All	3.0 V	1, 2, 3		0.1	V
	V_{OL2}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$, $V_{IL} = 1.35\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ \mu A$	All All	4.5 V	1, 2, 3		0.1	
	V_{OL3} 6/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$, $V_{IL} = 1.65\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ \mu A$	All All	5.5 V	1, 2, 3		0.1	
		M, D, P, L, R, F	01, 02 V		1		0.1	
	V_{OL4}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.10\ V$, $V_{IL} = 0.90\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 12\ mA$	All V	3.0 V	1, 3		0.4	
					2		0.5	
			All M		1		0.4	
					2, 3		0.5	
	V_{OL5} 6/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.15\ V$, $V_{IL} = 1.35\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 24\ mA$	All V	4.5 V	1, 3		0.4	
					2		0.5	
			All M		1		0.4	
					2, 3		0.5	
		M, D, P, L, R, F	01, 02 V		1		0.4	
	V_{OL6}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$, $V_{IL} = 1.65\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 24\ mA$	All V	5.5 V	1, 3		0.4	
					2		0.5	
			All M		1		0.4	
					2, 3		0.5	
	V_{OL7} 6/ 7/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 3.85\ V$, $V_{IL} = 1.65\ V$ For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 50\ mA$	All All	5.5 V	1, 2, 3		1.65	
		M, D, P, L, R, F	01, 02 V		1		1.65	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ -55°C ≤ T_C ≤ +125°C 3.0 V ≤ V_{CC} ≤ 5.5 V unless otherwise specified		Device type and device class 4/	V_{CC}	Group A subgroups	Limits 5/		Unit
							Min	Max	
Positive input clamp voltage 3022	V_{IC+} 6/	For input under test I_{IN} = 1 mA		All V	GND	1	0.4	1.5	V
			M, D, P, L, R, F	01, 02 V		1	0.4	1.5	
Negative input clamp voltage 3022	V_{IC-} 6/	For input under test I_{IN} = -1 mA		All V	Open	1	-0.4	-1.5	V
			M, D, P, L, R, F	01, 02 V		1	-0.4	-1.5	
Input current high 3010	I_{IH} 6/	For input under test V_{IN} = V_{CC} For all other inputs V_{IN} = V_{CC} or GND		All V	5.5 V	1		0.1	µA
						2, 3		1.0	
				All M		1		0.1	
						2, 3		1.0	
			M, D, P, L, R, F	01, 02 V		1		0.1	
Input current low 3009	I_{IL} 6/	For input under test V_{IN} = GND For all other inputs V_{IN} = V_{CC} or GND		All V	5.5 V	1		-0.1	µA
						2, 3		-1.0	
				All M		1		-0.1	
						2, 3		-1.0	
			M, D, P, L, R, F	01, 02 V		1		-0.1	
Quiescent supply current, output high 3005	I_{CCH} 6/	For all inputs V_{IN} = V_{CC} or GND		02 V	5.5 V	1		2	µA
						2, 3		40	
				All All		1		90	nA
						2, 3		80	µA
			M	01 V		1		50	µA
			D					200	
			P, L, R, F					700	
			M, D, P, L, R, F	02 V		1		50	µA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type and device class 4/	V_{CC}	Group A subgroups	Limits 5/		Unit
						Min	Max	
Quiescent supply current, output low 3005	I_{CCL} 6/	For all inputs $V_{IN} = V_{CC}$ or GND	02 V	5.5 V	1		2	µA
					2, 3		40	
			All All	5.5 V	1		90	nA
					2, 3		80	µA
		M	01 V	5.5 V	1		50	µA
		D					200	
		P, L, R, F					700	
		M, D, P, L, R, F	02 V	5.5 V	1		50	µA
Input capacitance 3012	C_{IN}	See 4.4.1c $T_C = +25°C$	All All	GND	4		10	pF
Power dissipation capacitance	C_{PD} 8/	For CK_{IN}: $f_{IN} = 1$ MHz $V_{IH} = V_{CC}$, V_{IL} = GND duty cycle = 50% See 4.4.1c, $T_C = +25°C$	All All	5.0 V	4		850	pF
Latch-up input/output over-voltage	I_{CC} (O/V1) 9/	$t_w \ge 100$ µs, $t_{cool} \ge t_w$ $5\ µs \le t_r \le 5$ ms, $5\ µs \le t_f \le 5$ ms $V_{test} = 6.0$ V, $V_{CCQ} = 5.5$ V $V_{over} = 10.5$ V	All V	5.5 V	2		200	mA
Latch-up input/output positive over-current	I_{CC} (O/I1+) 9/	$t_w \ge 100$ µs , $t_{cool} \ge t_w$ $5\ µs \le t_r \le 5$ ms, $5\ µs \le t_f \le 5$ ms $V_{test} = 6.0$ V, $V_{CCQ} = 5.5$ V $I_{trigger} = +120$ mA	All V	5.5 V	2		200	mA
Latch-up input/output negative over-current	I_{CC} (O/I1-) 9/	$t_w \ge 100$ µs, $t_{cool} \ge t_w$ $5\ µs \le t_r \le 5$ ms, $5\ µs \le t_f \le 5$ ms $V_{test} = 6.0$ V, $V_{CCQ} = 5.5$ V $I_{trigger} = -120$ mA	All V	5.5 V	2		200	mA
Latch-up supply over-voltage	I_{CC} (O/V2) 9/	$t_w \ge 100$ µs, $t_{cool} \ge t_w$ $5\ µs \le t_r \le 5$ ms, $5\ µs \le t_f \le 5$ ms $V_{test} = 6.0$ V, $V_{CCQ} = 5.5$ V $V_{over} = 9.0$ V	All V	5.5 V	2		100	mA
Truth table test output voltage 3014	6/ 10/	For all inputs, $V_{IN} = V_{IH}$ or V_{IL} Verify output V_O See 4.4.1d	02 V	2.0 V	7, 8	L	H	
			All All	3.0 V	7, 8	L	H	
		M, D, P, L, R, F	01, 02 V		7	L	H	
		For all inputs, $V_{IN} = V_{IH}$ or V_{IL} Verify output V_O See 4.4.1d	All All	4.5 V	7, 8	L	H	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $3.0\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Device type and device class 4/	V_{CC}	Group A subgroups	Limits 5/		Unit
							Min	Max	
Propagation delay time, clock to output, CKIN to Om 3003	t_{PLH1}, t_{PHL1} 6/ 11/	C_L = 50 pF minimum R_L = 500Ω See figure 4		02 V	2.0 V	9	1.0	12.0	ns
						10, 11	1.0	14.0	
					3.0 V	9	1.0	8.0	
						10, 11	1.0	9.5	
				01 All	3.0 V	9	4.0	9.5	
						10	5.0	11.0	
						11	3.0	8.5	
			M, D, P, L, R	01, V		9	4.0	9.5	
			F			9	4.0	10.5	
				02 V	4.5 V	9	1.0	7.0	
						10, 11	1.0	8.5	
				01 All	4.5 V	9	3.0	7.0	
						10	4.2	8.2	
						11	2.5	6.5	
			M, D, P, L, R	01, 02 V		9	3.0	7.0	
			F			9	3.0	8.5	
Common edge output skew time, Om to On 3003	t_{OSLH}, t_{OSHL} 12/	C_L = 50 pF minimum R_L = 500Ω See 4.4.1e See figure 4		All All	3.0 V	9		0.5	ns
						10, 11		0.6	
					4.5 V	9		0.5	
						10, 11		0.7	
Opposite edge output skew time, Om to On 3003	t_{OST} 12/			All All	3.0 V	9, 10, 11		1.5	ns
					4.5 V	9, 10, 11		1.0	
Pin skew time, Om 3003	t_{PS} 12/			All All	3.0 V	9, 10, 11		1.5	ns
					4.5 V	9, 10, 11		1.0	
Output rise and fall time, Om (20% to 80% of V_{CC}) 3004	t_{RISE1}, t_{FALL1}			All All	3.0 V	9, 11		4.0	ns
						10		5.0	
					4.5 V	9, 11		3.0	
						10		4.0	
Output rise and fall time, Om (20% to 80% of V_{CC}) 3004	t_{RISE2}, t_{FALL2} 13/	C_L = 14 pF min. or C_L = 50 pF R_L = 1000Ω or R_L = 500Ω See 4.4.1e See figure 4		All All	3.0 V	9, 10, 11		1.2	ns

See footnotes at next sheet.

TABLE IA. Electrical performance characteristics - Continued.

1/ For tests not listed in MIL-STD-883 [e.g. I_{CC}(O/V1)], utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:
   a. V_{IC} (pos) tests, the GND terminal can be open. T_C = +25°C.
   b. V_{IC} (neg) tests, the V_{CC} terminal shall be open. T_C = +25°C.
   c. All I_{CC} tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, R, and F of irradiation. However, these devices are only tested at the "F" level. Pre and post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

4/ The word "All" in the device type and device class column, means limits for all device types and classes.

5/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

6/ RHA sample do not have to be tested at -55°C and +125°C postirradiation.

7/ Transmission driving tests are performed at V_{CC} = 5.5 V dc with a 2 ms duration maximum. This test may be performed using V_{IN} = V_{CC} or GND. When V_{IN} = V_{CC} or GND is used, the test is guaranteed for V_{IN} = V_{IH} or V_{IL}.

8/ Power dissipation capacitance (C_{PD}) shall be tested by loading all outputs with a 50 pF minimum load capacitance (measure from output pin to GND) and conditioning CK_{IN} with the signal specified in table I, herein. The resulting I_{CC} current is then measured. C_{PD} is then calculated using the following equation:

$$C_{PD} = (I_{CCD} / (V_{CC} \times 10^6)) - 400 \text{ pF}$$

Where I_{CCD} is the I_{CC} measured.

Under the conditions specified in table I, herein, for CK_{IN} over frequencies (f) of 1 MHz to 100 MHz, C_{PD} is guaranteed to meet the limits calculated with the following equation: $C_{PD} = 850 \text{ pF} - (1.2 \times 10^{-18} \times f)$

C_{PD} determines both the power consumption (P_D) and current consumption (I_S). Where

$P_D = (C_{PD} + C_L)(V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L)V_{CC}f + I_{CC}$

For both P_D and I_S, f is the frequency of the input signal and C_L is the external output load capacitance.

9/ See EIA/JEDEC Standard No. 78 for electrically induced latch-up test methods and procedures. The values listed for $V_{trigger}$, $I_{trigger}$, and V_{over} are to be accurate within ± 5 percent.

10/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. For V_{CC} = 4.5 V and 5.5 V, H ≥ 2.5 V, L < 2.5 V. For V_{CC} = 3.0 V and 3.6 V, H ≥ 1.5 V, L < 1.5 V. For device classes Q and V, functional tests at V_{CC} = 3.0 V and 3.6 V are guaranteed, if not tested.

11/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. AC limits at V_{CC} = 3.6 V are equal to the limits at V_{CC} = 3.0 V and guaranteed by testing at V_{CC} = 3.0 V. Minimum ac limits for V_{CC} = 5.5 V and V_{CC} = 3.6 V are guaranteed by guard banding the minimum limits for testing at V_{CC} = 4.5 V and V_{CC} = 3.0 V, respectively, to 0.5 ns greater than the limits specified in table I, herein. For propagation delay tests, all paths must be tested.

12/ For skew parameters, t_{OSLH} is the absolute value of the difference between the t_{PLH} of an output Om and the t_{PLH} of any other output On; t_{OSHL} is the absolute value of the difference between the t_{PHL} of an output Om and the t_{PHL} of any other output On; t_{OST} is the absolute value of the difference between the maximum t_{PLH} of any output Om and the minimum t_{PHL} of any output On, and also the absolute value of the difference between the maximum t_{PHL} of any output Om and the minimum t_{PLH} of any output On; t_{PS} is the absolute value of the difference between the t_{PHL} and t_{PLH} of any output Om. The limits for t_{OST} specified in table I, herein, apply to either of the two test conditions for t_{OST} as described herein. For all skew parameters, m = 0 to 7; n = 0 to 7; and m is not equal to n.

13/ For t_{RISE2} and t_{FALL2} test of device type 01 (Class V) consider condition C_L = 14 pF(min) and R_L = 1000Ω, but device type 02 test condition consider C_L = 50 pF(min) and R_L = 500Ω.

TABLE IB. SEP test limits. 1/ 2/

Device Type	Bias for latch-up test V_{DD} = 5.5 V No latch-up at effective LET = 3/ 4/ [MeV-cm^2/mg]
01	LET = 100
02	LET = 110

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Tested at worst case temperature, T_A = +125°C ± 10°C for latch-up.
4/ Tested to an effective LET = 100 MeV-cm^2/mg for device type 01 and LET = 110 MeV-cm^2/mg for device type 02 with no latch-up (SEL).

Device type 01 and 02		
Case outlines	C, D and X	2
Terminal number	Terminal symbol	
1	O_0	NC
2	O_2	O_0
3	NC	O_2
4	GND	NC
5	V_{CC}	GND
6	O_4	NC
7	O_6	V_{CC}
8	O_7	NC
9	O_5	O_4
10	GND	O_6
11	V_{CC}	NC
12	CKIN	O_7
13	O_3	O_5
14	O_1	NC
15		GND
16		NC
17		V_{CC}
18		CKIN
19		O_3
20		O_1

NC = No internal connection

Terminal Description	
Terminal symbol	Description
CKIN	Clock Input
On (n = 0 to 7)	Outputs

FIGURE 1. Terminal connections.

Device type 01 and 02	
Inputs	Outputs 1/
CKIN	On
H L	H L

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

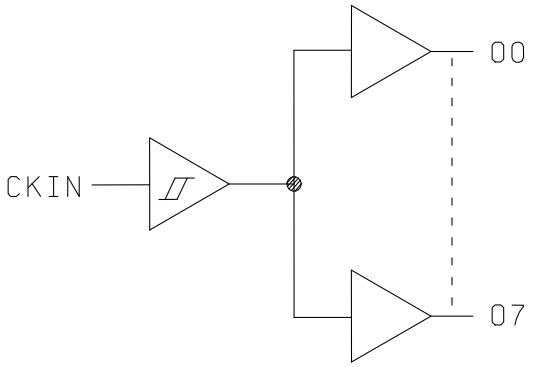
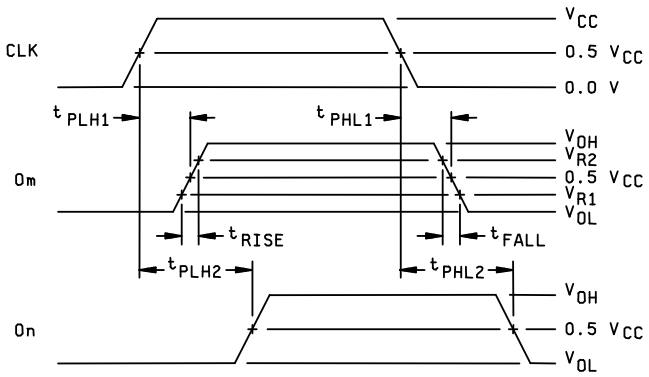
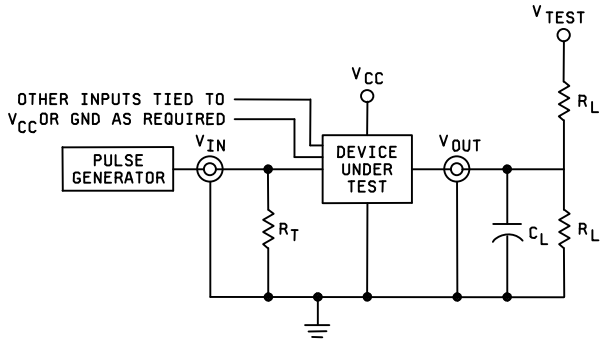


FIGURE 3. Logic diagram.



$t_{OSHL} = \left| t_{PHL1} - t_{PHL2} \right|$
$t_{OSLH} = \left| t_{PLH1} - t_{PLH2} \right|$
$t_{OST} = \left| t_{PHL1} - t_{PHL2} \right|$ and $\left| t_{PHL1} - t_{PLH2} \right|$
$t_{PS} = \left| t_{PHL1} - t_{PHL1} \right|$

t_{PHL1} and t_{PLH1} are the t_{PHL} and t_{PLH}, respectively, for the output under test, Om. t_{PHL2} and t_{PLH2} are the t_{PHL} and t_{PLH}, respectively, for any other output, On. Where m = 0 to 7, n = 0 to 7, and m is not equal to n.



NOTES:

1. When measuring t_{PLH}, t_{PHL}, t_{OSLH}, t_{OSHL}, t_{OST}, t_{PS}, t_{RISE1}, and t_{FALL1}: V_{TEST} = open; R_L = 500Ω or equivalent; C_L = 50 pF or equivalent (C_L includes test jig and probe capacitance).
2. When measuring t_{RISE2} and t_{FALL2}: $V_{TEST} = V_{CC}$; R_L = 1000Ω or equivalent; C_L = 14 pF or equivalent (C_L includes test jig and probe capacitance) for device type 01(class V), but for device type 02 test R_L = 500Ω or equivalent; C_L = 50 pF. All load circuit elements shall be within 0.5 inches from the output test pin.
3. V_{R1} = 20% of V_{CC}, V_{R2} = 80% of V_{CC} when measuring t_{RISE1} and t_{FALL1}.
4. V_{R1} = 20% of V_{CC}, V_{R2} = 80% of V_{CC} when measuring t_{RISE2} and t_{FALL2}.
5. Input signal from pulse generator: V_{IN} = 0.0 V to V_{CC}; PRR ≤ 10 MHz; $t_r \le 2.5$ ns; $t_f \le 2.5$ ns; t_r and t_f shall be measured from 10% of V_{CC} to 90% of V_{CC} and from 10% of V_{CC} to 90% of V_{CC}, respectively; duty cycle = 50 percent. For t_{OSHL}, t_{OSLH}, t_{OST}, t_{PS}, t_{RISE1}, t_{FALL1}, t_{RISE2}, and t_{FALL2}, PRR ≤ 100 MHz.
6. The t_{PHL} and t_{PLH} paramters shall be tested at a minimum input frequency of 1 MHz. The t_{OSHL}, t_{OSLH}, t_{OST}, t_{PS}, t_{RISE1}, and t_{FALL1} parameters shall be tested at a minimum input frequency of 50 MHz. The t_{RISE2} and t_{FALL2} parameters shall be tested at a minimum input frequency of 33.3 MHz.
7. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Latch-up and ground bounce tests are required for device classes Q and V. These tests shall be performed only for initial qualification and after process or design changes which may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up and ground-bounce tests, test all applicable pins on five devices with zero failures.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

d. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

e. The t_{OSHL}, t_{OSLH}, t_{OST}, t_{PS}, t_{RISE}, and t_{FALL} shall be measured only for initial qualification and after process or design changes which may affect dynamic performance. Test five devices at T_C = -55°C, +25°C, and +125°C with zero failures.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 3/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	3/ 1, 2, 3, 7,8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits, as specified in table III, shall be required the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE III. Burn-in and operating life test, delta parameters (+25°C).

Parameter 1/	Symbol	Device type	Delta Limits
Supply current	I_{CCH}, I_{CCL}	01	±100 nA 2/
		02	±150 nA
Input current	I_{IH}, I_{IL}	02	±20 nA
Output voltage low	V_{OL}	02	±0.04 V
Output voltage high	V_{OH}	02	±0.2 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine delta limits.
2/ The limit may not be production tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019, condition A, and as specified herein:

Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

1. Inputs tested high, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 5.0 V dc +5%, R_{IN} = 1 kΩ ±20%, and all outputs are open.
2. Inputs tested low, V_{CC} = 5.5 V dc +5%, R_{CC} = 10Ω ±20%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. When required by the customer, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process change which may affect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 micron in silicon.

e. The test temperature shall be +25°C for the upset measurements and the maximum rated operating temperature ±10°C for the latch-up measurements.

f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime -VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latch-up (SEP).

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 10-10-18

Approved sources of supply for SMD 5962-92174 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime -VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9217401MCA	0C7V7	54AC2525DMQB
5962-9217401MDA	0C7V7	54AC2525FMQB
5962-9217401M2A	0C7V7	54AC2525LMQB
5962R9217401VDA	3/	54AC2525WRQMLV
5962F9217401VDA	3/	54AC2525WFQMLV
5962F9217402VXC	F8859	RHFAC2525K01V
5962F9217402VXA	F8859	RHFAC2525K02V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051
F8859	ST Microelectronics 3 rue de Suisse BP4199 35041 RENNES cedex2 - France

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