MPC506A
MPC507A

SBFS018A – JANUARY 1988 – REVISED OCTOBER 2003

Single-Ended 16-Channel/Differential 8-Channel CMOS ANALOG MULTIPLEXERS

FEATURES

- **ANALOG OVERVOLTAGE PROTECTION: 70V_{PP}**
- **NO CHANNEL INTERACTION DURING OVERVOLTAGE**
- **BREAK-BEFORE-MAKE SWITCHING**
- **ANALOG SIGNAL RANGE: ±15V**
- **STANDBY POWER: 7.5mW typ**
- **TRUE SECOND SOURCE**

DESCRIPTION

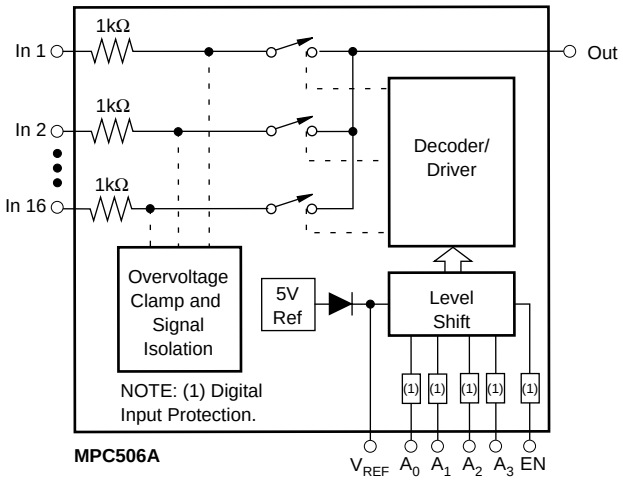
The MPC506A is a 16-channel single-ended analog multiplexer, and the MPC507A is an 8-channel differential multiplexer.

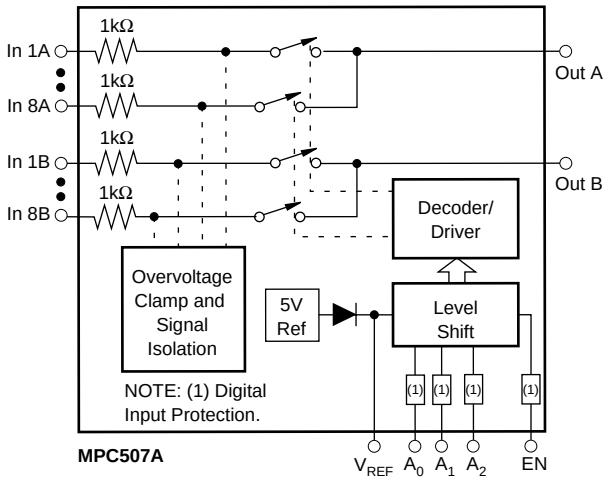
The MPC506A and MPC507A multiplexers have input overvoltage protection. Analog input voltages may exceed either power supply voltage without damaging the device or disturbing the signal path of other channels. The protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand 70V_{PP} signal levels and standard ESD tests. Signal sources are protected from short circuits should multiplexer power loss occur; each input presents a 1kΩ resistance under this condition. Digital inputs can also sustain continuous faults up to 4V greater than either supply voltage.

These features make the MPC506A and MPC507A ideal for use in systems where the analog signals originate from external equipment or separately powered sources.

The MPC506A and MPC507A are fabricated with Burr-Brown's dielectrically isolated CMOS technology. The multiplexers are available in plastic DIP and plastic SOIC packages. Temperature range is –40/+85°C.

FUNCTIONAL DIAGRAMS





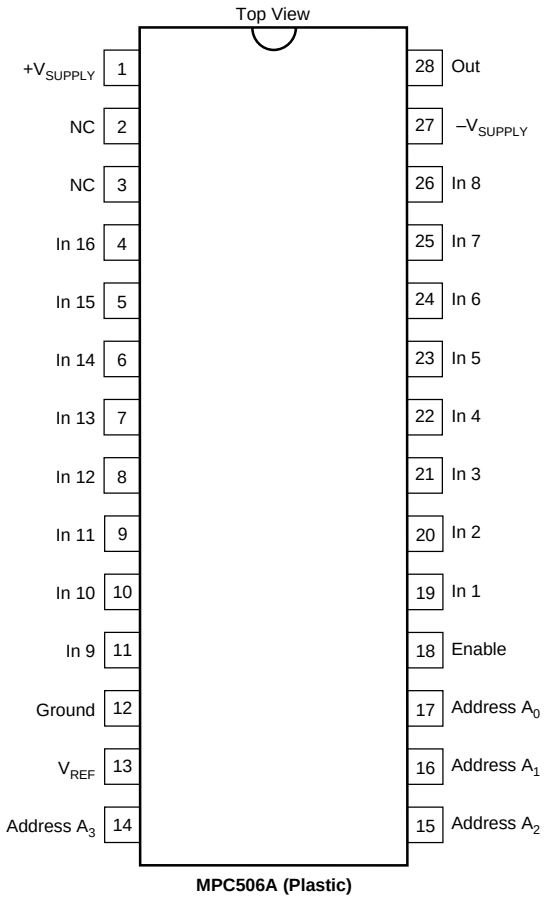
ELECTRICAL CHARACTERISTICS

Supplies = +15V, –15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V unless otherwise specified.

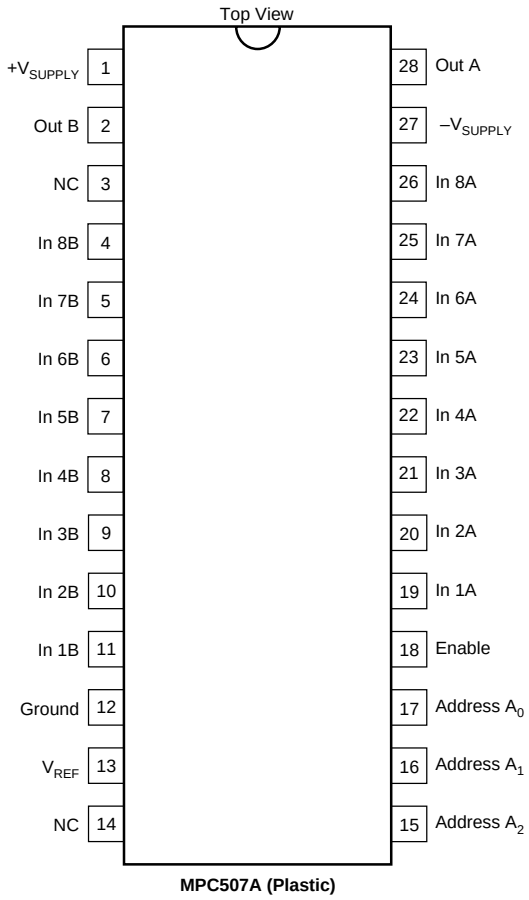
PARAMETER	TEMP	MPC506A/MPC507A MIN	MPC506A/MPC507A TYP	MPC506A/MPC507A MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS					
V_S, Analog Signal Range	Full	–15		+15	V
R_{ON}, On Resistance(1)	+25°C		1.3	1.5	kΩ
	Full		1.5	1.8	kΩ
I_S (OFF), Off Input Leakage Current	+25°C		0.5		nA
	Full			10	nA
I_D (OFF), Off Output Leakage Current	+25°C		0.2		nA
MPC506A	Full			5	nA
MPC507A	Full			5	nA
I_D (OFF) with Input Overvoltage Applied(2)	+25°C		2		µA
I_D (ON), On Channel Leakage Current	+25°C		2		nA
MPC506A	Full			10	nA
MPC507A	Full			10	nA
I_{DIFF} Differential Off Output Leakage Current (MPC507A Only)	Full			10	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold	Full			0.8	V
V_{AH}, Input High Threshold(3)	Full	4.0			V
V_{AL}, MOS Drive(4)	+25°C			0.8	V
V_{AH}, MOS Drive(4)	+25°C	6.0			V
I_A, Input Leakage Current (High or Low)(5)	Full			1.0	µA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		0.3		µs
	Full			0.6	µs
t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		200		ns
	Full			500	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		250		ns
	Full			500	ns
Settling Time (0.1%)	+25°C		1.2		µs
(0.01%)	+25°C		3.5		µs
"OFF Isolation"(6)	+25°C	50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5		pF
C_D (OFF), Channel Output Capacitance: MPC506A	+25°C		50		pF
MPC507A	+25°C		25		pF
C_A, Digital Input Capacitance	25°C		5		pF
C_{DS}, (OFF), Input to Output Capacitance	+25°C		0.1		pF
POWER REQUIREMENTS					
P_D, Power Dissipation	Full		7.5		mW
I+, Current Pin 1(7)	Full		0.7	1.5	mA
I–, Current Pin 27(7)	Full		5	20	µA

NOTES: (1) V_{OUT} = ±10V, I_{OUT} = –100µA. (2) Analog overvoltage = ±33V. (3) To drive from DTL/TTL circuits. 1kΩ pull-up resistors to +5.0V supply are recommended. (4) V_{REF} = +10V. (5) Digital input leakage is primarily due to the clamp diodes. Typical leakage is less than 1nA at 25°C. (6) V_{EN} = 0.8V, R_L = 1kΩ, C_L = 15pF, V_S = 7Vrms, f = 100kHz. Worst-case isolation occurs on channel 8 due to proximity of the output pins. (7) V_{EN}, V_A = 0V or 4.0V.

PIN CONFIGURATION



MPC506A (Plastic)



MPC507A (Plastic)

TRUTH TABLES

MPC506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

MPC507A

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

ABSOLUTE MAXIMUM RATINGS(1)

Voltage between supply pins 44V
V_{REF} to ground, V+ to ground 22V
V– to ground 25V
Digital input overvoltage:
V_{EN}, V_A: V_{SUPPLY} (+) ..... +4V
V_{SUPPLY} (–) ..... –4V
or 20mA, whichever occurs first.
Analog input overvoltage:
V_S: V_{SUPPLY} (+) ..... +20V
V_{SUPPLY} (–) ..... –20V
Continuous current, S or D 20mA
Peak current, S or D
(pulsed at 1ms, 10% duty cycle max) 40mA
Power dissipation* 2.0W
Operating temperature range ..... –40°C to +85°C
Storage temperature range ..... –65°C to +150°C

*Derate 20.0mW/°C above T_A = 70

NOTE: (1) Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.

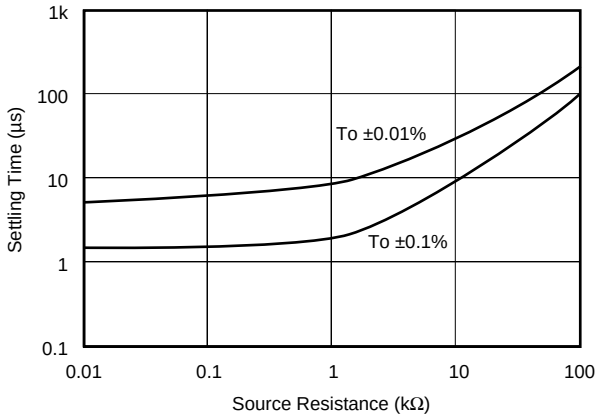
PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

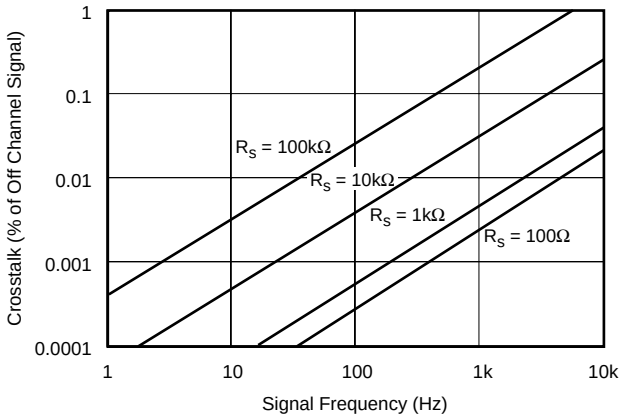
TYPICAL PERFORMANCE CURVES

T_A = +25°C unless otherwise noted.

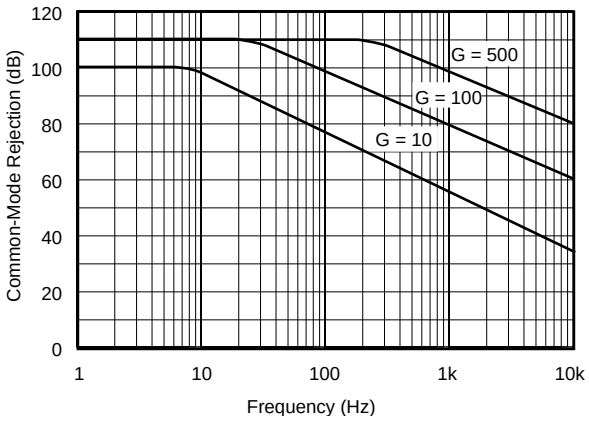
SETTLING TIME vs
SOURCE RESISTANCE FOR 20V STEP CHANGE



CROSSTALK vs SIGNAL FREQUENCY



COMBINED CMR vs
FREQUENCY MPC507A AND INA110



DISCUSSION OF SPECIFICATIONS

DC CHARACTERISTICS

The static or dc transfer accuracy of transmitting the multiplexer input voltage to the output depends on the channel ON resistance (R_{ON}), the load impedance, the source impedance, the load bias current and the multiplexer leakage current.

Single-Ended Multiplexer Static Accuracy

The major contributors to static transfer accuracy for single-ended multiplexers are:

Source resistance loading error
Multiplexer ON resistance error
dc offset error caused by both load bias current and multiplexer leakage current.

Resistive Loading Errors

The source and load impedances will determine the input resistive loading errors. To minimize these errors:

- *Keep loading impedance as high as possible.* This minimizes the resistive loading effects of the source resistance and multiplexer ON resistance. As a guideline, load impedance of $10^8\Omega$ or greater will keep resistive loading errors to 0.002% or less for 1000Ω source impedances. A $10^6\Omega$ load impedance will increase source loading error to 0.2% or more.
- *Use sources with impedances as low as possible.* A 1000Ω source resistance will present less than 0.001% loading error and 10kΩ source resistance will increase source loading error to 0.01% with a 10^8 load impedance.

Input resistive loading errors are determined by the following relationship (see Figure 1).

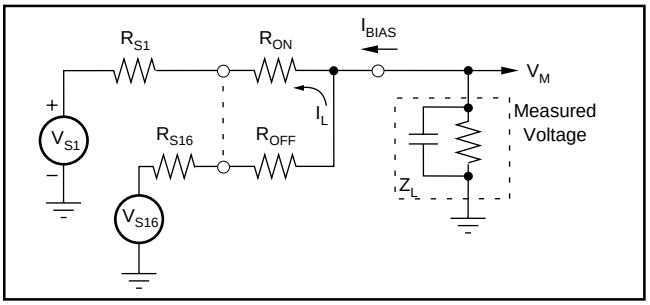


FIGURE 1. MPC506A Static Accuracy Equivalent Circuit.

Source and Multiplexer Resistive Loading Error

$$\in (R_S + R_{ON}) = \frac{R_S + R_{ON}}{R_S + R_{ON} + R_L} \times 100$$

where R_S = source resistance
R_L = load resistance
R_{ON} = multiplexer ON resistance

Input Offset Voltage

Bias current generates an input OFFSET voltage as a result of the IR drop across the multiplexer ON resistance and source resistance. A load bias current of 10nA will generate an offset voltage of 20µV if a 1kΩ source is used. In general, for the MPC506A, the OFFSET voltage at the output is determined by:

$$V_{OFFSET} = (I_B + I_L)(R_{ON} + R_S)$$

where I_B = Bias current of device multiplexer is driving
I_L = Multiplexer leakage current
R_{ON} = Multiplexer ON resistance
R_S = Source resistance

Differential Multiplexer Static Accuracy

Static accuracy errors in a differential multiplexer are difficult to control, especially when it is used for multiplexing low-level signals with full-scale ranges of 10mV to 100mV.

The matching properties of the multiplexer, source and output load play a very important part in determining the transfer accuracy of the multiplexer. The source impedance unbalance, common-mode impedance, load bias current mismatch, load differential impedance mismatch, and common-mode impedance of the load all contribute errors to the multiplexer. The multiplexer ON resistance mismatch, leakage current mismatch and ON resistance also contribute to differential errors.

Referring to Figure 2, the effects of these errors can be minimized by following the general guidelines described in this section, especially for low-level multiplexing applications.

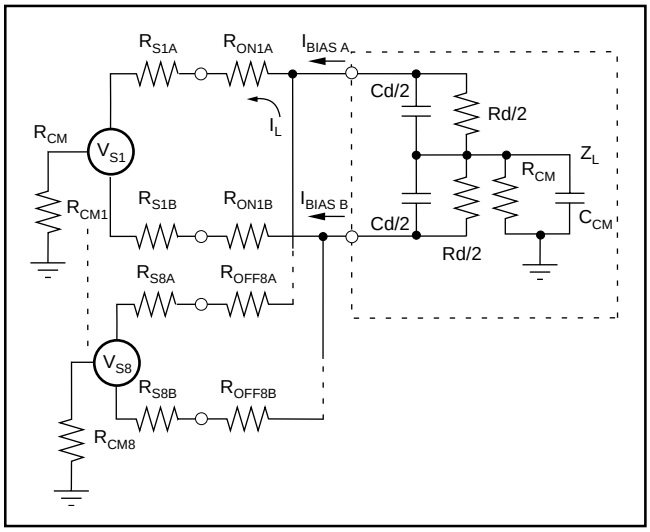


FIGURE 2. MPC507A Static Accuracy Equivalent Circuit.

Load (Output Device) Characteristics

- *Use devices with very low bias current.* Generally, FET input amplifiers should be used for low-level signals less than 50mV FSR. Low bias current bipolar input amplifiers are acceptable for signal ranges higher than 50mV FSR. Bias current matching will determine the input offset.
- The system dc common-mode rejection (CMR) can never be better than the combined CMR of the multiplexer and driven load. System CMR will be less than the device which has the lower CMR figure.
- Load impedances, differential and common-mode, should be $10^{10}\Omega$ or higher.

SOURCE CHARACTERISTICS

- The source impedance unbalance will produce offset, common-mode and channel-to-channel gain-scatter errors. Use sources which do not have large impedance unbalances if at all possible.
- Keep source impedances as low as possible to minimize resistive loading errors.
- Minimize ground loops. If signal lines are shielded, ground all shields to a common point at the system analog common.

If the MPC507A is used for multiplexing high-level signals of 1V to 10V full-scale ranges, the foregoing precautions should still be taken, but the parameters are not as critical as for low-level signal applications.

DYNAMIC CHARACTERISTICS

Settling Time

The gate-to-source and gate-to-drain capacitance of the CMOS FET switches, the RC time constants of the source and the load determine the settling time of the multiplexer.

Governed by the charge transfer relation i = C (dV/dt), the charge currents transferred to both load and source by the analog switches are determined by the amplitude and rise time of the signal driving the CMOS FET switches and the gate-to-drain and gate-to-source junction capacitances as shown in Figures 3 and 4. Using this relationship, one can see that the amplitude of the switching transients seen at the source and load decrease proportionally as the capacitance of the load and source increase. The trade-off for reduced switching transient amplitude is increased settling time. In effect, the amplitude of the transients seen at the source and load are:

$$dV_L = (i/C)\,dt$$

where i = C (dV/dt) of the CMOS FET switches

C = load or source capacitance

The source must then redistribute this charge, and the effect of source resistance on settling time is shown in the Typical Performance Curves. This graph shows the settling time for a 20V step change on the input. The settling time for smaller step changes on the input will be less than that shown in the curve.

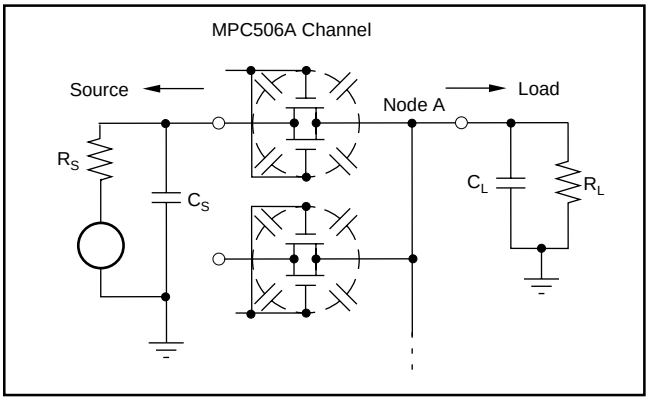


FIGURE 3. Settling Time Effects—MPC506A.

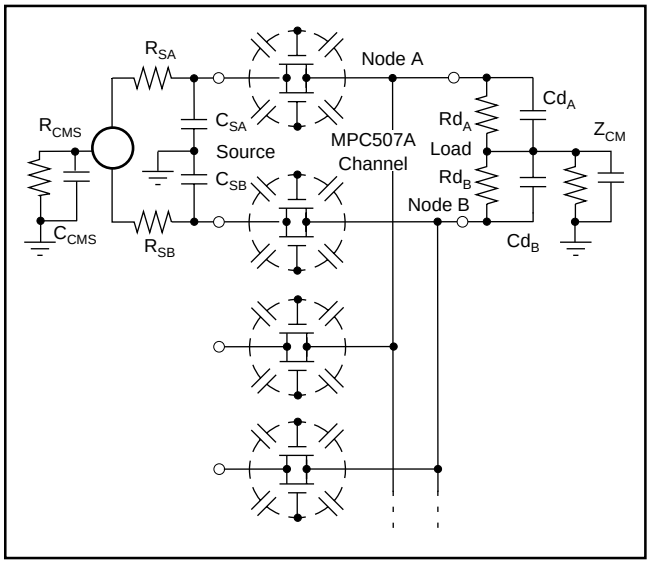


FIGURE 4. Settling and Common-Mode Effects—MPC507A

Switching Time

This is the time required for the CMOS FET to turn ON after a new digital code has been applied to the Channel Address inputs. It is measured from the 50 percent point of the address input signal to the 90 percent point of the analog signal seen at the output for a 10V signal change between channels.

Crosstalk

Crosstalk is the amount of signal feedthrough from the seven (MPC507A) or 15 (MPC506A) OFF channels appearing at the multiplexer output. Crosstalk is caused by the voltage divider effect of the OFF channel, OFF resistance and junction capacitances in series with the R_{ON} and R_S impedances of the ON channel. Crosstalk is measured with a 20Vp-p 1000Hz sine wave applied to all off channels. The crosstalk for these multiplexers is shown in the Typical Performance Curves.

Common-Mode Rejection (MPC507A Only)

The matching properties of the load, multiplexer and source affect the common-mode rejection (CMR) capability of a differentially multiplexed system. CMR is the ability of the multiplexer and input amplifier to reject signals that are common to both inputs, and to pass on only the signal difference to the output. For the MPC507A, protection is provided for common-mode signals of ±20V above the power supply voltages with no damage to the analog switches.

The CMR of the MPC507A and Burr-Brown's INA110 instrumentation amplifier (G = 100) is 110dB at DC to 10Hz with a 6dB/octave roll-off to 70dB at 1000Hz. This measurement of CMR is shown in the Typical Performance Curves and is made with a Burr-Brown INA110 instrumentation amplifier connected for gains of 500, 100, and 10.

Factors which will degrade multiplexer and system DC CMR are:

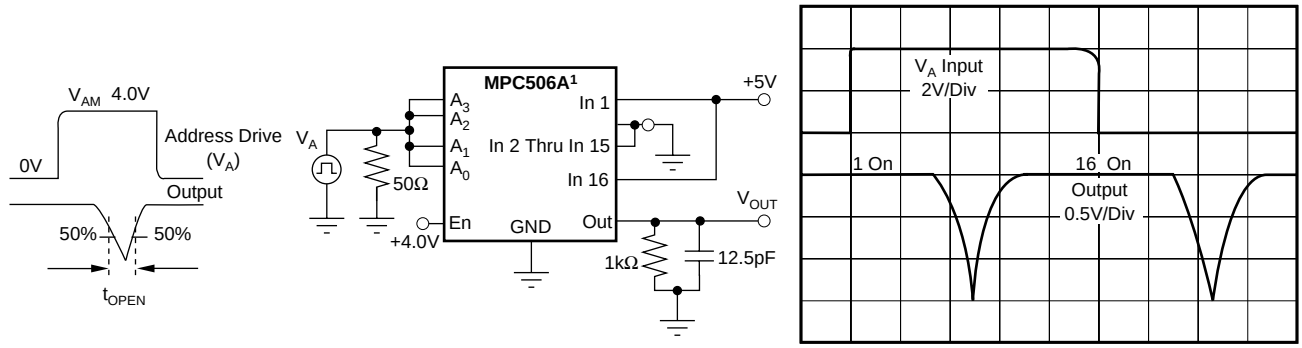
- Amplifier bias current and differential impedance mismatch
- Load impedance mismatch
- Multiplexer impedance and leakage current mismatch
- Load and source common-mode impedance

AC CMR roll-off is determined by the amount of common-mode capacitances (absolute and mismatch) from each signal line to ground. Larger capacitances will limit CMR at higher frequencies; thus, if good CMR is desired at higher frequencies, the common-mode capacitances and unbalance of signal lines and multiplexer to amplifier wiring must be minimized. Use twisted-shielded pair signal lines wherever possible.

SWITCHING WAVEFORMS

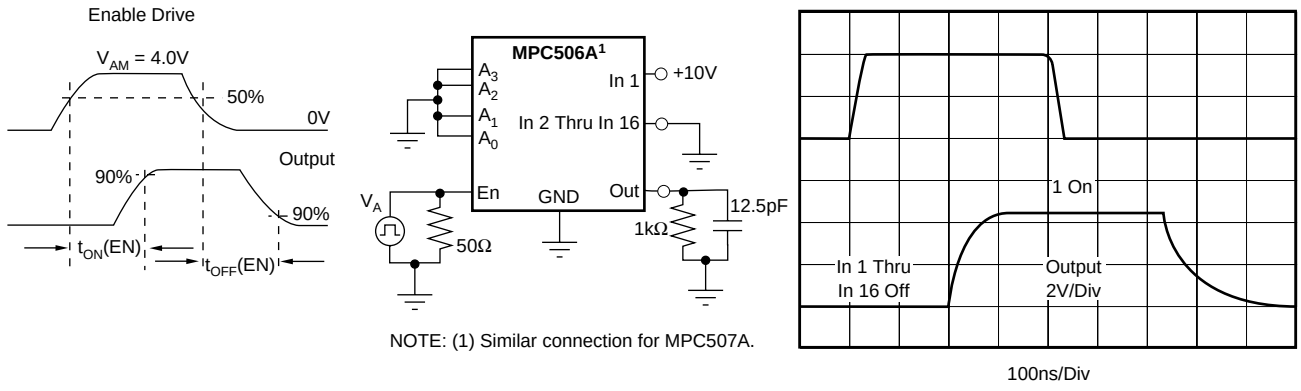
Typical at +25°C, unless otherwise noted.

BREAK-BEFORE-MAKE DELAY (t_{OPEN})



NOTE: (1) Similar connection for MPC507A.

ENABLE DELAY (t_{ON} (EN), t_{OFF} (EN))

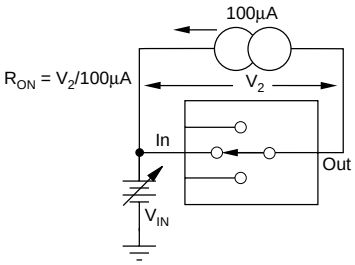


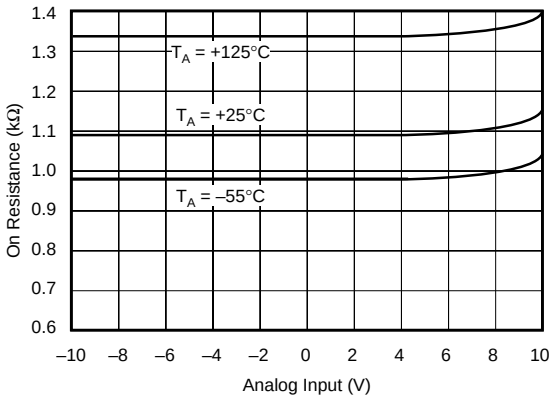
NOTE: (1) Similar connection for MPC507A.

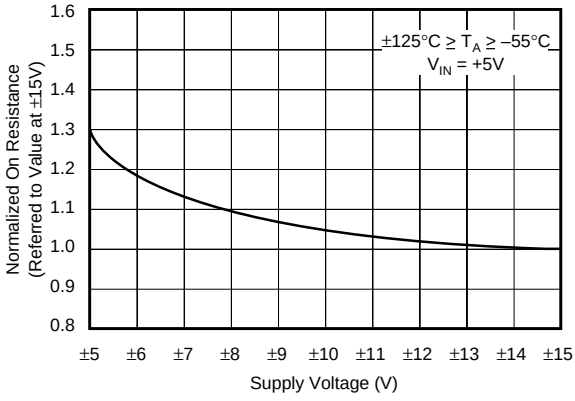
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

T_A = +25°C, V_S = ±15V, V_{AM} = +4V, V_{AL} = 0.8V and V_{REF} = Open, unless otherwise noted.

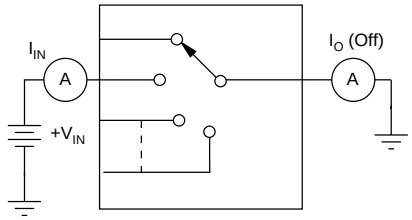
ON RESISTANCE vs INPUT SIGNAL, SUPPLY VOLTAGE

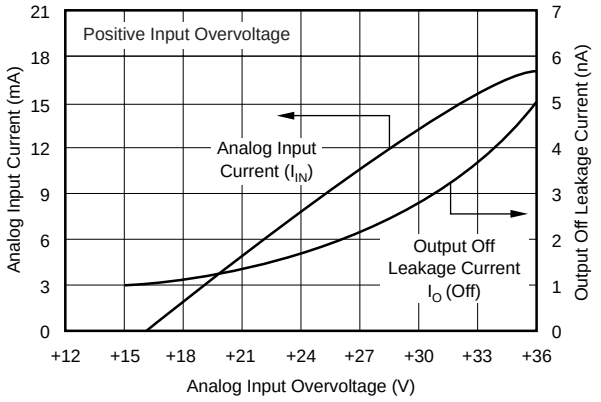


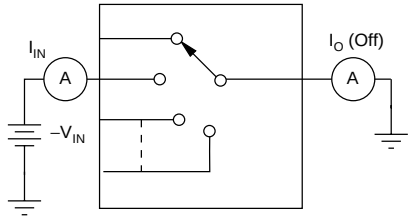


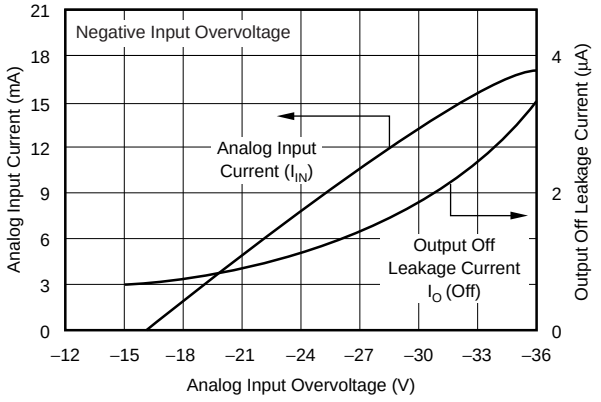


ANALOG INPUT OVERVOLTAGE CHARACTERISTICS





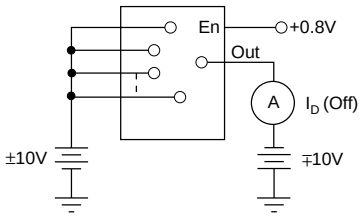


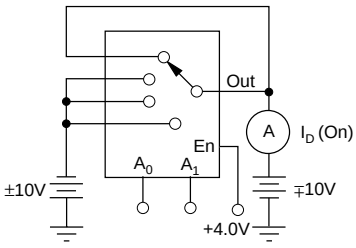


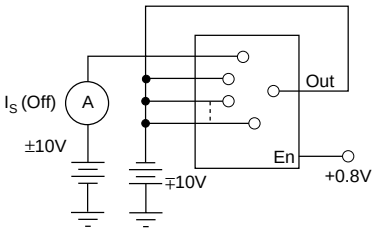
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

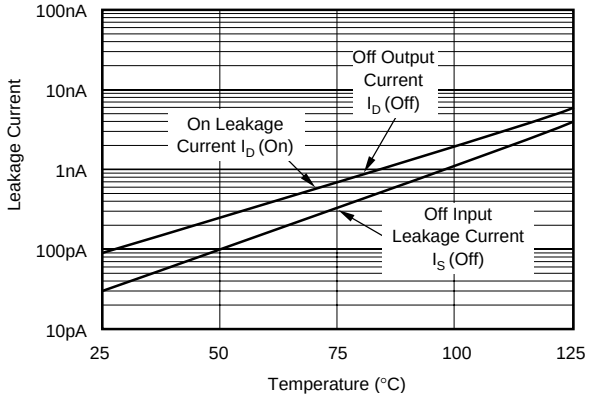
T_A = +25°C, V_S = ±15V, V_{AM} = +4V, V_{AL} = 0.8V and V_{REF} = Open, unless otherwise noted.

LEAKAGE CURRENT vs TEMPERATURE



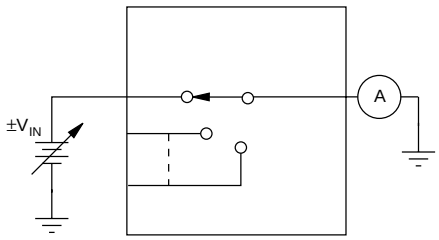


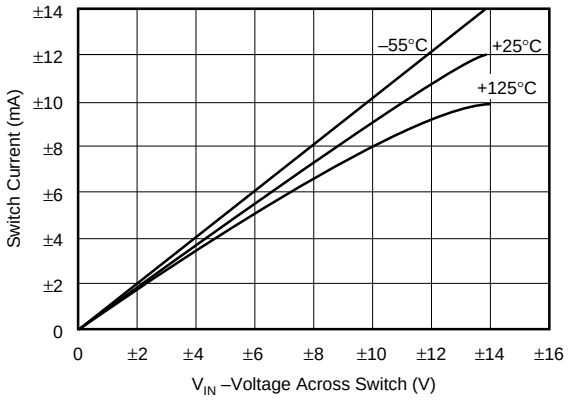




NOTE: (1) Two measurements per channel: +10V/–10V and –10V/+10V. (Two measurements per device for I_D (Off): +10V/–10V and –10V/+10V).

ON-CHANNEL CURRENT vs VOLTAGE

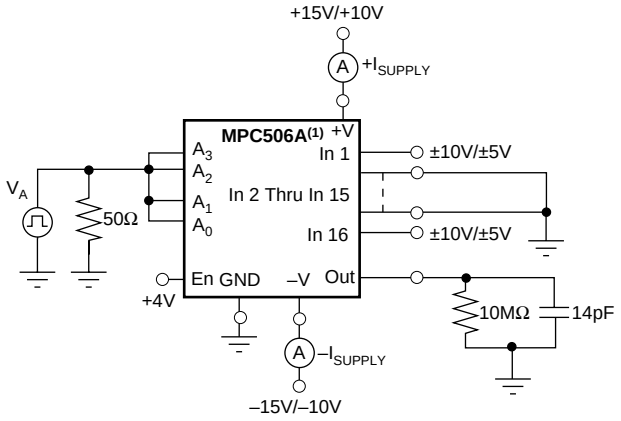




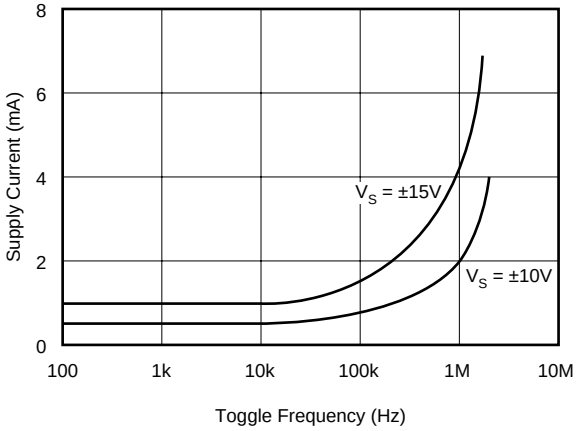
PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS (CONT)

T_A = +25°C, V_S = ±15V, V_{AM} = +4V, V_{AL} = 0.8V and V_{REF} = Open, unless otherwise noted.

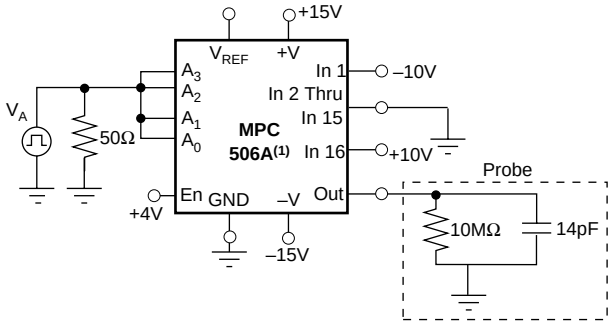
SUPPLY CURRENT vs TOGGLE FREQUENCY



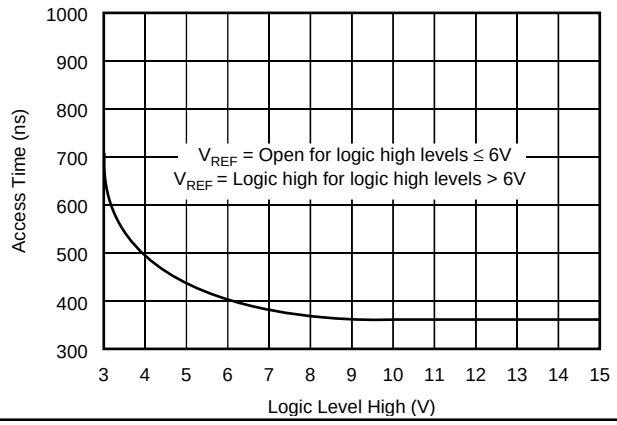
NOTE: (1) Similar connection for MPC507A.



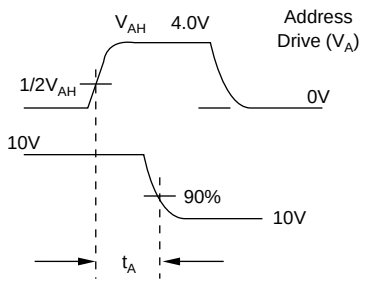
ACCESS TIME vs LOGIC LEVEL (High)

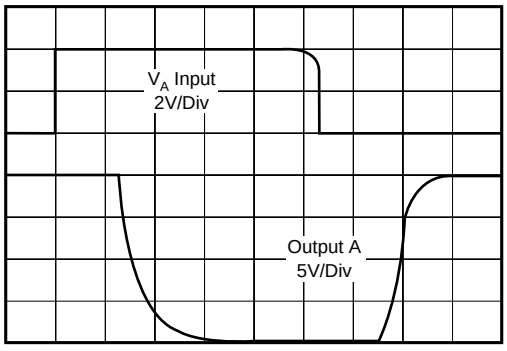


NOTE: (1) Similar connection for MPC507A.



ACCESS TIME WAVEFORM





INSTALLATION AND OPERATING INSTRUCTIONS

The ENABLE input, pin 18, is included for expansion of the number of channels on a single node as illustrated in Figure 5. With ENABLE line at a logic 1, the channel is selected by the 3-bit (MPC507A or 4-bit MPC506A) Channel Select Address (shown in the Truth Tables). If ENABLE is at logic 0, all channels are turned OFF, even if the Channel Address Lines are active. If the ENABLE line is not to be used, simply tie it to +V supply.

If the +15V and/or –15V supply voltage is absent or shorted to ground, the MPC507A and MPC506A multiplexers will not be damaged; however, some signal feedthrough to the output will occur. Total package power dissipation must not be exceeded.

For best settling speed, the input wiring and interconnections between multiplexer output and driven devices should be kept as short as possible. When driving the digital inputs from TTL, open collector output with pull up resistors are recommended (see Typical Performance Curves, Access Time).

To preserve common-mode rejection of the MPC507A, use twisted-shielded pair wire for signal lines and inter-tier connections and/or multiplexer output lines. This will help common-mode capacitance balance and reduce stray signal pickup. If shields are used, all shields should be connected as close as possible to system analog common or to the common-mode guard driver.

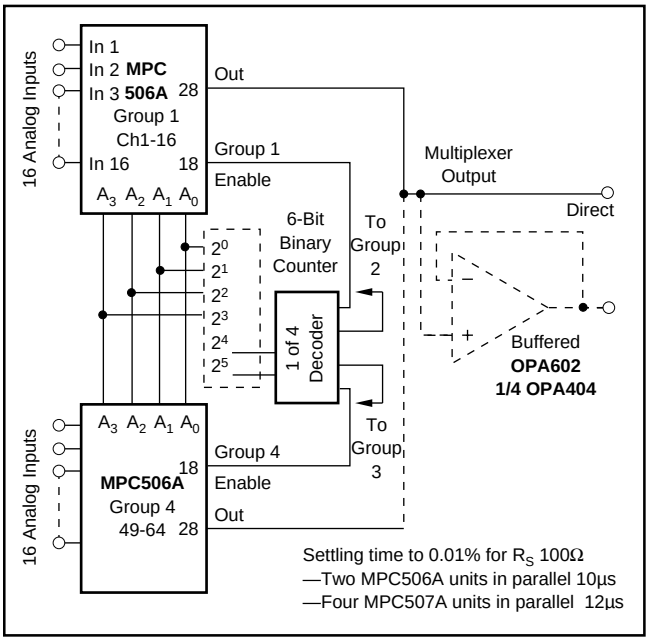


FIGURE 5. 64-Channel, Single-Tier Expansion.

CHANNEL EXPANSION

Single-Ended Multiplexer (MPC506A)

Up to 64 channels (four multiplexers) can be connected to a single node, or up to 256 channels using 17 MPC506A multiplexers on a two-tiered structure as shown in Figures 5 and 6.

Differential Multiplexer (MPC507A)

Single or multitiered configurations can be used to expand multiplexer channel capacity up to 64 channels using a 64 x 1 or an 8 x 8 configuration.

Single-Node Expansion

The 64 x 1 configuration is simply eight (MPC507A) units tied to a single node. Programming is accomplished with a 6-bit counter, using the 3LSBs of the counter to control Channel Address inputs A_0, A_1, A_2 and the 3MSBs of the counter to drive a 1-of-8 decoder. The 1-of-8 decoder then is used to drive the ENABLE inputs (pin 18) of the MPC507A multiplexers.

Two-Tier Expansion

Using an 8 x 8 two-tier structure for expansion to 64 channels, the programming is simplified. The 6-bit counter output does not require a 1-of-8 decoder. The 3LSBs of the counter drive the A_0, A_1 and A_2 inputs of the eight first-tier multiplexers and the 3MSBs of the counter are applied to the A_0, A_1, and A_2 inputs of the second-tier multiplexer.

Single vs Multitiered Channel Expansion

In addition to reducing programming complexity, two-tier configuration offers the added advantages over single-node expansion of reduced OFF channel current leakage (reduced OFFSET), better CMR, and a more reliable configuration if a channel should fail ON in the single-node configuration, data cannot be taken from any channel, whereas only one channel group is failed (8 or 16) in the multitiered configuration.

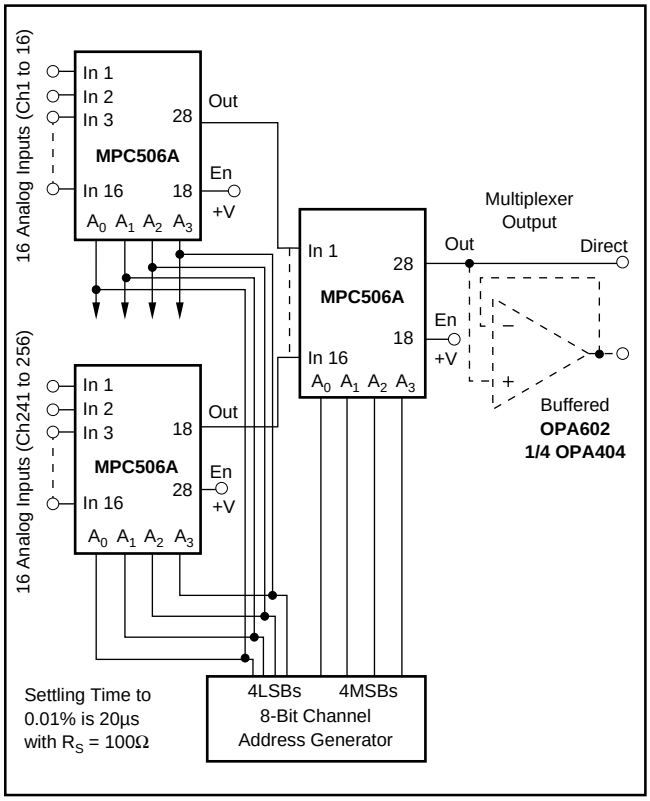


FIGURE 6. Channel Expansion up to 256 Channels Using 16x16 Two-Tiered Expansion

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MPC506AU	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MPC506AU	Samples
MPC506AU/1K	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		MPC506AU	Samples
MPC506AUG4	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MPC506AU	Samples
MPC507AU	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MPC507AU	Samples
MPC507AU/1K	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MPC507AU	Samples
MPC507AUG4	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	MPC507AU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

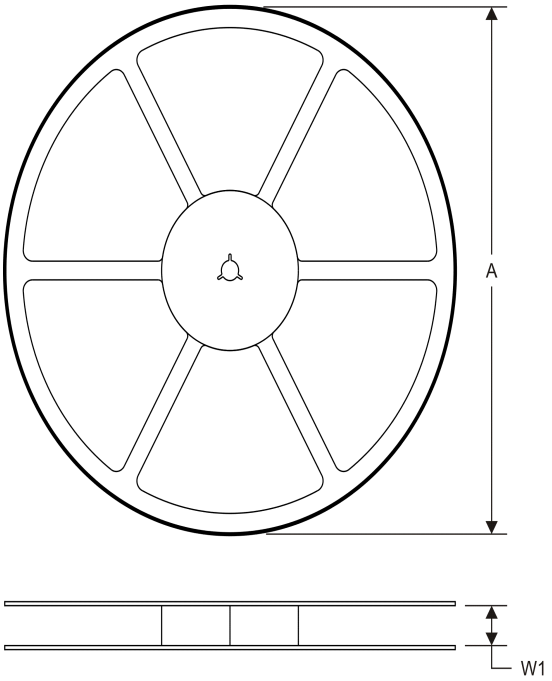
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

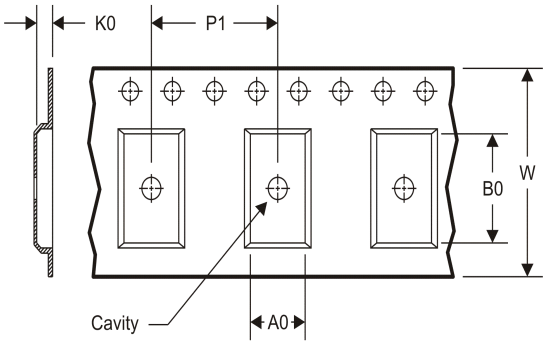
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



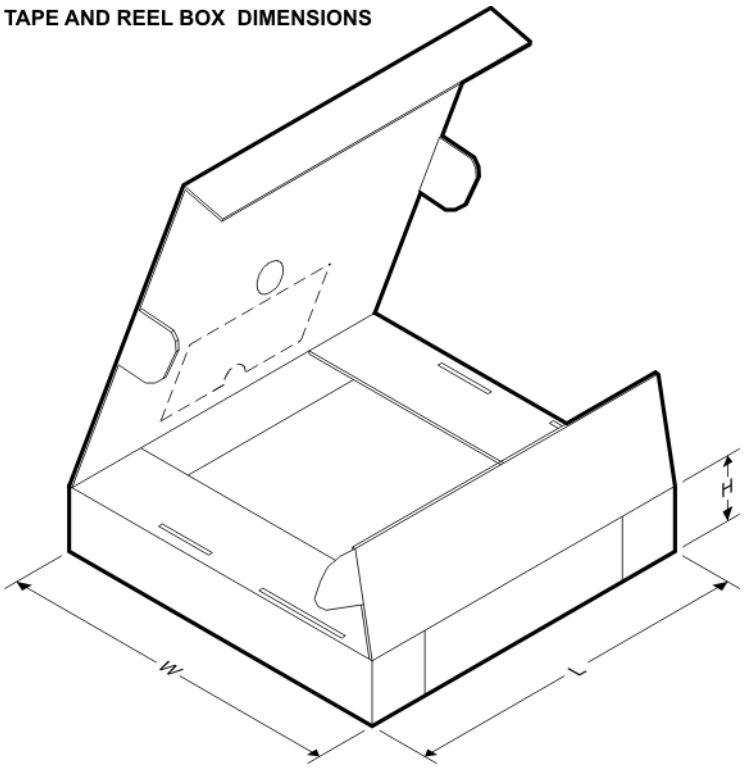
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MPC506AU/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
MPC507AU/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

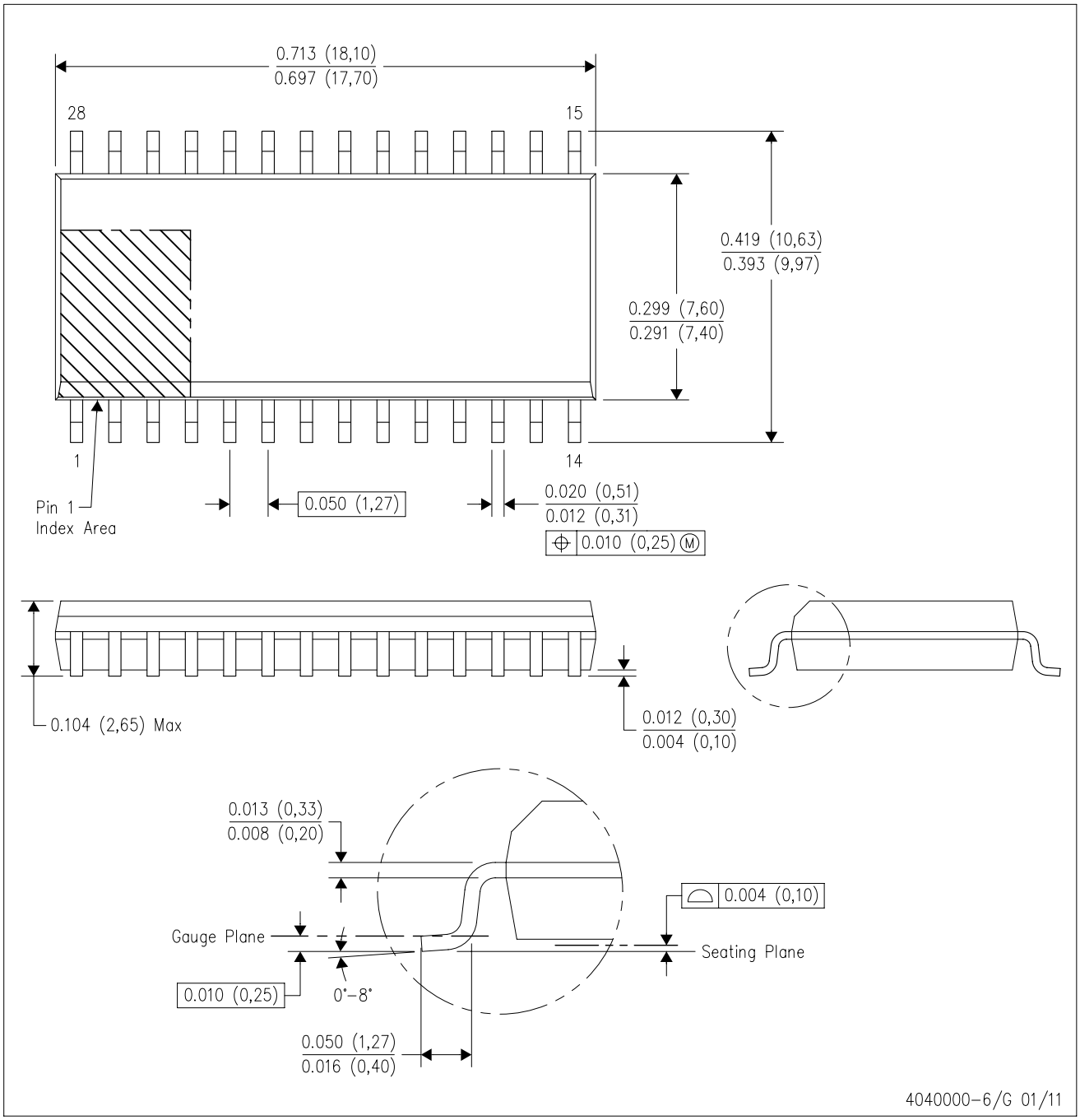
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

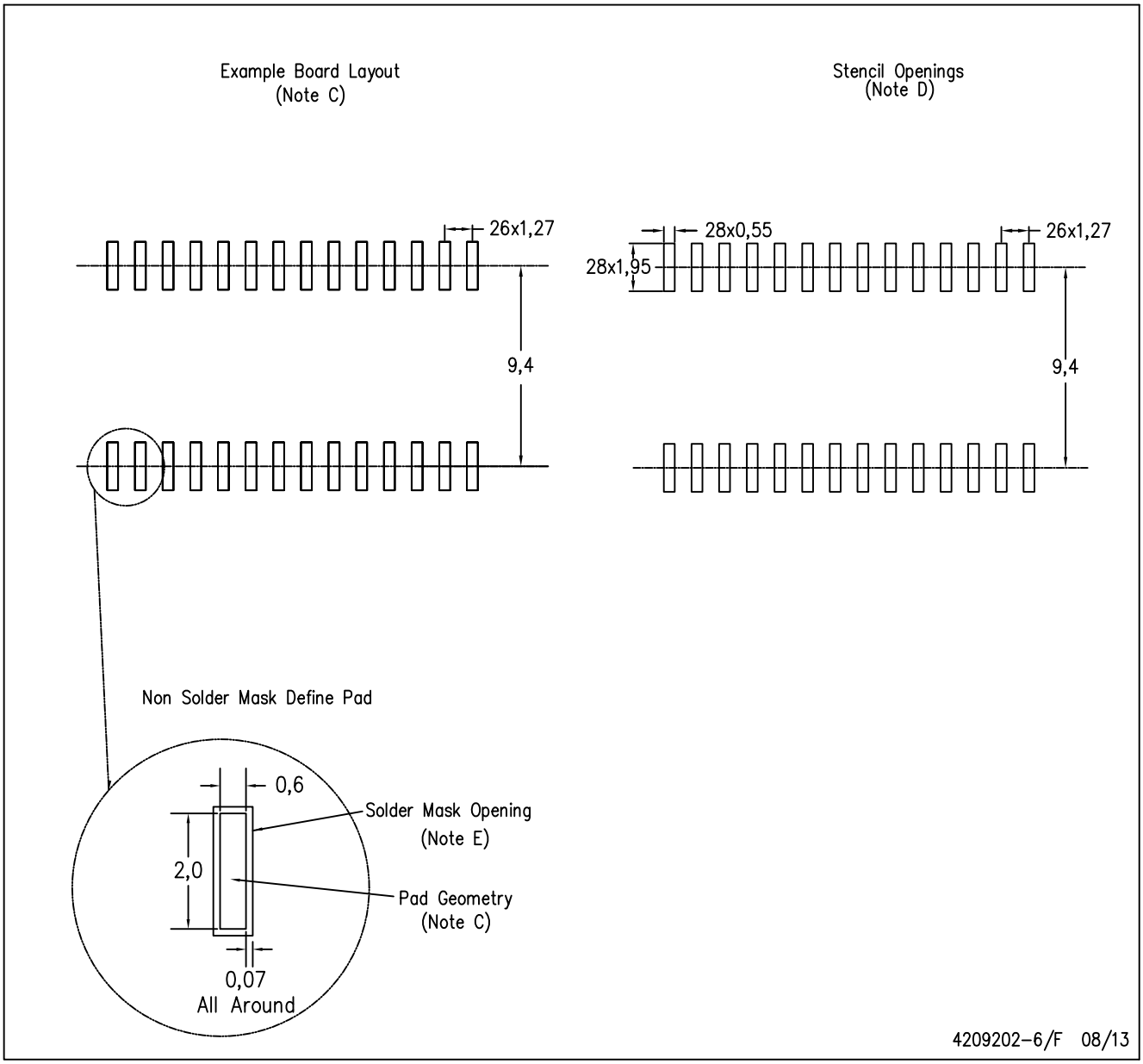
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MPC506AU/1K	SOIC	DW	28	1000	367.0	367.0	55.0
MPC507AU/1K	SOIC	DW	28	1000	367.0	367.0	55.0

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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