SY89833L

3.3V Ultra-Precision 1:4 LVDS Fanout Butter/Translator with Internal Termination

Features

- Guaranteed AC Performance Over-temperature and Voltage:
  - DC to > 2 GHz Throughput
  - <600 ps Propagation Delay (IN-to-Q)
  - <20 ps Within-device Skew
  - <150 ps Rise/Fall Times
- Ultra-low Jitter Design:
  - 98 fs_{RMS} Phase Jitter
- Patented Any-in Input Termination and VT Pin Accepts DC- and AC-coupled Inputs
- High-speed LVDS Outputs
- 3.3V Power Supply Operation:
  - Industrial Temperature Range: -40°C to +85°C
- Available in 16-Lead 3 mm × 3 mm VQFN Package

Applications

- Processor Clock Distribution
- SONET Clock Distribution
- Fibre Channel Clock Distribution
- Gigabit Ethernet Clock Distribution

General Description

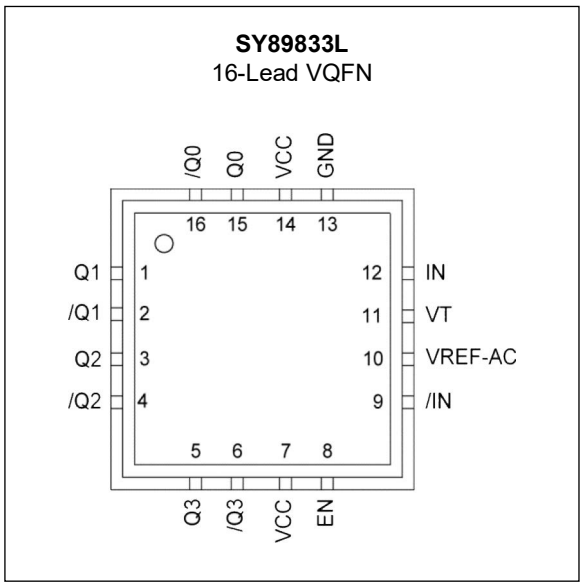
The SY89833L is a 3.3V, high-speed 2 GHz differential low voltage differential swing (LVDS) 1:4 fanout buffer optimized for ultra-low skew applications. Within device skew is guaranteed to be less than 20 ps over supply voltage and temperature.

The differential input buffer has a unique internal termination design that allows access to the termination network through a VT pin. This feature allows the device to easily interface to different logic standards. A V_{REF-AC} reference is included for AC-coupled applications.

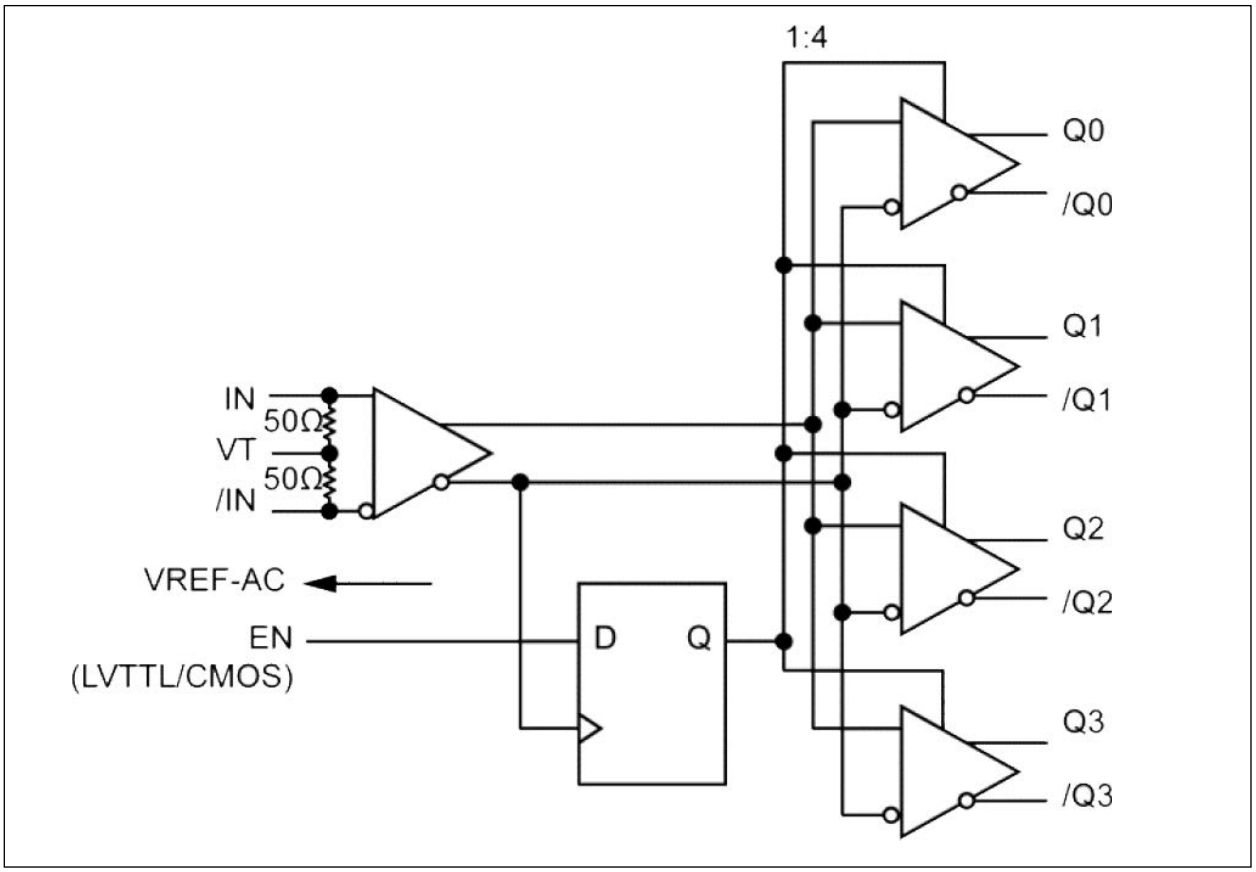
The SY89833L is part of Microchip's high-speed clock synchronization family. For 2.5V applications, the SY89832U provides similar functionality while operating from a 2.5V ±5% supply. For applications that require a different I/O combination, consult the Microchip website at www.microchip.com, and choose from a comprehensive product line of high-speed, low-skew fanout buffers, translators, and clock generators.

Package Type

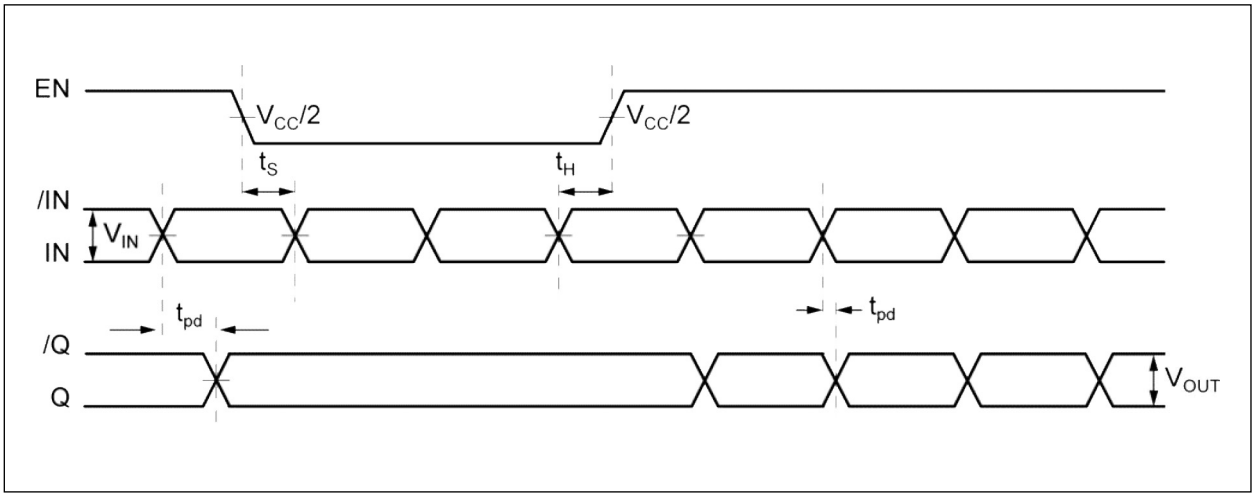
SY89833L
16-Lead VQFN



Functional Block Diagram



Timing Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
Input Voltage (V_{IN}) ..... –0.5V to V_{CC} + 0.3V
LVDS Output Current (I_{OUT}) ..... 10 mA
Input Current, Source or Sink Current on (VT) ..... ±2 mA

Operating Ratings††

Supply Voltage Range ..... +3.0V to +3.6V

† **Notice:** Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†† **Notice:** The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

TABLE 1-1: ELECTRICAL CHARACTERISTICS

T_A = –40°C to +85°C unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Power Supply	V_{CC}	3.0	3.3	3.6	V	—
Power Supply Current	I_{CC}	—	75	100	mA	No load, max. V_{CC}
Input Resistance (IN-to-VT)	R_{IN}	45	50	55	Ω	—
Differential Input Resistance (IN-to-/IN)	$R_{DIFF-IN}$	90	100	110	Ω	—
Input HIGH Voltage (IN-to-/IN)	V_{IH}	0.1	—	V_{CC} + 0.3	V	—
Input LOW Voltage (IN-to-/IN)	V_{IL}	–0.3	—	V_{IH} – 0.1	V	—
Input Voltage Swing (IN-to-/IN)	V_{IN}	0.1	—	V_{CC}	V	Note 2, see Figure 7-3
Differential Input Voltage Swing	V_{DIFF_IN}	0.2	—	—	V	Note 2, see Figure 7-4
Input Current (IN, /IN)	|IIN|	—	—	45	mA	Note 2
Reference Voltage	V_{REF-AC}	V_{CC} – 1.525	V_{CC} – 1.425	V_{CC} – 1.325	V	—

Note 1: The circuit is designed to meet the DC specifications shown in this table after thermal equilibrium has been established.

2: Due to the internal termination (see “Input Buffer Structure” section) the input current depends on the applied voltages at IN, /IN and VT inputs. Do not apply a combination of voltages that causes the input current to exceed the maximum limit.

TABLE 1-2: LVDS OUTPUTS DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V±10%, R_L = 100Ω across the outputs; T_A = -40°C to +85°C. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Output Voltage Swing	V_{OUT}	250	325	—	mV	See Figure 7-3
Differential Output Voltage Swing	V_{DIFF_OUT}	500	650	—	mV	See Figure 7-4
Output Common Mode Voltage	V_{OCM}	1.125	—	1.275	V	—
Change in Common Mode Voltage	ΔV_{OCM}	–50	—	50	mV	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

TABLE 1-3: LVTTL/LVCMOS DC ELECTRICAL CHARACTERISTICS

V_{CC} = 3.3V ±10%, T_A = -40°C to +85°C. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Input HIGH Voltage	V_{IH}	2.0	—	VCC	V	—
Input LOW Voltage	V_{IL}	0	—	0.8	V	—
Input HIGH Current	I_{IH}	–125	—	30	uA	—
Input LOW Current	I_{IL}	—	—	–300	uA	—

Note 1: The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

TABLE 1-4: AC ELECTRICAL CHARACTERISTICS

V_{CC} = 2.5V ±5% or 3.3V ±10%; R_L = 50Ω to V_{CC} − 2V; T_A = –40°C to + 85°C, unless otherwise noted. (Note 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Maximum Frequency	f_{MAX}	2.0	—	—	GHz	V_{OUT} ≥ 200 mV
Propagation Delay IN-to-Q	t_{pd}	400	500	600	ps	VIN < 400mV
		330	440	530		VIN ≥ 400mV
Within-Device Skew	t_{SKEW}	—	4	20	ps	Note 2
Part-to-Part Skew	t_{SKEW}	—	—	200	ps	Note 3
Set-up Time EN-to-IN, /IN	t_S	300	—	—	ps	Note 4
Hold Time EN-to-IN, /IN	t_H	500	—	—	ps	Note 4
RMS Phase Jitter	t_{JITTER}	—	98	—	fs	Output = 622 MHz, Integration Range: 12 kHz – 20 MHz
Output Rise/Fall Times (20% to 80%)	t_r, t_f	60	110	190	ps	At full output swing

Note 1: High-frequency AC parameters are guaranteed by design and characterization.

2: Within device skew is measured between two different outputs under identical input transitions.

3: Part-to-part skew is defined for two parts with identical power supply voltages at the same temperature and no skew at the edges at the respective inputs.

4: Set-up and hold times apply to synchronous applications that intend to enable/disable before the next clock cycle. For asynchronous applications, set-up and hold times do not apply.

TABLE 1-5: TEMPERATURE SPECIFICATIONS

Note 1						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Range						
Operating Temperature Range	T_A	–40	—	+85	°C	—
Maximum Operating Junction Temperature		—	—	+125	°C	—
Lead Temperature	T_{LEAD}	—	260	—	°C	Soldering, 20 sec.
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistance (Note 1)						
VQFN, Still Air	θ_{JA}	—	60	—	°C/W	—
VQFN	Ψ_{JB}	—	33	—	°C/W	—

Note 1: Package thermal resistance assumes the exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB. The Ψ_{JB} and θ_{JA} values are determined for a 4-layer board at the still-air package thermal resistance, unless otherwise stated.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

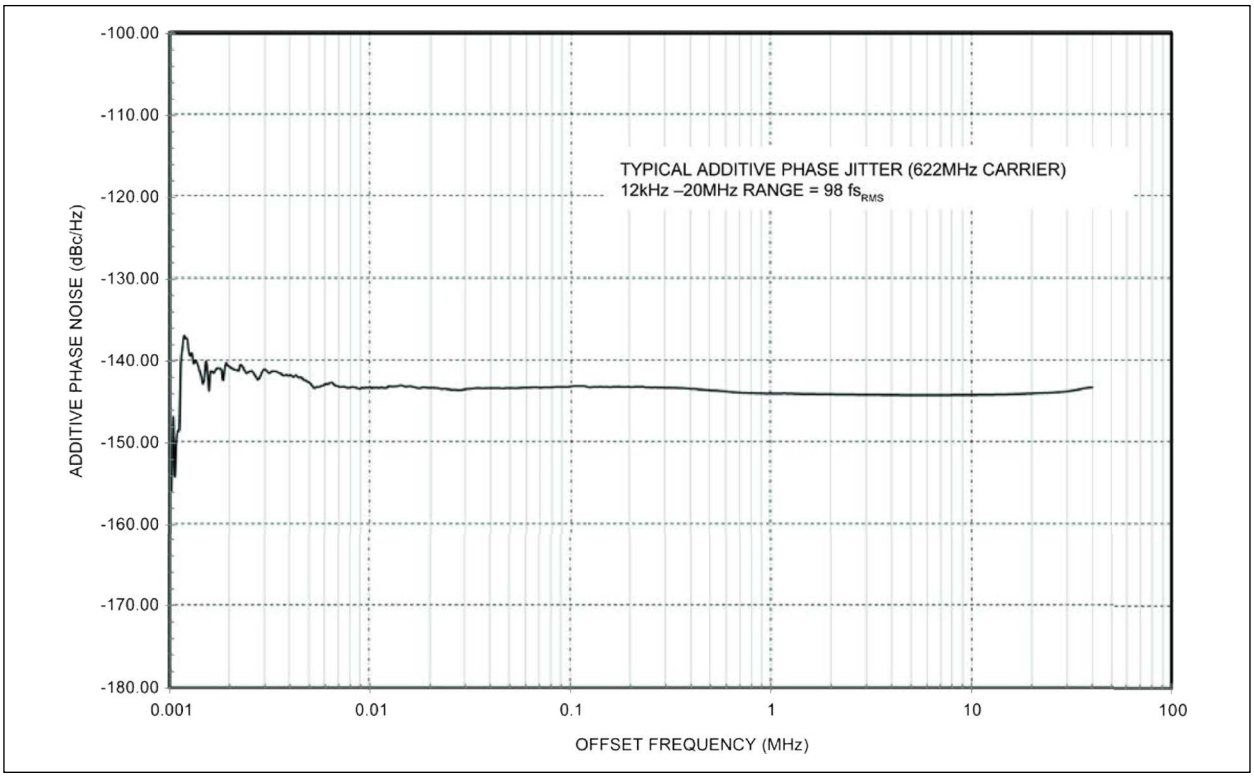
Pin Number	Pin Name	Description
15, 16	Q0, /Q0	LVDS Differential Outputs: Normally terminated with 100Ω across the pair (Q, /Q). See Section 7.0, LVDS Outputs. Unused outputs should be terminated with a 100Ω resistor across each pair.
1, 2	Q1, /Q1	
3, 4	Q2, /Q2	
5, 6	Q3, /Q3	
8	EN	This single-ended TTL/CMOS-compatible input functions as a synchronous output enable. The synchronous enable ensures that enable/disable will only occur when the outputs are in a logic LOW state. Note that this input is internally connected to a 25kΩ pull-up resistor and will default to logic HIGH state (enabled) if left open.
9, 12	/IN, IN	Differential Inputs: These input pairs are the differential signal inputs to the device. Inputs accept AC- or DC-Coupled differential signals as small as 100mV. Each pin of a pair internally terminates to a VT pin through 50Ω. Note that these inputs will default to an intermediate state if left open. Please refer to Section 8.0, Input Interface Applications for more details.
10	VREF-AC	Reference Voltage: These outputs bias to VCC-1.4V.They are used when AC coupling the inputs (IN, /IN). For AC-Coupled applications, connect VREF-AC to VT pin and bypass with 0.01µF low ESR capacitor to VCC. See Section 8.0, Input Interface Applications for more details. Maximum sink/source current is ±1.5mA. Due to the limited drive capability, each VREF-AC pin is only intended to drive its respective VT pin.
11	VT	Input Termination Center-Tap: Each side of the differential input pair terminates to a VT pin. The VT pins provide a center-tap to a termination network for maximum interface flexibility. See Section 8.0, Input Interface Applications for more details.
13	GND	Ground. GND pins and exposed pad must be connected to the most negative potential of the device ground.
7, 14	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors and place as close to each VCC pin as possible.

TABLE 2-2: TRUTH TABLE

IN	/IN	EN	Q	/Q
0	1	1	0	1
1	0	1	1	0
X	X	0	0 (Note 1)	1 (Note 1)

Note 1: On the next negative transition of the input signal (IN).

3.0 ADDITIVE PHASE NOISE PLOT



4.0 TYPICAL CHARACTERISTICS

V_{CC} = 3.3V, GND = 0V, V_{IN} = 400 mV, R_L = 100Ω across the outputs; T_A = 25°C, unless otherwise stated.

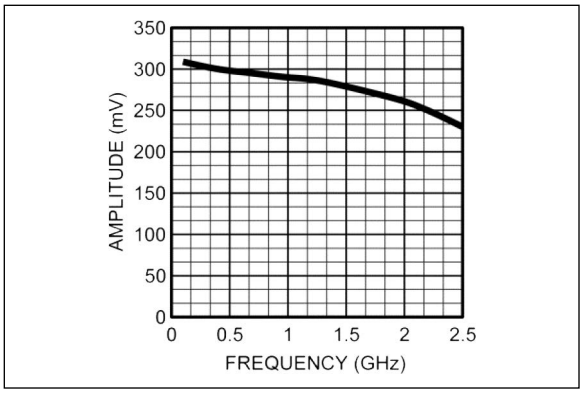


FIGURE 4-1: OUTPUT SWING VS. FREQUENCY.

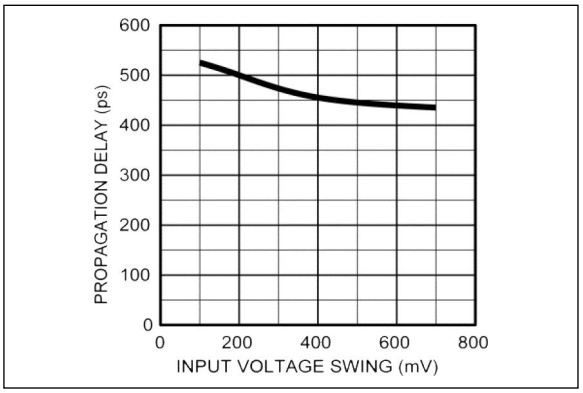


FIGURE 4-2: PROPAGATION DELAY VS. INPUT VOLTAGE SWING.

5.0 FUNCTIONAL CHARACTERISTICS

Typical output waveforms. V_{CC} = 3.3V; GND = 0V; V_{IN} = 800 mV; R_L = 50Ω to V_{CC} − 2V; T_A = 25°C, unless otherwise noted.

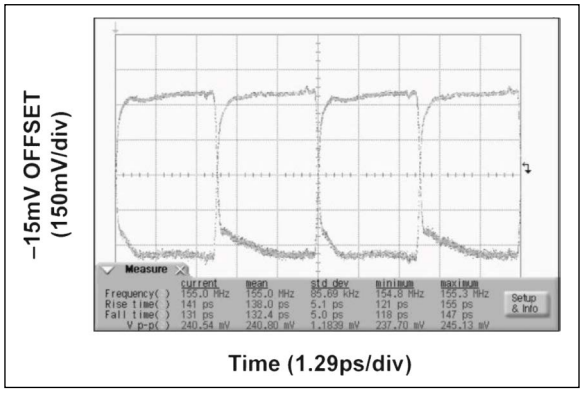


FIGURE 5-1: 155 MHZ OUTPUT.

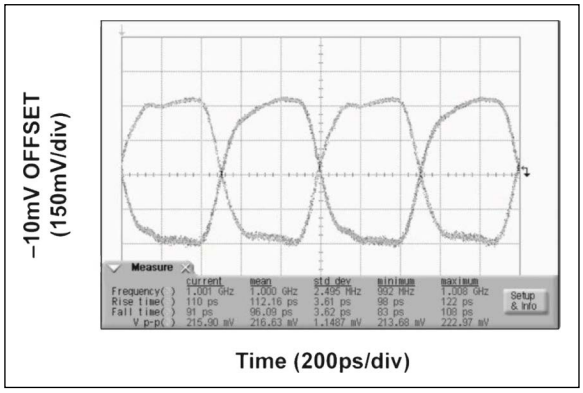


FIGURE 5-3: 1 GHZ OUTPUT.

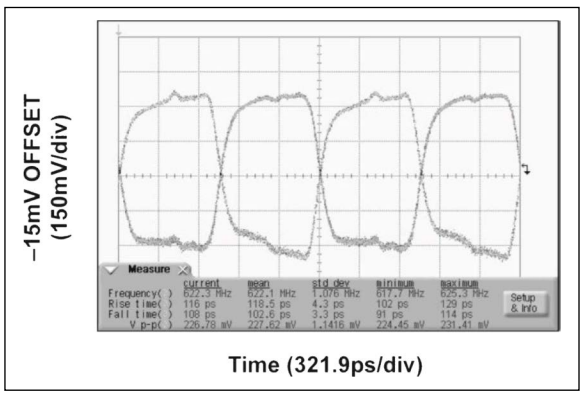


FIGURE 5-2: 622 MHZ OUTPUT.

6.0 INPUT STAGE

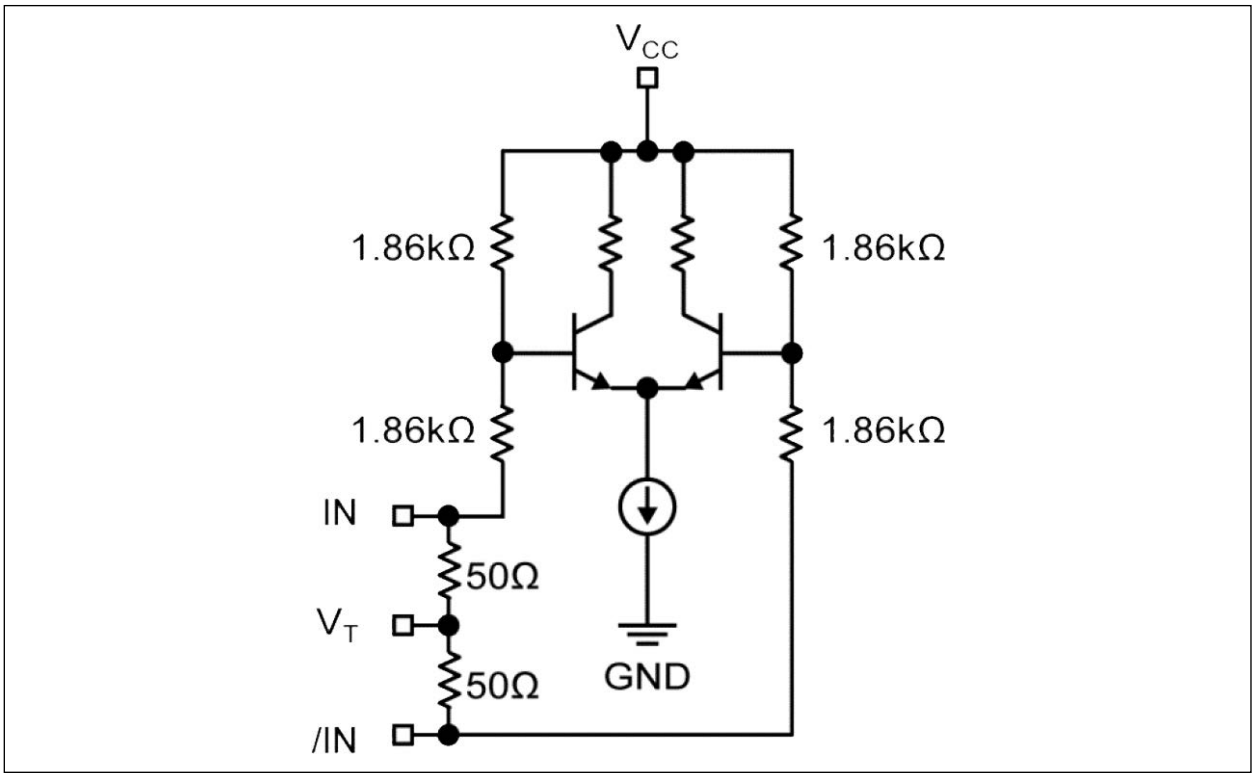


FIGURE 6-1: SIMPLIFIED DIFFERENTIAL INPUT BUFFER.

7.0 LVDS OUTPUTS

LVDS specifies a small swing of 325 mV typical, on a nominal 1.20V common mode above ground. The common-mode voltage has tight limits to permit large variations in ground noise between a LVDS driver and receiver.

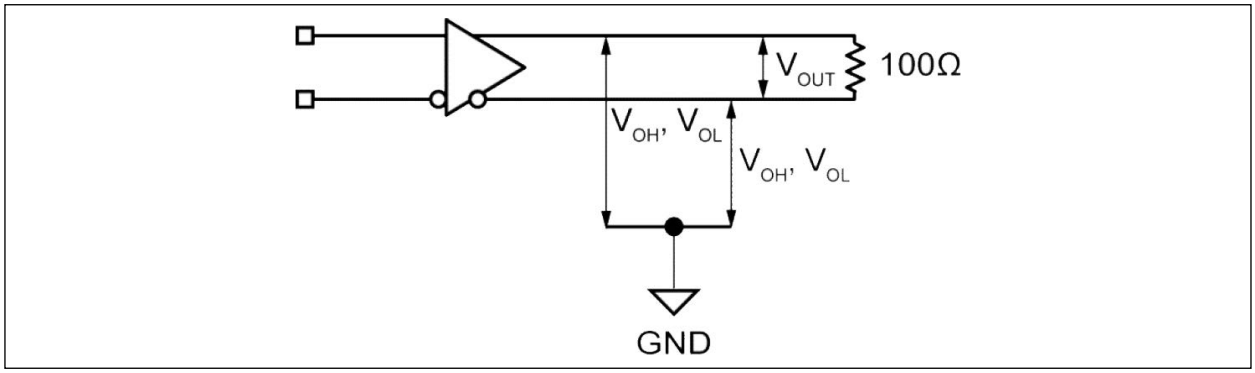


FIGURE 7-1: LVDS DIFFERENTIAL MEASUREMENT.

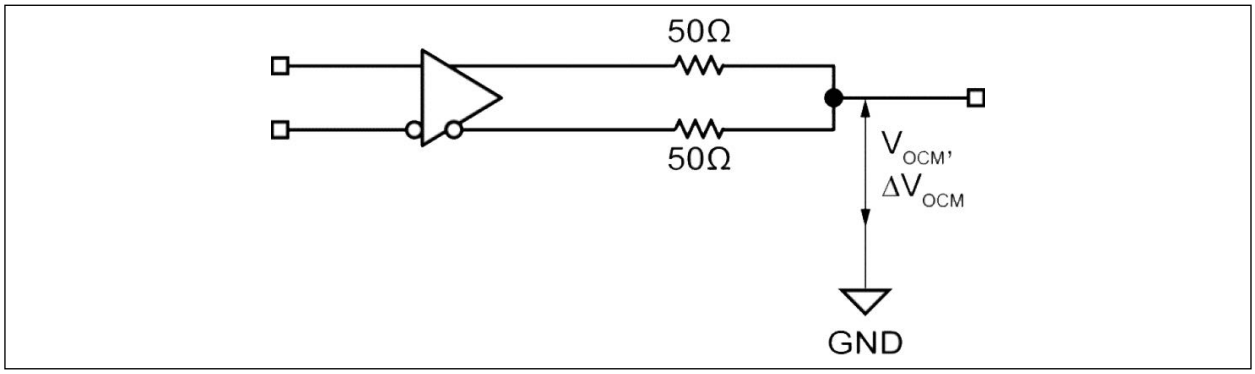


FIGURE 7-2: LVDS COMMON MODE MEASUREMENT.

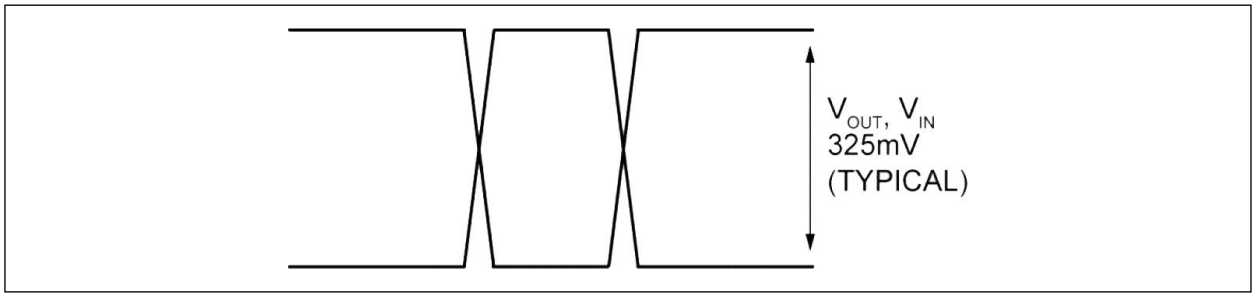


FIGURE 7-3: SINGLE-ENDED SWING.

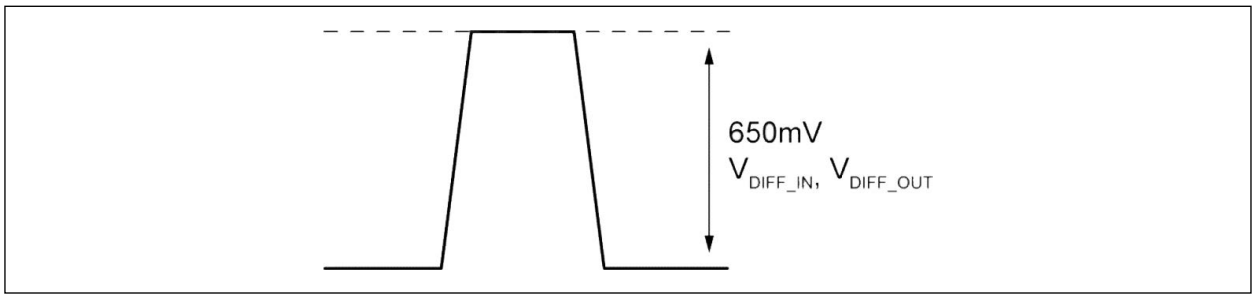


FIGURE 7-4: DIFFERENTIAL SWING.

8.0 INPUT INTERFACE APPLICATIONS

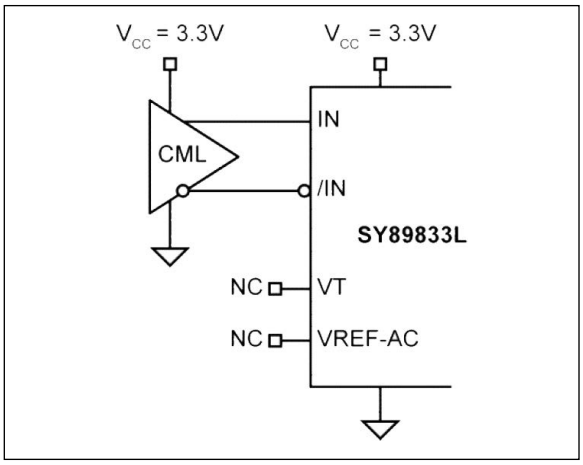


FIGURE 8-1: DC-COUPLED CML INPUT INTERFACE.

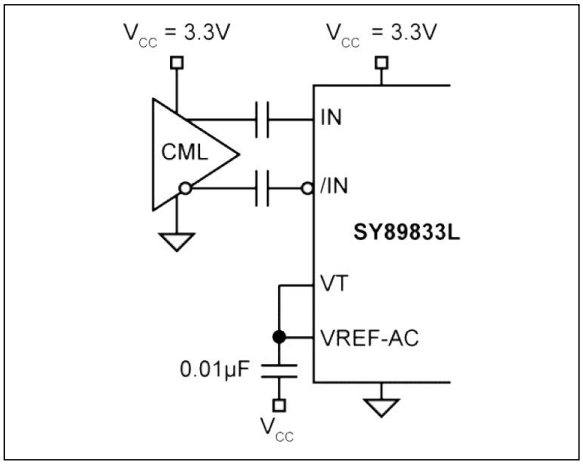


FIGURE 8-2: AC-COUPLED CML INPUT INTERFACE.

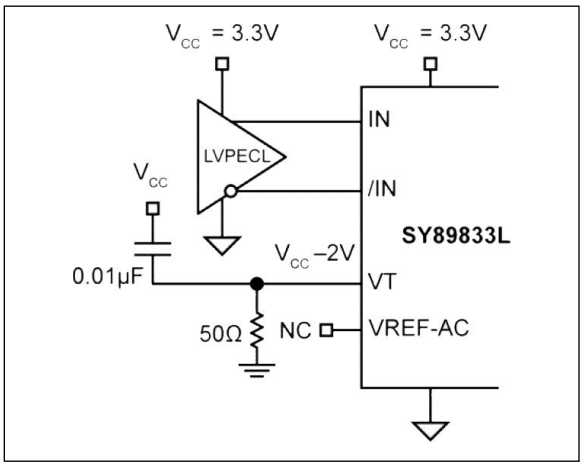


FIGURE 8-3: DC-COUPLED LVPECL INPUT INTERFACE.

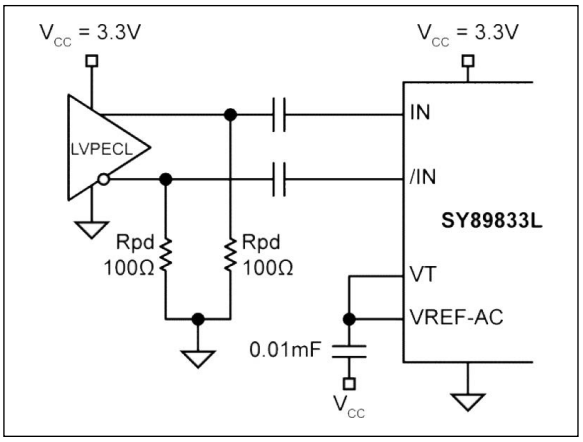


FIGURE 8-4: AC-COUPLED LVPECL INPUT INTERFACE.

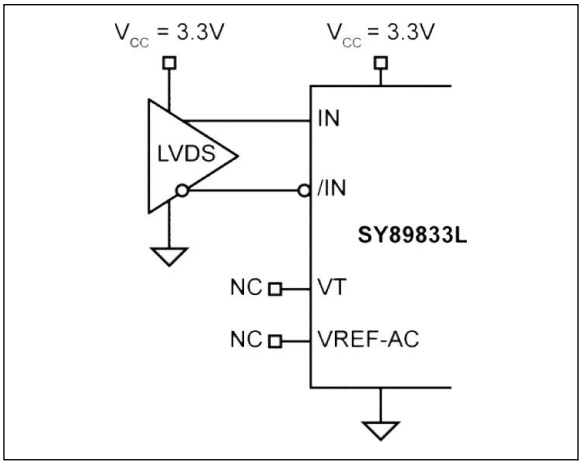


FIGURE 8-5: DC-COUPLED LVDS INPUT INTERFACE.

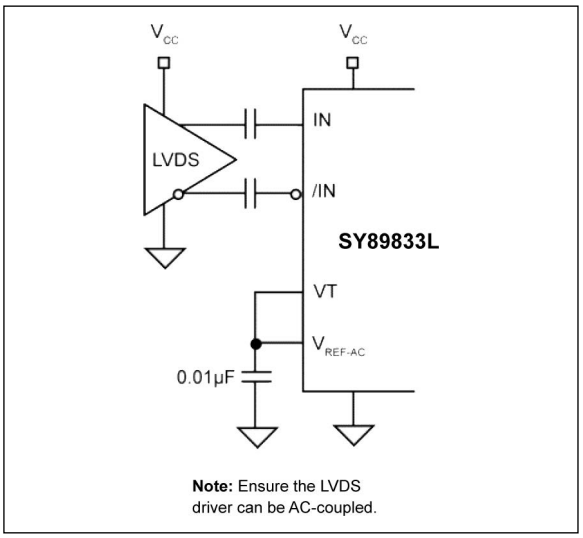
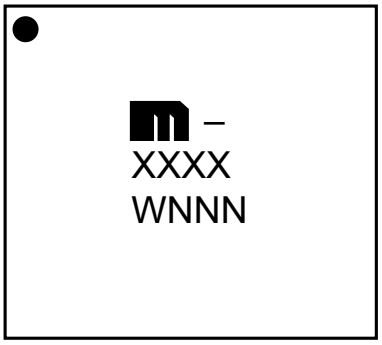


FIGURE 8-6: AC-COUPLED LVDS INPUT INTERFACE.

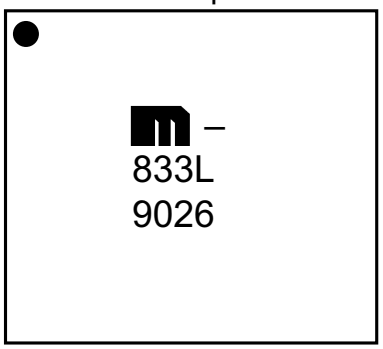
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

16-Lead VQFN*



Example*



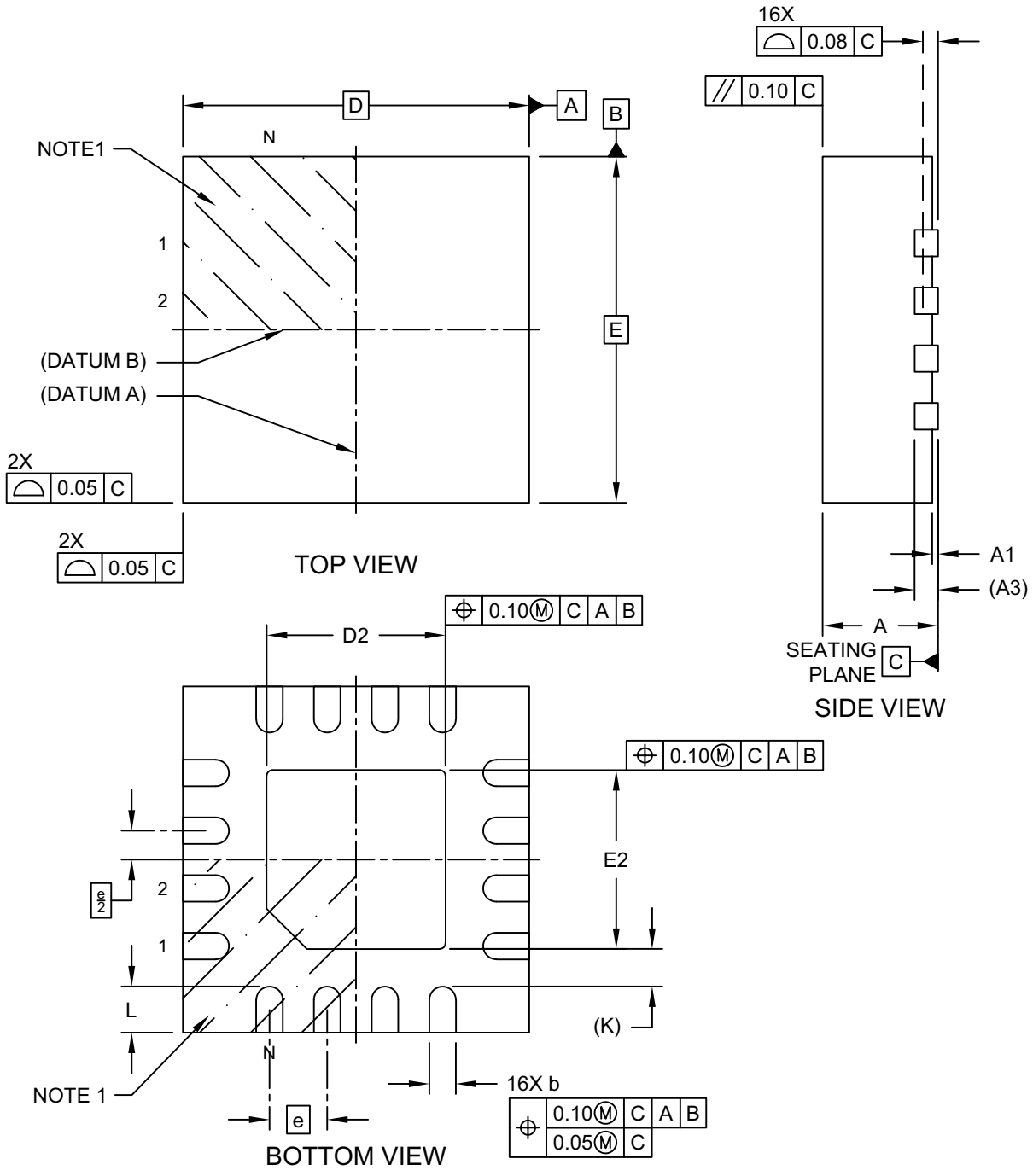
Legend:	XX...X	Product code or customer-specific information
	W	Week code
	NNN	Alphanumeric traceability code (week)
	*	This package is Pb-free. The Pb-free JEDEC designator can be found on the outer packaging for this package.
	●	Pin one index is identified by a dot

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (¯) symbol may not be to scale.

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

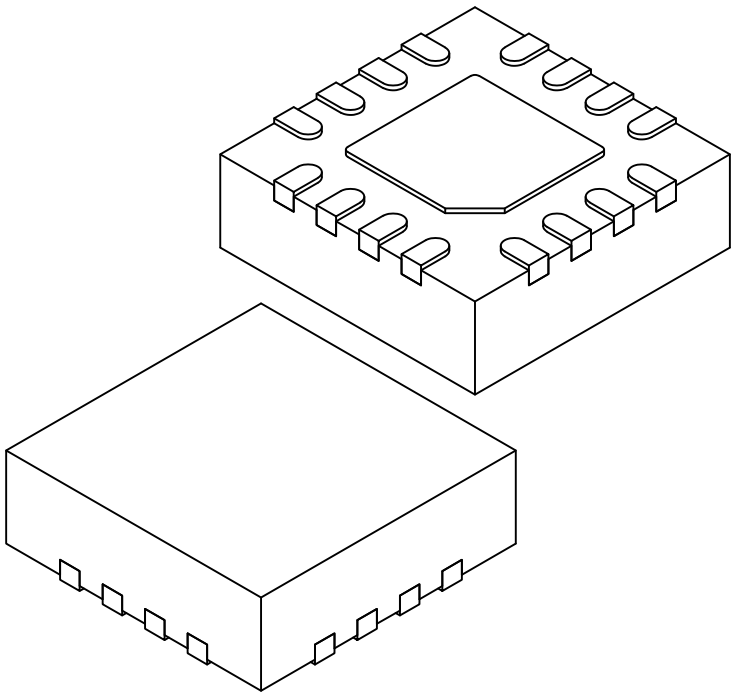
Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1103-NCA Rev C Sheet 1 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	1.50	1.55	1.60
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.55	1.60
Terminal Width	b	0.18	0.23	0.28
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K		0.33 REF	

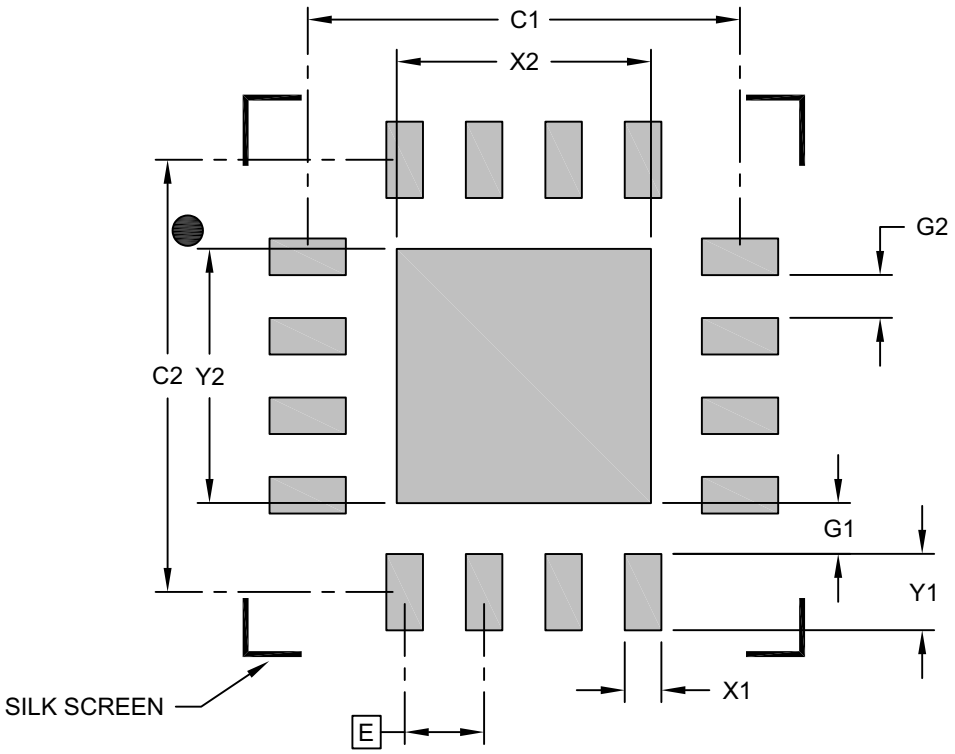
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev C Sheet 2 of 2

16-Lead 3 mm × 3 mm VQFN [NCA] Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			1.60
Center Pad Length	Y2			1.60
Contact Pad Spacing	C1		2.72	
Contact Pad Spacing	C2		2.72	
Contact Pad Width (Xnn)	X1			0.23
Contact Pad Length (Xnn)	Y1			0.48
Contact Pad to Center Pad (Xnn)	G1	0.32		
Contact Pad to Contact Pad (Xnn)	G2	0.27		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3103-NCA Rev C

APPENDIX A: REVISION HISTORY

Revision A (May 2025)

- Converted Micrel data sheet for SY89833L to Microchip format as DS20006846A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	X	X	-XX
Device	Supply Voltage Range	Package	Temperature Range	Special Processing

Device:	SY89833	=	Ultra-Precision 1:4 LVPECL Fanout Buffer/Translator with Internal Termination Precision Edge®
Voltage Option:	L	=	3.3V
Package:	M	=	16-Lead VQFN
Temperature Range:	G	=	–40°C to 85°C
Special Processing:	<blank>	=	100/Tube
	-TR	=	1,000/Tape & Reel

Examples:

a) **SY89833LMG**

3.3V, 16-Lead VQFN, –40°C to 85°C, 100/Tube

b) **SY89831LMG-TR**

3.3V, 16-Lead VQFN, –40°C to 85°C, 1,000/Tape & Reel

NOTES:

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-1220-6

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP "AS IS". MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP'S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip product is strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.