To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

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The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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3822 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 3822 group is the 8-bit microcomputer based on the 740 family core technology.

The 3822 group has the LCD drive control circuit, an 8-channel A-D converter, and a serial I/O as additional functions.

The various microcomputers in the 3822 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 3822 group, refer to the section on group expansion.

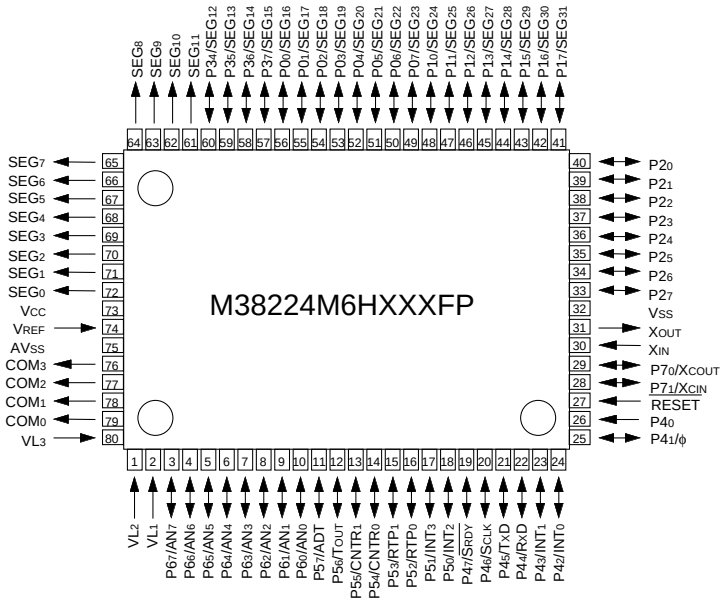
FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.5 µs
  (at 8 MHz oscillation frequency)
- Memory size
  - ROM ..... 4 K to 48 K bytes
  - RAM ..... 192 to 1024 bytes
- Programmable input/output ports 49
- Software pull-up/pull-down resistors (Ports P0-P7 except port $P4_0$)
- Interrupts ..... 17 sources, 16 vectors
  (includes key input interrupt)
- Timers ..... 8-bit × 3, 16-bit × 2
- Serial I/O ..... 8-bit × 1 (UART or Clock-synchronized)
- A-D converter ..... 8-bit × 8 channels
- LCD drive control circuit
  - Bias 1/2, 1/3
  - Duty 1/2, 1/3, 1/4
  - Common output 4
  - Segment output 32
- 2 clock generating circuits
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  - In high-speed mode ..... 4.0 to 5.5 V
  - In middle-speed mode ..... 2.5 to 5.5 V
    (Extended operating temperature version:
    2.0 to 5.5 V, Ta= – 20 to 85°C
    3.0 to 5.5 V, Ta= – 40 to – 20°C)
    (One time PROM version: 2.5 to 5.5 V)
    (M version: 2.2 to 5.5 V)
    (H version: 2.0 to 5.5 V)
  - In low-speed mode ..... 2.5 to 5.5 V
    (Extended operating temperature version:
    2.0 to 5.5 V, Ta= – 20 to 85°C
    3.0 to 5.5 V, Ta= – 40 to – 20°C)
    (One time PROM version: 2.5 to 5.5 V)
    (M version: 2.2 to 5.5 V)
    (H version: 2.0 to 5.5 V)
- Power dissipation
  - In high-speed mode ..... 32 mW
    (at 8 MHz oscillation frequency, at 5 V power source voltage)
  - In low-speed mode ..... 45 µW
    (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ..... – 20 to 85°C
  (Extended operating temperature version: – 40 to 85 °C)

APPLICATIONS

Camera, household appliances, consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)

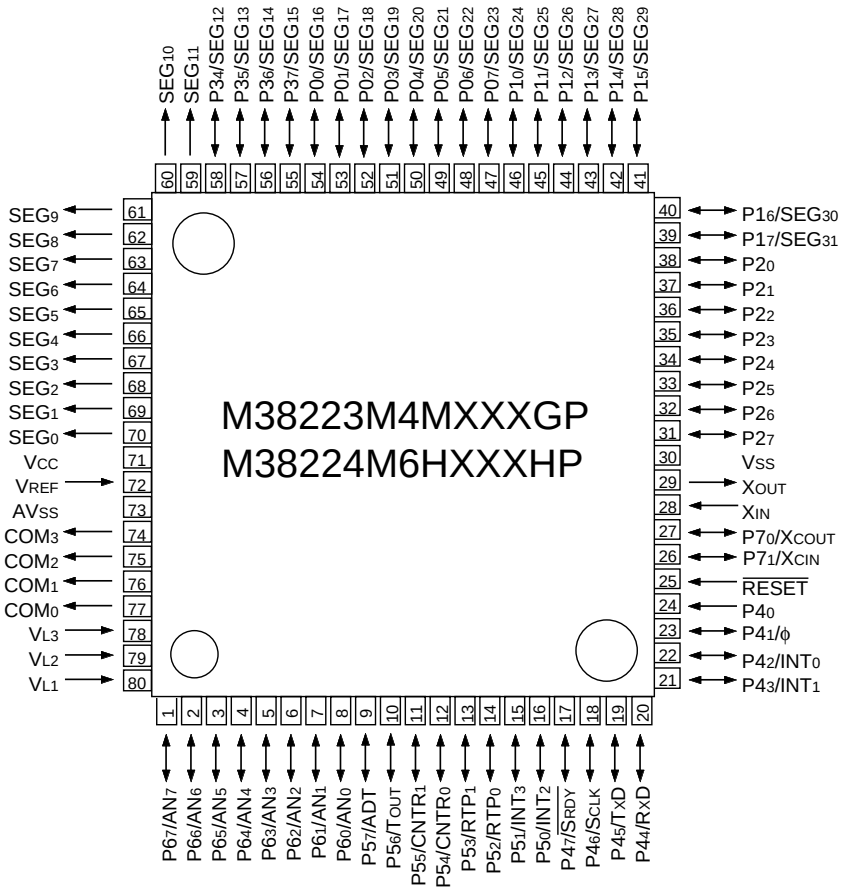


Package type : 80P6N-A (80-pin plastic-molded QFP)

Fig. 1 M38224M6HXXXFP pin configuration
(The pin configuration of 80D0 is same as this.)

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PIN CONFIGURATION (TOP VIEW)



Package type : 80P6S-A/80P6Q-A
(80-pin plastic-molded QFP)

Fig. 2 M38223M4MXXXGP/M38224M6HXXXHP pin configuration

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FUNCTIONAL BLOCK DIAGRAM (Package type : 80P6Q-A)

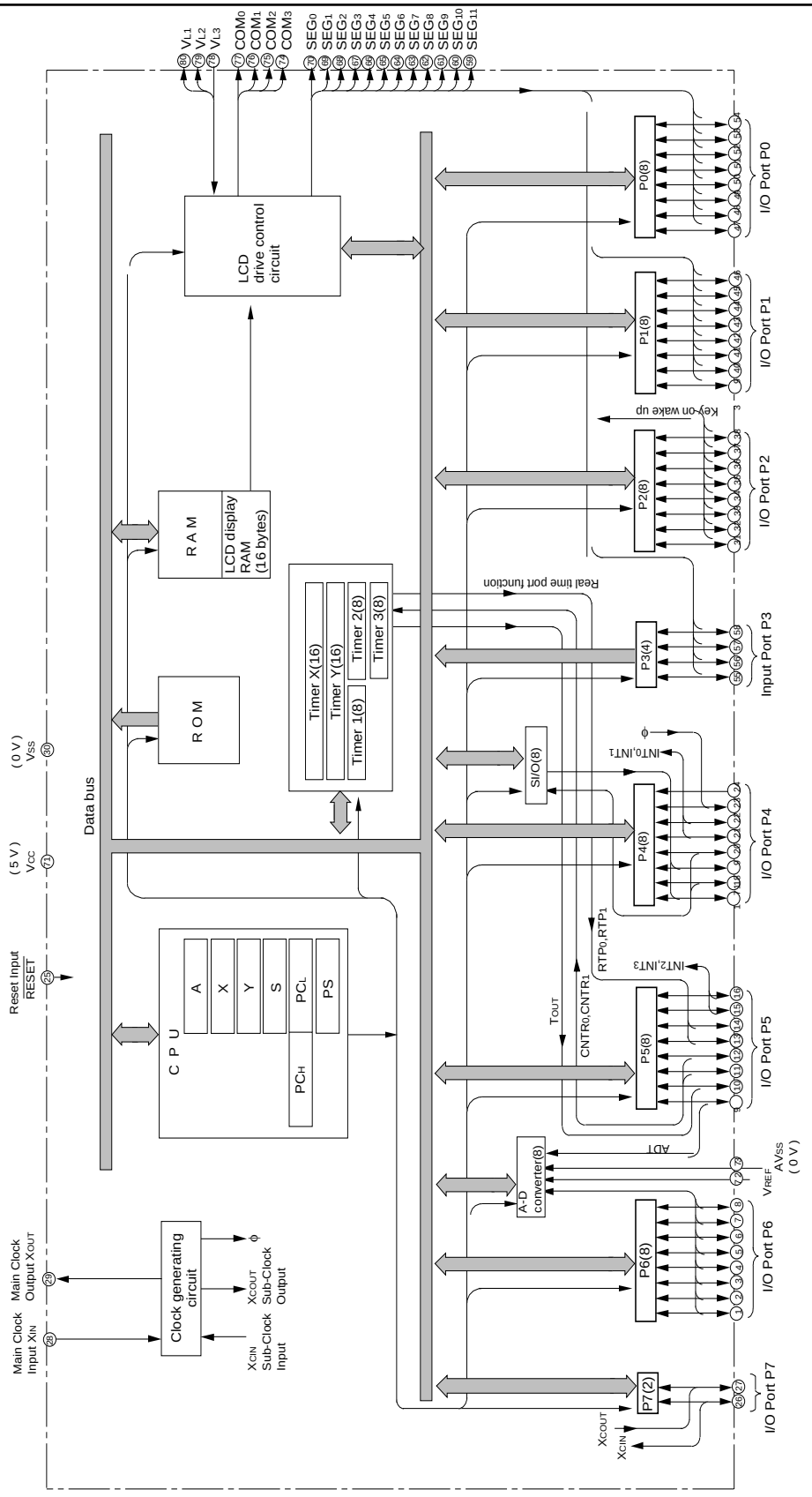


Fig. 3 Functional block diagram

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PIN DESCRIPTION

Table 1 Pin description (1)

Pin	Name	Function	Function except a port function
V_{CC}, V_{SS}	Power source	•Apply voltage of power source to V_{CC}, and 0 V to V_{SS}. (For the limits of V_{CC}, refer to "Recommended operating conditions").	
V_{REF}	Analog reference voltage	•Reference voltage input pin for A-D converter.	
AV_{SS}	Analog power source	•GND input pin for A-D converter. •Connect to V_{SS}.	
$\overline{RESET}$	Reset input	•Reset input pin for active "L".	
X_{IN}	Clock input	•Input and output pins for the main clock generating circuit. •Feedback resistor is built in between X_{IN} pin and X_{OUT} pin.	
X_{OUT}	Clock output	•Connect a ceramic resonator or a quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. •If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open. •This clock is used as the oscillating source of system clock.	
V_{L1}–V_{L3}	LCD power source	•Input 0 ≤ V_{L1} ≤ V_{L2} ≤ V_{L3} ≤ V_{CC} voltage. •Input 0 – V_{L3} voltage to LCD.	
COM_0–COM_3	Common output	•LCD common output pins. •COM_2 and COM_3 are not used at 1/2 duty ratio. •COM_3 is not used at 1/3 duty ratio.	
SEG_0–SEG_{11}	Segment output	•LCD segment output pins.	
$P0_0$/SEG_{16}–$P0_7$/SEG_{23}	I/O port P0	•8-bit output port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each port to be individually programmed as either input or output. •Pull-down control is enabled.	•LCD segment output pins
$P1_0$/SEG_{24}–$P1_7$/SEG_{31}	I/O port P1		
$P2_0$ – $P2_7$	I/O port P2	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•Key input (key-on wake-up) interrupt input pins
$P3_4$/SEG_{12} – $P3_7$/SEG_{15}	Input port P3	•4-bit input port. •CMOS compatible input level. •Pull-down control is enabled.	•LCD segment output pins

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Table 2 Pin description (2)

Pin	Name	Function	Function except a port function
P40	Input port P4	•1-bit Input port. •CMOS compatible input level.	
P41/ϕ	I/O port P4	•7-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•ϕ clock output pin
P42/INT0, P43/INT1			•Interrupt input pins
P44/RxD, P45/TxD, P46/SCLK, P47/SRDY			•Serial I/O function pins
P50/INT2, P51/INT3	I/O port P5	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•Interrupt input pins
P52/RTP0, P53/RTP1			•Real time port function pins
P54/CNTR0, P55/CNTR1			•Timer X, Y function pins
P56/TOUT			•Timer 2 output pins
P57/ADT			•A-D trigger input pins
P60/AN0–P67/AN7	I/O port P6	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•A-D conversion input pins
P70/XCOUT, P71/XCIN	I/O port P7	•2-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•Sub-clock generating circuit I/O pins. (Connect a resonator. External clock cannot be used.)

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PART NUMBERING

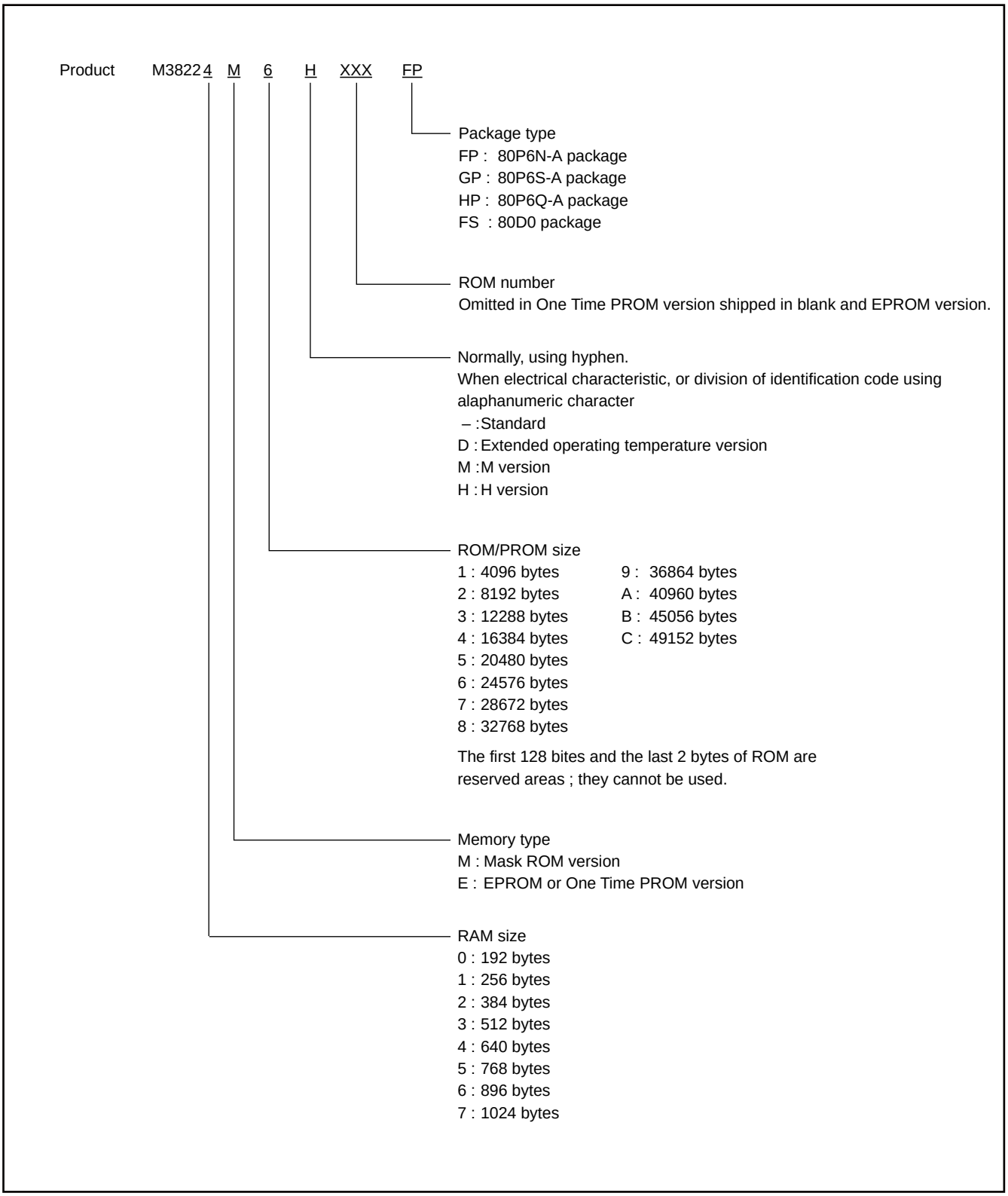


Fig. 4 Part numbering

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GROUP EXPANSION (STANDARD, ONE TIME PROM VERSION, EPROM VERSION)

Mitsubishi plans to expand the 3822 group (Standard, One Time PROM version, EPROM version) as follows:

Memory Type

Support for Mask ROM, One Time PROM, and EPROM versions

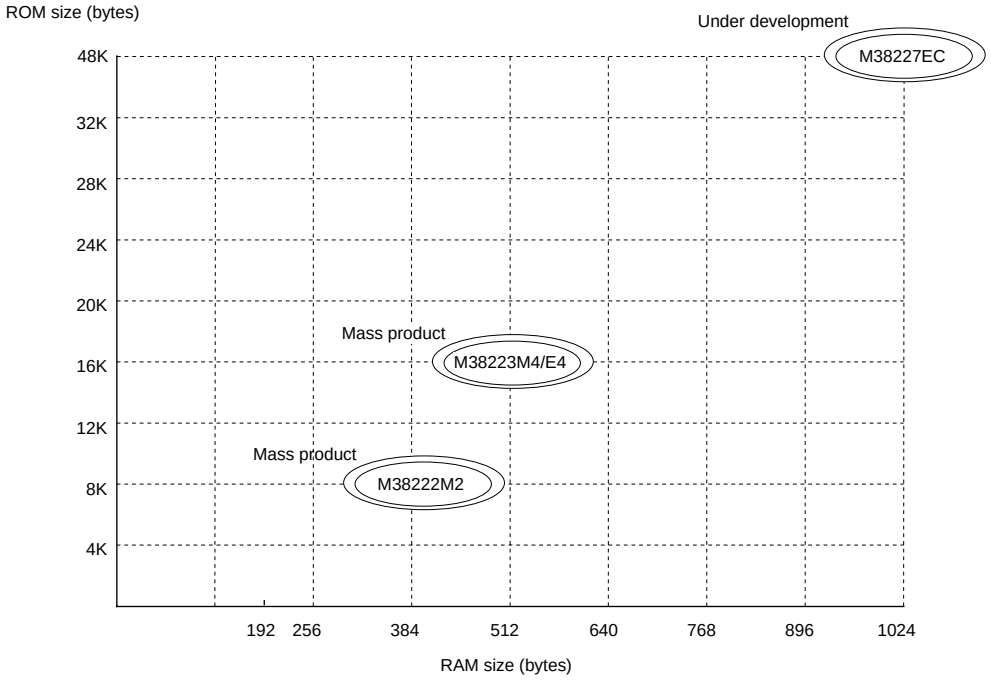
Memory Size

ROM size ..... 8 K to 48 K bytes
RAM size ..... 384 to 1024 bytes

Package

80P6N-A ..... 0.8 mm-pitch plastic molded QFP
80P6S-A ..... 0.65 mm-pitch plastic molded QFP
80P6Q-A ..... 0.5 mm-pitch plastic molded QFP
80D0 ..... 0.8 mm-pitch ceramic LCC (EPROM version)

Memory Expansion Plan



Note: Products under development or planning: the development schedule and specifications may be revised without notice.

Fig. 5 Memory expansion plan

Currently products are listed below.

Table 3 List of products

As of Feb. 2002

Product	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38222M2-XXXFP	8192 (8062)	384	80P6N-A	Mask ROM version
M38222M2-XXXGP			80P6S-A	Mask ROM version
M38222M2-XXXHP			80P6Q-A	Mask ROM version
M38223M4-XXXFP	16384 (16254)	512	80P6N-A	Mask ROM version
M38223E4FP				One Time PROM version (blank)
M38223M4-XXXGP			80P6S-A	Mask ROM version
M38223E4GP				One Time PROM version (blank)
M38223M4-XXXHP			80P6Q-A	Mask ROM version
M38223E4HP				One Time PROM version (blank)
M38223E4FS			80D0	EPROM version
M38227ECFP	49152 (49022)	1024	80P6N-A	One Time PROM version (blank)
M38227ECHP			80P6Q-A	One Time PROM version (blank)
M38227ECFS			80D0	EPROM version

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GROUP EXPANSION (EXTENDED OPERATING TEMPERATURE VERSION)

Mitsubishi plans to expand the 3822 group (extended operating temperature version) as follows:

Memory Type

Support for Mask ROM version.

Memory Size

ROM size ..... 48 K bytes
RAM size ..... 1024 bytes

Package

80P6N-A ..... 0.8 mm-pitch plastic molded QFP

Memory Expansion Plan

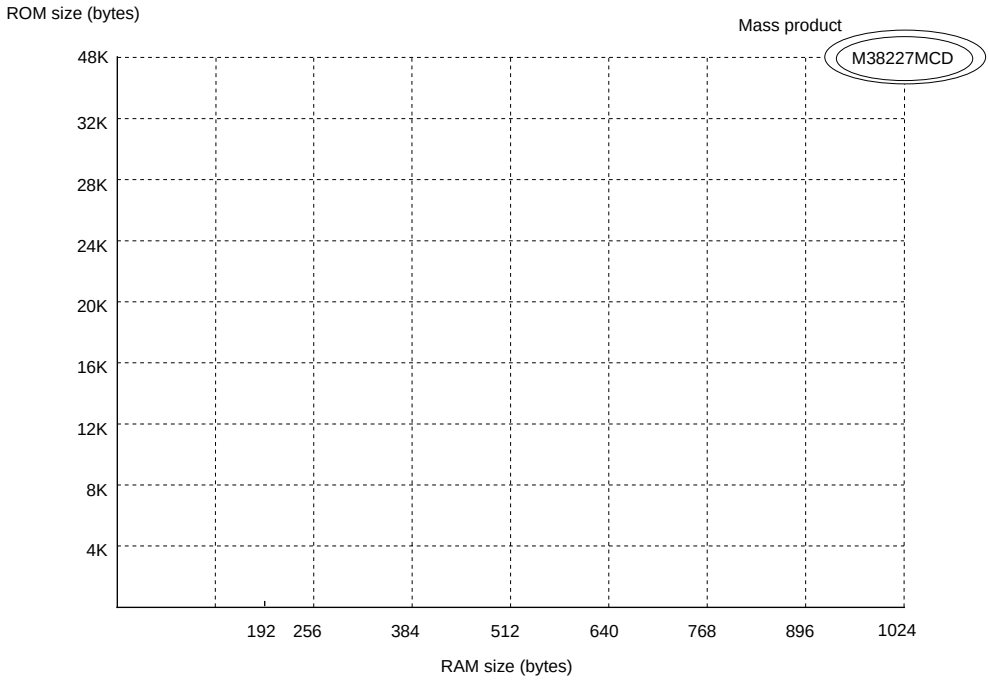


Fig. 6 Memory expansion plan for extended operating temperature version

Currently products are listed below.

Table 4 List of products for extended operating temperature version As of Feb. 2002

Product	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38227MCDXXXFP	49152(49022)	1024	80P6N-A	Mask ROM version

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GROUP EXPANSION (M VERSION)

Mitsubishi plans to expand the 3822 group (M version) as follows:

Memory Type

Support for Mask ROM version.

Memory Size

ROM size ..... 16 K to 24 K bytes
RAM size ..... 512 to 640 bytes

Package

80P6N-A ..... 0.8 mm-pitch plastic molded QFP
80P6S-A ..... 0.65 mm-pitch plastic molded QFP
80P6Q-A ..... 0.5 mm-pitch plastic molded QFP

Memory Expansion Plan

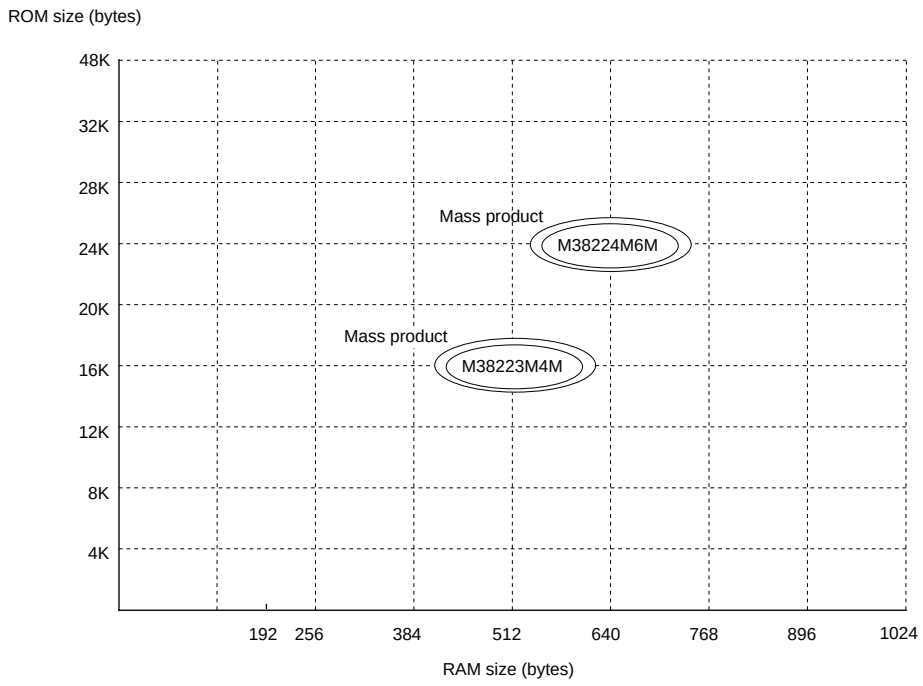


Fig. 7 Memory expansion plan for M version

Currently products are listed below.

Table 5 List of products for M version As of Feb. 2002

Product	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38223M4MXXXFP	16384 (16254)	512	80P6N-A	Mask ROM version
M38223M4MXXXGP			80P6S-A	Mask ROM version
M38223M4MXXXHP			80P6Q-A	Mask ROM version
M38224M6MXXXFP	24576 (24446)	640	80P6N-A	Mask ROM version
M38224M6MXXXHP			80P6Q-A	Mask ROM version

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GROUP EXPANSION (H VERSION)

Mitsubishi plans to expand the 3822 group (H version) as follows:

Memory Type

Support for Mask ROM version.

Memory Size

ROM size ..... 16 K to 48 K bytes
RAM size ..... 512 to 1024 bytes

Package

80P6N-A ..... 0.8 mm-pitch plastic molded QFP
80P6Q-A ..... 0.5 mm-pitch plastic molded QFP

Memory Expansion Plan

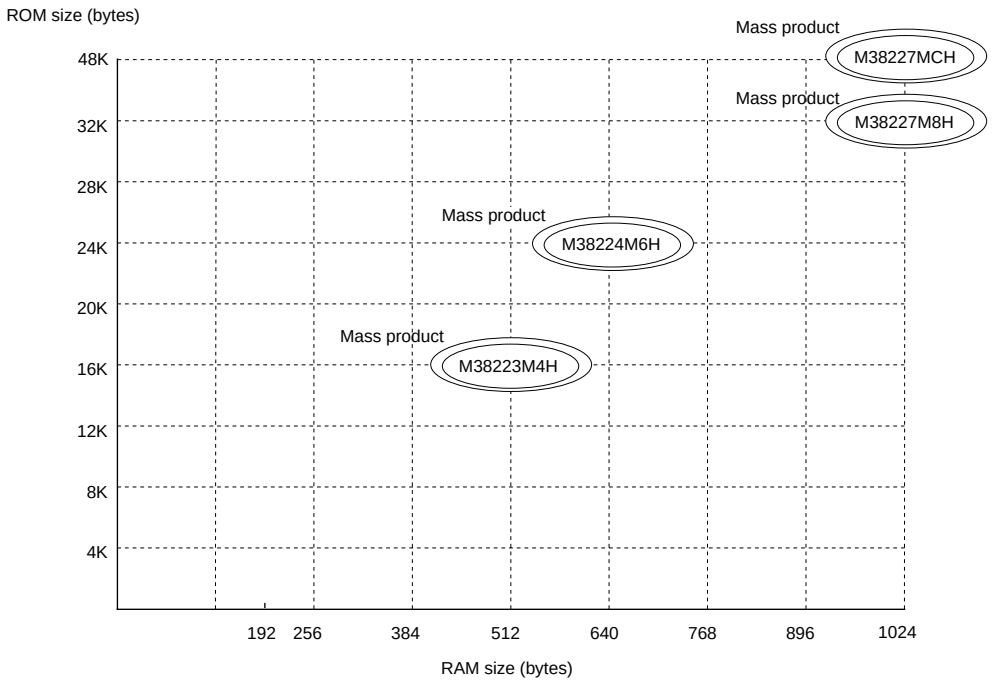


Fig. 8 Memory expansion plan for H version

Currently products are listed below.

Table 6 List of products for H version As of Feb. 2002

Product	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38223M4HXXXFP	16384 (16254)	512	80P6N-A	Mask ROM version
M38223M4HXXXHP			80P6Q-A	Mask ROM version
M38224M6HXXXFP	24576 (24446)	640	80P6N-A	Mask ROM version
M38224M6HXXXHP			80P6Q-A	Mask ROM version
M38227M8HXXXFP	32768 (32638)	1024	80P6N-A	Mask ROM version
M38227M8HXXXHP			80P6Q-A	Mask ROM version
M38227MCHXXXFP	49152 (49022)		80P6N-A	Mask ROM version
M38227MCHXXXHP			80P6Q-A	Mask ROM version

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FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 3822 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instruction cannot be used.

The STP, WIT, MUL, and DIV instruction can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 10.

Store registers other than those described in Figure 10 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

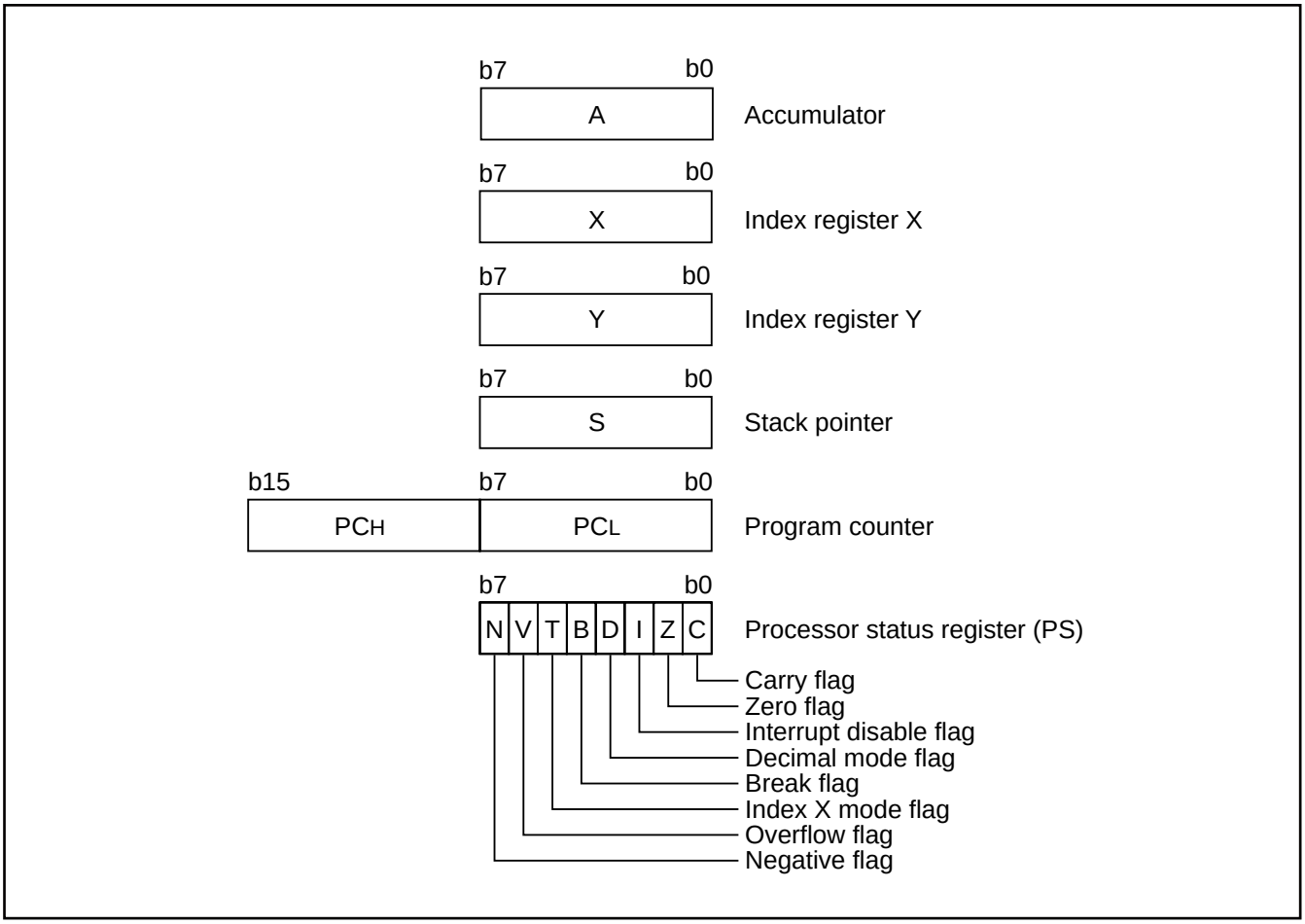


Fig.9 740 Family CPU register structure

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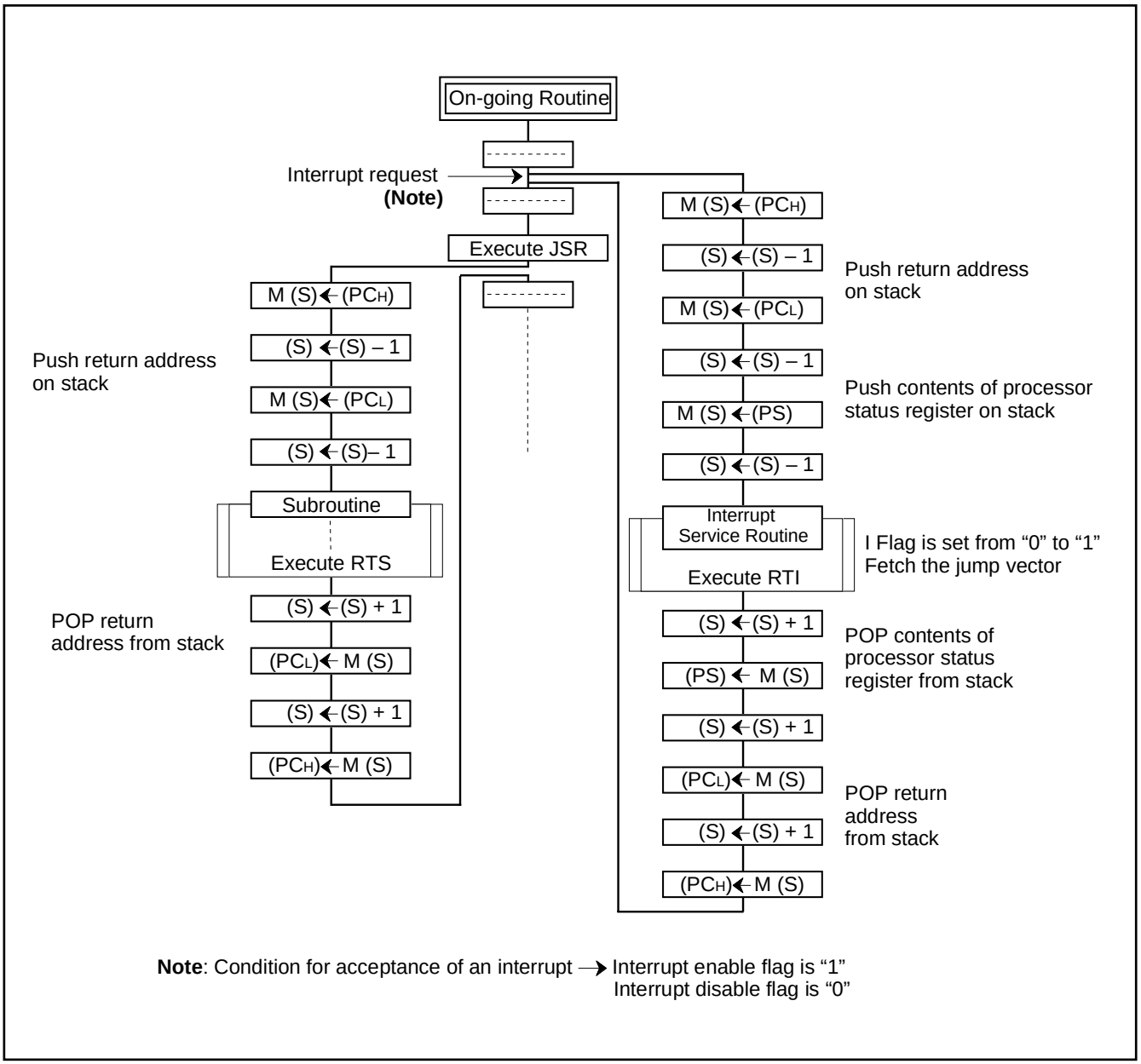


Fig. 10 Register push and pop at interrupt generation and subroutine call

Table 7 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

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[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)
The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)
The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

•Bit 2: Interrupt disable flag (I)
The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
Interrupts are disabled when the I flag is “1”.

•Bit 3: Decimal mode flag (D)
The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”. Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

•Bit 4: Break flag (B)
The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.

•Bit 5: Index X mode flag (T)
When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)
The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)
The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 8 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

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[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit and the internal system clock selection bit.
The CPU mode register is allocated at address 003B16.

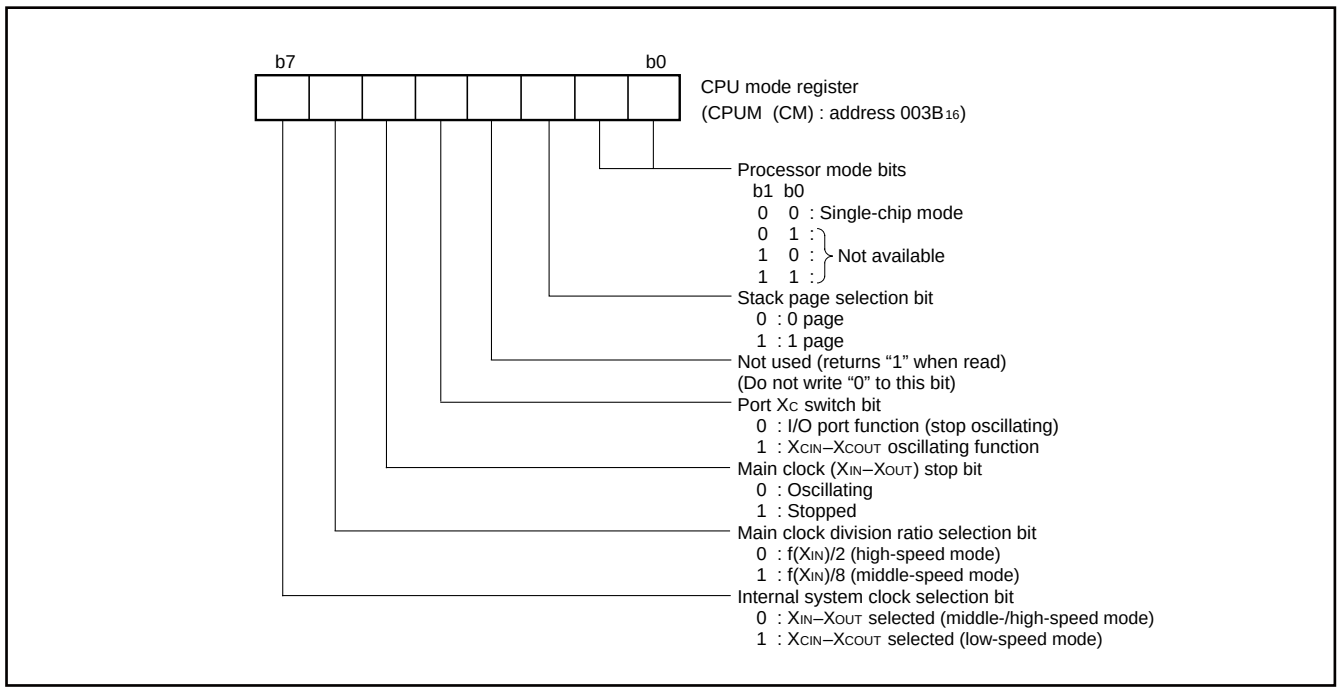


Fig. 11 Structure of CPU mode register

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MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function register (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address $XXXX_{16}$
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$

ROM area

ROM size (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}
36864	7000_{16}	7080_{16}
40960	6000_{16}	6080_{16}
45056	5000_{16}	5080_{16}
49152	4000_{16}	4080_{16}

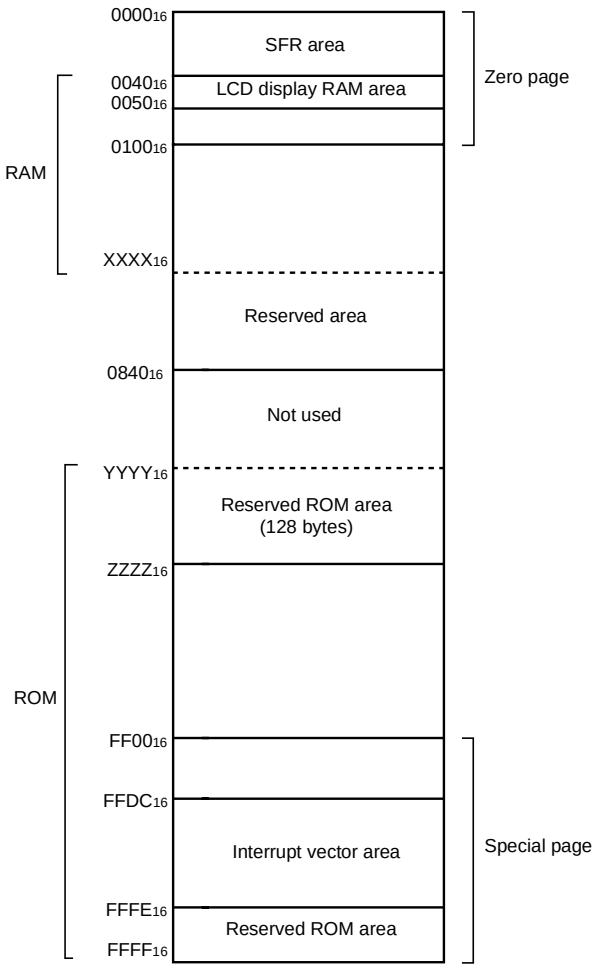


Fig. 12 Memory map diagram

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0000_{16}	Port P0 (P0)	0020_{16}	Timer X (low) (TXL)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Timer X (high) (TXH)
0002_{16}	Port P1 (P1)	0022_{16}	Timer Y (low) (TYL)
0003_{16}	Port P1 output control register (P1D)	0023_{16}	Timer Y (high) (TYH)
0004_{16}	Port P2 (P2)	0024_{16}	Timer 1 (T1)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer 2 (T2)
0006_{16}	Port P3 (P3)	0026_{16}	Timer 3 (T3)
0007_{16}		0027_{16}	Timer X mode register (TXM)
0008_{16}	Port P4 (P4)	0028_{16}	Timer Y mode register (TYM)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 123 mode register (T123M)
$000A_{16}$	Port P5 (P5)	$002A_{16}$	ϕ output control register (CKOUT)
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	
$000C_{16}$	Port P6 (P6)	$002C_{16}$	
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	
$000E_{16}$	Port P7 (P7)	$002E_{16}$	
$000F_{16}$	Port P7 direction register (P7D)	$002F_{16}$	
0010_{16}		0030_{16}	
0011_{16}		0031_{16}	
0012_{16}		0032_{16}	
0013_{16}		0033_{16}	
0014_{16}		0034_{16}	A-D control register (ADCON)
0015_{16}		0035_{16}	A-D conversion register (AD)
0016_{16}	PULL register A (PULLA)	0036_{16}	
0017_{16}	PULL register B (PULLB)	0037_{16}	
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	Segment output enable register (SEG)
0019_{16}	Serial I/O status register (SIOSTS)	0039_{16}	LCD mode register (LM)
$001A_{16}$	Serial I/O control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1(IREQ1)
$001D_{16}$		$003D_{16}$	Interrupt request register 2(IREQ2)
$001E_{16}$		$003E_{16}$	Interrupt control register 1(ICON1)
$001F_{16}$		$003F_{16}$	Interrupt control register 2(ICON2)

Fig. 13 Memory map of special function register (SFR)

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I/O PORTS

Direction Registers (ports P2, P41-P47, and P5-P7)

The 3822 group has 49 programmable I/O pins arranged in seven I/O ports (ports P0–P2, P41–P47 and P5-P7). The I/O ports P2, P41–P47 and P5-P7 have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Direction Registers (ports P0 and P1)

Ports P0 and P1 have direction registers which determine the input/output direction of each individual port.

Each port in a direction register corresponds to one port, each port can be set to be input or output. When "0" is written to the bit 0 of a direction register, that port becomes an input port. When "1" is written to that port, that port becomes an output port. Bits 1 to 7 of ports P0 and P1 direction registers are not used.

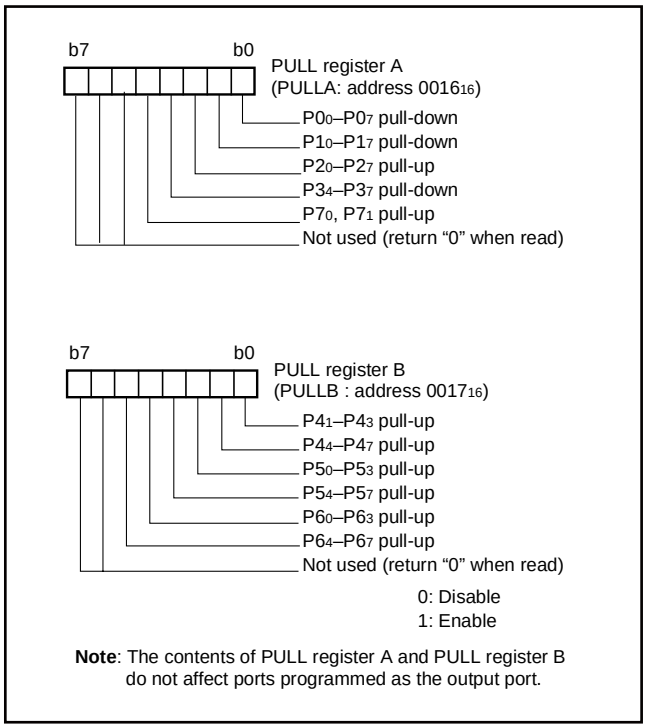
Ports P3 and P40

These ports are only for input.

Pull-up/Pull-down Control

By setting the PULL register A (address 0016$_{16}$) or the PULL register B (address 0017$_{16}$), ports except for port P40 can control either pull-down or pull-up (pins that are shared with the segment output pins for LCD are pull-down; all other pins are pull-up) with a program.

However, the contents of PULL register A and PULL register B do not affect ports programmed as the output ports.



Note: The contents of PULL register A and PULL register B do not affect ports programmed as the output port.

Fig. 14 Structure of PULL register A and PULL register B

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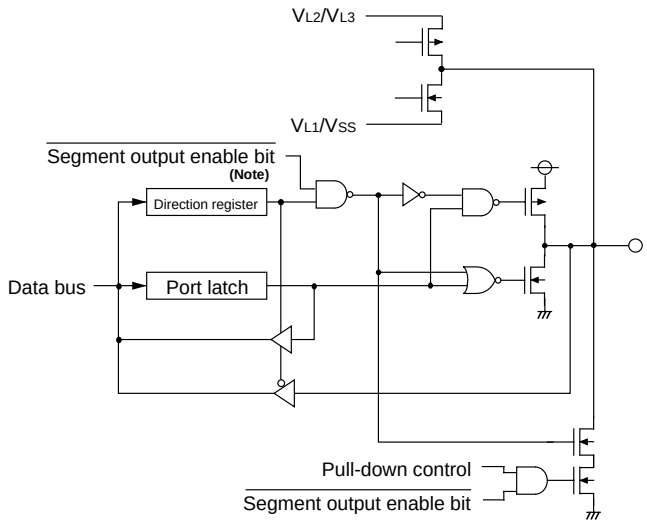
Table 9 List of I/O port function

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P00/SEG16–P07/SEG23	Port P0	Input/output, individual ports	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1)
P10/SEG24–P17/SEG31	Port P1					
P20–P27	Port P2	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Key input (key-on wake-up) interrupt input	PULL register A Interrupt control register 2	(2)
P34/SEG12–P37/SEG15	Port P3	Input	CMOS compatible input level	LCD segment output	PULL register A Segment output enable register	(3)
P40	Port P4	Input	CMOS compatible input level			(4)
P41/ϕ		Input/output, individual bits	CMOS compatible input level CMOS 3-state output	ϕ clock output	PULL register B ϕ output control register	(5)
P42/INT0, P43/INT1				External interrupt input	PULL register B Interrupt edge selection register	(2)
P44/RxD				Serial I/O function I/O	PULL register B	(6)
P45/TxD					Serial I/O control register	(7)
P46/SCLK					Serial I/O status register	(8)
P47/$\overline{SRDY}$					UART control register	(9)
P50/INT2, P51/INT3	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	External interrupt input	PULL register B Interrupt edge selection register	(2)
P52/RTP0, P53/RTP1				Real time port function output	PULL register B Timer X mode register	(10)
P54/CNTR0				Timer X function I/O	PULL register B Timer X mode register	(11)
P55/CNTR1				Timer Y function input	PULL register B Timer Y mode register	(12)
P56/TOUT				Timer 2 function output	PULL register B Timer 123 mode register	(13)
P57/ADT				A-D trigger input	PULL register B A-D control register	(12)
P60/AN0–P67/AN7	Port P6	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	A-D conversion input		(14)
P70/XCOUT	Port P7	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Sub-clock generating circuit I/O	PULL register A CPU mode register	(15)
P71/XCIN						(16)
COM0–COM3	Common	Output	LCD common output		LCD mode register	(17)
SEG0–SEG11	Segment	Output	LCD segment output			(18)

Notes1: How to use double-function ports as function I/O ports, refer to the applicable sections.
2: Make sure that the input level at each pin is either 0 V or VCC during execution of the STP instruction. When an input level is at an intermediate potential, a current will flow VCC to VSS through the input-stage gate.

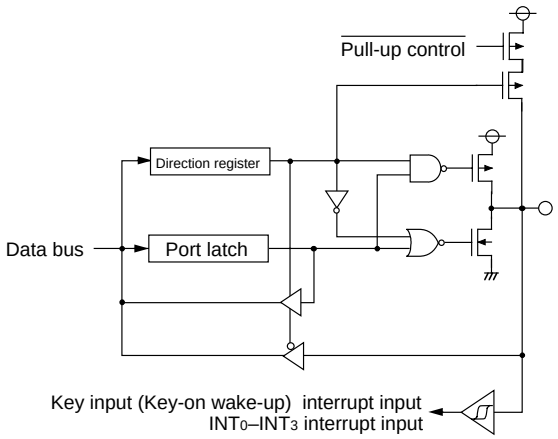
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(1) Ports P0, P1

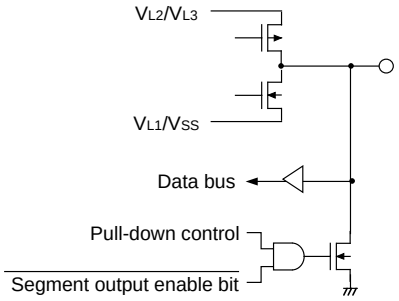


Note: Bit 0 of direction register.

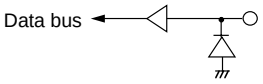
(2) Ports P2, P42, P43, P50, P51



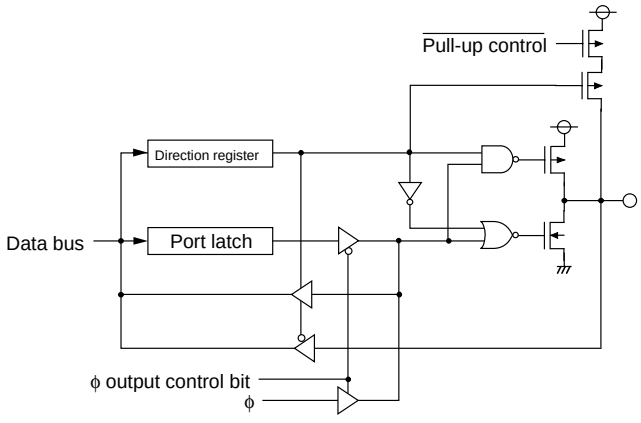
(3) Ports P34–P37



(4) Port P40



(5) Port P41



(6) Port P44

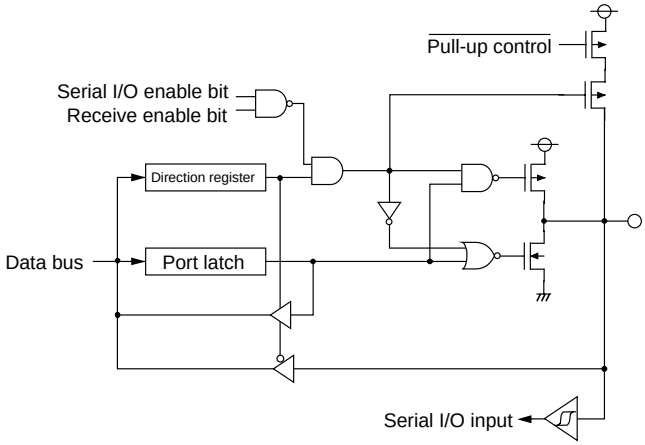


Fig. 15 Port block diagram (1)

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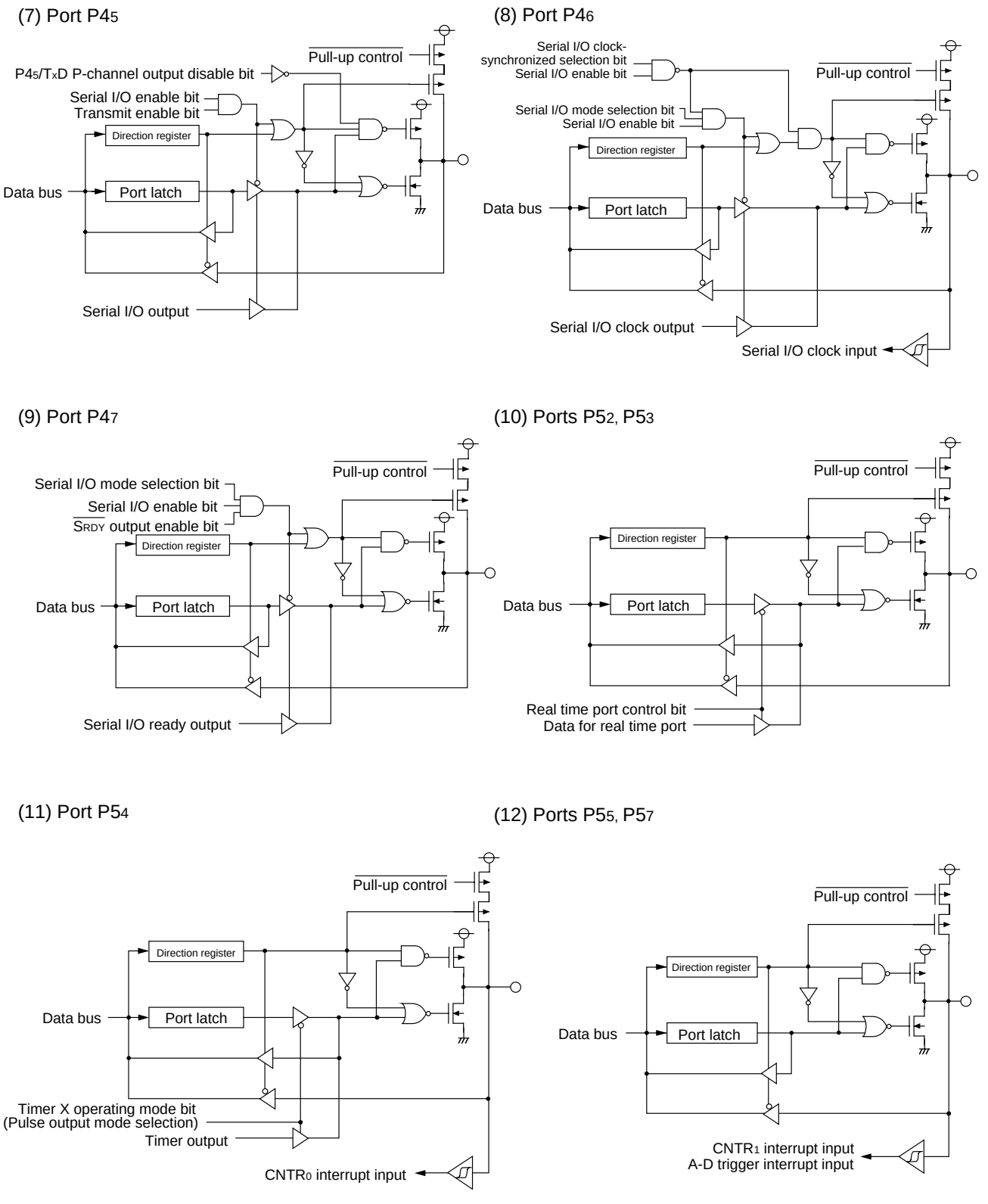
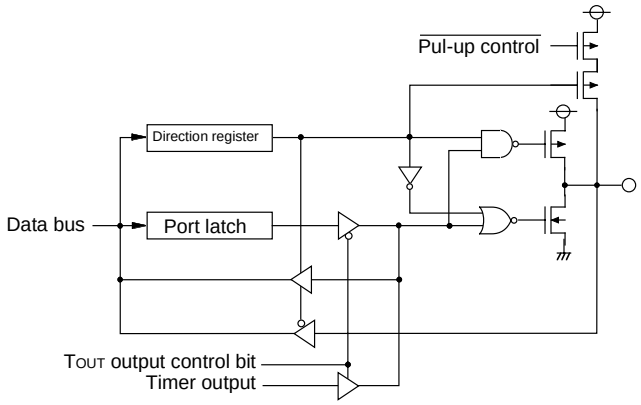


Fig. 16 Port block diagram (2)

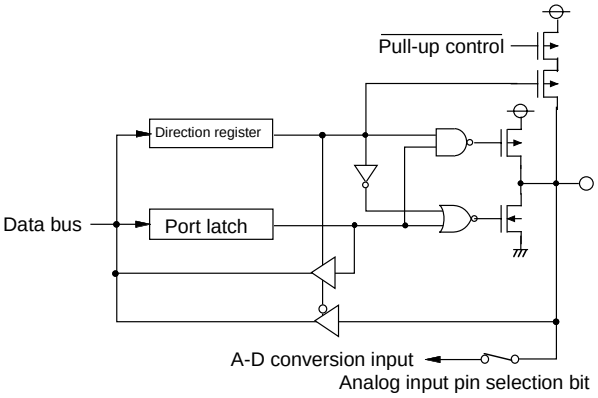
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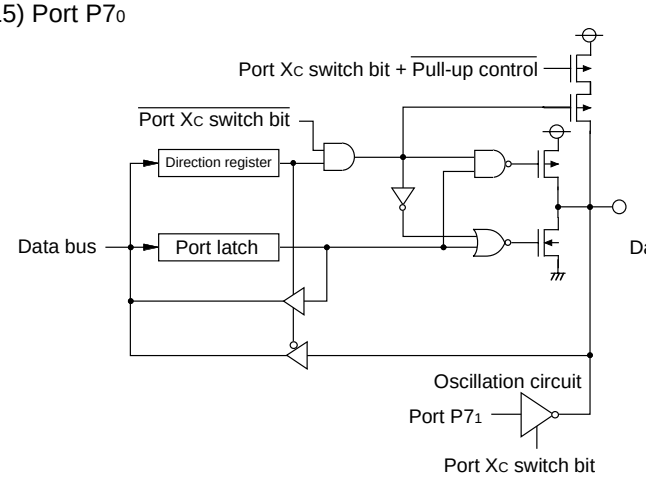
(13) Port $P5_6$



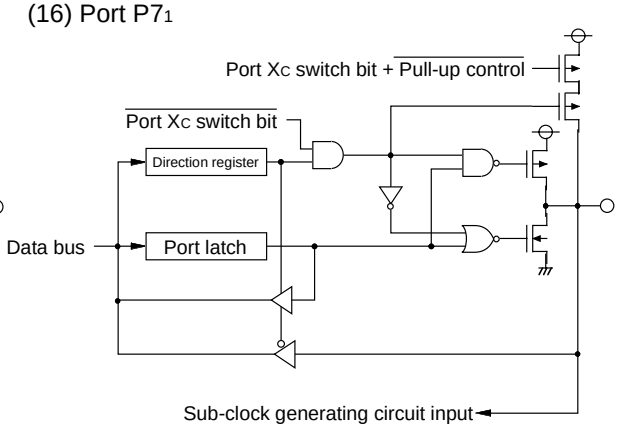
(14) Port P6



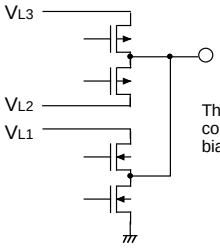
(15) Port $P7_0$



(16) Port $P7_1$

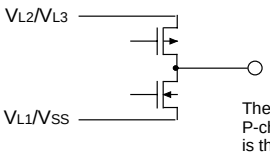


(17) COM_0–COM_3



The gate input signal of each transistor is controlled by the LCD duty ratio and the bias value.

(18) SEG_0–SEG_{11}



The voltage applied to the sources of P-channel and N-channel transistors is the controlled voltage by the bias value.

Fig. 17 Port block diagram (3)

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INTERRUPTS

Interrupts occur by seventeen sources: eight external, eight internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”.

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The contents of the program counter and processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

■Notes on interrupts

When setting the followings, the interrupt request bit may be set to “1”.

•When setting external interrupt active edge
Related register: Interrupt edge selection register (address $3A_{16}$)
Timer X mode register (address 27_{16})
Timer Y mode register (address 28_{16})

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
Related register: A-D control regsiter (address 34_{16})

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

①Set the corresponding interrupt enable bit to “0” (disabled).
②Set the interrupt edge select bit or the interrupt source select bit to “1”.
③Set the corresponding interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the corresponding interrupt enable bit to “1” (enabled).

Table 10 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses **(Note 1)**		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset **(Note 2)**	1	$FFFD_{16}$	$FFFC_{16}$	At reset	Non-maskable
INT_0	2	$FFFB_{16}$	$FFFA_{16}$	At detection of either rising or falling edge of INT_0 input	External interrupt (active edge selectable)
INT_1	3	$FFF9_{16}$	$FFF8_{16}$	At detection of either rising or falling edge of INT_1 input	External interrupt (active edge selectable)
Serial I/O reception	4	$FFF7_{16}$	$FFF6_{16}$	At completion of serial I/O data reception	Valid when serial I/O is selected
Serial I/O transmission	5	$FFF5_{16}$	$FFF4_{16}$	At completion of serial I/O transmit shift or when transmission buffer is empty	Valid when serial I/O is selected
Timer X	6	$FFF3_{16}$	$FFF2_{16}$	At timer X underflow	
Timer Y	7	$FFF1_{16}$	$FFF0_{16}$	At timer Y underflow	
Timer 2	8	$FFEF_{16}$	$FFEE_{16}$	At timer 2 underflow	
Timer 3	9	$FFED_{16}$	$FFEC_{16}$	At timer 3 underflow	
$CNTR_0$	10	$FFEB_{16}$	$FFEA_{16}$	At detection of either rising or falling edge of $CNTR_0$ input	External interrupt (active edge selectable)
$CNTR_1$	11	$FFE9_{16}$	$FFE8_{16}$	At detection of either rising or falling edge of $CNTR_1$ input	External interrupt (active edge selectable)
Timer 1	12	$FFE7_{16}$	$FFE6_{16}$	At timer 1 underflow	
INT_2	13	$FFE5_{16}$	$FFE4_{16}$	At detection of either rising or falling edge of INT_2 input	External interrupt (active edge selectable)
INT_3	14	$FFE3_{16}$	$FFE2_{16}$	At detection of either rising or falling edge of INT_3 input	External interrupt (active edge selectable)
Key input (Key-on wake-up)	15	$FFE1_{16}$	$FFE0_{16}$	At falling of conjunction of input level for port P2 (at input mode)	External interrupt (Valid at falling)
ADT	16	$FFDF_{16}$	$FFDE_{16}$	At falling of ADT input	Valid when ADT interrupt is selected, External interrupt (Valid at falling)
A-D conversion				At completion of A-D conversion	Valid when A-D interrupt is selected
BRK instruction	17	$FFDD_{16}$	$FFDC_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

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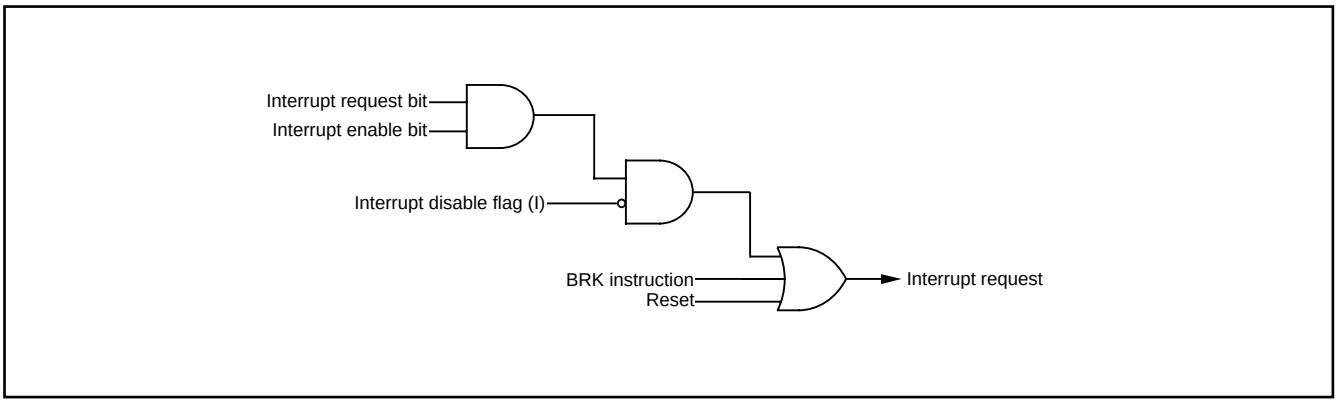


Fig. 18 Interrupt control

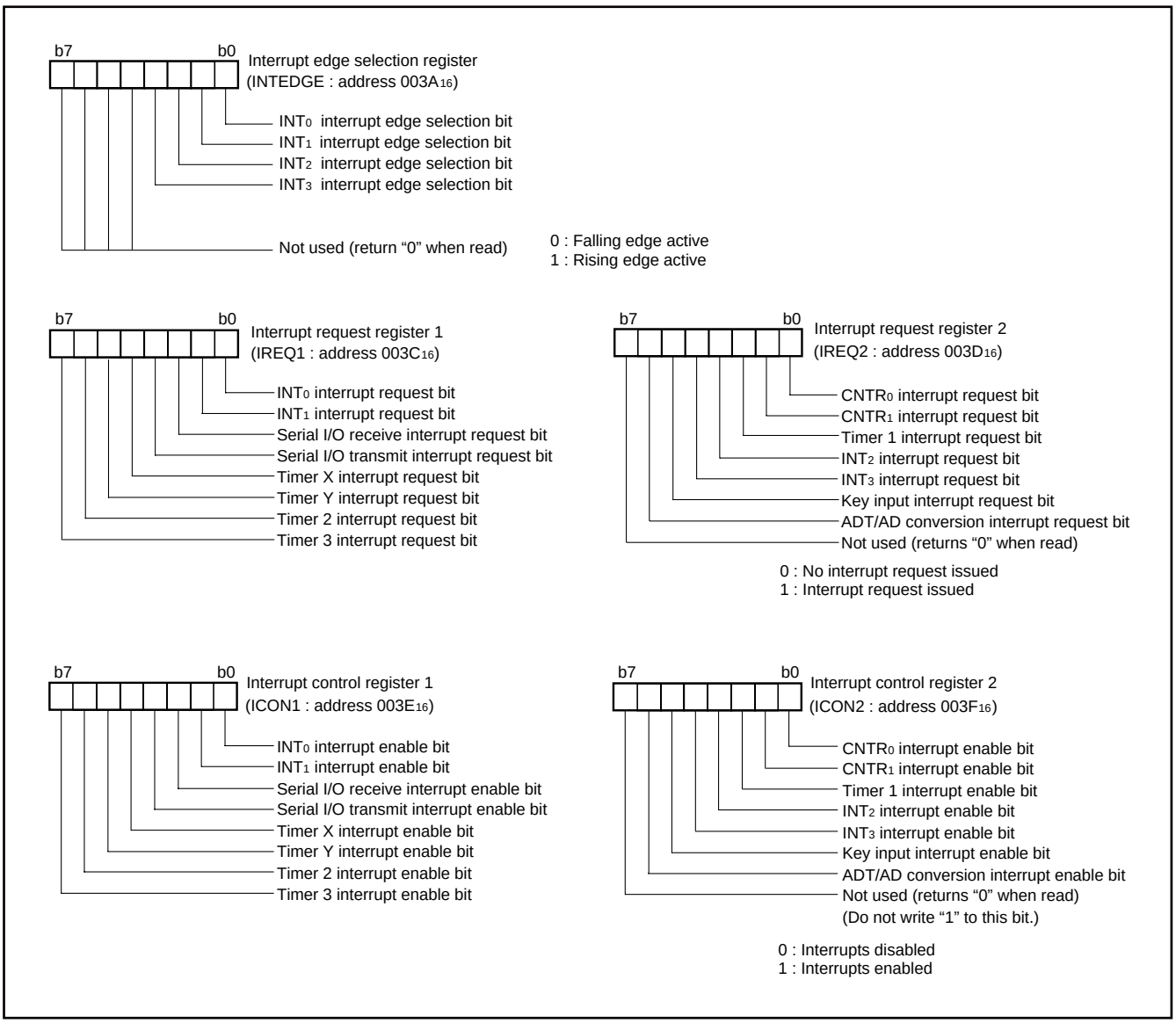


Fig. 19 Structure of interrupt-related registers

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Key Input Interrupt (Key-on wake-up)

A Key-on wake-up interrupt request is generated by applying a falling edge to any pin of port P2 that have been set to input mode. In other words, it is generated when AND of input level goes from "1" to "0". An example of using a key input interrupt is shown in Figure 20, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P20–P23.

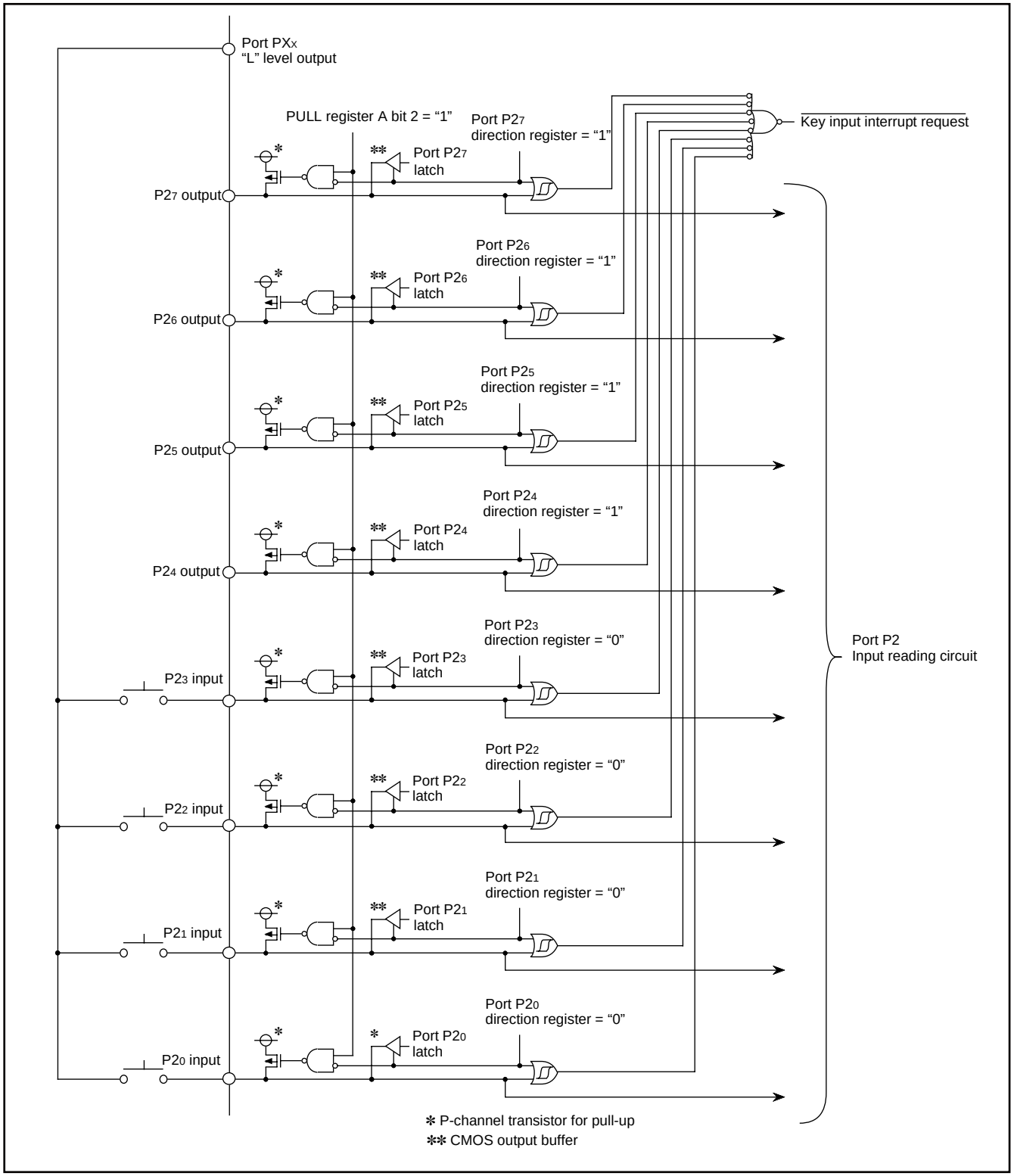


Fig. 20 Connection example when using key input interrupt and port P2 block diagram

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TIMERS

The 3822 group has five timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, and timer 1, timer 2, and timer 3 are 8-bit timers.

All timers are down count timers. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

Read and write operation on 16-bit timer must be performed for both high and low-order bytes. When reading a 16-bit timer, read the high-order byte first. When writing to a 16-bit timer, write the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during the write operation, or when writing during the read operation.

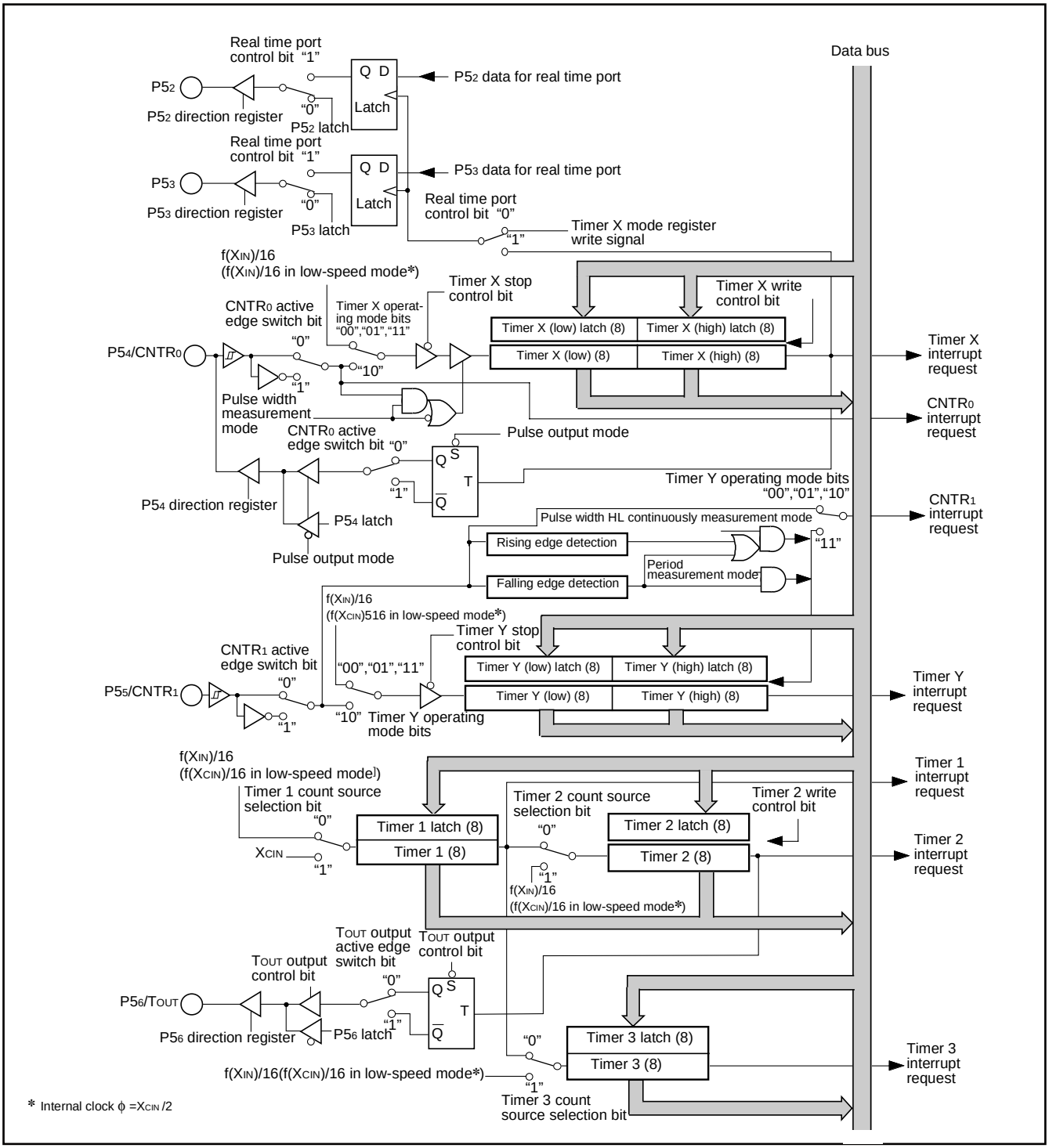


Fig. 21 Timer block diagram

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Timer X

Timer X is a 16-bit timer that can be selected in one of four modes and can be controlled the timer X write and the real time port by setting the timer X mode register.

(1) Timer Mode

The timer counts f(XIN)/16 (or f(XCIN)/16 in low-speed mode).

(2) Pulse Output Mode

Each time the timer underflows, a signal output from the CNTR0 pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to output mode.

(3) Event Counter Mode

The timer counts signals input through the CNTR0 pin.
Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P54 direction register to input mode.

(4) Pulse Width Measurement Mode

The count source is f(XIN)/16 (or f(XCIN)/16 in low-speed mode). If CNTR0 active edge switch bit is “0”, the timer counts while the input signal of CNTR0 pin is at “H”. If it is “1”, the timer counts while the input signal of CNTR0 pin is at “L”. When using a timer in this mode, set the corresponding port P54 direction register to input mode.

●Timer X write control

If the timer X write control bit is “0”, when the value is written in the address of timer X, the value is loaded in the timer X and the latch at the same time.
If the timer X write control bit is “1”, when the value is written in the address of timer X, the value is loaded only in the latch. The value in the latch is loaded in timer X after timer X underflows.
If the value is written in latch only, when writing in the timer latch at the timer underflow, the value is set in the timer and the latch at one time. Additionally, unexpected value may be set in the high-order counter when the writing in high-order latch and the underflow of timer X are performed at the same timing.

●Real time port control

While the real time port function is valid, data for the real time port are output from ports P52 and P53 each time the timer X underflows. (However, after rewriting a data for real time port, if the real time port control bit is changed from “0” to “1”, data are output independent of the timer X operation.) If the data for the real time port is changed while the real time port function is valid, the changed data are output at the next underflow of timer X.
Before using this function, set the corresponding port direction registers to output mode.

■Note on CNTR0 interrupt active edge selection

CNTR0 interrupt active edge depends on the CNTR0 active edge switch bit.

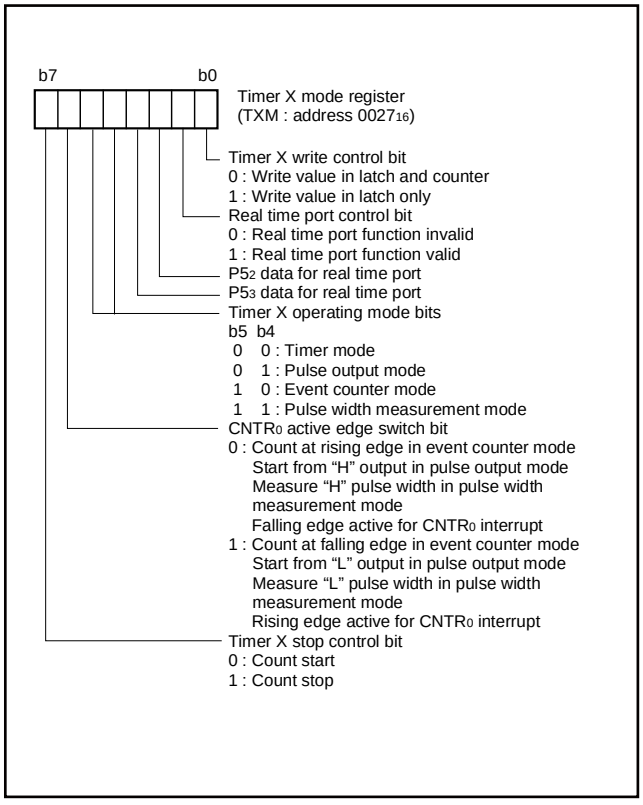


Fig. 22 Structure of timer X mode register

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Timer Y

Timer Y is a 16-bit timer that can be selected in one of four modes.

(1) Timer Mode

The timer counts f(XIN)/16 (or f(XCIN)/16 in low-speed mode).

(2) Period Measurement Mode

CNTR1 interrupt request is generated at rising/falling edge of CNTR1 pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down. Except for the above-mentioned, the operation in period measurement mode is the same as in timer mode.

The timer value just before the reloading at rising/falling of CNTR1 pin input signal is retained until the timer Y is read once after the reload.

The rising/falling timing of CNTR1 pin input signal is found by CNTR1 interrupt. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

(3) Event Counter Mode

The timer counts signals input through the CNTR1 pin.

Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

(4) Pulse Width HL Continuously Measurement Mode

CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode. When using a timer in this mode, set the corresponding port P55 direction register to input mode.

■Note on CNTR1 interrupt active edge selection

CNTR1 interrupt active edge depends on the CNTR1 active edge switch bit. However, in pulse width HL continuously measurement mode, CNTR1 interrupt request is generated at both rising and falling edges of CNTR1 pin input signal regardless of the setting of CNTR1 active edge switch bit.

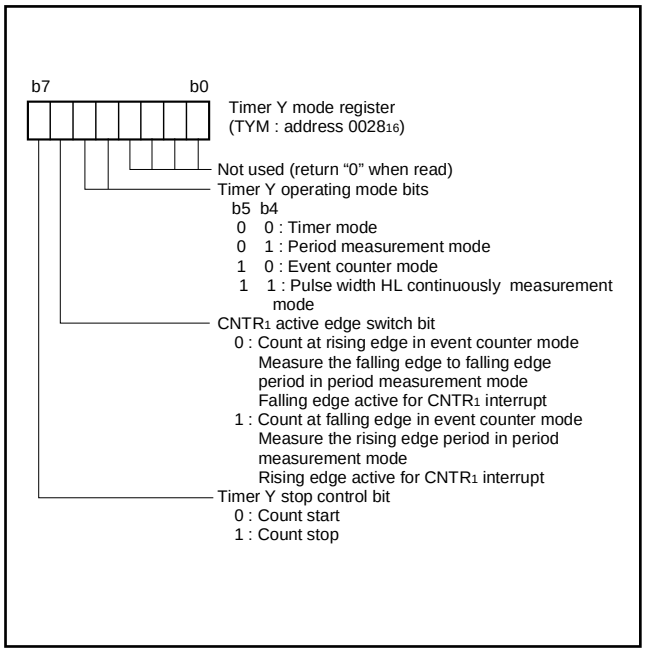


Fig. 23 Structure of timer Y mode register

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Timer 1, Timer 2, Timer 3

Timer 1, timer 2, and timer 3 are 8-bit timers. The count source for each timer can be selected by timer 123 mode register. The timer latch value is not affected by a change of the count source. However, because changing the count source may cause an inadvertent count down of the timer, rewrite the value of timer whenever the count source is changed.

●Timer 2 write control

If the timer 2 write control bit is "0", when the value is written in the address of timer 2, the value is loaded in the timer 2 and the latch at the same time.

If the timer 2 write control bit is "1", when the value is written in the address of timer 2, the value is loaded only in the latch. The value in the latch is loaded in timer 2 after timer 2 underflows.

●Timer 2 output control

When the timer 2 (TOUT) is output enabled, an inversion signal from the TOUT pin is output each time timer 2 underflows.

In this case, set the port shared with the TOUT pin to the output mode.

■Notes on timer 1 to timer 3

When the count source of timer 1 to 3 is changed, the timer counting value may be changed large because a thin pulse is generated in count input of timer . If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may be changed large because a thin pulse is generated in timer 1 output.

Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.

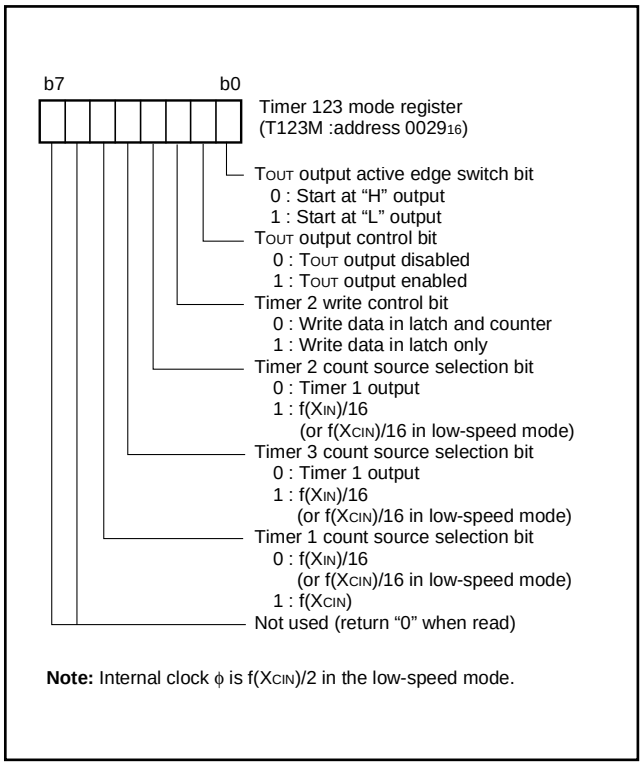


Fig. 24 Structure of timer 123 mode register

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SERIAL I/O

Serial I/O can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O can be selected by setting the mode selection bit of the serial I/O control register to “1”.

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer register.

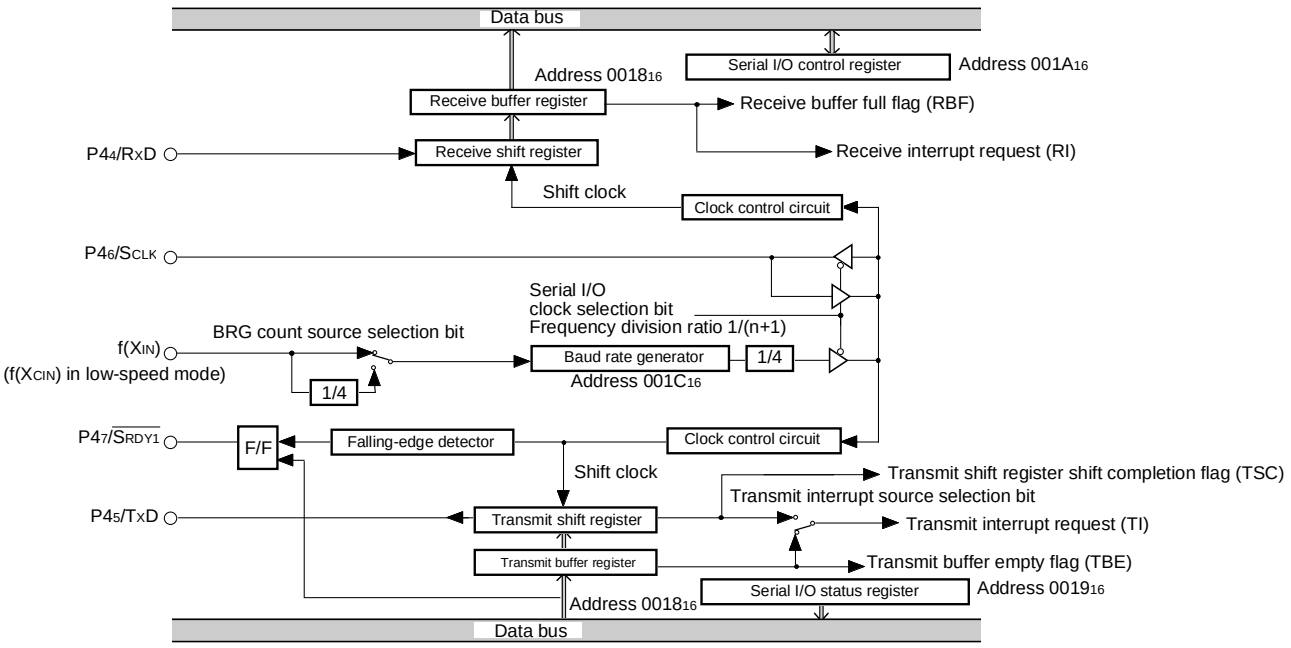
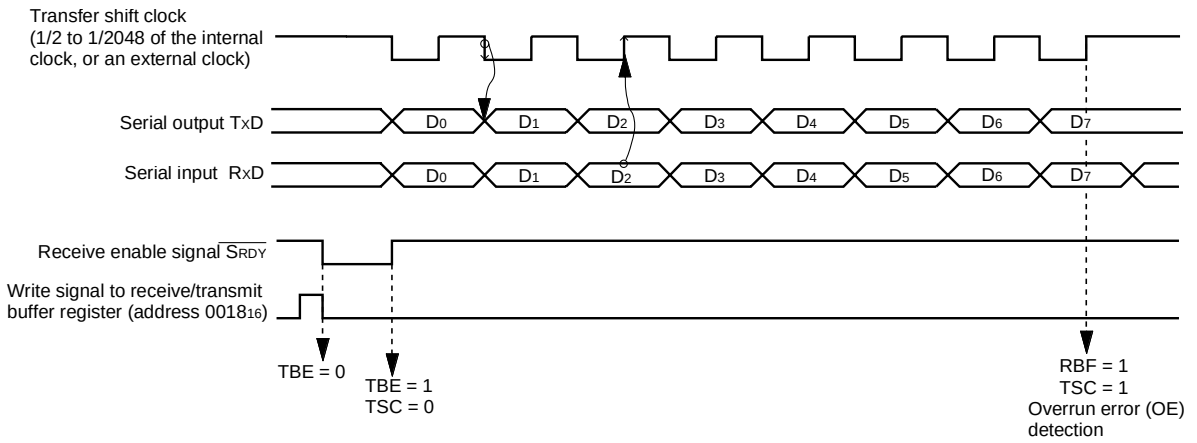


Fig. 25 Block diagram of clock synchronous serial I/O



Notes
1 : The transmit interrupt (TI) can be generated either when the transmit buffer register has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O control register.
2 : If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3 : The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes “1” .

Fig. 26 Operation of clock synchronous serial I/O function

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(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer register, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

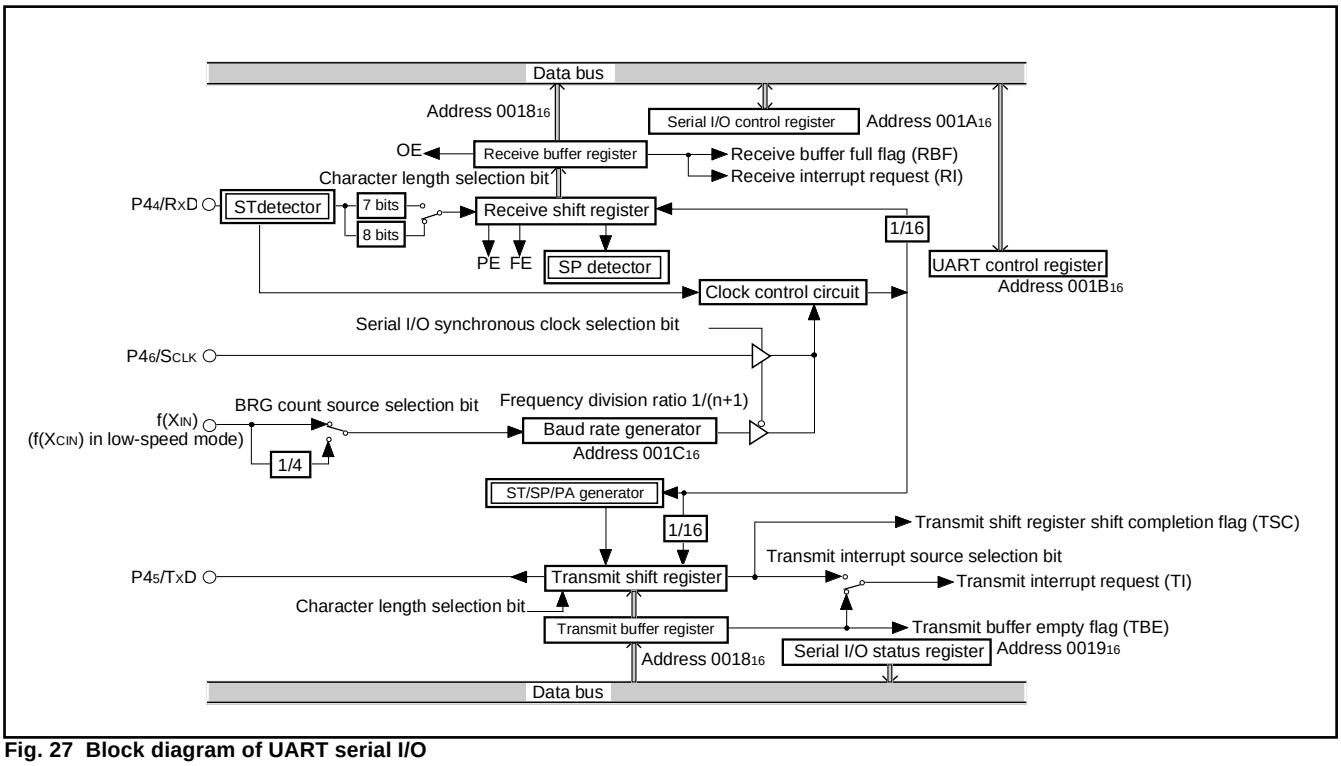
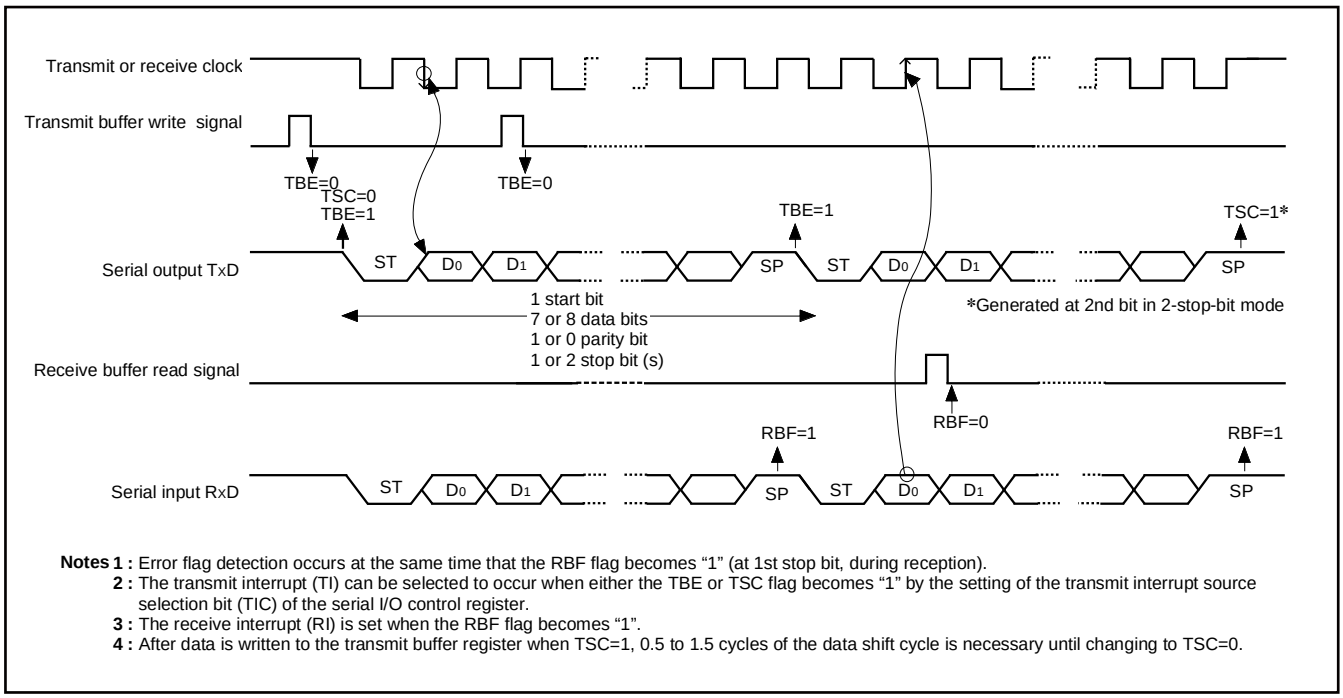


Fig. 27 Block diagram of UART serial I/O



Notes 1 : Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2 : The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes "1" by the setting of the transmit interrupt source selection bit (TIC) of the serial I/O control register.
3 : The receive interrupt (RI) is set when the RBF flag becomes "1".
4 : After data is written to the transmit buffer register when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 28 Operation of UART serial I/O function

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[Transmit Buffer/Receive Buffer Register (TB/RB)] 0018$_{16}$

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is “0”.

[Serial I/O Status Register (SIOSTS)] 0019$_{16}$

The read-only serial I/O status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE. Writing “0” to the serial I/O enable bit (SIOE) also clears all the status flags, including the error flags.

All bits of the serial I/O status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to “1”, the transmit shift register shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O Control Register (SIOCON)] 001A$_{16}$

The serial I/O control register contains eight control bits for the serial I/O function.

[UART Control Register (UARTCON)]001B$_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P4$_5$/TxD pin.

[Baud Rate Generator (BRG)] 001C$_{16}$

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■Notes on serial I/O

When setting the transmit enable bit to “1”, the serial I/O transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronized with the transmission enalbed, take the following sequence.

①Set the serial I/O transmit interrupt enable bit to “0” (disabled).
②Set the transmit enable bit to “1”.
③Set the serial I/O transmit interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the serial I/O transmit interrupt enable bit to “1” (enabled).

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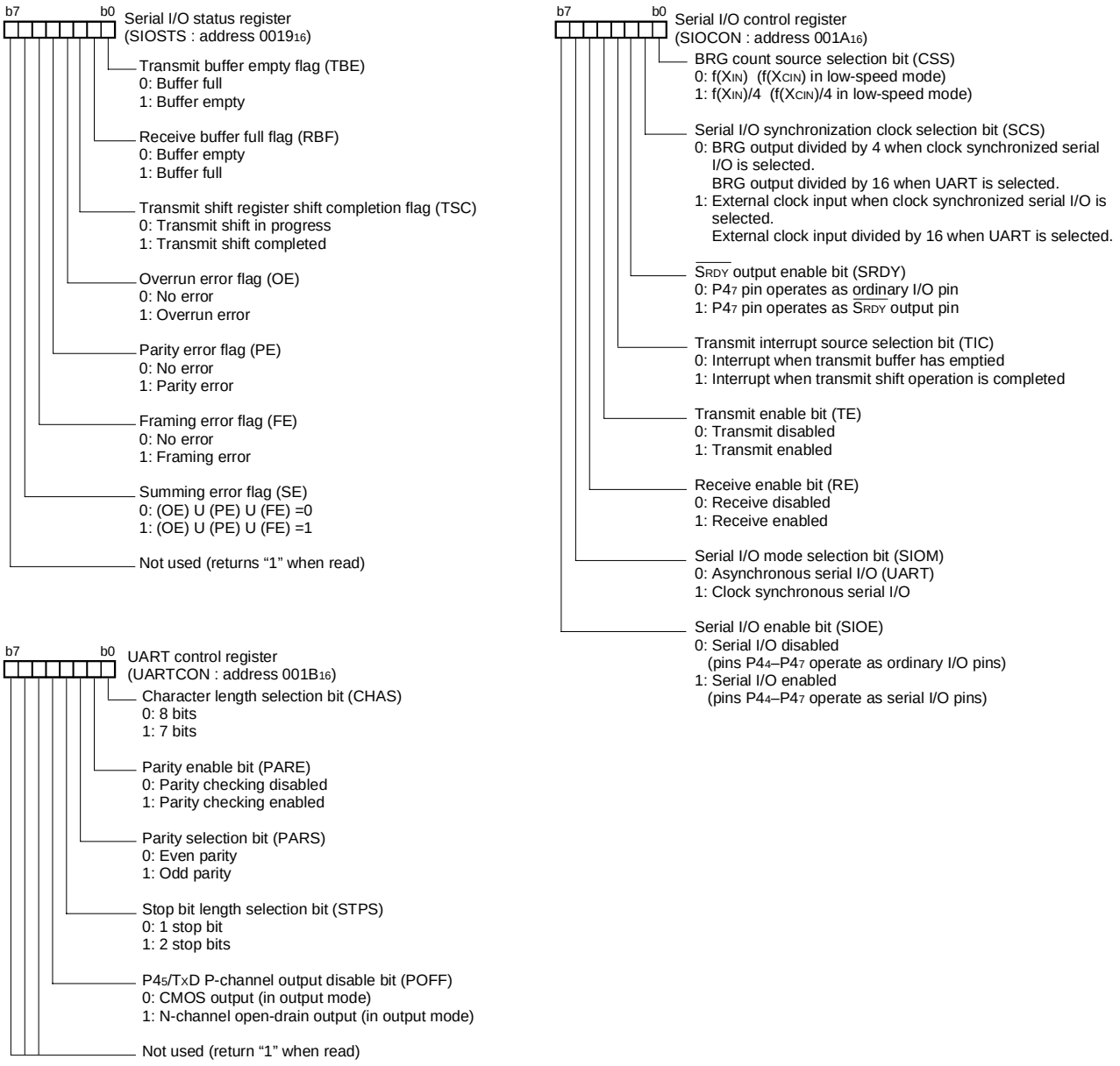


Fig. 29 Structure of serial I/O control registers

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A-D CONVERTER

[A-D Conversion Register (AD)] 0035$_{16}$

The A-D conversion register is a read-only register that contains the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

[A-D Control Register (ADCON)] 0034$_{16}$

The A-D control register controls the A-D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion. Bit 4 controls the transistor which breaks the through current of the resistor ladder. When bit 5, which is the AD external trigger valid bit, is set to "1", this bit enables A-D conversion even by a falling edge of an ADT input. Set ports which share with ADT pins to input when using an A-D external trigger.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AVSS and VREF by 256, and outputs the divided voltages.

[Channel Selector]

The channel selector selects one of the input ports P67/AN7–P60/AN0, and inputs it to the comparator.

[Comparator and Control Circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Note that the comparator is constructed linked to a capacitor, so set f(XIN) to at least 500 kHz during A-D conversion.

Use the clock divided from the main clock XIN as the internal clock ϕ.

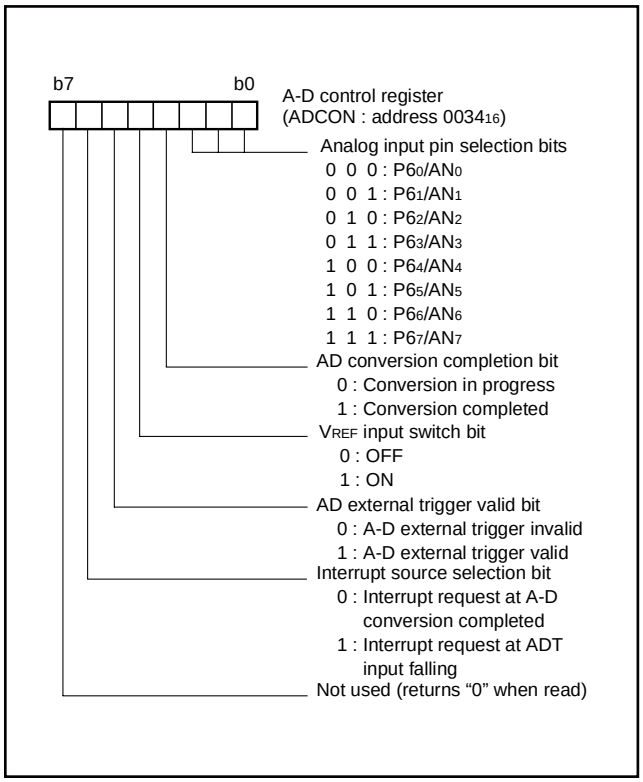


Fig. 30 Structure of A-D control register

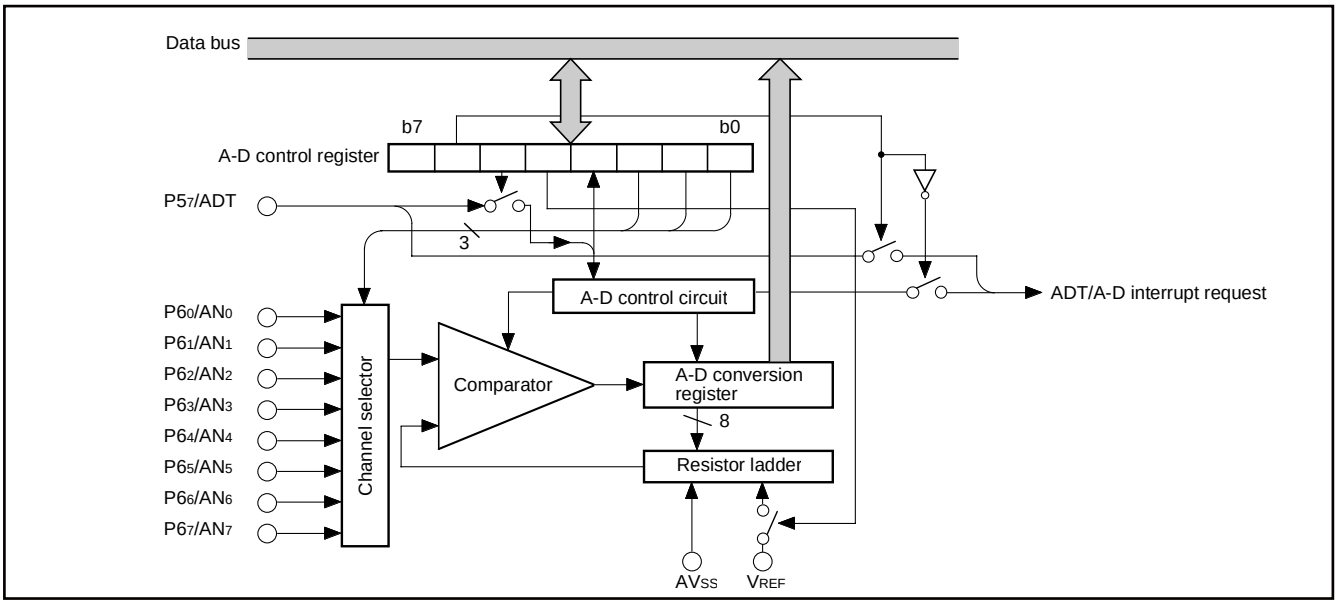


Fig. 31 A-D converter block diagram

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LCD DRIVE CONTROL CIRCUIT

The 3822 group has the built-in Liquid Crystal Display (LCD) drive control circuit consisting of the following.

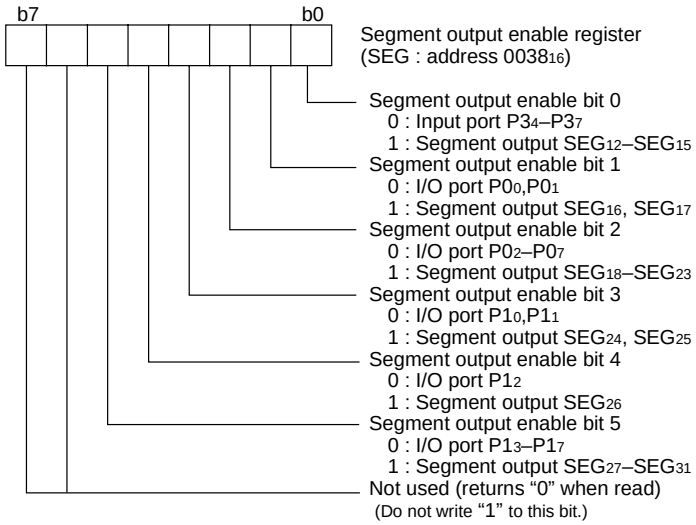
- LCD display RAM
- Segment output enable register
- LCD mode register
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

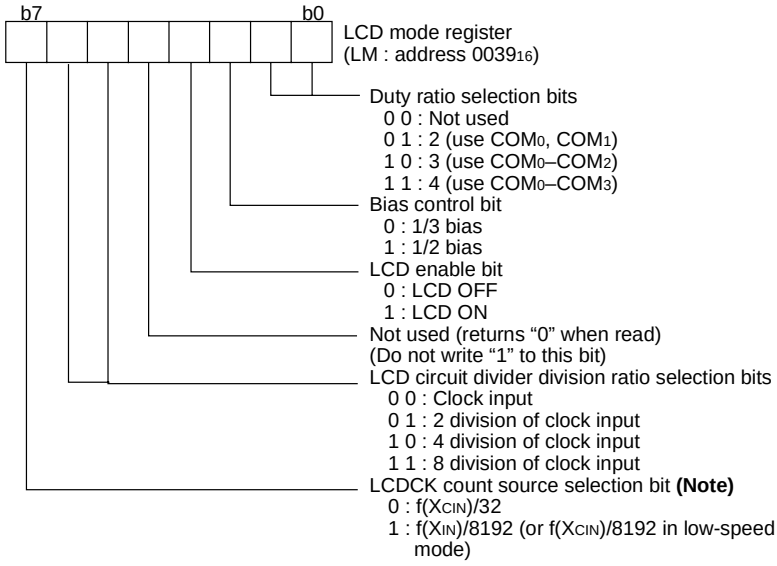
A maximum of 32 segment output pins and 4 common output pins can be used.

Up to 128 pixels can be controlled for LCD display. When the LCD enable bit is set to "1" after data is set in the LCD mode register, the segment output enable register and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 11 Maximum number of display pixels at each duty ratio

Duty ratio	Maximum number of display pixel
2	64 dots or 8 segment LCD 8 digits
3	96 dots or 8 segment LCD 12 digits
4	128 dots or 8 segment LCD 16 digits





Note: LCDCK is a clock for a LCD timing controller.

Fig. 32 Structure of segment output enable register and LCD mode register

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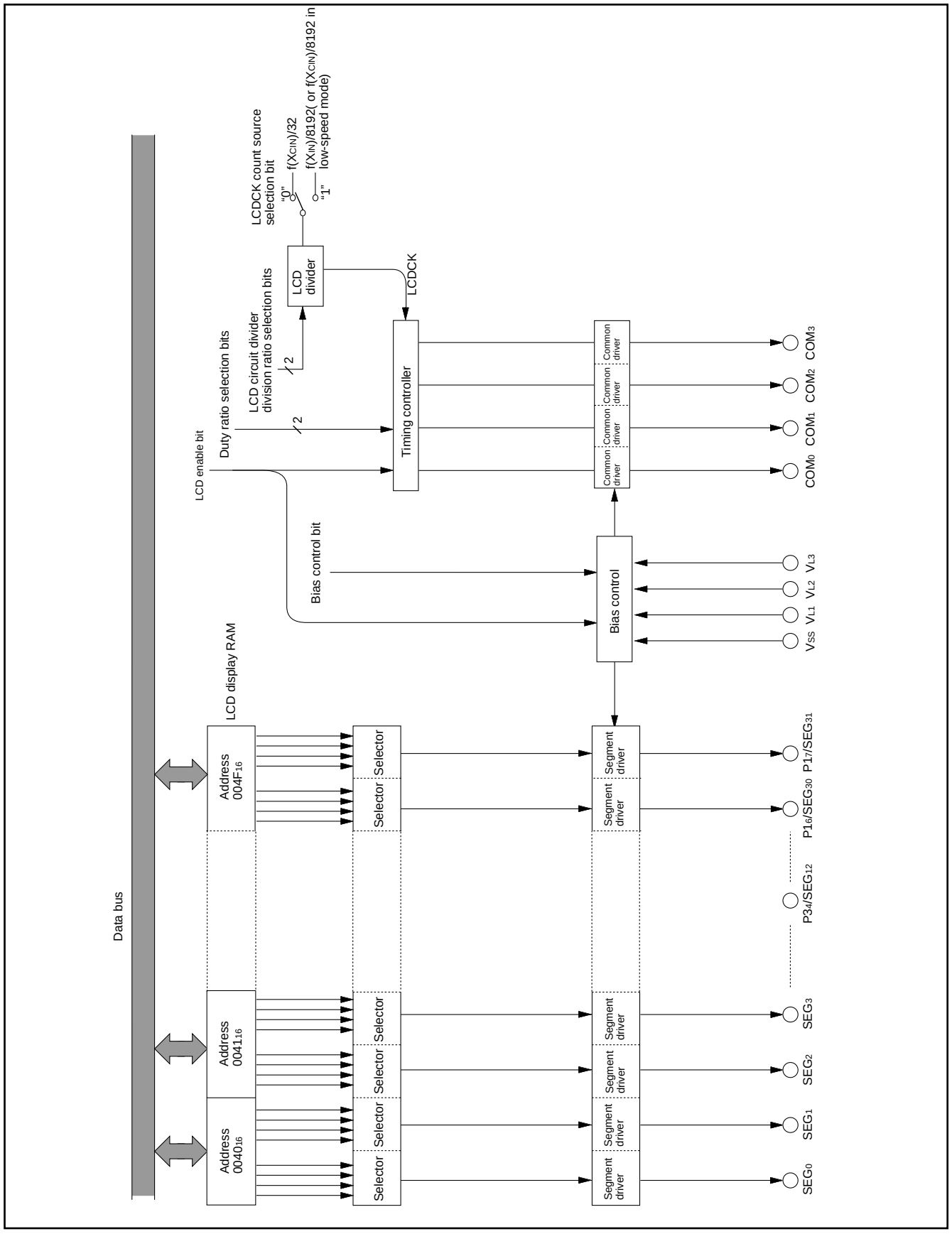


Fig. 33 Block diagram of LCD controller/driver

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Bias Control and Applied Voltage to LCD Power Input Pins

To the LCD power input pins (V_{L1}–V_{L3}), apply the voltage shown in Table 12 according to the bias value.
Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Common Pin and Duty Ratio Control

The common pins (COM_0–COM_3) to be used are determined by duty ratio.
Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).

Table 12 Bias control and applied voltage to V_{L1}–V_{L3}

Bias value	Voltage value
1/3 bias	$V_{L3}=V_{LCD}$ $V_{L2}=2/3\ V_{LCD}$ $V_{L1}=1/3\ V_{LCD}$
1/2 bias	$V_{L3}=V_{LCD}$ $V_{L2}=V_{L1}=1/2\ V_{LCD}$

Note 1: V_{LCD} is the maximum value of supplied voltage for the LCD panel.

Table 13 Duty ratio control and common pins used

Duty ratio	Duty ratio selection bit		Common pins used
	Bit 1	Bit 0	
2	0	1	COM_0, COM_1 **(Note 1)**
3	1	0	COM_0–COM_2 **(Note 2)**
4	1	1	COM_0–COM_3

Notes1: COM_2 and COM_3 are open.
2: COM_3 is open.

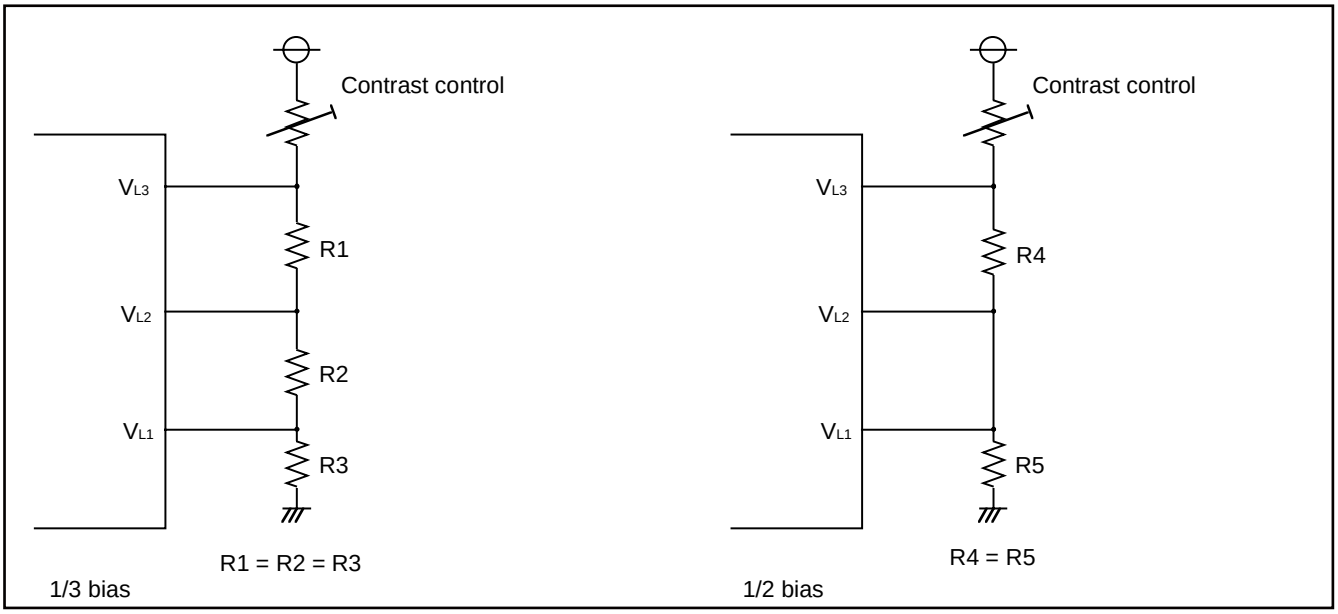


Fig. 34 Example of circuit at each bias

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LCD Display RAM

Address 0040_{16} to $004F_{16}$ is the designated RAM for the LCD display. When "1" are written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

The LCDCK timing frequency (LCD drive timing) is generated internally and the frame frequency can be determined with the following equation;

$$f(LCDCK) = \frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency} = \frac{f(LCDCK)}{\text{(duty ratio)}}$$

Address \ Bit	7	6	5	4	3	2	1	0
0040_{16}	SEG1				SEG0			
0041_{16}	SEG3				SEG2			
0042_{16}	SEG5				SEG4			
0043_{16}	SEG7				SEG6			
0044_{16}	SEG9				SEG8			
0045_{16}	SEG11				SEG10			
0046_{16}	SEG13				SEG12			
0047_{16}	SEG15				SEG14			
0048_{16}	SEG17				SEG16			
0049_{16}	SEG19				SEG18			
$004A_{16}$	SEG21				SEG20			
$004B_{16}$	SEG23				SEG22			
$004C_{16}$	SEG25				SEG24			
$004D_{16}$	SEG27				SEG26			
$004E_{16}$	SEG29				SEG28			
$004F_{16}$	SEG31				SEG30			
	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0

Fig. 35 LCD display RAM map

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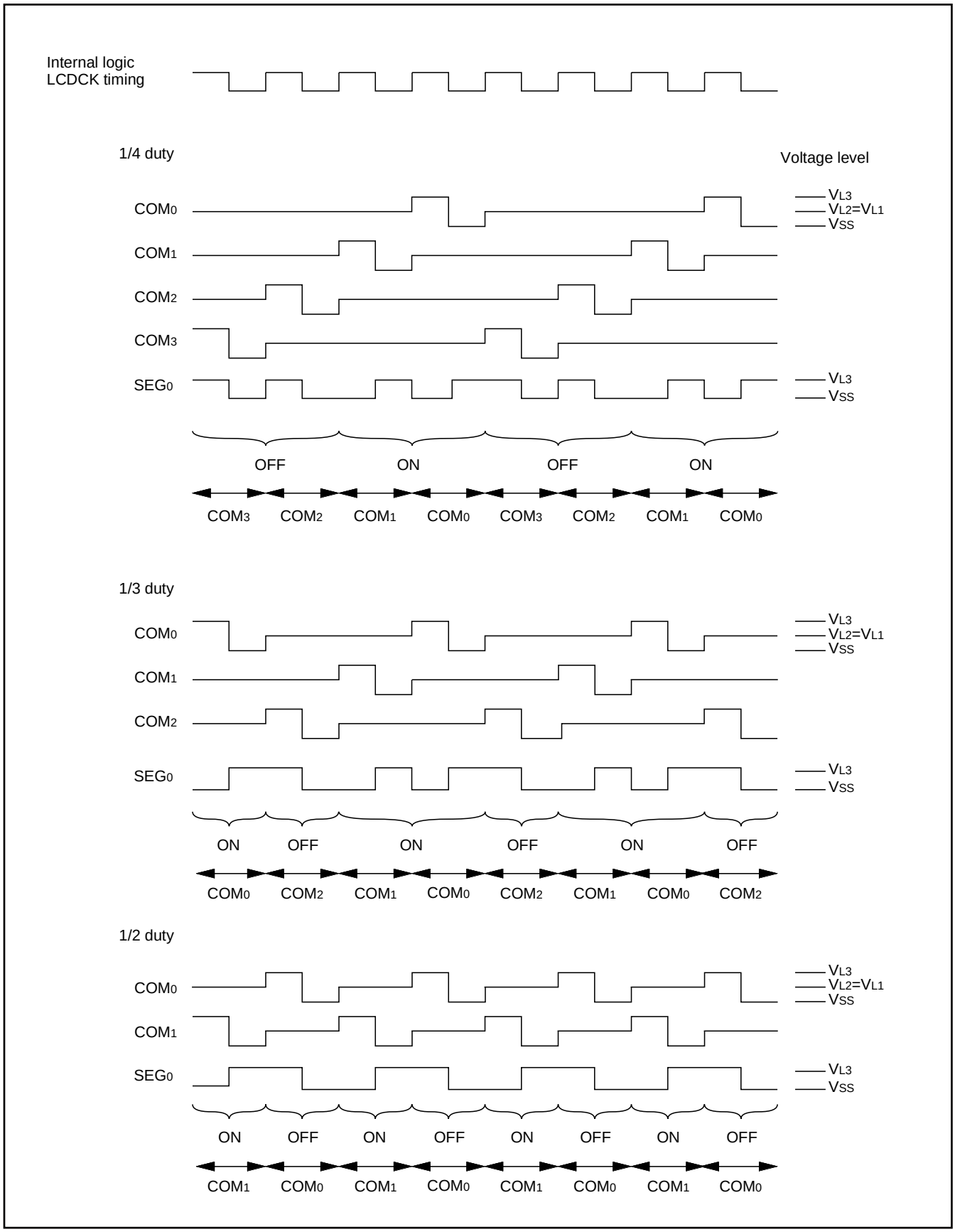


Fig. 36 LCD drive waveform (1/2 bias)

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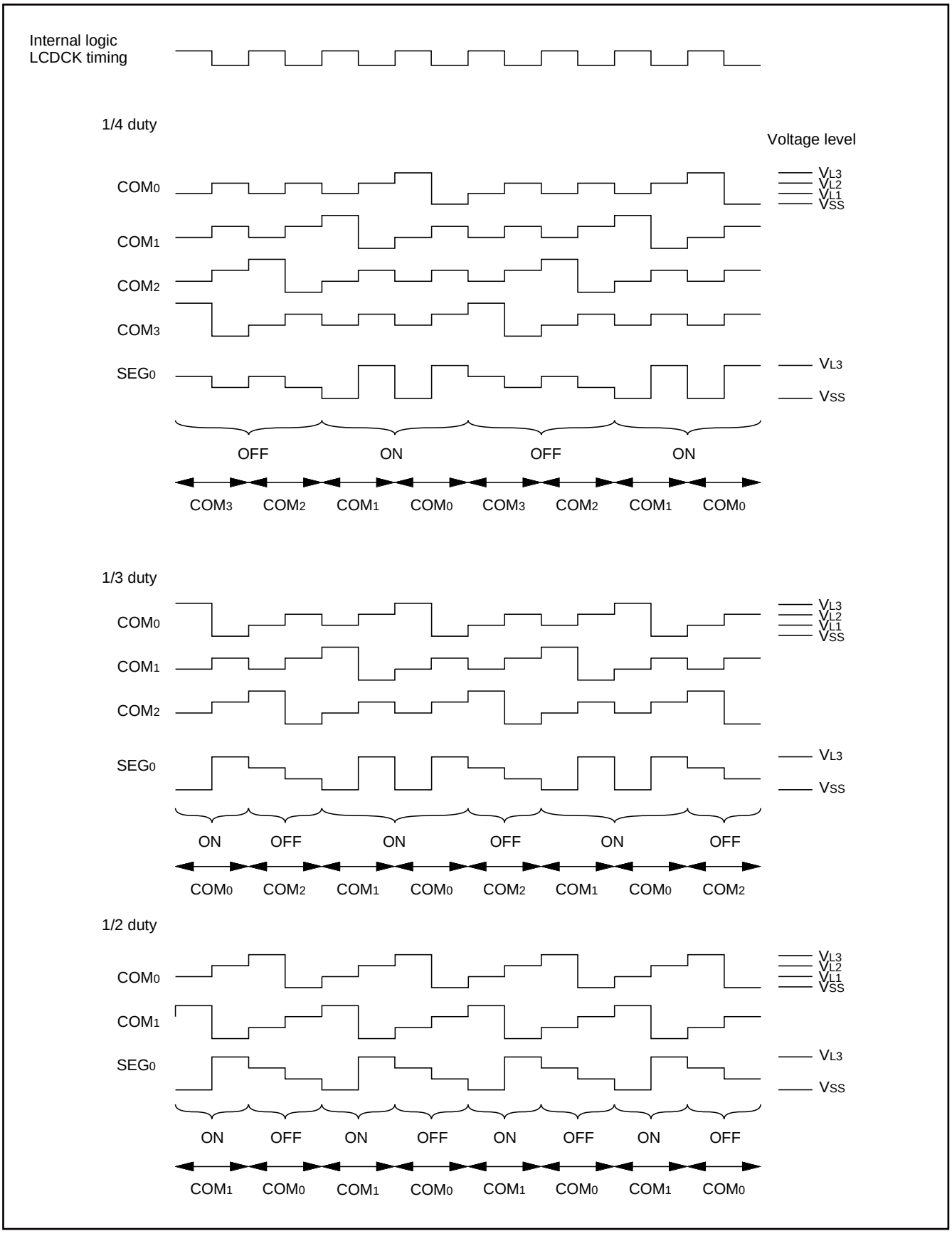


Fig. 37 LCD drive waveform (1/3 bias)

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φ CLOCK SYSTEM OUTPUT FUNCTION

The internal system clock φ can be output from port P41 by setting the φ output control register. Set bit 1 of the port P4 direction register to "1" when outputting φ clock.

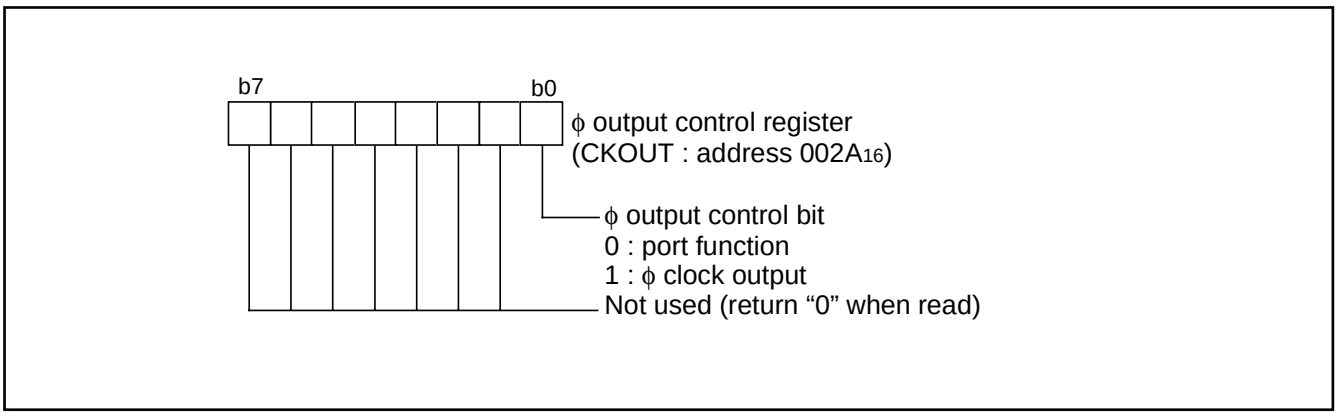


Fig. 38 Structure of φ output control register

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RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 µs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between V_{CC}(min.) and 5.5 V, and the quartz-crystal oscillator should be stable), reset is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage meets V_{IL} spec. when a power source voltage passes V_{CC}(min.).

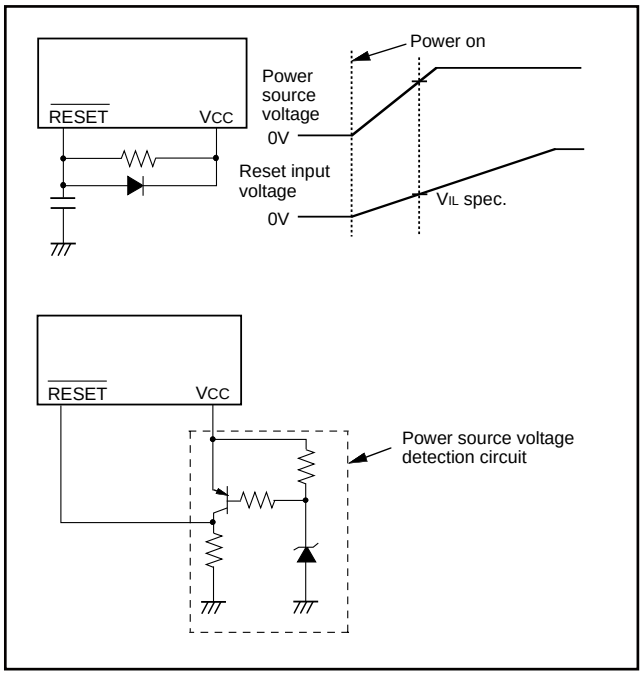
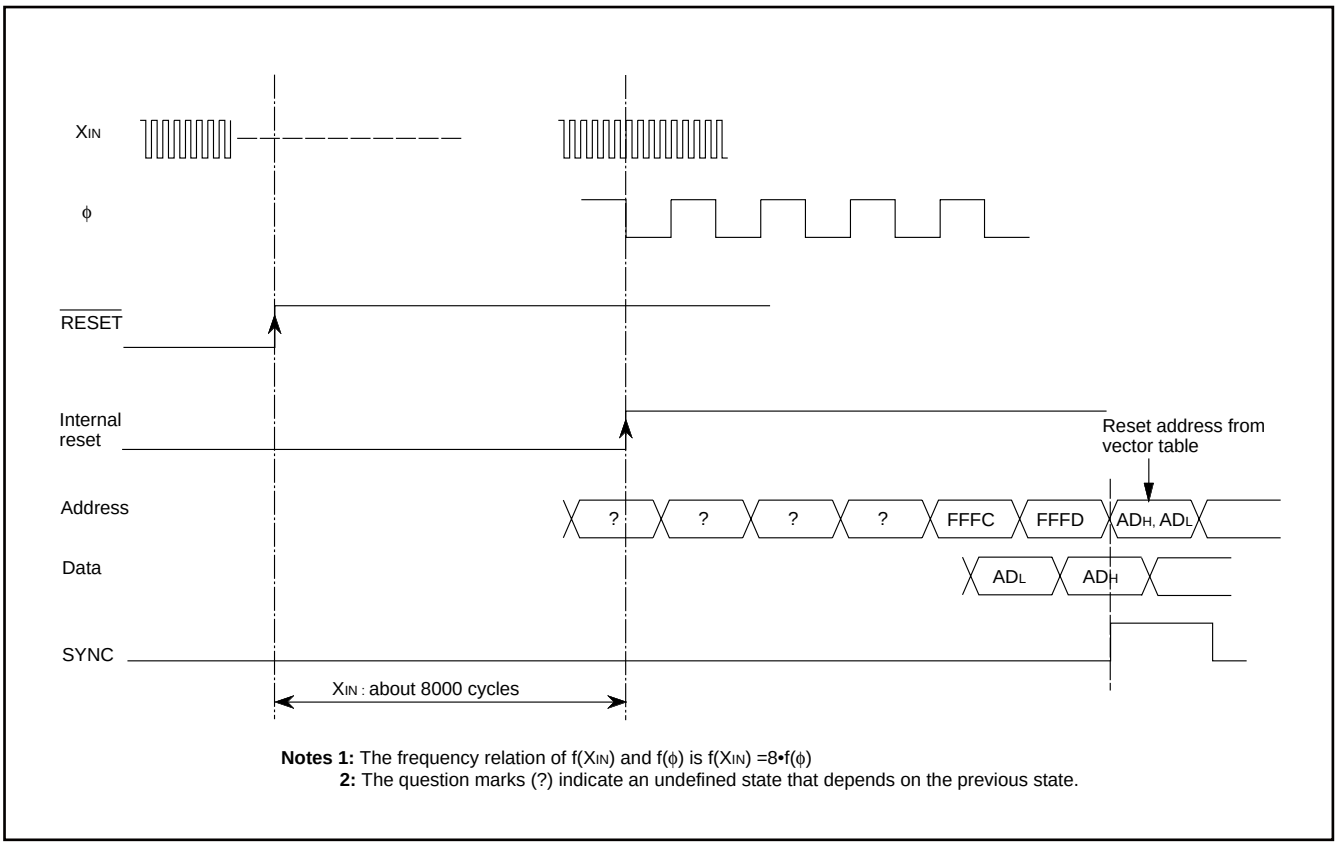


Fig. 39 Reset Circuit Example



Notes 1: The frequency relation of f(X_{IN}) and f(ϕ) is f(X_{IN}) =8•f(ϕ)
2: The question marks (?) indicate an undefined state that depends on the previous state.

Fig. 40 Reset Sequence

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		Address	Register Contents
(1)	Port P0 direction register	0001_{16}	00_{16}
(2)	Port P1 direction register	0003_{16}	00_{16}
(3)	Port P2 direction register	0005_{16}	00_{16}
(4)	Port P4 direction register	0009_{16}	00_{16}
(5)	Port P5 direction register	$000B_{16}$	00_{16}
(6)	Port P6 direction register	$000D_{16}$	00_{16}
(7)	Port P7 direction register	$000F_{16}$	00_{16}
(8)	PULL register A	0016_{16}	0 0 0 0 1 0 1 1
(9)	PULL register B	0017_{16}	00_{16}
(10)	Sirial I/O status register	0019_{16}	1 0 0 0 0 0 0 0
(11)	Sirial I/O control register	$001A_{16}$	00_{16}
(12)	UART control register	$001B_{16}$	1 1 1 0 0 0 0 0
(13)	Timer X(Low)	0020_{16}	FF_{16}
(14)	Timer X(High)	0021_{16}	FF_{16}
(15)	Timer Y(Low)	0022_{16}	FF_{16}
(16)	Timer Y(High)	0023_{16}	FF_{16}
(17)	Timer 1	0024_{16}	FF_{16}
(18)	Timer 2	0025_{16}	01_{16}
(19)	Timer 3	0026_{16}	FF_{16}
(20)	Timer X mode register	0027_{16}	00_{16}
(21)	Timer Y mode register	0028_{16}	00_{16}
(22)	Timer 123 mode register	0029_{16}	00_{16}
(23)	ϕ output control register	$002A_{16}$	00_{16}
(24)	A-D control register	0034_{16}	0 0 0 0 1 0 0 0
(25)	Segment output enable register	0038_{16}	00_{16}
(26)	LCD mode register	0039_{16}	00_{16}
(27)	Interrupt edge selection register	$003A_{16}$	00_{16}
(28)	CPU mode register	$003B_{16}$	0 1 0 0 1 0 0 0
(29)	Interrupt request register 1	$003C_{16}$	00_{16}
(30)	Interrupt request register 2	$003D_{16}$	00_{16}
(31)	Interrupt control register 1	$003E_{16}$	00_{16}
(32)	Interrupt control register 2	$003F_{16}$	00_{16}
(33)	Processor status register	(PS)	X X X X X 1 X X
(34)	Program counter	(PC_H)	Contents of address $FFFD_{16}$
		(PC_L)	Contents of address $FFFC_{16}$

Note: The contents of all other registers and RAM are undefined after reset, so they must be initialized by software.
X: undefined

Fig. 41 Initial status of microcomputer after reset

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CLOCK GENERATING CIRCUIT

The 3822 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.

To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open. The sub-clock XCIN-XCOUT oscillation circuit cannot directly input clocks that are externally generated. Accordingly, be sure to cause an external resonator to oscillate.

Immediately after poweron, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency Control
(1) Middle-speed Mode

The internal clock ϕ is the frequency of XIN divided by 8.
After reset, this mode is selected.

(2) High-speed Mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed Mode

- The internal clock ϕ is half the frequency of XCIN.
- A low-power consumption operation can be realized by stopping the main clock XIN in this mode. To stop the main clock, set bit 5 of the CPU mode register to "1".
  When the main clock XIN is restarted, set enough time for oscillation to stabilize by programming.

Note: If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after poweron and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3f(XCIN).

Oscillation Control
(1) Stop Mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116".

Either XIN or XCIN divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2. The bits of the timer 123 mode register except bit 4 are cleared to "0". Set the timer 1 and timer 2 interrupt enable bits to disabled ("0") before executing the STP instruction. Oscillator restarts at reset or when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU until timer 2 underflows. This allows timer for the clock circuit oscillation to stabilize.

(2) Wait Mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level. The states of XIN and XCIN are the same as the state before the executing the WIT instruction. The internal clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

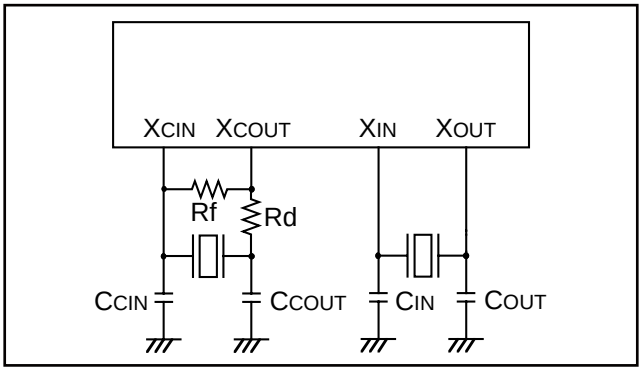


Fig. 42 Ceramic resonator circuit

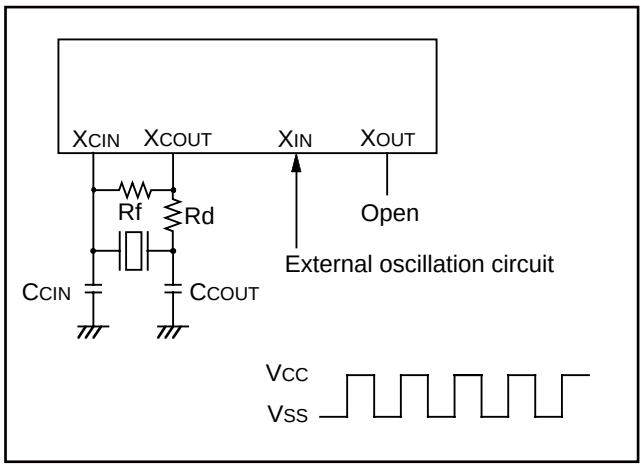
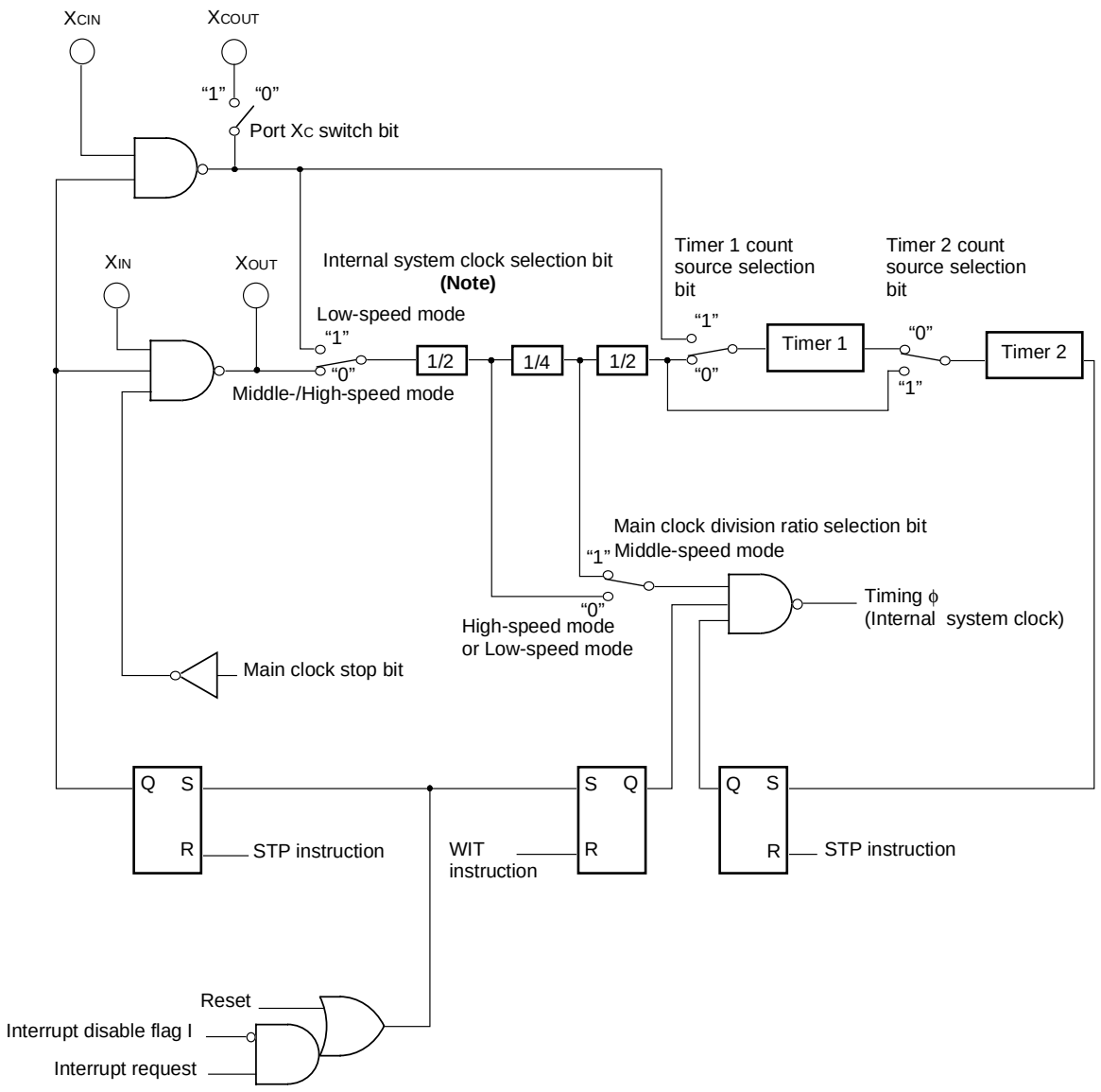


Fig. 43 External clock input circuit

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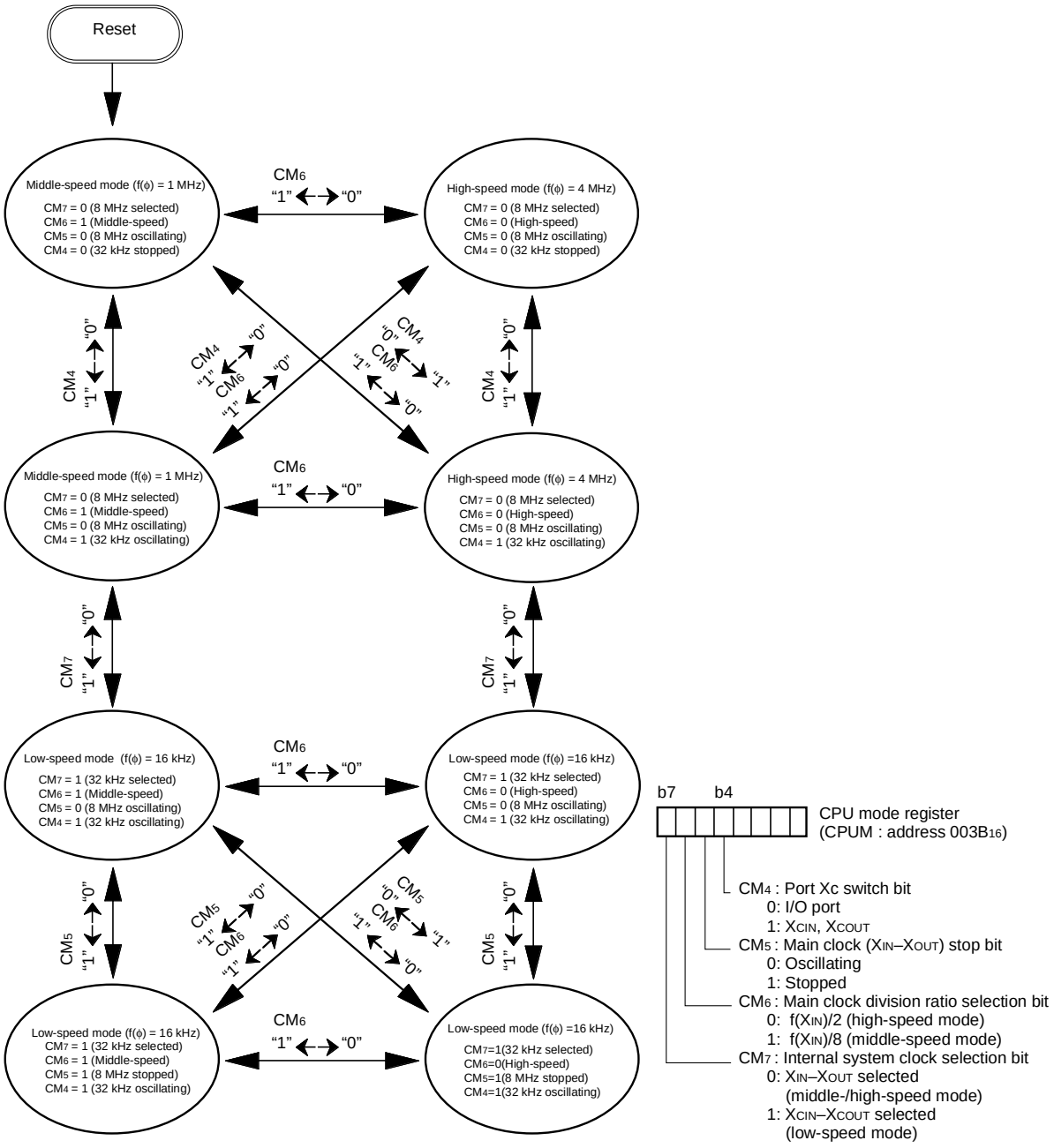


Note : When using the low-speed mode, set the port XC switch bit to "1" .

Fig.44 Clock generating circuit block diagram

Renesas Technology Corp.

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Notes 1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the mode directly without an allow.)
2 : The all modes can be switched to the stop mode or the wait mode and returned to the source mode when the stop mode or the wait mode is ended.
3 : Timer and LCD operate in the wait mode.
4 : When the stop mode is ended, a delay of approximately 1 ms occurs automatically by timer 1 and timer 2 in middle-/high-speed mode.
5 : When the stop mode is ended, a delay of approximately 0.25 s occurs automatically by timer 1 and timer 2 in low-speed mode.
6 : Wait until oscillation stabilizes after oscillating the main clock XIN before the switching from the low-speed mode to middle-/high-speed mode.
7 : The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. ϕ indicates the internal clock.

Fig. 45 State transitions of system clock

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NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution.
In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupt

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n + 1).

Multiplication and Division Instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read.
The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1".
Serial I/O continues to output the final bit from the TxD pin after transmission is completed.

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.
Make sure that f(XIN) is at least 500 kHz during an A-D conversion.
Do not execute the STP or WIT instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The frequency of the internal clock ϕ is half of the XIN frequency.

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NOTES ON USE
Countermeasures against noise

(1) Shortest wiring length

① Wiring for RESET pin

Make the length of wiring which is connected to the RESET pin as short as possible. Especially, connect a capacitor across the RESET pin and the Vss pin with the shortest possible wiring (within 20mm).

● Reason

The width of a pulse input into the RESET pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the RESET pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

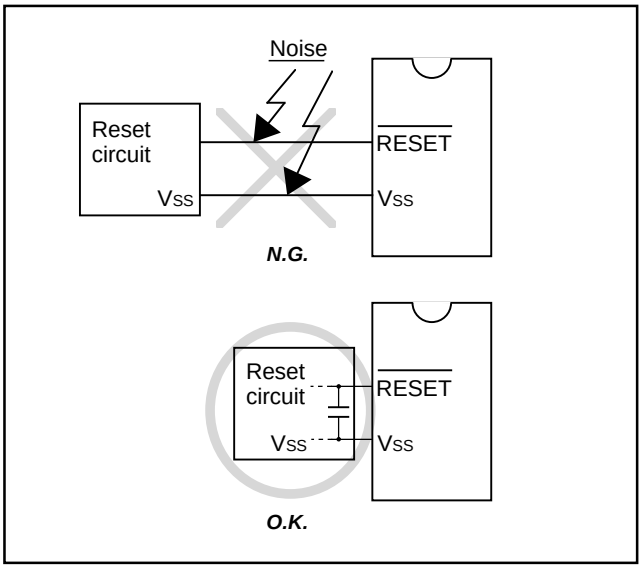


Fig. 46 Wiring for the RESET pin

② Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

● Reason

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

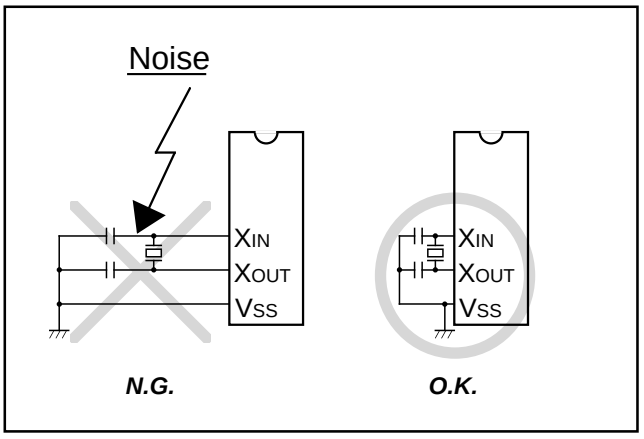


Fig. 47 Wiring for clock I/O pins

(2) Connection of bypass capacitor across Vss line and Vcc line

In order to stabilize the system operation and avoid the latch-up, connect an approximately 0.1 μF bypass capacitor across the Vss line and the Vcc line as follows:

- Connect a bypass capacitor across the Vss pin and the Vcc pin at equal length.
- Connect a bypass capacitor across the Vss pin and the Vcc pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for Vss line and Vcc line.
- Connect the power source wiring via a bypass capacitor to the Vss pin and the Vcc pin.

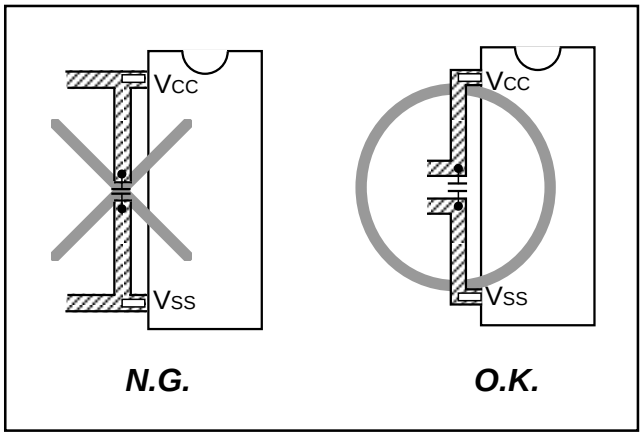


Fig. 48 Bypass capacitor across the Vss line and the Vcc line

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(3) Oscillator concerns

In order to obtain the stabilized operation clock on the user system and its condition, contact the oscillator manufacturer and select the oscillator and oscillation circuit constants. Be careful especially when range of votage and temperature is wide.

Also, take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

① Keeping oscillator away from large current signal lines

Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

● Reason

In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

② Installing oscillator away from signal lines where potential levels change frequently

Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

● Reason

Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

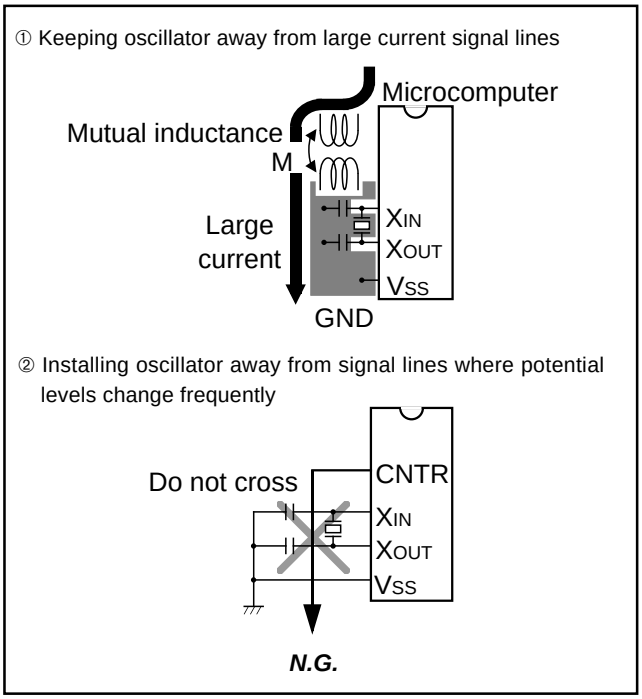


Fig. 49 Wiring for a large current signal line/Wiring of signal lines where potential levels change frequently

(4) Analog input

The analog input pin is connected to the capacitor of a voltage comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A-D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A-D conversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

(5) Difference of memory type and size

When Mask ROM and PROM version and memory size differ in one group, actual values such as an electrical characteristics, A-D conversion accuracy, and the amount of -proof of noise incorrect operation may differ from the ideal values.

When these products are used switching, perform system evaluation for each product of every after confirming product specification.

(6) Wiring to V_{PP} pin of One Time PROM version

Connect an approximately 5 kΩ resistor to the V_{PP} pin the shortest possible in series and also to the V_{SS} pin.

Note: Even when a circuit which included an approximately 5 kΩ resistor is used in the Mask ROM version, the microcomputer operates correctly.

● Reason

The V_{PP} pin of the One Time PROM version is the power source input pin for the built-in PROM. When programming in the built-in PROM, the impedance of the V_{PP} pin is low to allow the electric current for writing flow into the built-in PROM. Because of this, noise can enter easily. If noise enters the V_{PP} pin, abnormal instruction codes or data are read from the built-in PROM, which may cause a program runaway.

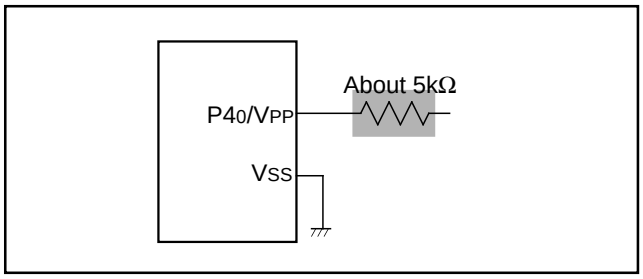


Fig. 50 Wiring for the V_{PP} pin of One Time PROM

Electric Characteristic Differences Between Mask ROM and One Time PROM Version MCUs

There are differences in electric characteristics, operation margin, noise immunity, and noise radiation between Mask ROM and One Time PROM version MCUs due to the difference in the manufacturing processes.

When manufacturing an application system with the One TIme PROM version and then switching to use of the Mask ROM version, please perform sufficient evaluations for the commercial samples of the Mask ROM version.

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DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form*
2. Mark Specification Form*
3. Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk

*For the mask ROM confirmation and the mark specifications, refer to the "Mitsubishi MCU Technical Information" Homepage (http://www.infomicom.maec.co.jp/).

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 14 Programming adapter

Package	Name of Programming Adapter
80P6N-A	PCA4738F-80A
80P6S-A	PCA4738G-80A
80P6Q-A	PCA4738H-80A
80D0	PCA4738L-80A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 51 is recommended to verify programming.

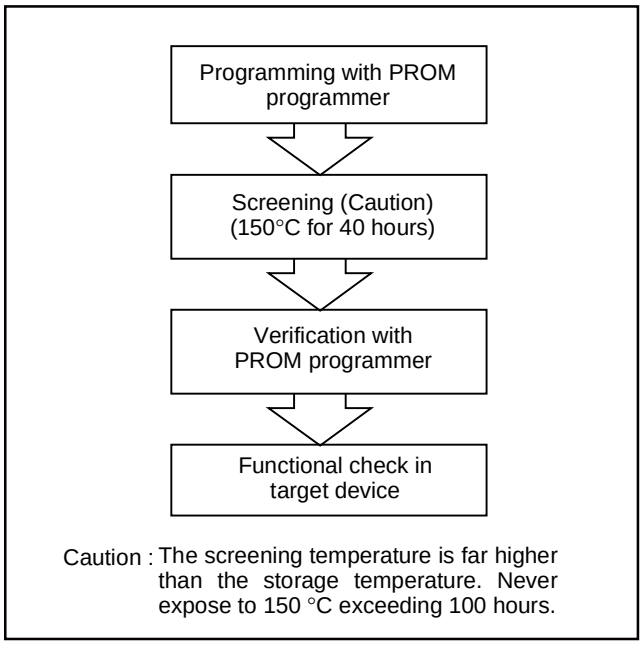


Fig. 51 Programming and testing of One Time PROM version

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Table 15 Absolute maximum ratings (Standard, One Time PROM version)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_4$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	At output port	–0.3 to V_{CC} +0.3	V
		At segment output	–0.3 to V_{L3}+0.3	V
V_O	Output voltage $P3_4$–$P3_7$	At segment output	–0.3 to V_{L3}+0.3	V
V_O	Output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage SEG_0–SEG_{11}		–0.3 to V_{L3}+0.3	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC} +0.3	V
Pd	Power dissipation	Ta = 25°C	300	mW
Topr	Operating temperature		–20 to 85	°C
Tstg	Storage temperature		–40 to 125	°C

Table 16 Recommended operating conditions (Standard, One Time PROM version)

(V_{CC} = 2.5 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	High-speed mode f(X_{IN}) = 8 MHz	4.0	5.0	5.5	V
		Middle-speed mode f(X_{IN}) = 8 MHz	2.5	5.0	5.5	
		Low-speed mode	2.5	5.0	5.5	
V_{SS}	Power source voltage			0		V
V_{REF}	A-D conversion reference voltage		2.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage AN_0–AN_7		AV_{SS}		V_{CC}	V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$,$P3_4$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_2$, $P5_3$, $P5_6$,$P6_0$–$P6_7$,$P7_0$,$P7_1$ (CM_4= 0)	0.7V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$,$P4_6$,$P5_0$, $P5_1$, $P5_4$, $P5_5$, $P5_7$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$,$P3_4$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_2$, $P5_3$, $P5_6$,$P6_0$–$P6_7$,$P7_0$,$P7_1$ (CM_4= 0)	0		0.3 V_{CC}	V
V_{IL}	“L” input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$,$P4_6$,$P5_0$, $P5_1$, $P5_4$, $P5_5$, $P5_7$	0		0.2 V_{CC}	V
V_{IL}	“L” input voltage	$\overline{RESET}$	0		0.2 V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}	0		0.2 V_{CC}	V

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Table 17 Recommended operating conditions (Standard, One Time PROM version)

(V_{CC} = 2.5 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			–40	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			–40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			–20	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			–20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			20	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 2)**			–2	mA
$I_{OH(peak)}$	"H" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 2)**			–5	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 2)**			5	mA
$I_{OL(peak)}$	"L" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 2)**			10	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 3)**			–1.0	mA
$I_{OH(avg)}$	"H" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 3)**			–2.5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 3)**			2.5	mA
$I_{OL(avg)}$	"L" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 3)**			5.0	mA
$f(CNTR_0)$ $f(CNTR_1)$	Input frequency for timers X and Y (duty cycle 50%)	($4.0\ V \le V_{CC} \le 5.5\ V$)			4.0	MHz
		($2.5\ V \le V_{CC} \le 4.0\ V$)			$(2 \times V_{CC})-4$	MHz
$f(X_{IN})$	Main clock input oscillation frequency **(Note 4)**	High-speed mode ($4.0\ V \le V_{CC} \le 5.5\ V$)			8.0	MHz
		High-speed mode ($2.5\ V \le V_{CC} \le 4.0\ V$)			$(4 \times V_{CC})-8$	MHz
		Middle-speed mode			8.0	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency **(Notes 4, 5)**			32.768	50	kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current is an average value measured over 100 ms.
4: When the oscillation frequency has a duty cycle of 50 %.
5: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

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Table 18 Electrical characteristics (Standard, One Time PROM version)
(V_{CC} =4.0 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	I_{OH} = –2.5 mA	V_{CC}–2.0			V
		I_{OH} = –0.6 mA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OH}	"H" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	I_{OH} = –5 mA	V_{CC}–2.0			V
		I_{OH} = –1.25 mA	V_{CC}–0.5			V
		I_{OH} = –1.25 mA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, P10–P17	I_{OL} = 5 mA			2.0	V
		I_{OL} = 1.25 mA			0.5	V
		I_{OL} = 1.25 mA V_{CC} = 2.5 V			1.0	V
V_{OL}	"L" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	I_{OL} = 10 mA			2.0	V
		I_{OL} = 2.5 mA			0.5	V
		I_{OL} = 2.5 mA V_{CC} = 2.5 V			1.0	V
V_{T+} – V_{T-}	Hysteresis INT_0–INT_3, ADT, $CNTR_0$, $CNTR_1$, $P2_0$–$P2_7$			0.5		V
V_{T+} – V_{T-}	Hysteresis S_{CLK}, R_XD			0.5		V
V_{T+} – V_{T-}	Hysteresis $\overline{RESET}$	$\overline{RESET}$: V_{CC} = 2.5 V to 5.5 V		0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_4$–$P3_7$	V_I = V_{CC} Pull-downs "off"			5.0	µA
		V_{CC} = 5 V, V_I = V_{CC} Pull-downs "on"	30	70	140	µA
		V_{CC} = 3 V, V_I = V_{CC} Pull-downs "on"	6.0	25	45	µA
I_{IH}	"H" input current $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_4$–$P3_7$,$P4_0$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	V_I = V_{SS} Pull-ups "off"			–5.0	µA
		V_{CC} = 5 V, V_I = V_{SS} Pull-ups "on"	–30	–70	–140	µA
		V_{CC} = 3 V, V_I = V_{SS} Pull-ups "on"	–6.0	–25	–45	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA

Note: When "1" is set to port X_C switch bit (bit 4 at address $003B_{16}$) of the CPU mode register, the drive ability of port $P7_0$ is different from the value above mentioned.

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Table 19 Electrical characteristics (Standard, One Time PROM version)
(V_{CC} = 2.5 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{RAM}	RAM retention voltage	At clock stop mode		2.0		5.5	V
I_{CC}	Power source current	• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off” A-D converter in operating			6.4	13	mA
		• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off” A-D converter stopped			1.6	3.2	mA
		• Low-speed mode, V_{CC} = 5 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			25	36	µA
		• Low-speed mode, V_{CC} = 5 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			7.0	14	µA
		• Low-speed mode, V_{CC} = 3 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			15	22	µA
		• Low-speed mode, V_{CC} = 3 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			4.5	9.0	µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	

Table 20 A-D converter characteristics (Standard, One Time PROM version)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, 4 MHz ≤ $f(X_{IN})$ ≤ 8 MHz, middle-/high-speed mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy (excluding quantization error)	V_{CC} = V_{REF} = 5V			±2	LSB
t_{CONV}	Conversion time	$f(X_{IN})$ = 8 MHz			12.5 **(Note)**	µs
R_{LADDER}	Ladder resistor		12	35	100	kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5 V	50	150	200	µA
I_{IA}	Analog port input current				5.0	µA

Note: When an internal trigger is used in middle-speed mode, it is 14 µs.

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Table 21 Timing requirements 1 (Standard, One Time PROM version)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	250			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	105			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	105			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	80			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	80			ns
$t_{c(S_{CLK})}$	Serial I/O clock input cycle time **(Note)**	800			ns
$t_{wH(S_{CLK})}$	Serial I/O clock input “H” pulse width **(Note)**	370			ns
$t_{wL(S_{CLK})}$	Serial I/O clock input “L” pulse width **(Note)**	370			ns
$t_{su(R_{XD}–S_{CLK})}$	Serial I/O input set up time	220			ns
$t_{h(S_{CLK}–R_{XD})}$	Serial I/O input hold time	100			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 22 Timing requirements 2 (Standard, One Time PROM version)
(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	500/(V_{CC}-2)			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	250/(V_{CC}-2)-20			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	250/(V_{CC}-2)-20			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	230			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	230			ns
$t_{c(S_{CLK})}$	Serial I/O clock input cycle time **(Note)**	2000			ns
$t_{wH(S_{CLK})}$	Serial I/O clock input “H” pulse width **(Note)**	950			ns
$t_{wL(S_{CLK})}$	Serial I/O clock input “L” pulse width **(Note)**	950			ns
$t_{su(R_{XD}–S_{CLK})}$	Serial I/O input set up time	400			ns
$t_{h(S_{CLK}–R_{XD})}$	Serial I/O input hold time	200			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

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Table 23 Switching characteristics 1 (Standard, One Time PROM version)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O clock output “H” pulse width	$t_{C(SCLK)}$/2–30			ns
$t_{WL(SCLK)}$	Serial I/O clock output “L” pulse width	$t_{C(SCLK)}$/2–30			ns
$t_{d(SCLK-TxD)}$	Serial I/O output delay time **(Note 1)**			140	ns
$t_{v(SCLK-TxD)}$	Serial I/O output valid time **(Note 1)**	–30			ns
$t_{r(SCLK)}$	Serial I/O clock output rising time			30	ns
$t_{f(SCLK)}$	Serial I/O clock output falling time			30	ns
$t_{r(CMOS)}$	CMOS output rising time **(Note 2)**		10	30	ns
$t_{f(CMOS)}$	CMOS output falling time **(Note 2)**		10	30	ns

Notes 1: When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: X_{OUT} and X_{COUT} pins are excluded.

Table 24 Switching characteristics 2 (Standard, One Time PROM version)
(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O clock output “H” pulse width	$t_{C(SCLK)}$/2–50			ns
$t_{WL(SCLK)}$	Serial I/O clock output “L” pulse width	$t_{C(SCLK)}$/2–50			ns
$t_{d(SCLK-TxD)}$	Serial I/O output delay time **(Note 1)**			350	ns
$t_{v(SCLK-TxD)}$	Serial I/O output valid time **(Note 1)**	–30			ns
$t_{r(SCLK)}$	Serial I/O clock output rising time			50	ns
$t_{f(SCLK)}$	Serial I/O clock output falling time			50	ns
$t_{r(CMOS)}$	CMOS output rising time **(Note 2)**		20	50	ns
$t_{f(CMOS)}$	CMOS output falling time **(Note 2)**		20	50	ns

Notes 1: When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: X_{OUT} and X_{COUT} pins are excluded.

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Table 25 Absolute maximum ratings (Extended operating temperature version)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_4$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	At output port	–0.3 to V_{CC} +0.3	V
		At segment output	–0.3 to V_{L3}	V
V_O	Output voltage $P3_4$–$P3_7$	At segment output	–0.3 to V_{L3}	V
V_O	Output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage SEG_0–SEG_{11}		–0.3 to V_{L3}	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC} +0.3	V
Pd	Power dissipation	Ta = 25°C	300	mW
Topr	Operating temperature		–40 to 85	°C
Tstg	Storage temperature		–65 to 150	°C

Table 26 Recommended operating conditions (Extended operating temperature version)

(V_{CC} = 2.0 to 5.5 V, Ta = –20 to 85 °C, and V_{CC} = 3.0 to 5.5 V, Ta = –40 to –20°C, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Power source voltage	High-speed mode f(X_{IN}) = 8 MHz		4.0	5.0	5.5	V
		Middle-speed mode f(X_{IN}) = 8 MHz	Ta = −20 to 85°C	2.0	5.0	5.5	
			Ta = −40 to −20°C	3.0	5.0	5.5	
		Low-speed mode	Ta = −20 to 85°C	2.0	5.0	5.5	
			Ta = −40 to −20°C	3.0	5.0	5.5	
V_{SS}	Power source voltage				0		V
V_{REF}	A-D conversion reference voltage			2.0		V_{CC}	V
AV_{SS}	Analog power source voltage				0		V
V_{IA}	Analog input voltage AN_0–AN_7			AV_{SS}		V_{CC}	V
V_{IH}	“H” input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$,$P3_4$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_2$, $P5_3$, $P5_6$,$P6_0$–$P6_7$,$P7_0$,$P7_1$ (CM_4 = 0)			0.7V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage $P2_0$–$P2_7$, $P4_2$–$P4_4$,$P4_6$,$P5_0$, $P5_1$, $P5_4$, $P5_5$, $P5_7$			0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage $\overline{RESET}$			0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage X_{IN}			0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$,$P3_4$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_2$, $P5_3$, $P5_6$,$P6_0$–$P6_7$,$P7_0$,$P7_1$ (CM_4 = 0)			0		0.3 V_{CC}	V
V_{IL}	“L” input voltage $P2_0$–$P2_7$, $P4_2$–$P4_4$,$P4_6$,$P5_0$, $P5_1$, $P5_4$, $P5_5$, $P5_7$			0		0.2 V_{CC}	V
V_{IL}	“L” input voltage $\overline{RESET}$			0		0.2 V_{CC}	V
V_{IL}	“L” input voltage X_{IN}			0		0.2 V_{CC}	V

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Table 27 Recommended operating conditions (Extended operating temperature version)

(V_{CC} = 2.0 to 5.5 V, Ta = –20 to 85 °C, and V_{CC} = 3.0 to 5.5 V, Ta = –40 to –20° C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			–40	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			–40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			–20	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			–20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			20	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 2)**			–2	mA
$I_{OH(peak)}$	"H" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 2)**			–5	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 2)**			5	mA
$I_{OL(peak)}$	"L" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 2)**			10	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 3)**			–1.0	mA
$I_{OH(avg)}$	"H" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 3)**			–2.5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 3)**			2.5	mA
$I_{OL(avg)}$	"L" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 3)**			5.0	mA
f($CNTR_0$) f($CNTR_1$)	Input frequency for timers X and Y (duty cycle 50%)	(4.0 V ≤ V_{CC} ≤ 5.5 V)			4.0	MHz
		(2.0 V ≤ V_{CC} ≤ 4.0 V)			V_{CC}	MHz
f(X_{IN})	Main clock input oscillation frequency **(Note 4)**	High-speed mode (4.0 V ≤ V_{CC} ≤ 5.5 V)			8.0	MHz
		High-speed mode (2.0 V ≤ V_{CC} ≤ 4.0 V)			2×V_{CC}	MHz
		Middle-speed mode			8.0	MHz
f(X_{CIN})	Sub-clock input oscillation frequency **(Notes 4, 5)**			32.768	50	kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value mesured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is an average value measured over 100 ms.

4: When the oscillation frequency has a duty cycle of 50 %.

5: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that f(X_{CIN}) < f(X_{IN})/3.

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Table 28 Electrical characteristics (Extended operating temperature version)

(V_{CC} =2.0 to 5.5 V, Ta = –20 to 85 °C, and V_{CC} = 3.0 to 5.5 V, Ta = –40 to –20 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	I_{OH} = –2.5 mA	V_{CC}–2.0			V
		I_{OH} = –0.6 mA V_{CC} = 3.0 V	V_{CC}–0.9			V
V_{OH}	"H" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	I_{OH} = –5 mA	V_{CC}–2.0			V
		I_{OH} = –1.25 mA	V_{CC}–0.5			V
		I_{OH} = –1.25 mA V_{CC} = 3.0 V	V_{CC}–0.9			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	I_{OL} = 5 mA			2.0	V
		I_{OL} = 1.25 mA			0.5	V
		I_{OL} = 1.25 mA V_{CC} = 3.0 V			1.1	V
V_{OL}	"L" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	I_{OL} = 10 mA			2.0	V
		I_{OL} = 2.5 mA			0.5	V
		I_{OL} = 2.5 mA V_{CC} = 3.0 V			1.1	V
V_{T+} – V_{T-}	Hysteresis INT_0–INT_3, ADT, $CNTR_0$, $CNTR_1$, $P2_0$–$P2_7$			0.5		V
V_{T+} – V_{T-}	Hysteresis S_{CLK}, R_XD			0.5		V
V_{T+} – V_{T-}	Hysteresis $\overline{RESET}$	$\overline{RESET}$: V_{CC} = 2.0 V to 5.5 V		0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_4$–$P3_7$	V_I = V_{CC} Pull-downs "off"			5.0	µA
		V_{CC} = 5 V, V_I = V_{CC} Pull-downs "on"	30	70	170	µA
		V_{CC} = 3 V, V_I = V_{CC} Pull-downs "on"	6.0	25	55	µA
I_{IH}	"H" input current $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_4$–$P3_7$,$P4_0$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	V_I = V_{SS} Pull-ups "off"			–5.0	µA
		V_{CC} = 5 V, V_I = V_{SS} Pull-ups "on"	–30	–70	–140	µA
		V_{CC} = 3 V, V_I = V_{SS} Pull-ups "on"	–6.0	–25	–45	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA

Note: When "1" is set to port X_C switch bit (bit 4 at address $003B_{16}$) of CPU mode register, the drive ability of port $P7_0$ is different from the value above mentioned.

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Table 29 Electrical characteristics (Extended operating temperature version)

(V_{CC} =2.0 to 5.5 V, Ta = –20 to 85 °C, and V_{CC} = 3.0 to 5.5 V, Ta = –40 to –20 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{RAM}	RAM retention voltage	At clock stop mode		2.0		5.5	V
I_{CC}	Power source current	• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off” A-D converter in operating			6.4	13	mA
		• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off” A-D converter stopped			1.6	3.2	mA
		• Low-speed mode, V_{CC} = 5 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			25	36	µA
		• Low-speed mode, V_{CC} = 5 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			7.0	14	µA
		• Low-speed mode, V_{CC} = 3 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			15	22	µA
		• Low-speed mode, V_{CC} = 3 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			4.5	9.0	µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	

Table 30 A-D converter characteristics (Extended operating temperature version)

(V_{CC} = 3.0 to 5.5 V, V_{SS} =AV_{SS} = 0 V, Ta = –40 to 85 °C, 4 MHz ≤ $f(X_{IN})$ ≤ 8 MHz, in middle/high-speed mode unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy (excluding quantization error)	V_{CC} = V_{REF} = 4.0V to 5.5V $f(X_{IN})$ = 8 MHz			±2	LSB
		V_{CC} = V_{REF} = 3.0 V to 4.0V $f(X_{IN})$ = 2 ✕ V_{CC} MHz				
t_{CONV}	Conversion time	$f(X_{IN})$ = 8 MHz			12.5 **(Note)**	µs
R_{LADDER}	Ladder resistor		12	35	100	kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5 V	50	150	200	µA
I_{IA}	Analog port input current				5.0	µA

Note: When an internal trigger is used in middle-speed mode, it is 14 µs.

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Table 31 Timing requirements 1 (Extended operating temperature version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	250			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	105			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	105			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	80			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	80			ns
$t_{c(S_{CLK})}$	Serial I/O clock input cycle time **(Note)**	800			ns
$t_{wH(S_{CLK})}$	Serial I/O clock input “H” pulse width **(Note)**	370			ns
$t_{wL(S_{CLK})}$	Serial I/O clock input “L” pulse width **(Note)**	370			ns
$t_{su(R_{XD}–S_{CLK})}$	Serial I/O input set up time	220			ns
$t_{h(S_{CLK}–R_{XD})}$	Serial I/O input hold time	100			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 32 Timing requirements 2 (Extended operating temperature version)

(V_{CC} = 2.0 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, and V_{CC} = 3.0 to 4.0 V, Ta = –40 to –20 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	900/(V_{CC}–0.4)			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	450/(V_{CC}–0.4)–20			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	450/(V_{CC}–0.4)–20			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	230			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	230			ns
$t_{c(S_{CLK})}$	Serial I/O clock input cycle time **(Note)**	2000			ns
$t_{wH(S_{CLK})}$	Serial I/O clock input “H” pulse width **(Note)**	950			ns
$t_{wL(S_{CLK})}$	Serial I/O clock input “L” pulse width **(Note)**	950			ns
$t_{su(R_{XD}–S_{CLK})}$	Serial I/O input set up time	400			ns
$t_{h(S_{CLK}–R_{XD})}$	Serial I/O input hold time	200			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

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Table 33 Switching characteristics 1 (Extended operating temperature version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O clock output “H” pulse width	$t_{C(SCLK)}$/2–30			ns
$t_{WL(SCLK)}$	Serial I/O clock output “L” pulse width	$t_{C(SCLK)}$/2–30			ns
$t_{d(SCLK-TxD)}$	Serial I/O output delay time **(Note 1)**			140	ns
$t_{v(SCLK-TxD)}$	Serial I/O output valid time **(Note 1)**	–30			ns
$t_{r(SCLK)}$	Serial I/O clock output rising time			30	ns
$t_{f(SCLK)}$	Serial I/O clock output falling time			30	ns
$t_{r(CMOS)}$	CMOS output rising time **(Note 2)**		10	30	ns
$t_{f(CMOS)}$	CMOS output falling time **(Note 2)**		10	30	ns

Notes 1: When the $P4_5/TxD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: X_{OUT} and X_{COUT} pins are excluded.

Table 34 Switching characteristics 2 (Extended operating temperature version)

(V_{CC} = 2.0 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, and V_{CC} = 3.0 to 4.0 V, V_{SS} = 0 V, Ta = –40 to –20 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O clock output “H” pulse width	$t_{C(SCLK)}$/2–50			ns
$t_{WL(SCLK)}$	Serial I/O clock output “L” pulse width	$t_{C(SCLK)}$/2–50			ns
$t_{d(SCLK-TxD)}$	Serial I/O output delay time **(Note 1)**			350	ns
$t_{v(SCLK-TxD)}$	Serial I/O output valid time **(Note 1)**	–30			ns
$t_{r(SCLK)}$	Serial I/O clock output rising time			50	ns
$t_{f(SCLK)}$	Serial I/O clock output falling time			50	ns
$t_{r(CMOS)}$	CMOS output rising time **(Note 2)**		20	50	ns
$t_{f(CMOS)}$	CMOS output falling time **(Note 2)**		20	50	ns

Notes 1: When the $P4_5/TxD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: X_{OUT} and X_{COUT} pins are excluded.

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Table 35 Absolute maximum ratings (M version)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_4$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	At output port	–0.3 to V_{CC} +0.3	V
		At segment output	–0.3 to V_{L3} +0.3	V
V_O	Output voltage $P3_4$–$P3_7$	At segment output	–0.3 to V_{L3} +0.3	V
V_O	Output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage SEG_0–SEG_{11}		–0.3 to V_{L3} +0.3	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC} +0.3	V
Pd	Power dissipation	Ta = 25°C	300	mW
Topr	Operating temperature		–20 to 85	°C
Tstg	Storage temperature		–40 to 150	°C

Table 36 Recommended operating conditions (M version)
(V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	High-speed mode f(X_{IN}) = 8 MHz	4.0	5.0	5.5	V
		Middle-speed mode f(X_{IN}) = 8 MHz	2.2	5.0	5.5	
		Low-speed mode	2.2	5.0	5.5	
V_{SS}	Power source voltage			0		V
V_{REF}	A-D conversion reference voltage		2.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage AN_0–AN_7		AV_{SS}		V_{CC}	V

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Table 37 Recommended operating conditions (M version)

(V_{CC} = 2.5 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$,$P3_4$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_2$, $P5_3$,$P5_6$,$P6_0$–$P6_7$,$P7_0$,$P7_1$ (CM_4= 0)	0.7V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$,$P4_6$,$P5_0$, $P5_1$, $P5_4$, $P5_5$, $P5_7$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$,$P3_4$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_2$, $P5_3$, $P5_6$,$P6_0$–$P6_7$,$P7_0$,$P7_1$ (CM_4= 0)	0		0.3 V_{CC}	V
V_{IL}	"L" input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$,$P4_6$,$P5_0$, $P5_1$, $P5_4$, $P5_5$, $P5_7$	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage	$\overline{RESET}$	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage	X_{IN}	0		0.2 V_{CC}	V

Table 38 Recommended operating conditions (M version)

(V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$,$P3_4$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_2$, $P5_3$,$P5_6$,$P6_0$–$P6_7$,$P7_0$,$P7_1$ (CM_4= 0)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$,$P4_6$,$P5_0$, $P5_1$, $P5_4$, $P5_5$, $P5_7$	0.95V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$	0.95V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	X_{IN}	0.95V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$,$P3_4$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_2$, $P5_3$, $P5_6$,$P6_0$–$P6_7$,$P7_0$,$P7_1$ (CM_4= 0)	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage	$P2_0$–$P2_7$, $P4_2$–$P4_4$,$P4_6$,$P5_0$, $P5_1$, $P5_4$, $P5_5$, $P5_7$	0		0.05 V_{CC}	V
V_{IL}	"L" input voltage	$\overline{RESET}$	0		0.05 V_{CC}	V
V_{IL}	"L" input voltage	X_{IN}	0		0.05 V_{CC}	V

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Table 39 Recommended operating conditions (M version)

(V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			–40	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			–40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			–20	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			–20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			20	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 2)**			–2	mA
$I_{OH(peak)}$	"H" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 2)**			–5	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 2)**			5	mA
$I_{OL(peak)}$	"L" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 2)**			10	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 3)**			–1.0	mA
$I_{OH(avg)}$	"H" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 3)**			–2.5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 3)**			2.5	mA
$I_{OL(avg)}$	"L" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 3)**			5.0	mA
$f(CNTR_0)$ $f(CNTR_1)$	Input frequency for timers X and Y (duty cycle 50%)	(4.0 V ≤ V_{CC} ≤ 5.5 V)			4.0	MHz
		(2.2 V ≤ V_{CC} ≤ 4.0 V)			(10×V_{CC}-4)/9	MHz
$f(X_{IN})$	Main clock input oscillation frequency **(Note 4)**	High-speed mode (4.0 V ≤ V_{CC} ≤ 5.5 V)			8.0	MHz
		High-speed mode (2.2 V ≤ V_{CC} ≤ 4.0 V)			(20×V_{CC}-8)/9	MHz
		Middle-speed mode			8.0	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency **(Notes 4, 5)**			32.768	50	kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is an average value measured over 100 ms.

4: When the oscillation frequency has a duty cycle of 50%.

5: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.

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Table 40 Electrical characteristics (M version)
(V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	I_{OH} = –2.5 mA	V_{CC}–2.0			V
		I_{OH} = –0.6 mA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OH}	"H" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	I_{OH} = –5 mA	V_{CC}–2.0			V
		I_{OH} = –1.25 mA	V_{CC}–0.5			V
		I_{OH} = –1.25 mA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P7$	I_{OL} = 5 mA			2.0	V
		I_{OL} = 1.25 mA			0.5	V
		I_{OL} = 1.25 mA V_{CC} = 2.5 V			1.0	V
V_{OL}	"L" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	I_{OL} = 10 mA			2.0	V
		I_{OL} = 2.5 mA			0.5	V
		I_{OL} = 2.5 mA V_{CC} = 2.5 V			1.0	V
V_{T+} – V_{T-}	Hysteresis INT_0–INT_3, ADT, $CNTR_0$, $CNTR_1$, $P2_0$–$P2_7$			0.5		V
V_{T+} – V_{T-}	Hysteresis S_{CLK}, R_XD			0.5		V
V_{T+} – V_{T-}	Hysteresis $\overline{RESET}$	$\overline{RESET}$: V_{CC} = 2.2 V to 5.5 V		0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_4$–$P3_7$	V_I = V_{CC} Pull-downs "off"			5.0	µA
		V_{CC} = 5 V, V_I = V_{CC} Pull-downs "on"	30	70	140	µA
		V_{CC} = 3 V, V_I = V_{CC} Pull-downs "on"	6.0	25	45	µA
I_{IH}	"H" input current $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_4$–$P3_7$,$P4_0$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	V_I = V_{SS} Pull-ups "off"			–5.0	µA
		V_{CC} = 5 V, V_I = V_{SS} Pull-ups "on"	–30	–70	–140	µA
		V_{CC} = 3 V, V_I = V_{SS} Pull-ups "on"	–6.0	–25	–45	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA

Note: When "1" is set to the port X_C switch bit (bit 4 at address $003B_{16}$) of CPU mode register, the drive ability of port $P7_0$ is different from the value above mentioned.

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Table 41 Electrical characteristics (M version)

(V_{CC} = 2.2 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{RAM}	RAM retention voltage	At clock stop mode		2.0		5.5	V
I_{CC}	Power source current	• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off” A-D converter in operating			6.4	13	mA
		• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off” A-D converter stopped			1.6	3.2	mA
		• Low-speed mode, V_{CC} = 5 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			25	36	µA
		• Low-speed mode, V_{CC} = 5 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			7.0	14	µA
		• Low-speed mode, V_{CC} = 3 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			15	22	µA
		• Low-speed mode, V_{CC} = 3 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			4.5	9.0	µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	

Table 42 A-D converter characteristics (M version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, 4 MHz ≤ $f(X_{IN})$ ≤ 8 MHz, in middle/high-speed mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy (excluding quantization error)	V_{CC} = V_{REF} = 5V			±2	LSB
t_{CONV}	Conversion time	$f(X_{IN})$ = 8 MHz			12.5 **(Note)**	µs
R_{LADDER}	Ladder resistor		12	35	100	kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5 V	50	150	200	µA
I_{IA}	Analog port input current				5.0	µA

Note: When an internal trigger is used in middle-speed mode, it is 14 µs.

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Table 43 Timing requirements 1 (M version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	250			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	105			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	105			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	80			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	80			ns
$t_{c(S_{CLK})}$	Serial I/O clock input cycle time **(Note)**	800			ns
$t_{wH(S_{CLK})}$	Serial I/O clock input “H” pulse width **(Note)**	370			ns
$t_{wL(S_{CLK})}$	Serial I/O clock input “L” pulse width **(Note)**	370			ns
$t_{su(R_{XD}–S_{CLK})}$	Serial I/O input set up time	220			ns
$t_{h(S_{CLK}–R_{XD})}$	Serial I/O input hold time	100			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 44 Timing requirements 2 (M version)

(V_{CC} = 2.2 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	900/(V_{CC}–0.4)			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	450/(V_{CC}–0.4)–20			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	450/(V_{CC}–0.4)–20			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	230			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	230			ns
$t_{c(S_{CLK})}$	Serial I/O clock input cycle time **(Note)**	2000			ns
$t_{wH(S_{CLK})}$	Serial I/O clock input “H” pulse width **(Note)**	950			ns
$t_{wL(S_{CLK})}$	Serial I/O clock input “L” pulse width **(Note)**	950			ns
$t_{su(R_{XD}–S_{CLK})}$	Serial I/O input set up time	400			ns
$t_{h(S_{CLK}–R_{XD})}$	Serial I/O input hold time	200			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

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Table 45 Switching characteristics 1 (M version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O clock output “H” pulse width	t_C (S_{CLK})/2–30			ns
$t_{WL(SCLK)}$	Serial I/O clock output “L” pulse width	t_C (S_{CLK})/2–30			ns
$t_{d(SCLK-TxD)}$	Serial I/O output delay time **(Note 1)**			140	ns
$t_{v(SCLK-TxD)}$	Serial I/O output valid time **(Note 1)**	–30			ns
$t_{r(SCLK)}$	Serial I/O clock output rising time			30	ns
$t_{f(SCLK)}$	Serial I/O clock output falling time			30	ns
$t_{r(CMOS)}$	CMOS output rising time **(Note 2)**		10	30	ns
$t_{f(CMOS)}$	CMOS output falling time **(Note 2)**		10	30	ns

Notes 1: When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: X_{OUT} and X_{COUT} pins are excluded.

Table 46 Switching characteristics 2 (M version)

(V_{CC} = 2.2 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O clock output “H” pulse width	t_C (S_{CLK})/2–50			ns
$t_{WL(SCLK)}$	Serial I/O clock output “L” pulse width	t_C (S_{CLK})/2–50			ns
$t_{d(SCLK-TxD)}$	Serial I/O output delay time **(Note 1)**			350	ns
$t_{v(SCLK-TxD)}$	Serial I/O output valid time **(Note 1)**	–30			ns
$t_{r(SCLK)}$	Serial I/O clock output rising time			50	ns
$t_{f(SCLK)}$	Serial I/O clock output falling time			50	ns
$t_{r(CMOS)}$	CMOS output rising time **(Note 2)**		20	50	ns
$t_{f(CMOS)}$	CMOS output falling time **(Note 2)**		20	50	ns

Notes 1: When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: X_{OUT} and X_{COUT} pins are excluded.

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Table 47 Absolute maximum ratings (H version)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_4$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	At output port	–0.3 to V_{CC} +0.3	V
		At segment output	–0.3 to V_{L3}	V
V_O	Output voltage $P3_4$–$P3_7$	At segment output	–0.3 to V_{L3}	V
V_O	Output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage SEG_0–SEG_{11}		–0.3 to V_{L3}	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC} +0.3	V
Pd	Power dissipation	Ta = 25°C	300	mW
Topr	Operating temperature		–20 to 85	°C
Tstg	Storage temperature		–40 to 150	°C

Table 48 Recommended operating conditions (H version)

(V_{CC} = 2.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	High-speed mode f(X_{IN}) = 8 MHz	4.0	5.0	5.5	V
		Middle-speed mode f(X_{IN}) = 8 MHz	2.0	5.0	5.5	
		Low-speed mode	2.0	5.0	5.5	
V_{SS}	Power source voltage			0		V
V_{REF}	A-D conversion reference voltage		2.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage AN_0–AN_7		AV_{SS}		V_{CC}	V
V_{IH}	“H” input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$,$P3_4$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_2$, $P5_3$, $P5_6$,$P6_0$–$P6_7$,$P7_0$,$P7_1$ (CM_4= 0)		0.7V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage $P2_0$–$P2_7$, $P4_2$–$P4_4$,$P4_6$,$P5_0$, $P5_1$, $P5_4$, $P5_5$, $P5_7$		0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage $\overline{RESET}$		0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage X_{IN}		0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$,$P3_4$–$P3_7$, $P4_0$, $P4_1$, $P4_5$, $P4_7$, $P5_2$, $P5_3$, $P5_6$,$P6_0$–$P6_7$,$P7_0$,$P7_1$ (CM_4= 0)		0		0.3 V_{CC}	V
V_{IL}	“L” input voltage $P2_0$–$P2_7$, $P4_2$–$P4_4$,$P4_6$,$P5_0$, $P5_1$, $P5_4$, $P5_5$, $P5_7$		0		0.2 V_{CC}	V
V_{IL}	“L” input voltage $\overline{RESET}$		0		0.2 V_{CC}	V
V_{IL}	“L” input voltage X_{IN}		0		0.2 V_{CC}	V

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Table 49 Recommended operating conditions (H version)

(V_{CC} = 2.0 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			–40	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			–40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			40	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			–20	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			–20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ **(Note 1)**			20	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 1)**			20	mA
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 2)**			–2	mA
$I_{OH(peak)}$	"H" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 2)**			–5	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 2)**			5	mA
$I_{OL(peak)}$	"L" peak output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 2)**			10	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 3)**			–1.0	mA
$I_{OH(avg)}$	"H" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 3)**			–2.5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$ **(Note 3)**			2.5	mA
$I_{OL(avg)}$	"L" average output current	$P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note 3)**			5.0	mA
f($CNTR_0$) f($CNTR_1$)	Input frequency for timers X and Y (duty cycle 50%)	(4.0 V ≤ V_{CC} ≤ 5.5 V)			4.0	MHz
		(2.0 V ≤ V_{CC} ≤ 4.0 V)			V_{CC}	MHz
f(X_{IN})	Main clock input oscillation frequency **(Note 4)**	High-speed mode (4.0 V ≤ V_{CC} ≤ 5.5 V)			8.0	MHz
		High-speed mode (2.0 V ≤ V_{CC} ≤ 4.0 V)			2×V_{CC}	MHz
		Middle-speed mode			8.0	MHz
f(X_{CIN})	Sub-clock input oscillation frequency **(Notes 4, 5)**			32.768	50	kHz

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current is an average value measured over 100 ms.

4: When the oscillation frequency has a duty cycle of 50 %.

5: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that f(X_{CIN}) < f(X_{IN})/3.

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Table 50 Electrical characteristics (H version)

(V_{CC} = 4.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$	I_{OH} = –2.5 mA	V_{CC}–2.0			V
		I_{OH} = –0.6 mA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OH}	"H" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	I_{OH} = –5 mA	V_{CC}–2.0			V
		I_{OH} = –1.25 mA	V_{CC}–0.5			V
		I_{OH} = –1.25 mA V_{CC} = 2.5 V	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P7$	I_{OL} = 5 mA			2.0	V
		I_{OL} = 1.25 mA			0.5	V
		I_{OL} = 1.25 mA V_{CC} = 2.5 V			1.0	V
V_{OL}	"L" output voltage $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	I_{OL} = 10 mA			2.0	V
		I_{OL} = 2.5 mA			0.5	V
		I_{OL} = 2.5 mA V_{CC} = 2.5 V			1.0	V
V_{T+} – V_{T-}	Hysteresis INT_0–INT_3, ADT, $CNTR_0$, $CNTR_1$, $P2_0$–$P2_7$			0.5		V
V_{T+} – V_{T-}	Hysteresis S_{CLK}, R_XD			0.5		V
V_{T+} – V_{T-}	Hysteresis $\overline{RESET}$	$\overline{RESET}$: V_{CC} = 2.0 V to 5.5 V		0.5		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_4$–$P3_7$	V_I = V_{CC} Pull-downs "off"			5.0	µA
		V_{CC} = 5 V, V_I = V_{CC} Pull-downs "on"	30	70	140	µA
		V_{CC} = 3 V, V_I = V_{CC} Pull-downs "on"	6.0	25	45	µA
I_{IH}	"H" input current $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{RESET}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_4$–$P3_7$,$P4_0$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current $P2_0$–$P2_7$, $P4_1$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$, $P7_1$ **(Note)**	V_I = V_{SS} Pull-ups "off"			–5.0	µA
		V_{CC} = 5 V, V_I = V_{SS} Pull-ups "on"	–30	–70	–140	µA
		V_{CC} = 3 V, V_I = V_{SS} Pull-ups "on"	–6.0	–25	–45	µA
I_{IL}	"L" input current $\overline{RESET}$	V_I = V_{SS}			5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–4.0		µA

Note: When "1" is set to the port X_C switch bit (bit 4 at address $003B_{16}$) of CPU mode register, the drive ability of port $P7_0$ is different from the value above mentioned.

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Table 51 Electrical characteristics (H version)
(V_{CC} =2.0 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{RAM}	RAM retention voltage	At clock stop mode		2.0		5.5	V
I_{CC}	Power source current	• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off” A-D converter in operating			6.4	13	mA
		• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off” A-D converter stopped			1.6	3.2	mA
		• Low-speed mode, V_{CC} = 5 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			25	36	µA
		• Low-speed mode, V_{CC} = 5 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			7.0	14	µA
		• Low-speed mode, V_{CC} = 3 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			15	22	µA
		• Low-speed mode, V_{CC} = 3 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			4.5	9.0	µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	

Table 52 A-D converter characteristics (H version)
(V_{CC} = 2.2 to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85 °C, 4 MHz ≤ $f(X_{IN})$ ≤ 8 MHz, in middle/high-speed mode unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy (excluding quantization error)	V_{CC} = V_{REF} = 4.0 V to 5.5 V $f(X_{IN})$ = 8 MHz			±2	LSB
		V_{CC} = V_{REF} = 2.2 V to 4.0V $f(X_{IN})$ = 2 × V_{CC} MHz				
t_{CONV}	Conversion time	$f(X_{IN})$ = 8 MHz			12.5 **(Note)**	µs
R_{LADDER}	Ladder resistor		12	35	100	kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5 V	50	150	200	µA
I_{IA}	Analog port input current				5.0	µA

Note: When an internal trigger is used in middle-speed mode, it is 14 µs.

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Table 53 Timing requirements 1 (H version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	250			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	105			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	105			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	80			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	80			ns
$t_{c(S_{CLK})}$	Serial I/O clock input cycle time **(Note)**	800			ns
$t_{wH(S_{CLK})}$	Serial I/O clock input “H” pulse width **(Note)**	370			ns
$t_{wL(S_{CLK})}$	Serial I/O clock input “L” pulse width **(Note)**	370			ns
$t_{su(R_{XD}–S_{CLK})}$	Serial I/O input set up time	220			ns
$t_{h(S_{CLK}–R_{XD})}$	Serial I/O input hold time	100			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 54 Timing requirements 2 (H version)

(V_{CC} = 2.0 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	900/(V_{CC}–0.4)			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	450/(V_{CC}–0.4)–20			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	450/(V_{CC}–0.4)–20			ns
$t_{wH(INT)}$	INT_0 to INT_3 input “H” pulse width	230			ns
$t_{wL(INT)}$	INT_0 to INT_3 input “L” pulse width	230			ns
$t_{c(S_{CLK})}$	Serial I/O clock input cycle time **(Note)**	2000			ns
$t_{wH(S_{CLK})}$	Serial I/O clock input “H” pulse width **(Note)**	950			ns
$t_{wL(S_{CLK})}$	Serial I/O clock input “L” pulse width **(Note)**	950			ns
$t_{su(R_{XD}–S_{CLK})}$	Serial I/O input set up time	400			ns
$t_{h(S_{CLK}–R_{XD})}$	Serial I/O input hold time	200			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

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Table 55 Switching characteristics 1 (H version)

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O clock output “H” pulse width	$t_{C(SCLK)}$/2–30			ns
$t_{WL(SCLK)}$	Serial I/O clock output “L” pulse width	$t_{C(SCLK)}$/2–30			ns
$t_{d(SCLK-TxD)}$	Serial I/O output delay time **(Note 1)**			140	ns
$t_{v(SCLK-TxD)}$	Serial I/O output valid time **(Note 1)**	–30			ns
$t_{r(SCLK)}$	Serial I/O clock output rising time			30	ns
$t_{f(SCLK)}$	Serial I/O clock output falling time			30	ns
$t_{r(CMOS)}$	CMOS output rising time **(Note 2)**		10	30	ns
$t_{f(CMOS)}$	CMOS output falling time **(Note 2)**		10	30	ns

Notes1: When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: X_{OUT} and X_{COUT} pins are excluded.

Table 56 Switching characteristics 2 (H version)

(V_{CC} = 2.0 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH(SCLK)}$	Serial I/O clock output “H” pulse width	$t_{C(SCLK)}$/2–50			ns
$t_{WL(SCLK)}$	Serial I/O clock output “L” pulse width	$t_{C(SCLK)}$/2–50			ns
$t_{d(SCLK-TxD)}$	Serial I/O output delay time **(Note 1)**			350	ns
$t_{v(SCLK-TxD)}$	Serial I/O output valid time **(Note 1)**	–30			ns
$t_{r(SCLK)}$	Serial I/O clock output rising time			50	ns
$t_{f(SCLK)}$	Serial I/O clock output falling time			50	ns
$t_{r(CMOS)}$	CMOS output rising time **(Note 2)**		20	50	ns
$t_{f(CMOS)}$	CMOS output falling time **(Note 2)**		20	50	ns

Notes1: When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: X_{OUT} and X_{COUT} pins are excluded.

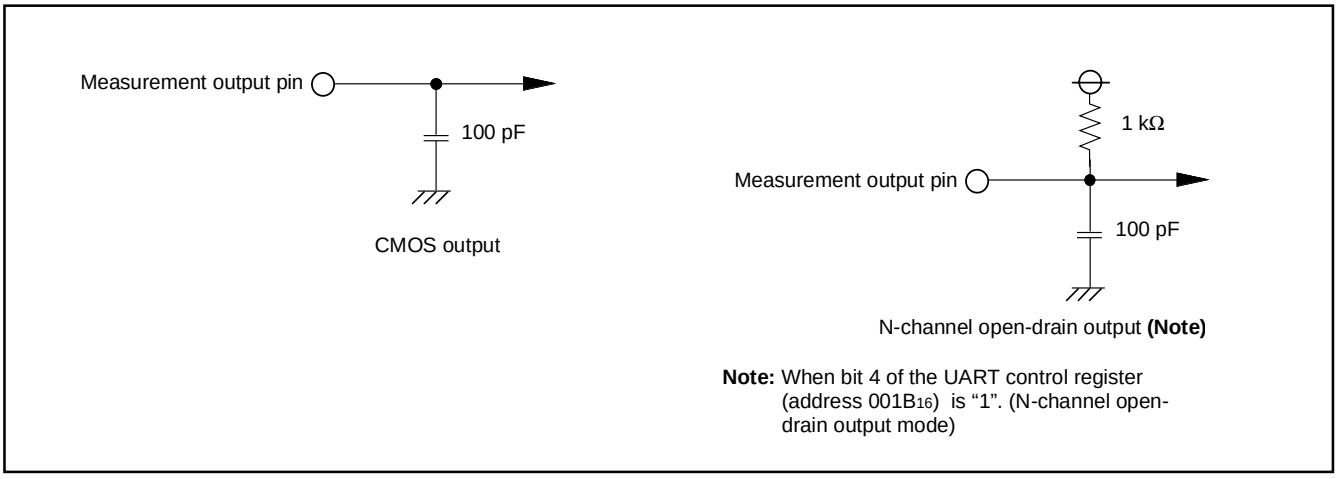


Fig. 52 Circuit for measuring output switching characteristics

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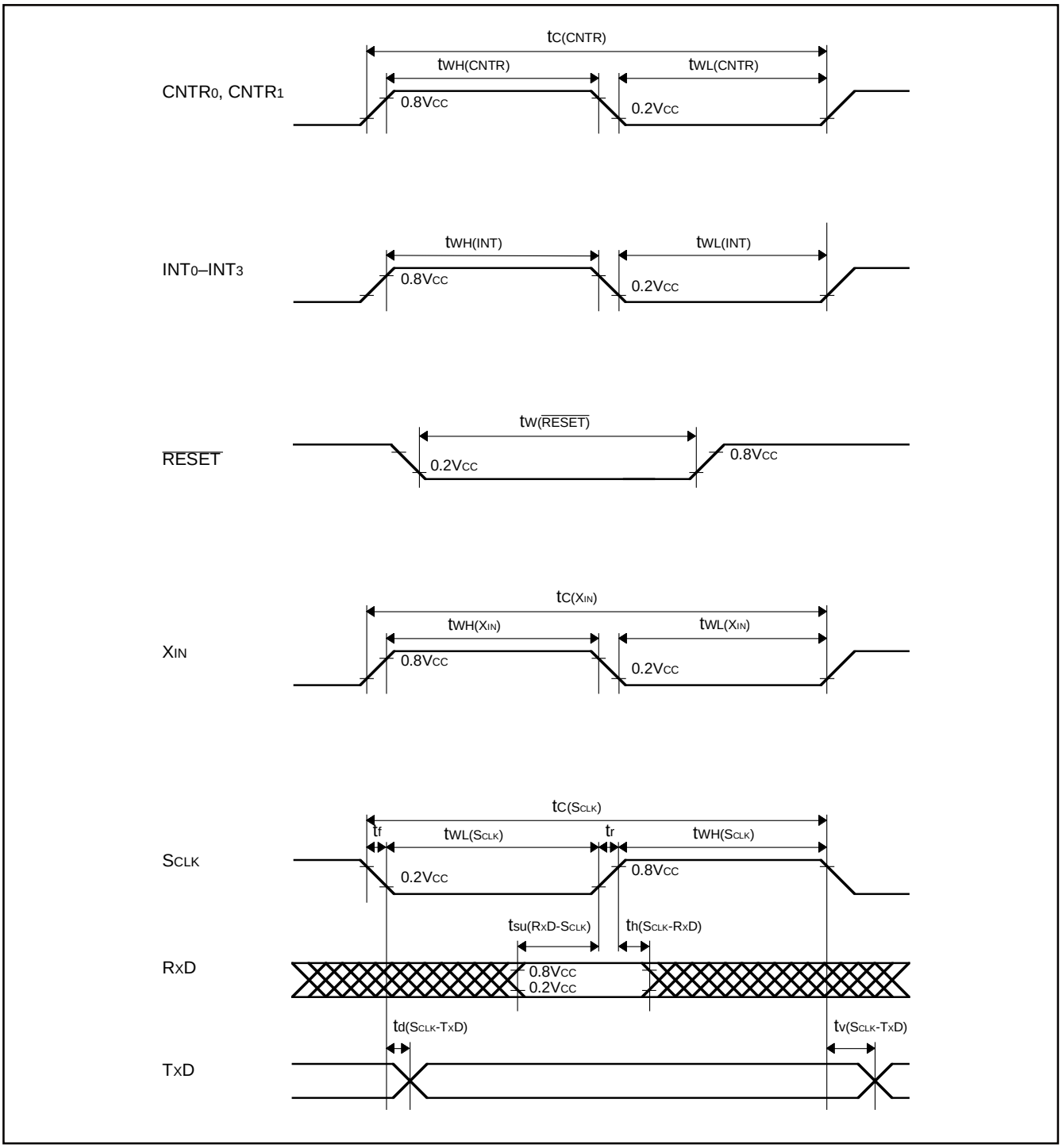


Fig. 53 Timing diagram

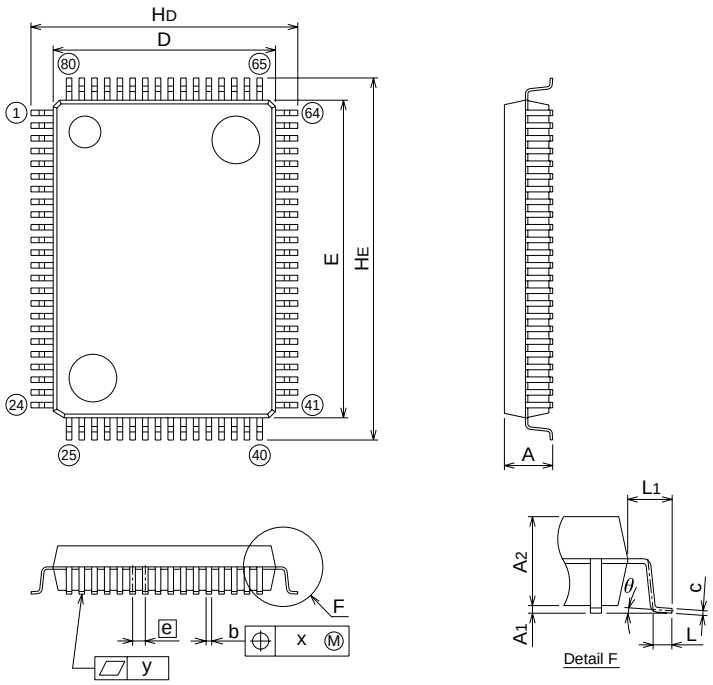
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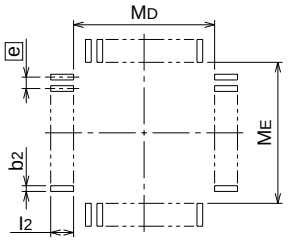
PACKAGE OUTLINE

80P6N-A (MMP)

Plastic 80pin 14×20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP80-P-1420-0.80	–	1.58	Alloy 42





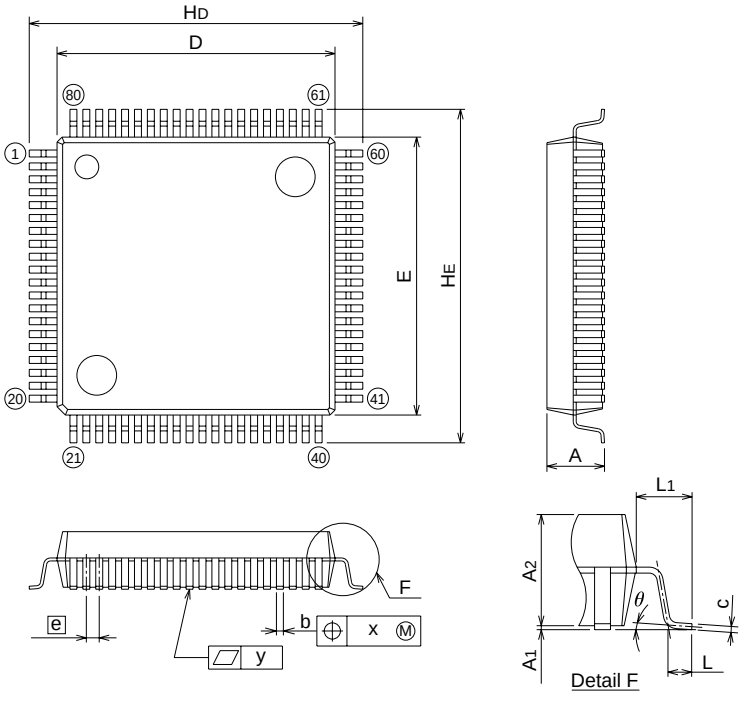
Recommended Mount Pad

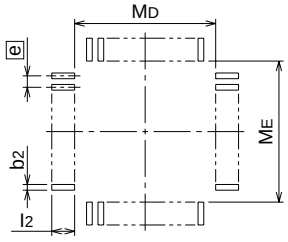
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.3	0.35	0.45
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	–	0.8	–
HD	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	–	1.4	–
x	–	–	0.2
y	–	–	0.1
θ	0°	–	10°
b2	–	0.5	–
I2	1.3	–	–
MD	–	14.6	–
ME	–	20.6	–

80P6S-A (MMP)

Plastic 80pin 14×14mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP80-P-1414-0.65		1.11	Alloy 42





Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	3.05
A1	0	0.1	0.2
A2	–	2.8	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	13.8	14.0	14.2
e	–	0.65	–
HD	16.5	16.8	17.1
HE	16.5	16.8	17.1
L	0.4	0.6	0.8
L1	–	1.4	–
x	–	–	0.13
y	–	–	0.1
θ	0°	–	10°
b2	–	0.35	–
I2	1.3	–	–
MD	–	14.6	–
ME	–	14.6	–

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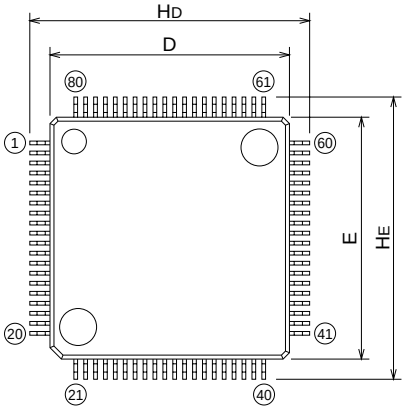
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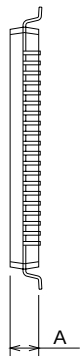
80P6Q-A

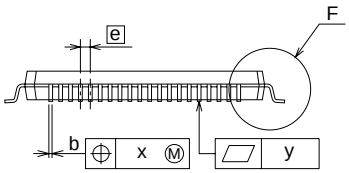
MMP

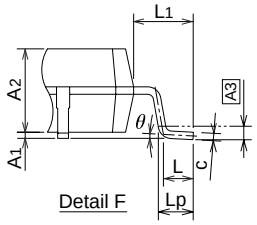
Plastic 80pin 12×12mm body LQFP

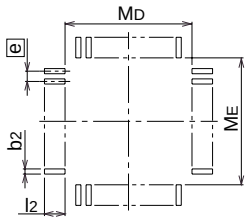
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.5	–	0.47	Cu Alloy











Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	–	0.5	–
HD	13.8	14.0	14.2
HE	13.8	14.0	14.2
L	0.3	0.5	0.7
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	10°
b2	–	0.225	–
l2	0.9	–	–
MD	–	12.4	–
ME	–	12.4	–

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REVISION HISTORY	3822 GROUP DATA SHEET

Rev.	Date	Description	
		Page	Summary
1.0	01/20/98		First Edition
2.0	10/23/00	1	“●Memory size” of “FEATURES” is partly revised.
		1	“●Serial I/O” of “FEATURES” is partly revised.
		1	“●A-D converter” of “FEATURES” is added.
		1	“●2 clock generating circuits” of “FEATURES” is partly revised.
		1	“●Power source voltage” of “FEATURES” is partly revised.
		1	“●Power dissipation” of “FEATURES” is partly added.
		1	Product name into Figure 1 is revised.
		2	Product name into Figure 2 is revised.
		3	Figure 3 is partly revised.
		4	“Function” of “Vcc, Vss” into Table 1 is partly revised.
		5	“Function except a port function” into Table 2 is partly revised.
		6	Figure 4 is partly revised.
		7	Explanations of “GROUP EXPANSION (STANDARD, ONE TIME PROM VERSION, EPROM VERSION)” are partly revised.
		7	Figure 5 is partly revised.
		7	Table 3 is partly revised.
		8	Explanations of “GROUP EXPANSION (EXTENDED OPERATING TEMPERATURE VERSION)” are partly revised.
		8	Figure 6 is partly revised.
		8	Table 4 is partly revised.
		9	“GROUP EXPANSION (M VERSION)” is added.
		9	Figure 7 is added.
		9	Table 5 is added.
		10	“GROUP EXPANSION (H VERSION)” is added.
		10	Figure 8 is added.
		10	Table 6 is added.
		11–13	Explanations of “CENTRAL PROCESSING UNIT (CPU)” are added.
		11	Figure 9 is added.
		12	Figure 10 is added.
		12	Table 7 is added.
		13	Table 8 is added.
		15	Figure 12 is partly revised.
		17	Figure 14 is partly revised.
		18	Table 9 is partly revised.
		21	Figure 17 is partly revised.
		22	Explanations of “Interrupt Control” is partly added.
		22	Explanations of “Interrupt Operation” is partly revised.
		22	Explanations of “■Notes” are partly revised.
		22	Table 9 is partly revised.
		24	Explanations of “Key Input Interrupt (Key-on wake up)” are partly revised.
		25	Figure 21 is partly revised.
		26	Explanations of “●Timer X write control” are partly revised.
		26	Explanations of “●Real time port control” are partly revised.
		29	Figure 25 is partly revised.
		30	Figure 27 is partly revised.
		32	Figure 29 is partly revised.
		33	Explanations of “[Channel Selector]” are partly added.
		33	Explanations of “[Comparator and Control Circuit]” are partly added.
		34	Figure 32 is partly revised.

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Rev.	Date	Description	
		Page	Summary
2.0	10/23/00	35 40 41 41 43 46 47 47 50 52 52 52 52 52 52 54–72 74, 75	Figure 33 is partly revised. Explanations of “ϕ CLOCK SYSTEM OUTPUT FUNCTION” are partly revised. Explanations of “RESET CIRCUIT” are partly revised. Figure 39 is partly revised. Explanations of “CLOCK GENERATING CIRCUIT” are partly eliminated. Explanations of “Decimal Calculations” are partly eliminated. Explanations of “DATA REQUIRED FOR MASK ORDERS” are partly added. Table 14 is partly revised. Test conditions of I_{IL} of $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P3_4$–$P3_7$, $P4_0$ is added. Limit of $t_{C(CNTR)}$ into Table 21 is revised. Limit of $t_{WH(CNTR)}$ into Table 21 is revised. Limit of $t_{WL(CNTR)}$ into Table 21 is revised. Limit of $t_{C(CNTR)}$ into Table 22 is revised. Limit of $t_{WH(CNTR)}$ into Table 22 is revised. Limit of $t_{WL(CNTR)}$ into Table 22 is revised. Tables 25 to 56 are added. “PACKAGE OUTLINE” is added.
2.1	01/31/01	13 21 22 25 31 44 47	Explanations of “•Bit 3: Decimal mode flag (D)” are partly added. Figure 17 is partly revised. Explanations of “■Notes on interrupts” are revised. Figure 21 is partly revised. “■Notes on serial I/O” is added. Figure 44 is partly revised. Explanations of “DATA REQUIRED FOR MASK ORDERS” are partly revised.
2.2	02/28/02	47-48 48	“NOTES ON USE - Countermeasures against noise” is added. “Electric Characteristic Differences Between Mask Rom and One Time PROM Version MCUs” is added.

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