EFR32MR21 RCP Multiprotocol Wireless SoC Data Sheet

The EFR32MR21 RCP multiprotocol SoC is part of the Wireless Gecko portfolio. EFR32MR21 SoCs are ideal for enabling energy-friendly multiprotocol, multiband networking for IoT devices.

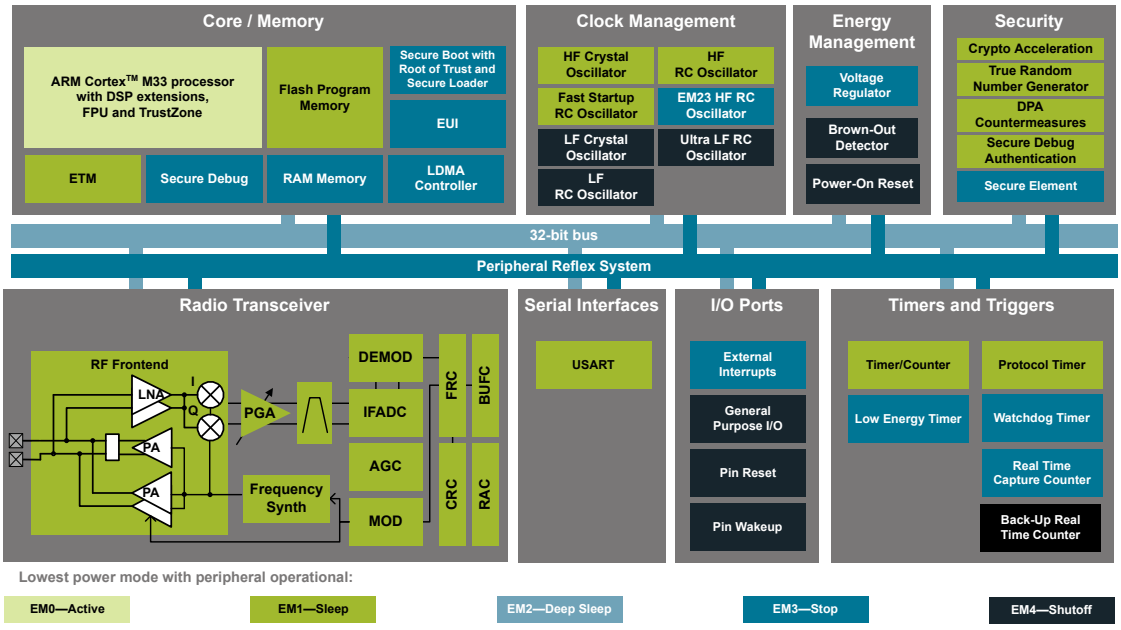
The single-die solution combines an 80 MHz ARM Cortex-M33 with a high-performance 2.4 GHz radio to provide an industry-leading, energy-efficient wireless SoC for IoT connected applications.

EFR32MR21 applications include:

- Gateways
- Border Routers

KEY FEATURES

- 32-bit ARM® Cortex®-M33 core with 80 MHz maximum operating frequency
- 512 kB of flash and 64 kB of RAM
- 12-channel Peripheral Reflex System enabling autonomous interaction of MCU peripherals
- Integrated PA with up to 20 dBm (2.4 GHz) TX power
- Robust peripheral set and up to 20 GPIO in a 4x4 QFN package



1. Feature List

The EFR32MR21 highlighted features are listed below.

- **Low Power Wireless System-on-Chip**
  - High-performance 32-bit 80 MHz ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
  - 512 kB flash program memory
  - 64 kB RAM data memory
  - 2.4 GHz radio operation
  - TX power up to 20 dBm
- **Low Energy Consumption**
  - 8.8 mA RX current at 2.4 GHz (1 Mbps GFSK)
  - 9.4 mA RX current at 2.4 GHz (250 kbps O-QPSK DSSS)
  - 186.5 mA TX current @ 20 dBm output power at 2.4 GHz
  - 50.9 µA/MHz in Active Mode (EM0)
  - 24.9 µA EM2 DeepSleep current

    (64 kB RAM retention and RTC running from LFXO)
  - 23.0 µA EM2 DeepSleep current

    (16 kB RAM retention and RTC running from LFRCO)
- **High Receiver Performance**
  - -104.3 dBm sensitivity @ 250 kbps O-QPSK DSSS
  - -97.1 dBm sensitivity @ 1 Mbit/s GFSK
  - -94 dBm sensitivity @ 2 Mbit/s GFSK
  - -105 dBm sensitivity @ 125 kbps GFSK
- **Supported Modulation Formats**
  - GFSK
  - OQPSK
- **Protocol Support**
  - Bluetooth HCI
  - Zigbee RCP
  - OpenThread RCP
  - Matter Thread RCP
- **Wide Selection of MCU Peripherals**
  - Up to 20 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 12 Channel Peripheral Reflex System (PRS)
  - 3 × 16-bit Timer/Counter
    - 3 Compare/Capture/PWM channels
  - 1 × 32-bit Timer/Counter
    - 3 Compare/Capture/PWM channels
  - 32-bit Real Time Counter
  - 24-bit Low Energy Timer for waveform generation
  - 2 × Watchdog Timer
  - 3 × Universal Synchronous/Asynchronous Receiver/Transmitter (UART/SPI/SmartCard(ISO 7816)/IrDA/I^2S)
- **Wide Operating Range**
  - 1.71 to 3.8 V single power supply
  - -40 to 125 °C ambient
- **Security**
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
  - Hardware Cryptographic Acceleration with DPA countermeasures for AES128/256, SHA-1, SHA-2 (up to 256-bit), ECC (up to 256-bit), ECDSA, ECDH and J-Pake
  - True Random Number Generator (TRNG) compliant with NIST SP800-90 and AIS-31
  - ARM® TrustZone®
  - Secure Debug with lock/unlock
- **QFN32 4x4 mm Package**
  - 0.4 mm pitch

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Max TX Power	Flash (kB)	RAM (kB)	Secure Vault	GPIO	Package
EFR32MR21A020F512IM32-C	• Bluetooth HCI • Zigbee RCP • OpenThread RCP	20 dBm	512	64	Mid	20	QFN32

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3. System Overview

3.1 Introduction

The EFR32 product family combines an energy-friendly MCU with a high performance radio transceiver. The devices are well suited for secure connected IoT multiprotocol devices requiring high performance and low energy consumption. This section gives a short introduction to the full radio and MCU system. The detailed functional description can be found in the EFR32xG21 Reference Manual.

A block diagram of the EFR32MR21 family is shown in the figure below. The diagram shows a superset of features available on the family, which vary by OPN. For more information about specific device features, consult the Ordering Information table.

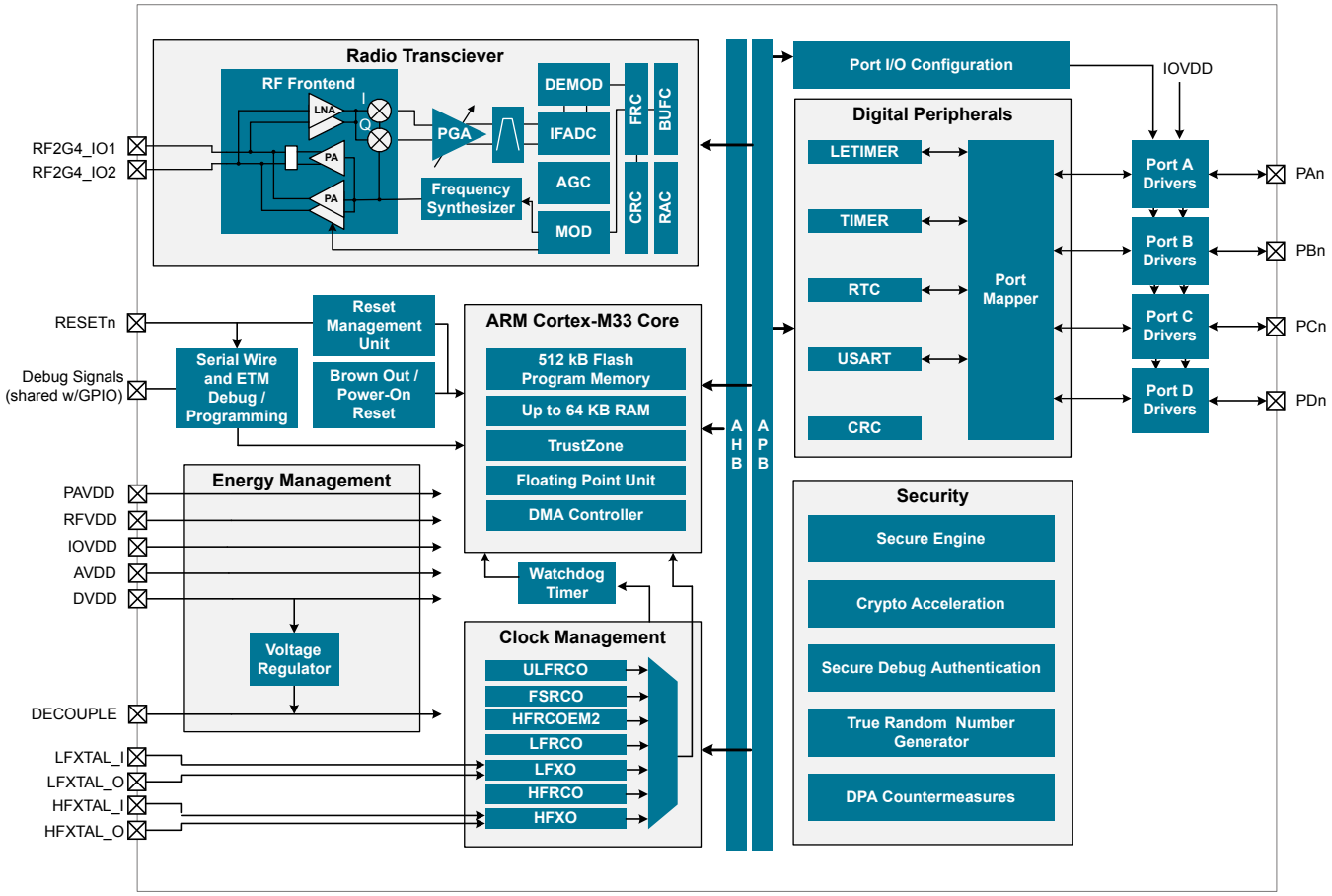

Figure 3.1. Detailed EFR32MR21 Block Diagram

3.2 Radio

The EFR32MR21 features a highly configurable radio transceiver supporting Zigbee RCP, OpenThread RCP, and Bluetooth HCI wireless protocols.

3.2.1 Antenna Interface

The 2.4 GHz antenna interface consists of two single-ended pins (RF2G4_IO1 and RF2G4_IO2) that interface directly to two LNAs and the 20 dBm PA and on-chip balun. Integrated switches select either RF2G4_IO1 or RF2G4_IO2 to be the active path.

The external components and power supply connections for the antenna interface typical applications are shown in the RF Matching Networks section.

3.2.2 Fractional-N Frequency Synthesizer

The EFR32MR21 contains a high performance, low phase noise, fully integrated fractional-N frequency synthesizer. The synthesizer is used in receive mode to generate the LO frequency for the down-conversion mixer. It is also used in transmit mode to directly generate the modulated RF carrier.

The fractional-N architecture provides excellent phase noise performance, frequency resolution better than 100 Hz, and low energy consumption. The synthesizer's fast frequency settling allows for very short receiver and transmitter wake up times to reduce system energy consumption.

3.2.3 Receiver Architecture

The EFR32MR21 uses a low-IF receiver architecture, consisting of a Low-Noise Amplifier (LNA) followed by an I/Q down-conversion mixer. The I/Q signals are further filtered and amplified before being sampled by the IF analog-to-digital converter (IFADC).

The IF frequency is configurable from 150 kHz to 1371 kHz. The IF can further be configured for high-side or low-side injection, providing flexibility with respect to known interferers at the image frequency.

The Automatic Gain Control (AGC) module adjusts the receiver gain to optimize performance and avoid saturation for excellent selectivity and blocking performance. The 2.4 GHz radio is calibrated at production to improve image rejection performance.

Demodulation is performed in the digital domain. The demodulator performs configurable decimation and channel filtering to allow receive bandwidths ranging from 0.1 to 2530 kHz. High carrier frequency and baud rate offsets are tolerated by active estimation and compensation. Advanced features supporting high quality communication under adverse conditions include forward error correction by block and convolutional coding as well as Direct Sequence Spread Spectrum (DSSS).

A Received Signal Strength Indicator (RSSI) is available for signal quality metrics, for level-based proximity detection, and for RF channel access by Collision Avoidance (CA) or Listen Before Talk (LBT) algorithms. An RSSI capture value is associated with each received frame and the dynamic RSSI measurement can be monitored throughout reception.

3.2.4 Transmitter Architecture

The EFR32MR21 uses a direct-conversion transmitter architecture. For constant envelope modulation formats, the modulator controls phase and frequency modulation in the frequency synthesizer. Transmit symbols or chips are optionally shaped by a digital shaping filter. The shaping filter is fully configurable, including the BT product, and can be used to implement Gaussian or Raised Cosine shaping.

Carrier Sense Multiple Access - Collision Avoidance (CSMA-CA) or Listen Before Talk (LBT) algorithms can be automatically timed by the EFR32MR21. These algorithms are typically defined by regulatory standards to improve inter-operability in a given bandwidth between devices that otherwise lack synchronized RF channel access.

3.2.5 Packet and State Trace

The EFR32MR21 Frame Controller has a packet and state trace unit that provides valuable information during the development phase. It features:

- Non-intrusive trace of transmit data, receive data and state information
- Data observability on a single-pin UART data output, or on a two-pin SPI data output
- Configurable data output bitrate / baudrate
- Multiplexed transmitted data, received data and state / meta information in a single serial data stream

3.2.6 Data Buffering

The EFR32MR21 features an advanced Radio Buffer Controller (BUFC) capable of handling up to 4 buffers of adjustable size from 64 bytes to 4096 bytes. Each buffer can be used for RX, TX or both. The buffer data is located in RAM, enabling zero-copy operations.

3.2.7 Radio Controller (RAC)

The Radio Controller controls the top level state of the radio subsystem in the EFR32MR21. It performs the following tasks:

- Precisely-timed control of enabling and disabling of the receiver and transmitter circuitry
- Run-time calibration of receiver, transmitter and frequency synthesizer
- Detailed frame transmission timing, including optional LBT or CSMA-CA

3.3 General Purpose Input/Output (GPIO)

EFR32MR21 has up to 20 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by Low-Energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have EM4 wake functionality. These pins are listed in 6.2 Alternate Function Table.

3.4 Clocking

3.4.1 Clock Management Unit (CMU)

The Clock Management Unit controls oscillators and clocks in the EFR32MR21. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

3.4.2 Internal and External Oscillators

The EFR32MR21 supports two crystal oscillators and fully integrates five RC oscillators, listed below.

- A high frequency crystal oscillator (HFXO) with integrated load capacitors, tunable in small steps, provides a precise timing reference for the MCU and RF synthesizer. The HFXO provides excellent RF clocking performance using a 38.4 MHz crystal. The HFXO can also support an external clock source such as a TCXO for applications that require an extremely accurate clock frequency over temperature.
- A 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast start-up at minimal energy consumption combined with a wide frequency range, from 1 MHz to 80 MHz.
- An integrated high frequency RC oscillator (HFRCOEM2) runs down to EM2 and is available for timing the general-purpose ADC and the Serial Wire Viewer port with a wide frequency range.
- An integrated fast start-up RC oscillator (FSRCO) that runs at a fixed 20 MHz
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO) for low power operation where high accuracy is not required.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.5 Counters/Timers and PWM

3.5.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 16-bit or 32-bit counter with up to 3 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers. In addition some timers offer dead-time insertion.

See 3.11 Configuration Summary for information on the feature set of each timer.

3.5.2 Low Energy Timer (LETIMER)

The unique LETIMER is a 24-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Peripheral Reflex System (PRS), and can be configured to start counting on compare matches from other peripherals such as the Real Time Clock.

3.5.3 Real Time Clock with Capture (RTCC)

The Real Time Clock with Capture (RTCC) is a 32-bit counter providing timekeeping down to EM3. The RTCC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user defined intervals.

A secondary RTC is used by the RF protocol stack for event scheduling, leaving the primary RTCC block available exclusively for application software.

3.5.4 Back-Up Real Time Counter (BURTC)

The Back-Up Real Time Counter (BURTC) is a 32-bit counter providing timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

3.5.5 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the Peripheral Reflex System (PRS).

3.6 Communications and Other Digital Peripherals

3.6.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.6.2 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality such as simple logic operations (AND, OR, NOT) can be applied by the PRS to the signals. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

3.7 Security Features

A dedicated security CPU enables the Secure Element function. It isolates cryptographic functions and data from the host Cortex-M33 core and provides the following security features:

- Secure Boot with Root of Trust and Secure Loader (RTSL)
- Cryptographic Accelerator
- True Random Number Generator (TRNG)
- Secure Debug with Lock/Unlock

3.7.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over The Air updates.

For more information about this feature, see AN1218: Series 2 Secure Boot with RTSL.

3.7.2 Cryptographic Accelerator

The Cryptographic Accelerator in Secure Element is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption (Secure Vault only), and Elliptic Curve Cryptography (ECC) to support public key operations and hashes.

Supported block cipher modes of operation for AES include:

- ECB (Electronic Code Book)
- CTR (Counter Mode)
- CBC (Cipher Block Chaining)
- CFB (Cipher Feedback)
- GCM (Galois Counter Mode)
- CCM (Counter with CBC-MAC)
- CBC-MAC (Cipher Block Chaining Message Authentication Code)
- GMAC (Galois Message Authentication Code)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the NIST (National Institute of Standards and Technology) recommended curves including P-192 and P-256 for ECDH (Elliptic Curve Diffie-Hellman) key derivation and ECDSA (Elliptic Curve Digital Signature Algorithm) sign and verify operations. Secure Vault also supports NIST recommended curves P-384 and P521, as well as the non-NIST Curve25519 for ECDH and Ed25519 for EdDSA (Edwards-curve Digital Signature Algorithm)

Secure Element also supports ECJ-PAKE (Elliptic Curve variant of Password Authenticated Key Exchange by Juggling). Secure Vault additionally supports PBKDF2 (Password-Based Key Derivation Function 2).

Supported hashes include SHA-1, SHA2/224, and SHA-2/256. Secure Vault also supports SHA-2/384, SHA-2/512, and Poly1305.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

Note: AES_ECB, AES_CBC, AES_CBCMAC, and SHA-1 are provided for legacy compatibility and are not recommended for cryptographic purposes without thoroughly understanding their potential security weaknesses.

3.7.3 True Random Number Generator

The True Random Number Generator module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31 as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.7.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

Secure Vault also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

For more information about this feature, see AN1190: Series 2 Secure Debug.

3.8 Reset Management Unit (RMU)

The RMU is responsible for handling reset of the EFR32MR21. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

3.9 Core and Memory

3.9.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M33 RISC processor achieving 1.50 Dhrystone MIPS/MHz
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- 512 kB flash program memory
- 64 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.9.2 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M33 and LDMA. In addition to the main flash array where Program code is normally written the MSC also provides an Information block where additional information such as special user information or flash-lock bits are stored. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.9.3 Linked Direct Memory Access Controller (LDMA)

The Linked Direct Memory Access (LDMA) controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.10 Memory Map

The EFR32MR21 memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

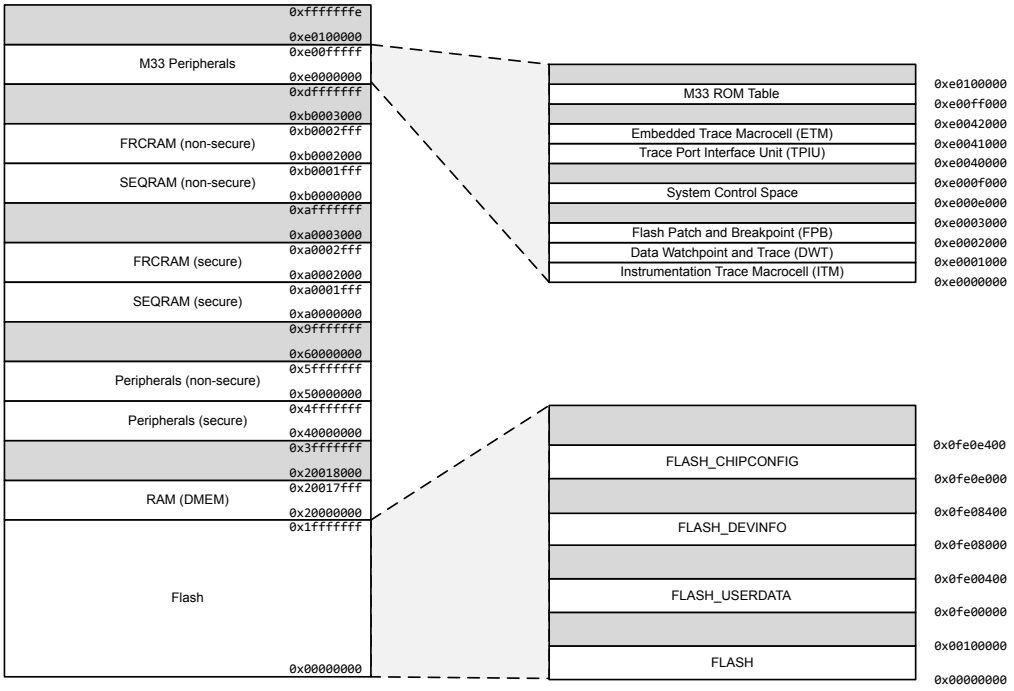

Figure 3.2. EFR32MR21 Memory Map — Core Peripherals and Code Space

3.11 Configuration Summary

The features of the EFR32MR21 are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration.

Table 3.1. Configuration Summary

Module	Lowest Energy Mode	Configuration
TIMER0	EM1	32-bit, 3-channels, +DTI
TIMER1	EM1	16-bit, 3-channels, +DTI
TIMER2	EM1	16-bit, 3-channels, +DTI
TIMER3	EM1	16-bit, 3-channels, +DTI
USART0	EM1	+IrDA, +I2S, +SmartCard
USART1	EM1	+IrDA, +I2S, +SmartCard
USART2	EM1	+IrDA, +I2S, +SmartCard

4. Electrical Specifications

4.1 Electrical Characteristics

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A = 25 °C and all supplies at 3.0 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

Power Supply Pin Dependencies

Due to on-chip circuitry (e.g., diodes), some EFR32 power supply pins have a dependent relationship with one or more other power supply pins. These internal relationships between the external voltages applied to the various EFR32 supply pins are defined below. Exceeding the below constraints can result in damage to the device and/or increased current draw.

- DVDD ≥ DECOUPLE
- PAVDD ≥ RFVDD
- AVDD, IOVDD: No dependency with each other or any other supply pin. Additional leakage may occur if DVDD remains unpowered with power applied to these supplies.

4.1.1 Absolute Maximum Ratings

Stresses above those listed below may cause permanent damage to the device. This is a stress rating only and functional operation of the devices at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-50	—	+150	°C
Junction temperature	T_{JMAX}	-I grade	—	—	+135	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs
Voltage on HFXO pins	$V_{HFXOPIN}$		-0.3	—	1.2	V
DC voltage on any GPIO pin	V_{DIGPIN}		-0.3	—	V_{IOVDD} + 0.3	V
Input RF level on pins RF2G4_IO1 and RF2G4_IO2	$P_{RFMAX2G4}$		—	—	+10	dBm
Absolute voltage on RF pins RF2G4_IOx	V_{MAX2G4}		-0.3	—	V_{PAVDD}	V
Total current into VDD power lines	I_{VDDMAX}	Source	—	—	200	mA
Total current into VSS ground lines	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

4.1.2 General Operating Conditions

This table specifies the general operating temperature range and supply voltage range for all supplies. The minimum and maximum values of all other tables are specifed over this operating range, unless otherwise noted.

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range	T_A	-I temperature grade [1]	-40	—	+125	° C
DVDD supply voltage	V_{DVDD}	EM0/1	1.71	3.0	3.8	V
		EM2/3/4[2]	1.71	3.0	3.8	V
AVDD supply voltage	V_{AVDD}		1.71	3.0	3.8	V
IOVDDx operating supply voltage (All IOVDD pins)	V_{IOVDDx}		1.71	3.0	3.8	V
PAVDD operating supply voltage	V_{PAVDD}		1.71	3.0	3.8	V
RFVDD operating supply voltage	V_{RFVDD}		1.71	3.0	V_{PAVDD}	V
DECOUPLE output capacitor[3]	$C_{DECOUPLE}$		0.75	1.0	2.75	µF
HCLK and Core frequency	f_{HCLK}	MODE = WS1, RAMWSEN = 1[4]	—	—	80	MHz
		MODE = WS1, RAMWSEN = 0[4]	—	—	50	MHz
		MODE = WS0, RAMWSEN = 0[4]	—	—	39	MHz
PCLK frequency	f_{PCLK}		—	—	50	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$		—	—	80	MHz
HCLK Radio frequency[5]	$f_{HCLKRADIO}$		38	38.4	40	MHz

Note:

1. The device may operate continuously at the maximum allowable ambient T_A rating as long as the absolute maximum T_{JMAX} is not exceeded. For an application with significant power dissipation, the allowable T_A may be lower than the maximum T_A rating. T_A = T_{JMAX} - ($THETA_{JA}$ x PowerDissipation). Refer to the Absolute Maximum Ratings table and the Thermal Characteristics table for T_{JMAX} and $THETA_{JA}$.
2. The DVDD supply is monitored by the DVDD BOD in EM0/1 and the LE DVDD BOD in EM2/3/4.
3. The system designer should consult the characteristic specs of the capacitor used on DECOUPLE to ensure its capacitance value stays within the specified bounds across temperature and DC bias.
4. Flash wait states are set by the MODE field in the MSC_READCTRL register. RAM wait states are enabled by setting the RAMWSEN bit in the SYSYCFG_DMEM0RAMCTRL register.
5. The recommended radio crystal frequency is 38.4 MHz. Any crystal frequency other than 38.4 MHz is expressly not supported. The minimum and maximum HCLKRADIO frequency in this table represent the design limits, which are much wider than the typical crystal tolerance.

4.1.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient QFN32 (4x4mm) Package	$THE\text{-}TA_{JA\_QFN32\_4X4}$	2-Layer PCB, Natural Convection[1]	—	94.3	—	°C/W
		4-Layer PCB, Natural Convection[1]	—	35.4	—	°C/W
Thermal Resistance Junction to Case QFN32 (4x4mm) Package	$THE\text{-}TA_{JC\_QFN32\_4X4}$	2-Layer PCB, Natural Convection[1]	—	36.3	—	°C/W
		4-Layer PCB, Natural Convection[1]	—	23.5	—	°C/W

Note:

1. Measured according to JEDEC standard JESD51-2A. Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air).

4.1.4 Current Consumption

4.1.4.1 MCU Current Consumption at 1.8 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = 1.8V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.4. MCU Current Consumption at 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled[1]	I_{ACTIVE}	80 MHz HFRCO, CPU running Prime from flash	—	50.9	—	µA/MHz
		80 MHz HFRCO, CPU running while loop from flash	—	45.5	—	µA/MHz
		80 MHz HFRCO, CPU running CoreMark loop from flash	—	59.7	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	63.6	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	55.5	—	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	59.1	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	67.0	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	360	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled[1]	I_{EM1}	80 MHz HFRCO	—	28.7	—	µA/MHz
		38.4 MHz crystal	—	46.7	—	µA/MHz
		38 MHz HFRCO	—	38.7	—	µA/MHz
		26 MHz HFRCO	—	42.2	—	µA/MHz
		16 MHz HFRCO	—	50.0	—	µA/MHz
		1 MHz HFRCO	—	343	—	µA/MHz
Current consumption in EM2 mode	I_{EM2}	Full RAM retention and RTC running from LFXO	—	24.9	—	µA
		Full RAM retention and RTC running from LFRCO	—	24.9	—	µA
		1 bank (16kB) RAM retention and RTC running from LFRCO	—	23.0	—	µA
Current consumption in EM3 mode	I_{EM3}	Full RAM retention and RTC running from ULFRCO	—	24.7	—	µA
		1 bank (16kB) RAM retention and RTC running from ULFRCO	—	22.7	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.15	—	µA
		BURTC with LFXO	—	0.51	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	120	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current Consumption per retained 16kB RAM bank in EM2	I_{RAM}		—	0.10	—	µA

Note:

1. The typical EM0/EM1 current measurement includes some current consumed by the security core for periodical housekeeping purposes. This does not include current consumed by user-triggered security operations, such as cryptographic calculations.

4.1.4.2 MCU Current Consumption at 3.0 V

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = PAVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.5. MCU Current Consumption at 3.0 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled[1]	I_{ACTIVE}	80 MHz HFRCO, CPU running Prime from flash	—	50.9	—	µA/MHz
		80 MHz HFRCO, CPU running while loop from flash	—	45.6	55.5	µA/MHz
		80 MHz HFRCO, CPU running CoreMark loop from flash	—	59.8	—	µA/MHz
		38.4 MHz crystal, CPU running while loop from flash	—	63.8	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	55.6	75.1	µA/MHz
		26 MHz HFRCO, CPU running while loop from flash	—	59.1	—	µA/MHz
		16 MHz HFRCO, CPU running while loop from flash	—	67.1	—	µA/MHz
		1 MHz HFRCO, CPU running while loop from flash	—	362	1018	µA/MHz
Current consumption in EM1 mode with all peripherals disabled[1]	I_{EM1}	80 MHz HFRCO	—	28.7	37.6	µA/MHz
		38.4 MHz crystal	—	46.9	—	µA/MHz
		38 MHz HFRCO	—	38.7	57.5	µA/MHz
		26 MHz HFRCO	—	42.2	—	µA/MHz
		16 MHz HFRCO	—	50.2	—	µA/MHz
		1 MHz HFRCO	—	345	994	µA/MHz
Current consumption in EM2 mode	I_{EM2}	Full RAM retention and RTC running from LFXO	—	25.0	—	µA
		Full RAM retention and RTC running from LFRCO	—	25.0	—	µA
		1 bank (16 kB) RAM retention and RTC running from LFRCO	—	23.1	70	µA
Current consumption in EM3 mode	I_{EM3}	Full RAM retention and RTC running from ULFRCO	—	24.8	70	µA
		1 bank (16 kB) RAM retention and RTC running from ULFRCO	—	22.8	—	µA
Current consumption in EM4 mode	I_{EM4}	No BURTC, no LF oscillator	—	0.24	—	µA
		BURTC with LFXO	—	0.56	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	160	—	µA
Current consumption per retained 16kB RAM bank in EM2	I_{RAM}		—	0.10	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. The typical EM0/EM1 current measurement includes some current consumed by the security core for periodical housekeeping purposes. This does not include current consumed by user-triggered security operations, such as cryptographic calculations.

4.1.4.3 Radio Current Consumption at 1.8 V

RF current consumption measured with MCU in EM1, HCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = 1.8V. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.6. Radio Current Consumption at 1.8 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	9.1	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	8.8	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	9.4	—	mA
		802.15.4 receiving frame, f = 2.4 GHz	—	9.4	—	mA
Current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	9.8	—	mA
		802.15.4, f = 2.4 GHz	—	9.2	—	mA
Current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power	—	9.9	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 0 dBm output power	—	16.6	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 10 dBm output power	—	34.9	—	mA

4.1.4.4 Radio Current Consumption at 3.0 V

RF current consumption measured with MCU in EM1, HCLK = 38.4 MHz, and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = RFVDD = PAVDD = 3.0V. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.7. Radio Current Consumption at 3.0 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	9.1	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	8.8	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	9.4	—	mA
		802.15.4 receiving frame, f = 2.4 GHz	—	9.5	—	mA
Current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz	—	9.0	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz	—	9.8	—	mA
		802.15.4, f = 2.4 GHz	—	9.2	—	mA
Current consumption in transmit mode	I_{TX}	f = 2.4 GHz, CW, 0 dBm PA, 0 dBm output power	—	10.5	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 0 dBm output power	—	16.7	—	mA
		f = 2.4 GHz, CW, 10 dBm PA, 10 dBm output power	—	35.4	—	mA
		f = 2.4 GHz, CW, 20 dBm PA, 10 dBm output power, PAVDD = 3.0 V	—	60.8	—	mA
		f = 2.4 GHz, CW, 20 dBm PA, 20 dBm output power, PAVDD = 3.3 V	—	186.5	—	mA

4.1.5 2.4 GHz RF Transceiver Characteristics

4.1.5.1 RF Transmitter Characteristics

4.1.5.1.1 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, PAVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Antenna port 2.

Table 4.8. RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Maximum TX power [1]	$POUT_{MAX}$	20 dBm PA, PAVDD = 3.3 V	—	+20	—	dBm
Maximum TX power	$POUT_{MAX10}$	10 dBm PA	—	+10	—	dBm
Maximum TX power	$POUT_{MAX0}$	0 dBm PA	—	+0	—	dBm
Minimum active TX power	$POUT_{MIN}$	20 dBm PA, PAVDD = 3.3 V	—	-14.1	—	dBm
		10 dBm PA	—	-13.3	—	dBm
		0 dBm PA	—	-24.9	—	dBm
Output power step size	$POUT_{STEP}$	0 dBm PA,-15 dBm < Output Power < -5 dBm	—	1.5	—	dB
		0 dBm PA,-5 dBm < Output Power < 0 dBm	—	0.3	—	dB
		10 dBm PA, -5 dBm < Output power < 0 dBm	—	1.5	—	dB
		10 dBm PA, 0 dBm < Output power < 10 dBm	—	0.3	—	dB
		20 dBm PA, 0 dBm < Output Power < 5 dBm	—	0.7	—	dB
		20 dBm PA, 5 dBm < output power < $POUT_{MAX}$	—	0.5	—	dB
Output power variation vs PAVDD supply voltage variation, frequency = 2450 MHz	$POUT_{VAR\_V}$	20 dBm PA P_{out} = $POUT_{MAX}$ output power with PAVDD voltage swept from 3.0V to 3.8V.	—	0.9	—	dB
		10 dbm PA output power with PAVDD voltage swept from 1.8 V to 3.0 V	—	0.1	—	dB
		0 dBm PA output power with PAVDD voltage swept from 1.8 V to 3.0 V	—	0.1	—	dB
Output power variation vs temperature, Frequency = 2450 MHz	$POUT_{VAR\_T}$	AVDD = 3.3V supply, 20 dBm PA at P_{out} = $POUT_{MAX}$, (-40 to +125 °C)	—	2.1	—	dB
		10 dBm PA at 10 dBm, (-40 to +125 °C)	—	1.2	—	dB
		0 dBm PA at 0 dBm, (-40 to +125 °C)	—	3	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output power variation vs RF frequency	$POUT_{VAR\_F}$	20 dBm PA, $POUT_{MAX}$, PAVDD = 3.3 V.	—	0.2	—	dB
		10 dBm PA, 10 dBm	—	0.1	—	dB
		0 dBm PA, 0 dBm	—	0.2	—	dB
Spurious emissions of harmonics in restricted bands per FCC Part 15.205/15.209	$SPUR_{HRM\_FCC\_R}$	Continuous transmission of CW carrier. P_{out} = $POUT_{MAX}$. PAVDD = 3.3V. Test Frequency = 2450 MHz.	—	-47	—	dBm
		Continuous transmission of CW carrier, P_{out} = 10 dBm, Test Frequency = 2450 MHz.	—	-47	—	dBm
Spurious emissions of harmonics in non-restricted bands per FCC Part 15.247/15.35	$SPUR_{HRM\_FCC\_NRR}$	Continuous transmission of CW carrier, P_{out} = $POUT_{MAX}$, PAVDD = 3.3V, Test Frequency = 2450 MHz.	—	-26	—	dBc
		Continuous transmission of CW carrier. P_{out} = 10 dBm. Test Frequency = 2450 MHz.	—	-26	—	dBc

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band (above 2.483 GHz or below 2.4 GHz) in restricted bands, per FCC part 15.205/15.209	$SPUR_{OOB\_FCC\_R}$	Restricted bands 30-88 MHz, Continuous transmission of CW carrier, 20 dBm PA, P_{out} = $POUT_{MAX}$, PAVDD = 3.3V. Test Frequency = 2450 MHz.	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of CW carrier, 20 dBm PA, P_{out} = $POUT_{MAX}$, PAVDD = 3.3V. Test Frequency = 2450 MHz.	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of CW carrier, 20 dBm PA P_{out} = $POUT_{MAX}$, PAVDD = 3.3V. Test Frequency = 2450 MHz.	—	-47	—	dBm
		Restricted bands >960 MHz, Continuous transmission of CW carrier, 20 dBm PA, P_{out} = $POUT_{MAX}$, PAVDD = 3.3V, Test Frequency = 2450 MHz.	—	-47	—	dBm
		Restricted bands 30-88 MHz, Continuous transmission of CW carrier, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands 88 - 216 MHz, Continuous transmission of CW carrier, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands 216 - 960 MHz, Continuous transmission of CW carrier, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-47	—	dBm
		Restricted bands > 960 MHz, Continuous transmission of CW carrier, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-47	—	dBm
Spurious emissions per ETSI EN300.440	$SPUR_{ETSI440}$	1G-14G, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-36	—	dBm
		47-74 MHz,87.5-108 MHz, 174-230 MHz, 470-862 MHz, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-56	—	dBm
		25-1000 MHz, excluding above frequencies. P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-42	—	dBm
		1G-12.75 GHz, excluding bands listed above, P_{out} = 10 dBm, Test Frequency = 2450 MHz.	—	-50	—	dBm

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious emissions out-of-band in non-restricted bands per FCC Part 15.247	$SPUR_{OOB\_FCC\_NR}$	Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission CW carrier, 20 dBm PA, P_{out} = $POUT_{MAX}$, PAVDD = 3.3 V,Test Frequency = 2450 MHz	—	-26	—	dBc
		Frequencies above 2.483 GHz or below 2.4 GHz, continuous transmission CW carrier, P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-26	—	dBc
Spurious emissions out-of-band, per ETSI 300.328	$SPUR_{ETSI328}$	[2400-2BW to 2400-BW], [2483.5+BW to 2483.5+2BW], P_{out} = 10 dBm, Test Frequency = 2450 MHz	—	-26	—	dBm
		[2400-BW to 2400], [2483.5 to 2483.5+BW] P_{out} = 10 dBm, Test Frequency = 2450 MHz.	—	-16	—	dB

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this data sheet can be found in the Max TX Power column of the Ordering Information Table.

4.1.5.2 RF Receiver Characteristics

4.1.5.2.1 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: T_A = 25 °C, PAVDD = 3.0V, AVDD = DVDD = IOVDD = RFVDD = PAVDD. Crystal frequency=38.4 MHz. RF center frequency 2.45 GHz. Antenna port 2.

Table 4.9. RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2400	—	2483.5	MHz
Receive mode maximum spurious emission	$SPUR_{RX}$	30 MHz to 1 GHz	—	-54.8	—	dBm
		1 GHz to 12 GHz	—	-57.1	—	dBm
Max spurious emissions during active receive mode, per FCC Part 15.109(a)	$SPUR_{RX\_FCC}$	216 MHz to 960 MHz, conducted measurement	—	-54.8	—	dBm
		Above 960 MHz, conducted measurement.	—	-77.3	—	dBm

4.1.6 Flash Characteristics

Table 4.10. Flash Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure[1]	EC_{FLASH}	$T_A \leq 125$ °C	10,000	—	—	cycles
Flash data retention[1]	RET_{FLASH}	$T_A \leq 125$ °C	10	—	—	years
Program Time	t_{PROG}	one word (32-bits)	25	31	35	µs
		average per word over 128 words	8	9.5	11	µs
Page Erase Time[2]	t_{PERASE}		16	17.5	20	ms
Mass Erase Time[3] [4]	t_{MERASE}		8	9	10.2	ms
Page Erase Current	I_{ERASE}	$T_A = 25$ °C	—	—	2.13	mA
Program Current	I_{WRITE}	$T_A = 25$ °C	—	—	2.73	mA
Mass Erase Current	I_{MERASE}	$T_A = 25$ °C	—	—	2.30	mA
Flash Supply voltage during write or erase	V_{FLASH}		1.71	—	3.8	V

Note:

1. Flash data retention information is published in the Quarterly Quality and Reliability Report.
2. Page Erase time is measured from setting the ERASEPAGE bit in the MSC_WRITECMD register until the BUSY bit in the MSC-STATUS register is cleared to 0. Internal set-up and hold times are included.
3. Mass Erase is issued by the CPU and erases all of User space.
4. Mass Erase time is measured from setting the ERASEMAIN0 bit in the MSC_WRITECMD register until the BUSY bit in the MSC-STATUS register is cleared to 0. Internal set-up and hold times are included.

4.1.7 Energy Mode Wake-up and Entry Times

Unless otherwise specified, these times are measured using the HFRCO at 19 MHz.

Table 4.11. Energy Mode Wake-up and Entry Times

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Wake-up Time from EM1	t_{EM1_WU}	Code execution from flash	—	3	—	HCLKs
		Code execution from RAM	—	1.42	—	µs
Wake-up Time from EM2	t_{EM2_WU}	Code execution from flash	—	16.6	—	µs
		Code execution from RAM	—	4.39	—	µs
		Code execution from flash @ 80 MHz	—	13.1	—	µs
		Code execution from RAM @ 80 MHz	—	3.32	—	µs
Wake-up Time from EM3	t_{EM3_WU}	Code execution from flash	—	16.6	—	µs
		Code execution from RAM	—	4.39	—	µs
		Code execution from flash @ 80 MHz	—	13.1	—	µs
		Code execution from RAM @ 80 MHz	—	3.32	—	µs
Wake-up Time from EM4	t_{EM4_WU}	Code execution from Flash	—	15.1	—	ms
Entry time to EM1	t_{EM1_ENT}	Code execution from flash	—	1.49	—	µs
Entry time to EM2	t_{EM2_ENT}	Code execution from flash	—	59.0	—	µs
Entry time to EM3	t_{EM3_ENT}	Code execution from flash	—	59.0	—	µs
Entry time to EM4	t_{EM4_ENT}	Code execution from flash	—	68.6	—	µs

4.1.8 Oscillators

4.1.8.1 High Frequency Crystal Oscillator

Unless otherwise indicated, typical conditions are: AVDD = DVDD = RFVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.12. High Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supported crystal equivalent series resistance (ESR)	ESR_{HFXO_38M4}	38.4 MHz, CL = 10 pF[1]	—	—	40	Ω
Supported range of crystal load capacitance	C_{HFXO_LC}	38.4 MHz, ESR = 40[2]	—	10	—	pF
Supply Current	I_{HFXO}		—	500	—	µA
Startup Time[3]	$T_{STARTUP}$	38.4 MHz, ESR = 40 Ω, C_L = 10 pF	—	160	—	µs
On-chip tuning cap step size[4]	SS_{HFXO}		—	0.04	—	pF

Note:

1. The crystal should have a maximum ESR less than or equal to this maximum rating.
2. It is recommended to use a crystal with a 10 pF load capacitance rating. Only crystals with a 10 pF load cap rating have been characterized for RF use.
3. Startup time does not include time implemented by programmable TIMEOUTSTEADY delay.
4. The tuning step size is the effective step size when incrementing both of the tuning capacitors by one count. The step size for the each of the individual tuning capacitors is twice this value.

4.1.8.2 Low Frequency Crystal Oscillator

Table 4.13. Low Frequency Crystal Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{LFXO}		—	32.768	—	kHz
Supported Crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	—	—	80	kΩ
		GAIN = 1 to 3	—	—	100	kΩ
Supported range of crystal load capacitance [1]	C_{L_LFXO}	GAIN = 0	6	—	6	pF
		GAIN = 1	6	—	10	pF
		GAIN = 2 (see note[2])	10	—	12.5	pF
		GAIN = 3 (see note[2])	12.5	—	18	pF
Current consumption	I_{CL12p5}	ESR = 70 kΩ, C_L = 12.5 pF, GAIN[3] = 2, AGC[4] = 1	—	220	—	nA
Startup Time	$T_{STARTUP}$	ESR = 70 kΩ, C_L = 7 pF, GAIN[3] = 1, AGC[4] = 1	—	45	—	ms
On-chip tuning cap step size	SS_{LFXO}		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting[5]	C_{LFXO_MIN}	CAPTUNE = 0	—	4	—	pF
On-chip tuning capacitor value at maximum setting[5]	C_{LFXO_MAX}	CAPTUNE = 0x4F	—	24.5	—	pF

Note:

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal

4.1.8.3 High Frequency RC Oscillator (HFRCO)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = 3.0 V. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.14. High Frequency RC Oscillator (HFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Frequency Accuracy	F_{HFRCO_ACC}	For all production calibrated frequencies	-3	—	3	%
Current consumption on all supplies[1]	I_{HFRCO}	F_{HFRCO} = 1 MHz	—	27	—	µA
		F_{HFRCO} = 2 MHz	—	27	—	µA
		F_{HFRCO} = 4 MHz	—	27	—	µA
		F_{HFRCO} = 7 MHz	—	63	—	µA
		F_{HFRCO} = 13 MHz	—	82	—	µA
		F_{HFRCO} = 16 MHz	—	92	—	µA
		F_{HFRCO} = 19 MHz	—	96	—	µA
		F_{HFRCO} = 26 MHz	—	123	—	µA
		F_{HFRCO} = 32 MHz	—	148	—	µA
		F_{HFRCO} = 38 MHz[2]	—	181	—	µA
		F_{HFRCO} = 40 MHz[3]	—	185	—	µA
		F_{HFRCO} = 48 MHz[2]	—	219	—	µA
		F_{HFRCO} = 56 MHz[2]	—	242	—	µA
		F_{HFRCO} = 64 MHz[2]	—	284	—	µA
		F_{HFRCO} = 80 MHz[2]	—	310	—	µA
Clock Out current for HFRCODPLL[4]	$I_{CLKOUT\_HFRCODPLL}$	FORCEEN bit of HFRCO0_CTRL = 1	—	5.0	—	µA/MHz
Clock Out current for HFRCOEM23[4]	$I_{CLKOUT\_HFRCOEM23}$	FORCEEN bit of HFRCOEM23_CTRL = 1	—	1.25	—	µA/MHz
Coarse trim step Size (% of period)	SS_{HFRCO_COARSE}	Step size measured at coarse trim mid-scale. (Fine trim also set to mid scale.)	—	0.64	—	%
Fine trim step Size (% of period)	SS_{HFRCO_FINE}	Step size measured at fine trim mid-scale. (Coarse trim also set to mid scale.)	—	0.1	—	%
Period jitter	PJ_{HFRCO}	19 MHz	—	0.04	—	% RMS
Startup Time[5]	$T_{STARTUP}$	FREQRANGE = 0 to 7	—	3.2	—	µs
		FREQRANGE = 8 to 15	—	1.2	—	µs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Band Frequency Limits[6]	f_{HFRCO_BAND}	FREQRANGE = 0	3.71	—	5.24	MHz
		FREQRANGE = 1	4.39	—	6.26	MHz
		FREQRANGE = 2	5.25	—	7.55	MHz
		FREQRANGE = 3	6.22	—	9.01	MHz
		FREQRANGE = 4	7.88	—	11.6	MHz
		FREQRANGE = 5	9.9	—	14.6	MHz
		FREQRANGE = 6	11.5	—	17	MHz
		FREQRANGE = 7	14.1	—	20.9	MHz
		FREQRANGE = 8	16.4	—	24.7	MHz
		FREQRANGE = 9	19.8	—	30.4	MHz
		FREQRANGE = 10	22.7	—	34.9	MHz
		FREQRANGE = 11	28.6	—	44.4	MHz
		FREQRANGE = 12	33	—	51	MHz
		FREQRANGE = 13	42.2	—	64.6	MHz
		FREQRANGE = 14	48.8	—	74.8	MHz
		FREQRANGE = 15	57.6	—	87.4	MHz

Note:

1. Does not include additional clock tree current. See specifications for additional current when selected as a clock source for a particular clock multiplexer.
2. This frequency is calibrated for the HFRCODPLL (HFRCO0) only.
3. This frequency is calibrated for the HFRCOEM23 only.
4. When the HFRCO is enabled for characterization using the FORCEEN bit, the total current will be the HFRCO core current plus the specified CLKOUT current. When the HFRCO is enabled on demand, the clock current may be different.
5. Hardware delay ensures settling to within ± 0.5%. Hardware also enforces this delay on a band change.
6. The frequency band limits represent the lowest and highest frequency which each band can achieve over the operating range.

4.1.8.4 Fast Start_Up RC Oscillator (FSRCO)

Table 4.15. Fast Start_Up RC Oscillator (FSRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FSRCO frequency	F_{FSRCO}		17.2	20	21.2	MHz

4.1.8.5 Low Frequency RC Oscillator

Table 4.16. Low Frequency RC Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		31.785	32.768	33.751	kHz
Startup time	$T_{STARTUP}$		—	128	—	µs
Current consumption	I_{LFRCO}		—	177	—	nA

4.1.8.6 Ultra Low Frequency RC Oscillator

Table 4.17. Ultra Low Frequency RC Oscillator

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation Frequency	F_{ULFRCO}		0.944	1.0	1.095	kHz

4.1.9 GPIO Pins (3V GPIO pins)

Unless otherwise indicated, typical conditions are: AVDD = DVDD = IOVDD = 3.0 V.

Table 4.18. GPIO Pins (3V GPIO pins)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, IOVDD = 1.71V	—	1.9	—	nA
		MODEx = DISABLED, IOVDD = 3.0 V	—	2.5	—	nA
		PC03, PC04 and PD00 pins. MODEx = DISABLED, IOVDD = 3.8 V T_A = 125 °C	—	—	340	nA
		All other GPIO pins. MODEx = DISABLED, IOVDD = 3.8 V T_A = 125 °C	—	—	250	nA
Input low voltage[1]	V_{IL}	Any GPIO pin	—	—	0.3 * IOVDD	V
		RESETn	—	—	0.3 * DVDD	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7 * IOVDD	—	—	V
		RESETn	0.7 * DVDD	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05 * IOVDD	—	—	V
		RESETn	0.05 * DVDD	—	—	V
Output low voltage	V_{OL}	Sinking 20mA, IOVDD = 3.0 V	—	—	0.2 * IOVDD	V
		Sinking 8mA, IOVDD = 1.71 V	—	—	0.4 * IOVDD	V
Output high voltage	V_{OH}	Sourcing 20mA, IOVDD = 3.0 V	0.8 * IOVDD	—	—	V
		Sourcing 8mA, IOVDD = 1.71 V	0.6 * IOVDD	—	—	V
GPIO rise time	T_{GPIO_RISE}	IOVDD = 3.0V, C_{load} = 50 pF, SLEWRATE = 4, 10% to 90%	—	6.5	—	ns
		IOVDD = 1.7V, C_{load} = 50 pF, SLEWRATE = 4, 10% to 90%	—	9.4	—	ns
GPIO fall time	T_{GPIO_FALL}	IOVDD = 3.0V, C_{load} = 50 pF, SLEWRATE = 4, 90% to 10%	—	5.7	—	ns
		IOVDD = 1.7V, C_{load} = 50 pF, SLEWRATE = 4, 90% to 10%	—	9.2	—	ns
Pull up/down resistance[2]	R_{PULL}	Any GPIO pin. Pull-up to IOVDD: MODEn = DISABLE DOUT=1. Pull-down to VSS: MODEn = WIREDORPULLDOWN DOUT = 0.	33	44	55	kΩ
		RESETn pin. Pull-up to DVDD	33	44	55	kΩ

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	26	—	ns
RESETn low time to ensure pin reset	T_{RESET}		100	—	—	ns

Note:

1. GPIO input thresholds are proportional to the IOVDD pin. RESETn input thresholds are proportional to DVDD.
2. GPIO pull-ups connect to IOVDD supply, pull-downs connect to VSS. RESETn pull-up connects to DVDD.

4.1.10 Temperature Sensor

Table 4.19. Temperature Sensor

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Temperature sensor range	T_{sense_range}		-40	—	125	°C
Temperature sensor resolution	$T_{senseRes}$		—	0.25	—	°C

4.1.11 Brown Out Detectors

4.1.11.1 DVDD BOD

BOD thresholds on DVDD in EM0 and EM1 only, unless otherwise noted. Typical conditions are at T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation, operating supply voltage range, and operating temperature range.

Table 4.20. DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{DVDD_BOD}	Supply Rising	—	1.67	1.71	V
		Supply Falling	1.62	1.65	—	V
BOD response time	$t_{DVDD\_BOD\_DELAY}$	Supply dropping at 100 mV/µs slew rate[1]	—	0.95	—	µs
BOD hysteresis	$V_{DVDD\_BOD\_HYST}$		—	20	—	mV

Note:
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.1.11.2 LE DVDD BOD

BOD thresholds on DVDD pin for low energy modes EM2 to EM4, unless otherwise noted.

Table 4.21. LE DVDD BOD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	$V_{DVDD\_LE\_BOD}$	Supply Falling	1.5	—	1.71	V
BOD response time	$t_{DVDD\_LE\_BOD\_DELAY}$	Supply dropping at 2 mV/µs slew rate[1]	—	50	—	µs
BOD hysteresis	$V_{DVDD\_LE\_BOD\_HYST}$		—	20	—	mV

Note:
1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.1.11.3 AVDD and VIO BODs

BOD thresholds for AVDD BOD and BOD for VIO supply or supplies. All energy modes.

Table 4.22. AVDD and VIO BODs

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold	V_{BOD}	Supply falling	1.45	—	1.71	V
BOD response time	t_{BOD_DELAY}	Supply dropping at 2 mV/µs slew rate[1]	—	50	—	µs
BOD hysteresis	V_{BOD_HYST}		—	20	—	mV

Note:

1. If the supply slew rate exceeds the specified slew rate, the BOD may trip later than expected (at a threshold below the minimum specified threshold), or the BOD may not trip at all (e.g., if the supply ramps down and then back up at a very fast rate)

4.1.12 USART SPI Main Timing

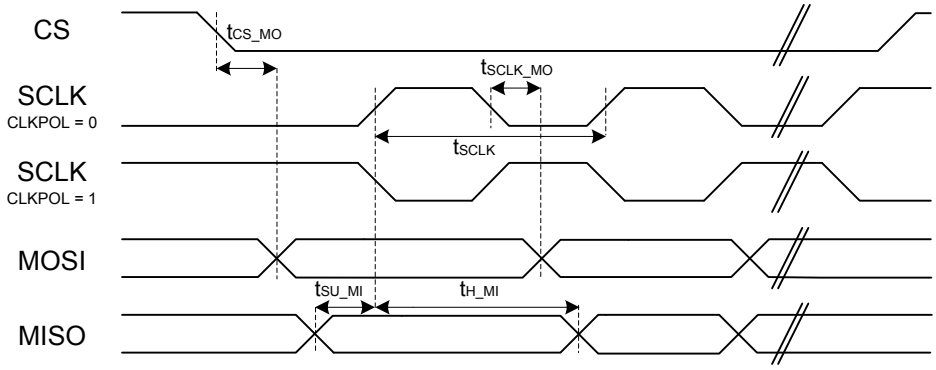

Figure 4.1. SPI Main Timing (SMSDELAY = 0)

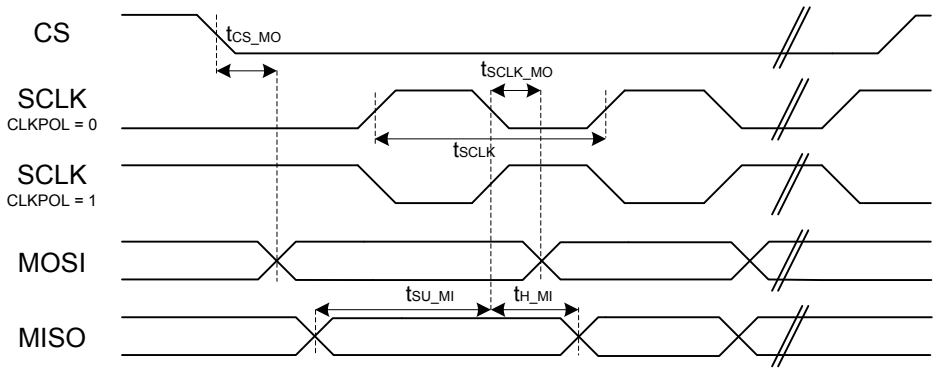

Figure 4.2. SPI Main Timing (SMSDELAY = 1)

4.1.12.1 USART SPI Main Timing

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.23. USART SPI Main Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		$2*t_{PCLK}$	—	—	ns
CS to MOSI[1 2]	t_{CS_MO}		-24	—	24.5	ns
SCLK to MOSI[1 2]	t_{SCLK_MO}		-17.5	—	16	ns
MISO setup time[1 2]	t_{SU_MI}	IOVDD = 1.62 V	50	—	—	ns
		IOVDD = 3.0 V	35	—	—	ns
MISO hold time[1 2]	t_{H_MI}		-9	—	—	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1.
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply.
3. t_{PCLK} is one period of the selected PCLK.

4.1.13 USART SPI Secondary Timing

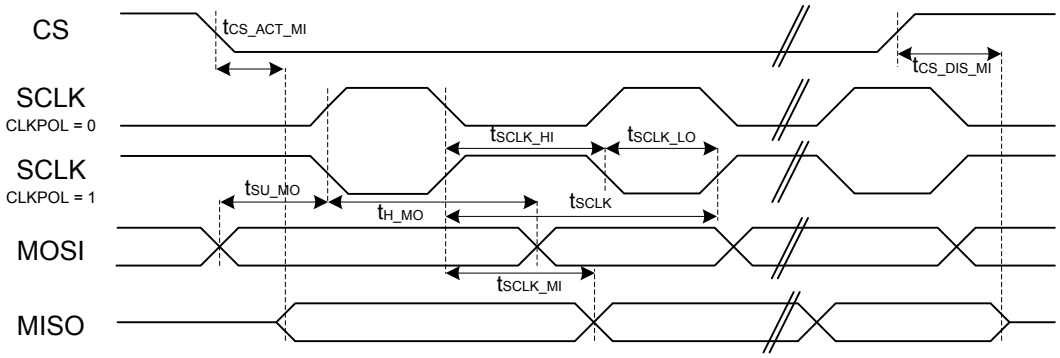

Figure 4.3. SPI Secondary Timing

4.1.13.1 USART SPI Secondary Timing

Timing specifications are for all SPI signals routed to the same DBUS (DBUSAB or DBUSCD). All GPIO set to slew rate = 6.

Table 4.24. USART SPI Secondary Timing

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SCLK period[1 2 3]	t_{SCLK}		6*t_{PCLK}	—	—	ns
SCLK high time[1 2 3]	t_{SCLK_HI}		2.5*t_{PCLK}	—	—	ns
SCLK low time[1 2 3]	t_{SCLK_LO}		2.5*t_{PCLK}	—	—	ns
CS active to MISO[1 2]	$t_{CS\_ACT\_MI}$		20	—	65	ns
CS disable to MISO[1 2]	$t_{CS\_DIS\_MI}$		19.5	—	57	ns
MOSI setup time[1 2]	t_{SU_MO}		3	—	—	ns
MOSI hold time[1 2 3]	t_{H_MO}		2	—	—	ns
SCLK to MISO[1 2 3]	t_{SCLK_MI}		16.5 + 1.5*t_{PCLK}	—	38 + 2.5*t_{PCLK}	ns

Note:
1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0).
2. Measurement done with 8 pF output loading at 10% and 90% of the I/O supply (figure shows 50%).
3. t_{PCLK} is one period of the selected PCLK.

4.2 Typical Performance Curves

Typical performance curves indicate typical characterized performance under the stated conditions.

4.2.1 Supply Current

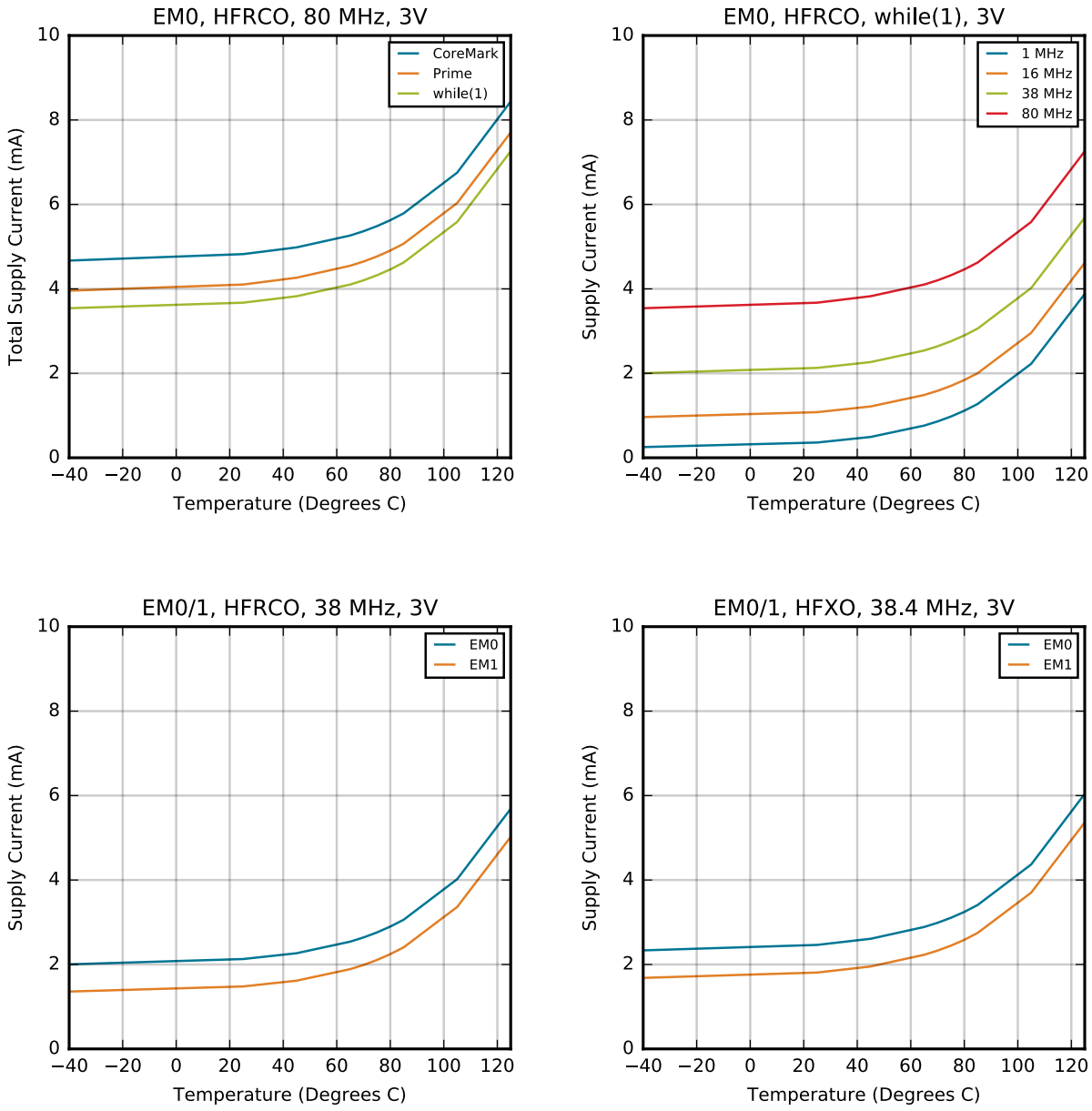

Figure 4.4. EM0 Active Mode Typical Supply Current vs. Temperature

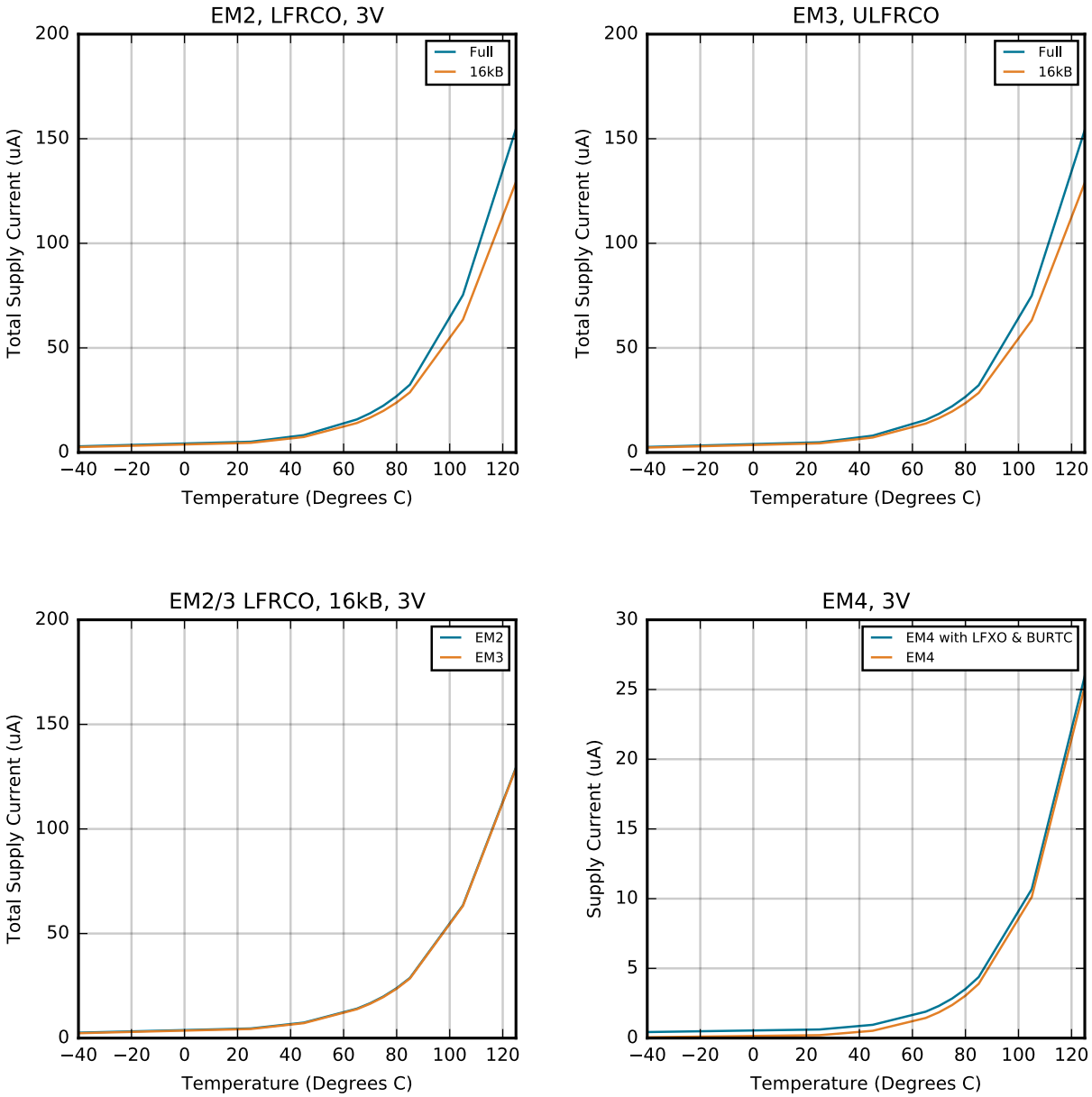

Figure 4.5. EM2, EM3, and EM4 Sleep Mode Typical Supply Current vs. Temperature

4.2.2 2.4 GHz Radio

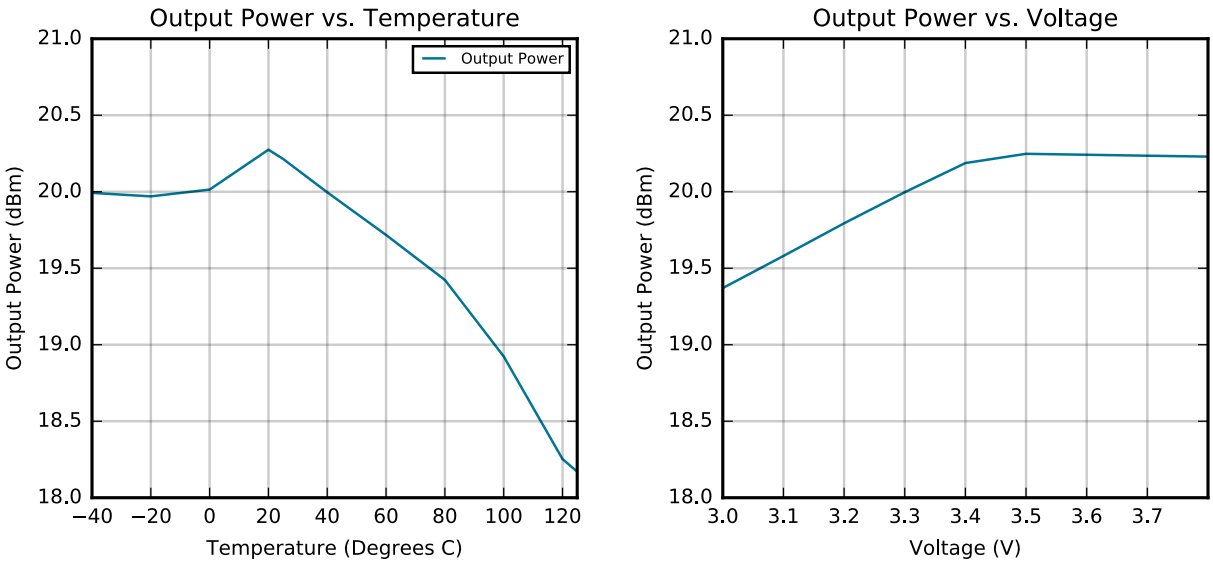

Figure 4.6. 2.4 GHz 20 dBm PA RF Transmitter Output Power

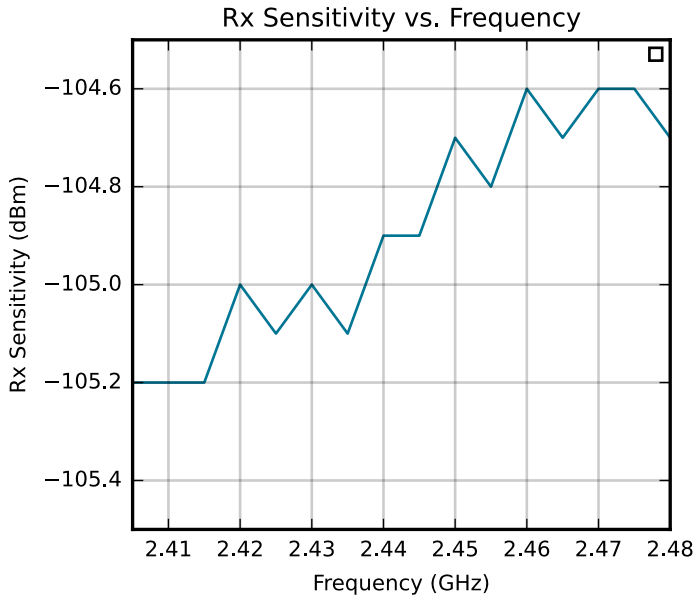

Figure 4.7. 2.4 GHz 802.15.4 RF Receiver Sensitivity

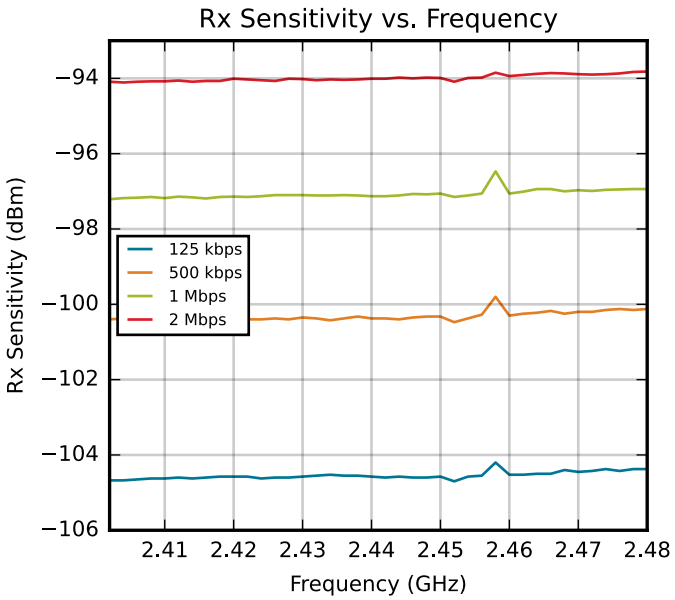

Figure 4.8. 2.4 GHz BLE RF Receiver Sensitivity

5. Typical Connection Diagrams

5.1 Power

Typical power supply connections are shown in the following figure.

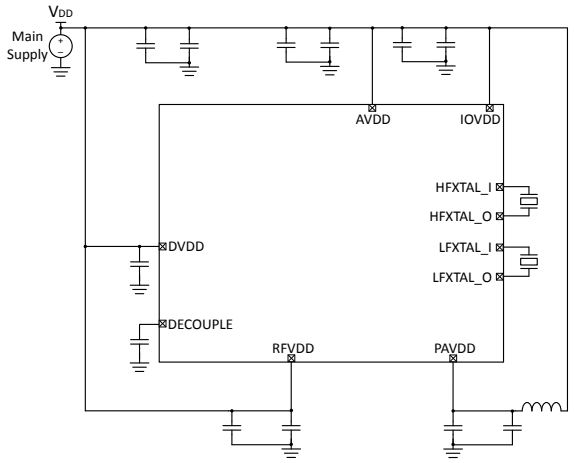

Figure 5.1. EFR32MR21 Typical Application Circuit: Direct Supply Configuration

5.2 RF Matching Networks

RF Matching Network connections are described in the following sub-sections. For more information on matching networks and recommendations, see AN930.2: EFR32 Series 2 2.4 GHz Matching Guide and AN928.2: EFR32 Series 2 Layout Design Guide.

5.2.1 2.4 GHz 20 dBm Matching Network

The recommended RF matching network circuit diagram for 2.4 GHz applications is shown in Figure 5.2 Typical 20 dBm 2.4 GHz RF impedance-matching network circuit on page 44. Typical component values are shown in Table 5.1 2.4 GHz 20 dBm Component Values on page 44. Please refer to the development board Bill of Materials for specific part recommendation including tolerance, component size, recommended manufacturer, and recommended part number.

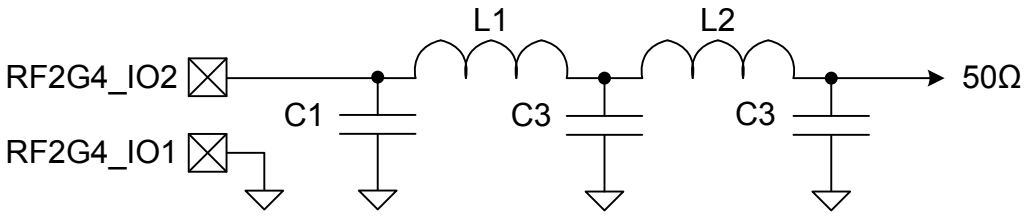

Figure 5.2. Typical 20 dBm 2.4 GHz RF impedance-matching network circuit

Table 5.1. 2.4 GHz 20 dBm Component Values

Designator	Value
C1	2.3 pF
L1	2.3 nH
C2	0.8 pF
L2	1.1 nH
C3	0.3 pF

5.3 Other Connections

Other components or connections may be required to meet the system-level requirements. Application note, AN0002.2: EFM32 and EFR32 Wireless Gecko Series 2 Hardware Design Considerations, contains detailed information on these connections. Application notes can be accessed on the Silicon Labs website (www.silabs.com/32bit-appnotes).

6. Pin Definitions

6.1 QFN32 Device Pinout

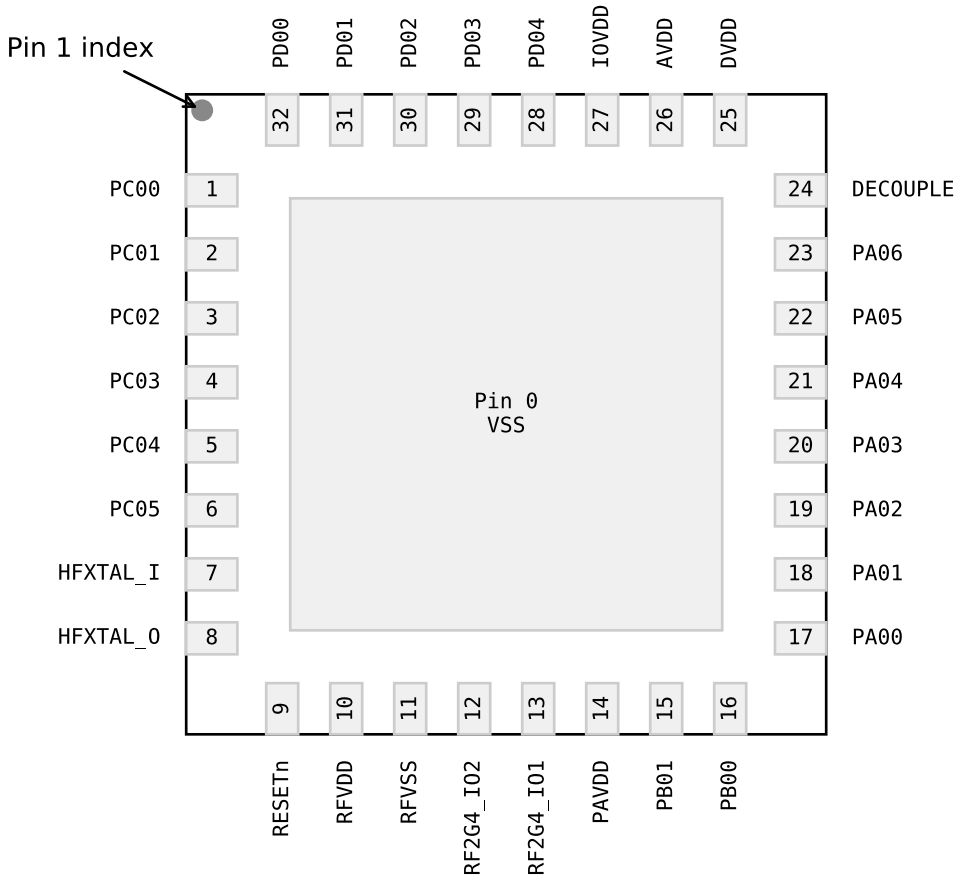

Figure 6.1. QFN32 Device Pinout

The following table provides package pin connections and general descriptions of pin functionality. For detailed information on the supported features for each GPIO pin, see 6.2 Alternate Function Table and 6.3 Digital Peripheral Connectivity.

Table 6.1. QFN32 Device Pinout

Pin Name	Pin(s)	Description	Pin Name	Pin(s)	Description
PC00	1	GPIO	PC01	2	GPIO
PC02	3	GPIO	PC03	4	GPIO
PC04	5	GPIO	PC05	6	GPIO
HFXTAL_I	7	High Frequency Crystal Input	HFXTAL_O	8	High Frequency Crystal Output
RESETn	9	Reset Pin	RFVDD	10	Radio power supply
RFVSS	11	Radio Ground	RF2G4_IO2	12	2.4 GHz RF input/output
RF2G4_IO1	13	2.4 GHz RF input/output	PAVDD	14	Power Amplifier (PA) power supply
PB01	15	GPIO	PB00	16	GPIO
PA00	17	GPIO	PA01	18	GPIO
PA02	19	GPIO	PA03	20	GPIO
PA04	21	GPIO	PA05	22	GPIO
PA06	23	GPIO	DECOUPLE	24	Decouple output for on-chip voltage regulator. An external decoupling capacitor is required at this pin.
DVDD	25	Digital power supply	AVDD	26	Analog power supply
IOVDD	27	Digital IO power supply.	PD04	28	GPIO
PD03	29	GPIO	PD02	30	GPIO
PD01	31	GPIO	PD00	32	GPIO

6.2 Alternate Function Table

A wide selection of alternate functionality is available for multiplexing to various pins. The following table shows GPIO pins with support for dedicated functions. Note that some functions may not be available on all device variants.

Table 6.2. GPIO Alternate Function Table

GPIO	Alternate Functions
PA01	GPIO.SWCLK
PA02	GPIO.SWDIO
PA03	GPIO.SWV GPIO.TDO GPIO.TRACEDATA0
PA04	GPIO.TDI GPIO.TRACECLK
PA05	GPIO.EM4WU0
PB01	GPIO.EM4WU3
PC00	GPIO.EM4WU6
PC05	GPIO.EM4WU7
PD00	LFXO.LFXTAL_O
PD01	LFXO.LFXTAL_I LFXO.LF_EXTCLK
PD02	GPIO.EM4WU9

6.3 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. Note that some functions may not be available on all device variants.

Table 6.3. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available
USART1.CLK	Available	Available		
USART1.CS	Available	Available		
USART1.CTS	Available	Available		
USART1.RTS	Available	Available		
USART1.RX	Available	Available		
USART1.TX	Available	Available		
USART2.CLK			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
USART2.CS			Available	Available
USART2.CTS			Available	Available
USART2.RTS			Available	Available
USART2.RX			Available	Available
USART2.TX			Available	Available

7. QFN32 Package Specifications

7.1 QFN32 Package Dimensions

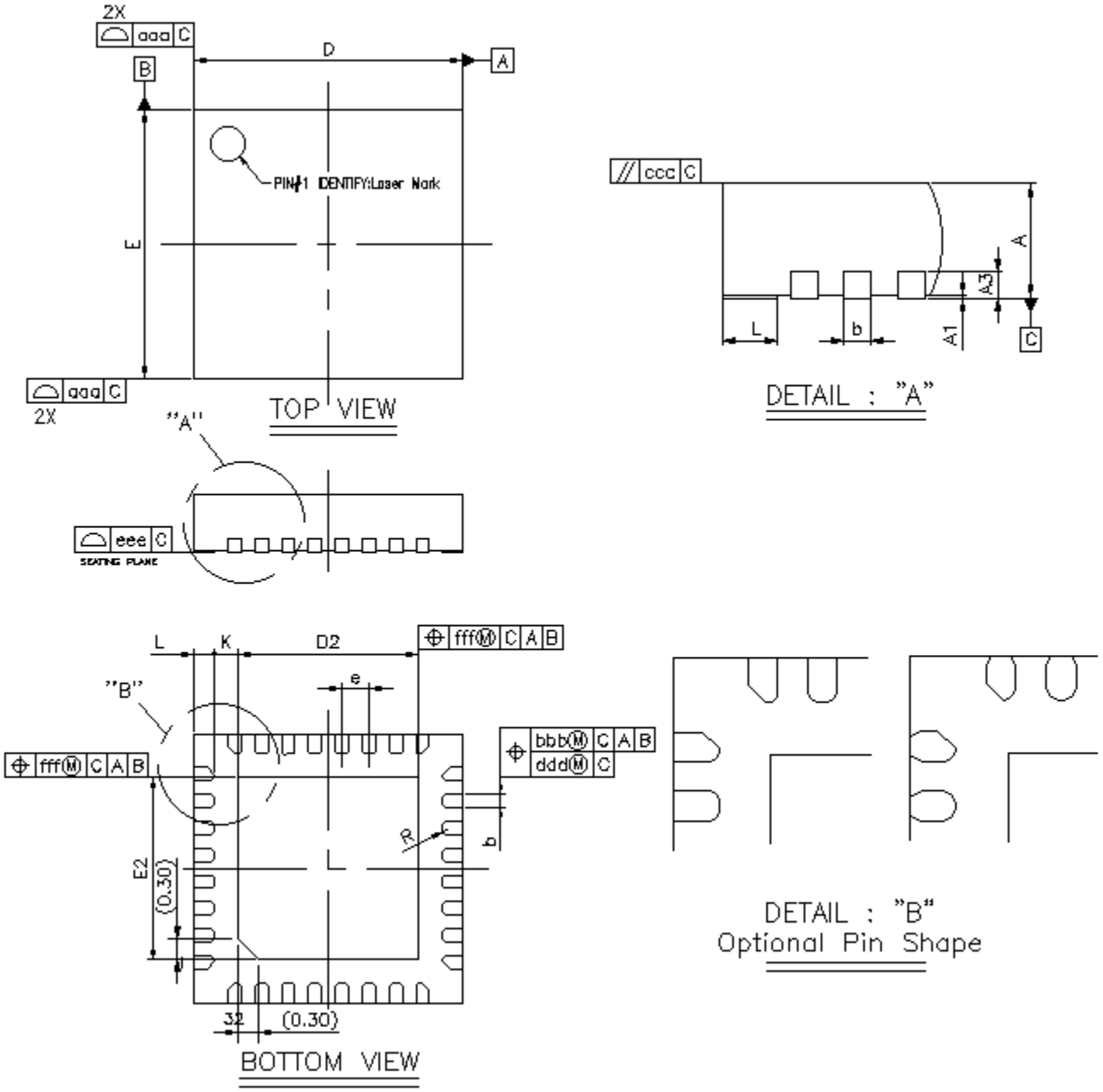

Figure 7.1. QFN32 Package Drawing

Table 7.1. QFN32 Package Dimensions

Dimension	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
e		0.40 BSC	
L	0.20	0.30	0.40
K	0.20	—	—
R	0.075	—	0.125
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 QFN32 PCB Land Pattern

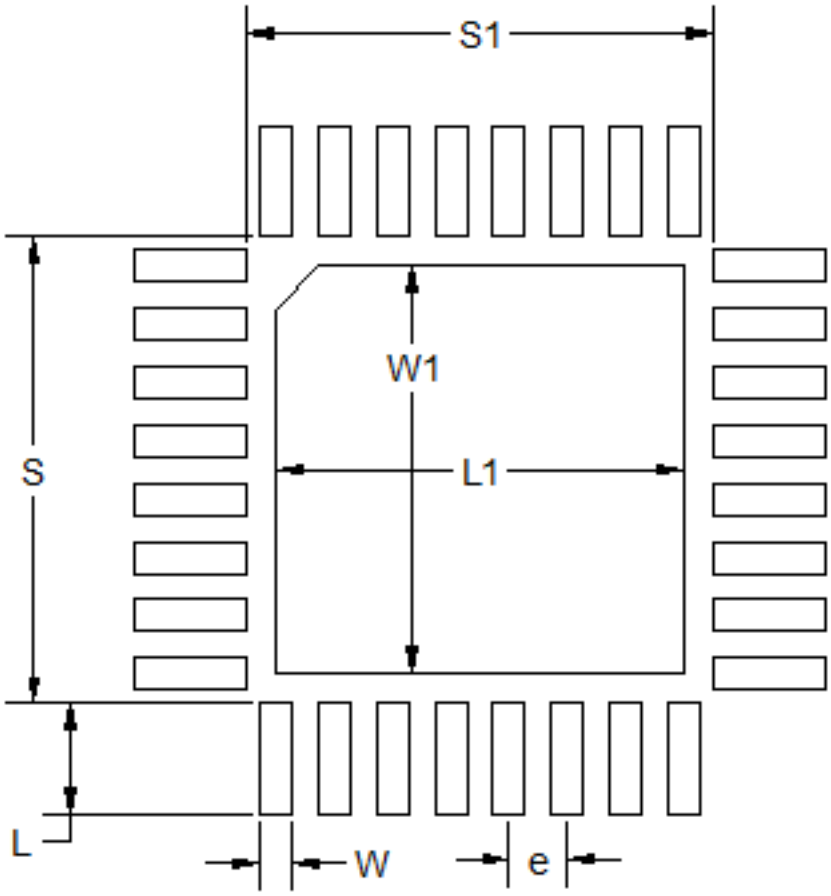

Figure 7.2. QFN32 PCB Land Pattern Drawing

Table 7.2. QFN32 PCB Land Pattern Dimensions

Dimension	Typ
L	0.76
W	0.22
e	0.40
S	3.21
S1	3.21
L1	2.80
W1	2.80

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.
4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.101 mm (4 mils).
6. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.
7. A 2x2 array of 1.10 mm x 1.10 mm openings on a 1.30 mm pitch can be used for the center ground pad.
8. A No-Clean, Type-3 solder paste is recommended.
9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
10. ***Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.***

7.3 QFN32 Package Marking

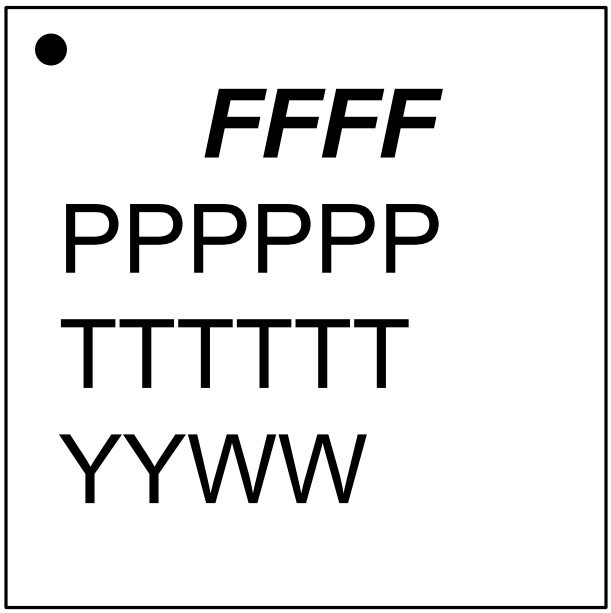

Figure 7.3. QFN32 Package Marking

The package marking consists of:

- FFFF – The product family codes.
  1. Family Code (M)
  2. R (RCP)
  3. Series (2)
  4. Device Configuration (1)
- PPPPPP – The product option codes.
  - 1-2. MCU Feature Codes
  - 3-4. Radio Feature Codes
  - 5. Flash (H = 512k)
  - 6. Temperature grade (I = -40 to 125 °C)
- TTTTTT – A trace or manufacturing code. The first letter is the device revision.
- YY – The last 2 digits of the assembly year.
- WW – The 2-digit workweek when the device was assembled.

8. Revision History

Revision 1.0

May, 2023

- Electrical performance specifications updated with final limits.
- Supply current errata for EM2/EM3 current rolled into specification tables.

Revision 0.2

April, 2023

- Added Matter Thread RCP to Supported Protocols list.
- Updated links to antenna matching and layout application notes.

Revision 0.1

February, 2022

- Initial release.

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Silicon Laboratories Inc.
400 West Cesar Chavez
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