TPS65233-1 LNB Voltage Regulator With I²C Interface

1 Features

- Complete Integration Solution for LNB and I²C
- DiSEqC 1.x Compatible
- Supports 9-V and 12-V Power Bus
- Up to 1000-mA Accurate Output Current Limit Adjustable by External Resistor and I²C
- Boost Converter With Low R_{dson} Internal Power Switch
- Dedicated Enable Pin for Non-I²C Application
- Low Noise, Low Drop Output With Push-Pull Output Stage
- Built-In Accurate 22-kHz Tone Generator or External Pin
- Adjustable Soft-Start and 13-V/18-V Voltage Transition Time
- Compliant With Main Satellite Receiver Systems Specifications
- LNB Short Circuit Dynamic Protection
- Diagnostics for Output Voltage Level, Input Supply UVLO, and DiSEqC Tone Output
- Cable Disconnect Diagnostic
- Available in a 16-Pin WQFN 3.00-mm × 3.00-mm (RTE) Package

2 Applications

- Set-Top Box Satellite Receiver
- TV Satellite Receiver
- PC Card Satellite Receiver

3 Description

Designed for analog and digital satellite receivers, the TPS65233-1 is a monolithic voltage regulator with I²C interface, specifically to provide the 13-V/18-V power supply and the 22-kHz tone signaling to the LNB down-converter in the antenna dish or to the multi-switch box. It offers a complete solution with very low component count, low power dissipation together with simple design and I²C standard interfacing.

TPS65233-1 features high power efficiency. The boost converter integrates a 120-mΩ power MOSFET running at 1-MHz switching frequency. Drop out voltage at the linear regulator is 0.8 V to minimize power loss. TPS65233-1 provides multiple ways to generate the 22-kHz signal. Integrated linear regulator with push-pull output stage generates clean 22-kHz tone signal superimposed at the output even at zero loading. Current limit of linear regulator can be programmed by external resistor with ±10% accuracy. Full range of diagnostic read by I²C is available for system monitoring.

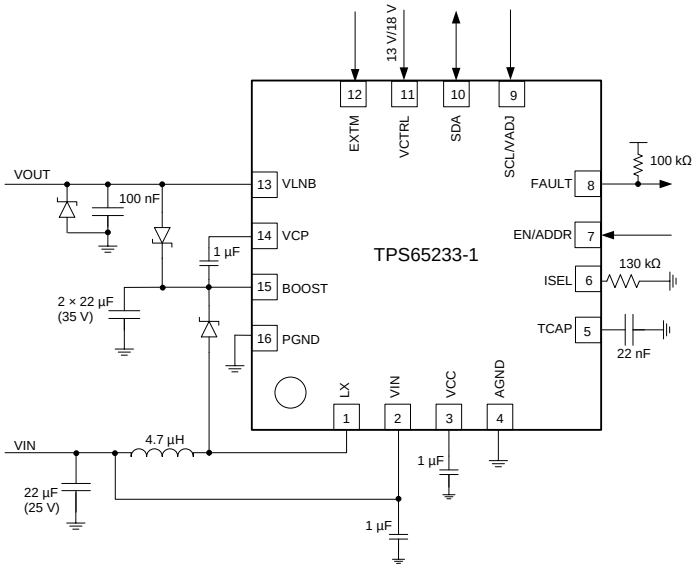
The part is available in a 16-pin WQFN 3.00-mm × 3.00-mm (RTE) package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65233-1	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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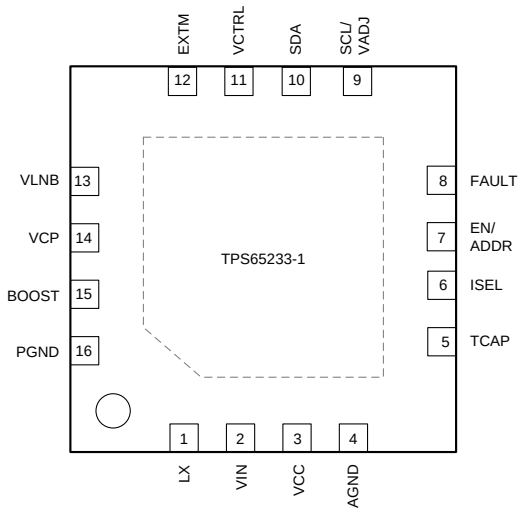
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2015	*	Initial release.

5 Pin Configuration and Functions

RTE Package
12-Pin WQFN
Top View



Exposed pad must be soldered to PCB for optimal thermal performance.

Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
AGND	4	Analog ground. Connect all ground pins and power pad together.
BOOST	15	Output of the boost regulator and input voltage of the internal linear regulator
EN/ADDR	7	Enable pin to enable the whole chip; pull to ground to disable output, output will be pulled to ground. For I^2C interface, pulling this pin high or low gives different I^2C addresses.
EXTM	12	External modulation logic input pin which activates the 22-kHz tone output, feeding signal can be 22-kHz tone or logic high or low.
FAULT	8	This pin is an open drain output pin, it goes low if any fault flag is set.
ISEL	6	Connect a resistor to this pin to set the LNB output current limit.
LX	1	Switching node of the boost converter
PGND	16	Power ground for boost converter
SCL/VADJ	9	I^2C compatible clock input; if I^2C function is not used, connect this pin to low set output voltage 13 V/18 V, connect to high set output voltage 13.4 V/18.6 V
SDA	10	I^2C compatible bi-directional data
TCAP	5	Connect a capacitor to this pin to set the rise time and fall time of the LNB output between 13 V and 18 V.
VCC	3	Internal 6.5-V power supply bias. Connect a 1-µF ceramic capacitor from this pin to ground. When V_{IN} is 5 V, connect VCC to V_{IN}.
VCP	14	Gate drive supply voltage, output of charge pump, connect a capacitor between this pin to pin BOOST.
VCTRL	11	Logic control pin for 13-V or 18-V voltage selection at LNB output
VIN	2	Input of internal linear regulator
VLNB	13	Output of the LNB power supply connected to satellite receiver or switch
Thermal pad	—	Must be soldered to PCB for optimal thermal performance. Have thermal vias on the PCB to enhance power dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range, all voltages are with respect to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VIN, LX, BOOST, VLNB	–1	30	V
	VCP		BOOST + 7	
	LX	–1	30	
	VCC, EN, FAULT, SCL, SDA, VCTRL, ISEL, EXTM	–0.3	7	
	TCAP	–0.3	3.6	
	PGND, AGND	–0.3	0.3	
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, other pins(1)	2000	V
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, pin 13 (VLNB)(1)	6000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		20	V
T_A	Junction temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS65233-1 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Input voltage range	VIN	4.5	12	20	V
IDD_{SDN}	Shutdown supply current	EN = 0		160		µA
IDD_Q	LDO input quiescent current	EN = 1, I_{OUT} = 0 A, V_{BOOST} = 14 V, I_{LNB} = 0 mA		10.5		mA
UVLO	V_{IN} under voltage lockout	Rising V_{IN}	4.05	4.25	4.45	V
		Falling V_{IN}	3.6	3.8	4.1	
		Hysteresis		450		mV
OUTPUT VOLTAGE						
V_{OUT}	Regulated output voltage (non-I^2C mode)	VCTRL = 1, SCL = 0, I_{OUT} = 500 mA		18		V
		VCTRL = 1, SCL = 1, I_{OUT} = 500 mA	18.2	18.6	19	
		VCTRL = 0, SCL = 0, I_{OUT} = 500 mA		13		
		VCTRL = 0, SCL = 1, I_{OUT} = 500 mA	13.1	13.4	13.7	
$V_{LINEREG}$	Line regulation-DC	V_{IN} = 7.5 V to 16 V, I_{OUT} = 500 mA		0.2		%/V
$V_{LOADREG}$	Load regulation-DC	I_{OUT} = (10-90%) × I_{OUTMAX}		0.7		%/A
IOCP	Output short circuit current limit	R_{SEL} = 200 kΩ, T_J = 25°C	580	650	720	mA
T_r, T_f	13-V/18-V transition rising/falling time	C_{TCAP} = 5.6 nF		0.33		ms
f_{SW}	Boost switching frequency			1040		kHz
$I_{limitsw}$	Switching current limit	V_{IN} = 12 V, V_{OUT} = 18.6 V		3.2		A
R_{dson_LS}	On resistance of low side FET on CH	V_{IN} = 12 V		120		mΩ
V_{drop}	Linear regulator voltage drop-out	I_{OUT} = 500 mA		0.8		V
I_{rev}	Reverse bias current	EN = 1, V_{LNB} = 21 V		50		mA
I_{rev_dis}	Disabled reverse bias current	EN = 0, V_{LNB} = 21 V		3		mA
LOGIC SIGNALS						
V_{EN}	Enable threshold level			1.15		V
V_{ENH}	Enable threshold level hysteresis			80		mV
V_{LOGICh}, V_{LOGICl}	VCTRL, EXTM Logic threshold level	High level input voltage	2			V
		Low level input voltage			0.8	
$V_{OL\ FAULT}$	FAULT output low voltage	FAULT open drain, I_{OL}= 1 mA			0.4	V
f_{I2C}	Maximum I^2C clock frequency		400			kHz
TONE						
f_{tone}	Tone frequency		20	22	24	kHz
A_{tone}	Tone amplitude	I_{OUT} = 0 mA to 500 mA, C_{OUT} = 100 nF	550	680	750	mV
D_{tone}	Tone duty cycle		45%	50%	55%	
PROTECTION						
TON	Over current protection on time			4		ms
TOFF	Over current protection off time			128		ms
THERMAL SHUTDOWN						
T_{TRIP}	Thermal shut down trip point	Rising temperature		160		°C
T_{HYST}	Thermal shut down hysteresis			20		°C

Electrical Characteristics (continued)

T_J = –40°C to 125°C, V_{IN} = 12 V, f_{SW} = 1 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I²C READ BACK FAULT STATUS						
V_{PGOOD}	PGOOD trip levels	Feedback voltage low side rising		95.3%		
		Feedback voltage low side falling		94.7%		
		Feedback voltage high side rising		105.3%		
		Feedback voltage high side falling		104.7%		
T_{warn}	Temperature warning threshold			125		°C
I²C INTERFACE						
V_{IH}	SDA,SCL input high voltage		2			V
V_{IL}	SDA,SCL input low voltage				0.8	V
I_I	Input current	SDA, SCL, V_I = 0.4 V to 4.5 V	–10		10	µA
V_{OL}	SDA output low voltage	SDA open drain, I_{OL} = 2 mA			0.4	V
$f_{(SCL)}$	Maximum SCL clock frequency		400			kHz
C_B	Capacitance of one bus line (SCL and SDA)				400	pF

6.6 I²C Interface Timing Requirements

		MIN	MAX	UNIT
t_{BUF}	Bus free time between a STOP and START condition	1.3		µs
$t_{HD, STA}$	Hold time (Repeated) START condition	0.6		µs
$t_{SU, STO}$	Setup time for STOP condition	0.6		µs
t_{LOW}	LOW period of the SCL clock	1.3		µs
t_{HIGH}	HIGH period of the SCL clock	0.6		µs
$t_{SU, STA}$	Setup time for a repeated START condition	0.6		µs
$t_{SU, DAT}$	Data setup time	0.1		µs
$t_{HD, DAT}$	Data hold time	0	0.9	µs
t_{RCL}	Rise time of SCL signal	20 + 0.1C_B	300	ns
t_{RCL1}	Rise time of SCL signal after a repeated START condition and after an acknowledge BIT	20 + 0.1C_B	300	ns
t_f	Fall time of SCL signal	20 + 0.1C_B	300	ns
t_r	Rise time of SDA signal	20 + 0.1C_B	300	ns
t_{FDA}	Fall time of SDA signal	20 + 0.1C_B	300	ns

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT VOLTAGE						
Tr, Tf	13-V/18-V Transition rising falling time	Ccap = 5.6 nF		0.33		ms
TONE						
T_{rtone}	Tone rise time	I_{OUT} = 0 to 500 mA, C_{OUT} = 100 nF		10		µs
T_{ftone}	Tone fall time	I_{OUT} = 0 to 500 mA, C_{OUT} = 100 nF		10		µs

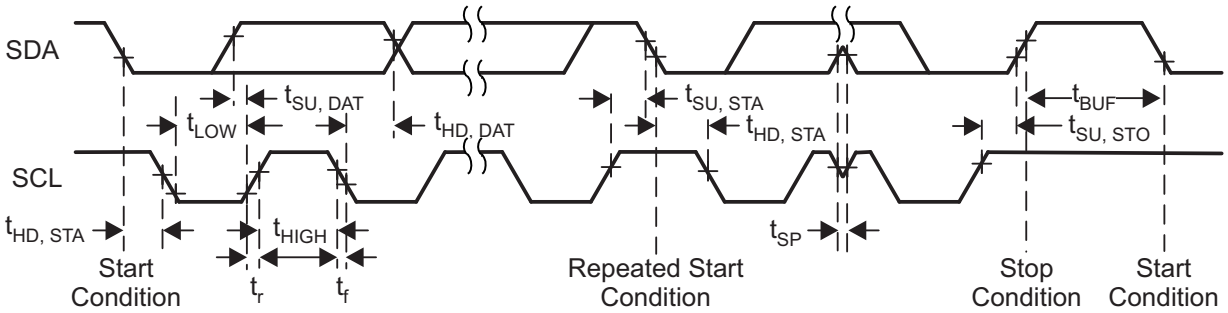


Figure 1. I²C Interface Timing Diagram

6.8 Typical Characteristics

T_A = 25°C, V_{IN} = 12 V, f_{SW} = 1 MHz, L = 4.7 µH, C_{Boost} = 2 × 22 µF/35 V (unless otherwise noted)

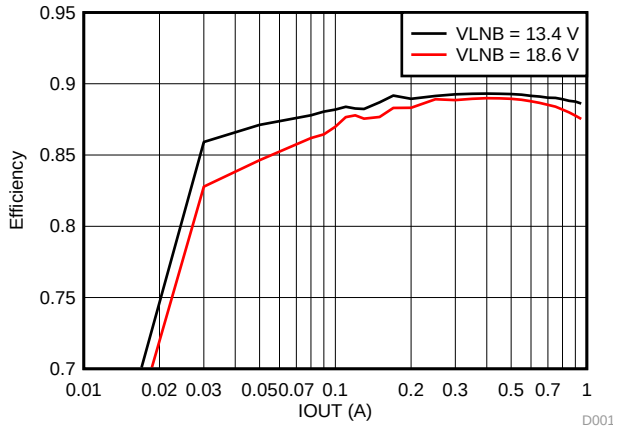


Figure 2. Power Efficiency

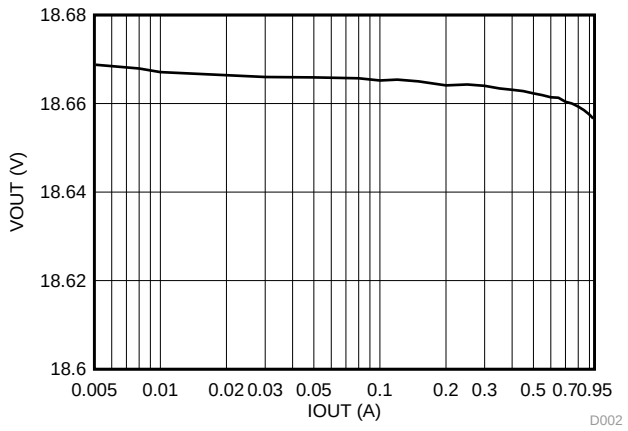


Figure 3. Load Regulation, VLNB = 18.6 V

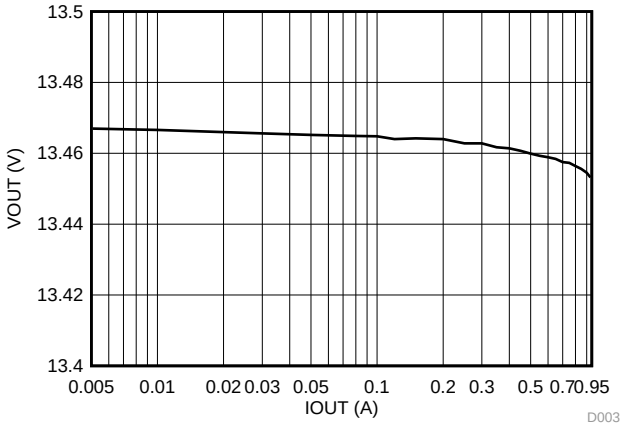


Figure 4. Load Regulation, VLNB = 13.4 V

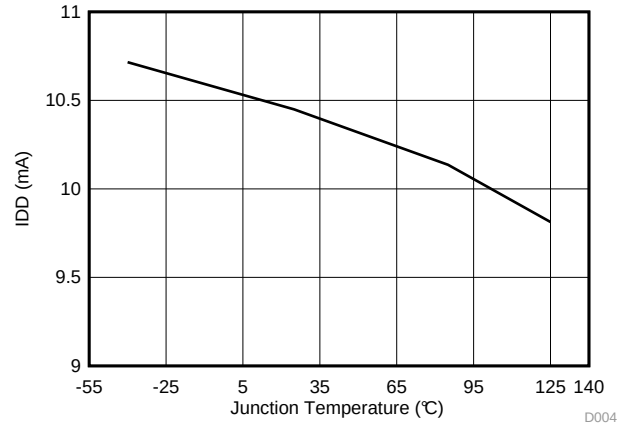


Figure 5. LDO Input Quiescent Current and Junction Temperature, V_{BOOST} = 14 V, I_{LNB} = 0 mA

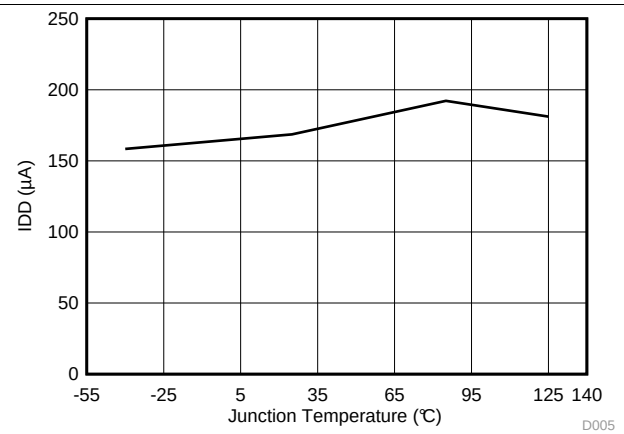


Figure 6. Shutdown Current and Junction Temperature

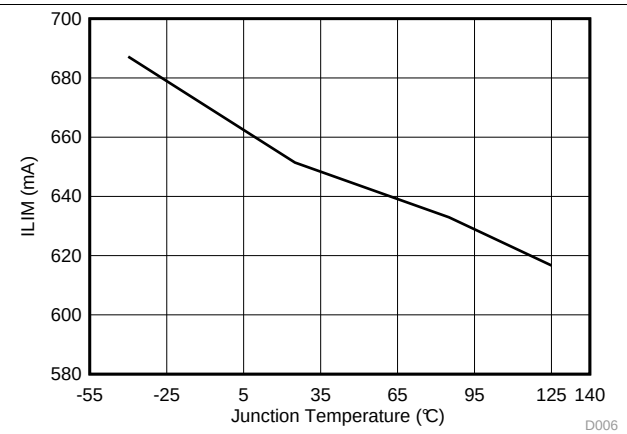


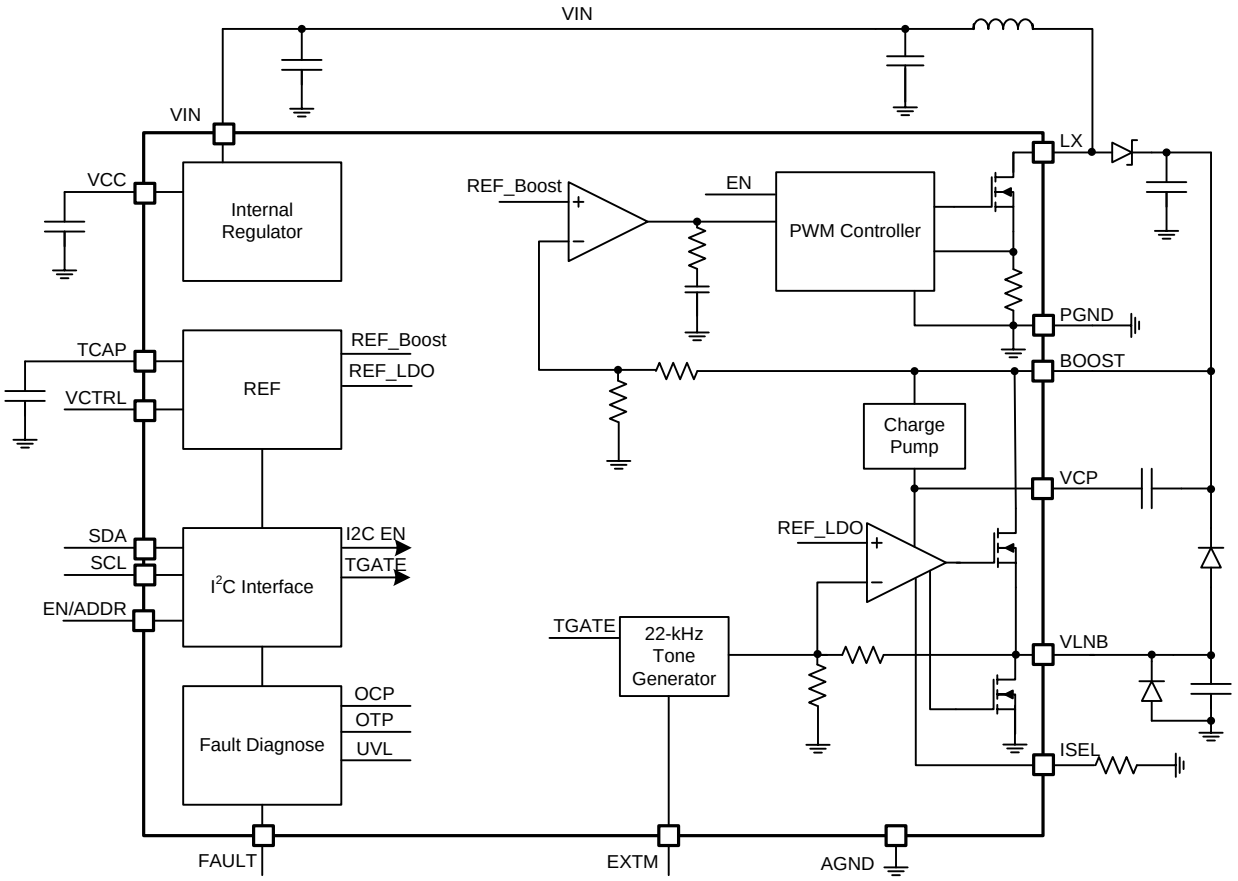
Figure 7. LNB Current Limit and Junction Temperature (ILIM = 650 mA)

7 Detailed Description

7.1 Overview

The TPS65233-1 is a power management IC that integrates a boost converter, a LDO, and a 22-kHz tone generator that serves as a LNB power supply. This solution compiles the DiSEqC 1.x standard with or without I^2C interface. Output current can be precisely programmed by an external resistor. There are five ways to generate the 22-kHz tone signal with or without I^2C. Integrated boost features low R_{dson} MOSFET and internal compensation. A fixed 1-MHz switching frequency is designed to reduce components size.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Boost Converter

The TPS65233-1 consists of an internal compensated boost converter and linear regulator. The boost converter tracks the output LNB voltage to within 800 mV even at loading 950 mA, to minimize power dissipation. Under conditions where the input voltage, VBOOST, is greater than the output voltage, VLNB, the linear regulator must drop the differential voltage. When operating in these conditions, taken care to ensure that the safe operating temperature range of the TPS65233-1 is not exceeded. The boost converter operates at 1 MHz typical. The TPS65233-1 has internal pulse-by-pulse current limiting on the boost converter and DC current limiting on the LNB output to protect the IC against short circuits. When the LNB output is shorted, the LNB output current is limited. The current limit is set by the external resistor. And the IC will be shut down if the overcurrent condition lasts for more than 4 ms, the converter enters hiccup mode and will retry startup in 128 ms. At extremely light loads, the boost converter operates in a pulse-skipping mode.

Feature Description (continued)

If two or more set top box LNB outputs are connected together, one output voltage could be set higher than others. The output with lower set voltage would be effectively turned off. Once the voltage drops to the set level, the LNB output with lower set output voltage will return to normal conditions.

7.3.2 Linear Regulator and Current Limit

The linear regulator is used to generate the 22-kHz tone signal by changing the reference voltage. The linear regulator features low drop out voltage to minimize power loss while keeping enough head room for the 0.68-V, 22-kHz tone. It also implements a tight current limit for over current protection. The current limit is set by an external resistor connected to the ISEL pin. The curve below shows the relationship between the current limit threshold and the resistor value.

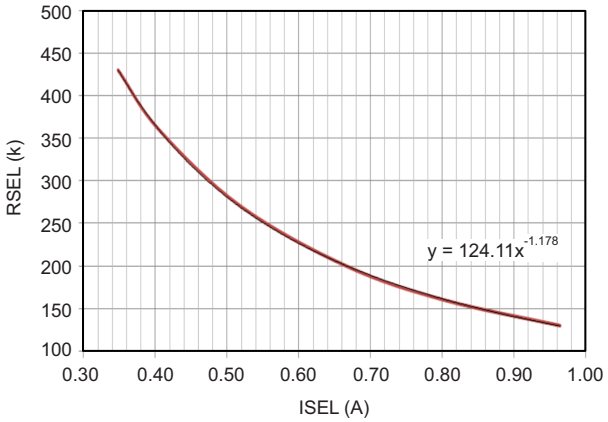


Figure 8. Linear Regulator Current Limit vs Resistor

$$R_{SEL}(k\Omega) = 124.11 \times I_{SEL}{}^{-1.178}(A) \quad (1)$$

A 280-kΩ resistor sets the current to 0.5 A. The current limit can also be set by I^2C through a register.

7.3.3 Charge Pump

The charge pump circuitry generates a voltage to drive the NMOS of the linear regulator. One end the charge pump capacitor is connected to the output of the boost converter. The voltage on the charge pump capacitor is about 6.25 V.

7.3.4 Slew Rate Control

When LNB output voltage transits from 13 V to 18 V or vice versa, the capacitor at pin TCAP controls the transition time. This transition is to make sure the boost converter can follow the voltage change. Usually boost converter has low bandwidth and can't response fast. The voltage at TCAP acts as the reference voltage of the linear regulator. The boost converter's reference is also based on TCAP with additional fixed voltage to generate 0.8 V above the output.

The charging and discharging current is 10 µA, thus the transition time can be calculated as:

$$T_{cad}(ms) = 0.5 \times \frac{C_{ss}(nF)}{I_{ss}(\mu A)} \quad (2)$$

A 22-nF capacitor generates a 1.1-ms transition time.

In light load conditions, when LNB output voltage is set from 18 to 13 V, the voltage might drops very slow, which might cause wrong logic detection at LNB side. The TPS65233-1 has an integrated pull down circuit to pull down the output during the transition. This ensures the voltage change can follow the voltage at TCAP. Meanwhile, when the 22-kHz tone signal is superimposing on the LNB output voltage, the pull down current can also provide a square wave instead of distorted waveforms, which could cause another detection problem.

Feature Description (continued)

7.3.5 Short Circuit Protection, Hiccup, and Overtemperature Protection

The LNB output limit can be set by an external resistor. When short circuit conditions occur, the output current is clamped at the current limit for 4 ms. If the condition remains, the converter will shut down for 128 ms and then try restart. This hiccup behavior prevents the IC from overheating.

The low side MOSFET of the boost converter has a current limit threshold at 3.2 A, which serves as secondary protection. If the boost converter's peak current limit is triggered, the peak current will clamp at 3.2 A. If loading current continues to increase, output voltage starts to drop and output power drops.

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 160°C, the output shuts down. When the temperature drops below its lower threshold, typically 140°C, the output is enabled.

When the chip is in over current protection or thermal shutdown, the I^2C interface and some logic are still active. The Fault pin is pulled down to signal the processor. The Fault pin signal will remain low unless the following actions are taken:

1. If I^2C interface is not used to control, Enable pin must be recycled in order to pull Fault pin back to high.
2. If I^2C interface is used, the I^2C master needs to read the OCP or OTP bit in the register, then the Fault pin returns to high.

7.4 Device Functional Modes

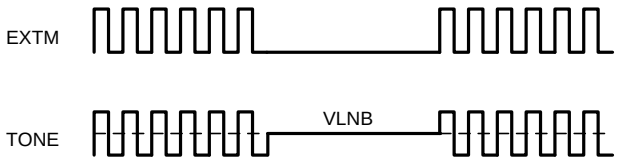
7.4.1 Tone Generation

A 22-kHz tone signal is superimposed at the LNB output voltage as a carrier for DiSEqC command. This tone signal can be generated by feeding an external 22-kHz clock at the EXTM pin. It can also be generated with its internal tone generator gated by control logic. The output stage of the regulator facilitates a push-pull circuit, so even at zero loading the 22-kHz tone at the output is still clear of distortion.

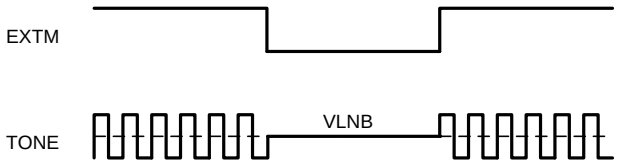
There are five ways to generate the 22-kHz tone signal at the output.

In non-I^2C mode, only option 1 and option 2 are supported in TPS65233-1. EXTM can be tone envelope or 22 kHz burst pulse as shown in Figure 9. Option 3 and option 4 are designed for I^2C interface communication mode. In I^2C communication mode, TGATE bit must be written through I^2C bus. If there is no bandwidth of I^2C bus to write TGATE bit, there is a supplemental option 5 to generate 22-kHz tone, as shown in Figure 10. In option 5, bit TMODE and TGATE must be set as 1.

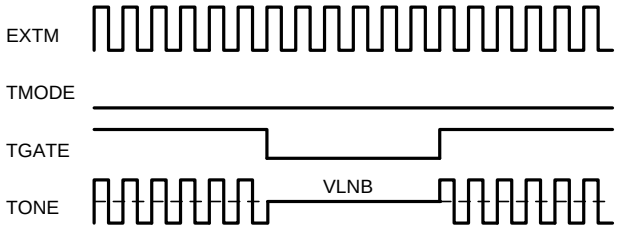
Device Functional Modes (continued)



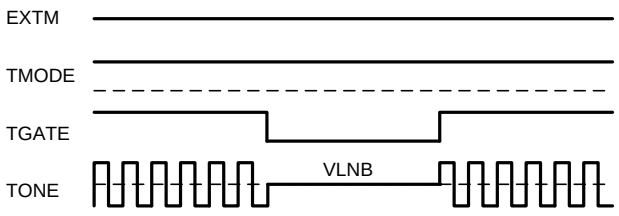
Option 1, Non-I²C Mode, bit I2C_CON = 0



Option 2, Non-I²C Mode, bit I2C_CON = 0



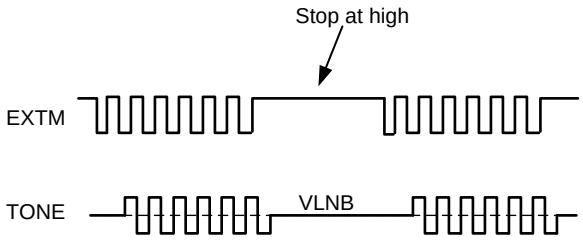
Option 3, I²C Mode, bit I2C_CON = 1 and TMODE = 0



Option 4, I²C Mode, EXTM = 0, bit I2C_CON = 1, and TMODE = 1

Figure 9. Four Ways to Generate 22-kHz Tone

Device Functional Modes (continued)



Option 5: I²C Mode, gated by EXTM, TMODE, and TGATE = 1

Figure 10. Supplemental Option for 22-kHz Tone in I²C Mode

7.4.2 Serial Interface

I²C is a 2-wire serial interface developed by Philips Semiconductor (see I²C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and transmits data on the bus under control of the master device.

The TPS65233-1 device works as a slave and supports the following data transfer modes, as defined in the I²C-Bus Specification: standard mode (100 kbps), and fast mode (400 kbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as supply voltage remains above 4.5 V (typical).

The data transfer protocol for standard and fast modes is exactly the same; therefore, they are referred to as F/S-mode in this document. The TPS65233-1 device supports 7-bit addressing; 10-bit addressing and general call address are not supported.

The TPS65233-1 device has a 7-bit address with the 2 LSB bits set by EN pin. Connecting EN to ground set the address 0x60H, connecting to high set the address 0x61H.

Table 1. I²C Address Selection

EN/ADDR PIN	I²C ADDRESS	ADDRESS FORMAT (A6...A0)
Connect to ground	0x60H	110 0000
Connect to high	0x61H	110 0001

7.5 Programming

7.5.1 I²C Update Sequence

The TPS65233-1 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single update. After the receipt of each byte, the TPS65233-1 device acknowledges by pulling the SDA line low during the high period of a single clock pulse. The TPS65233-1 performs an update on the falling edge of the LSB byte.

When the TPS65233-1 is disabled (EN pin tied to ground) the device can still be updated via the I²C interface.

Figure 11. I²C Write Data Format

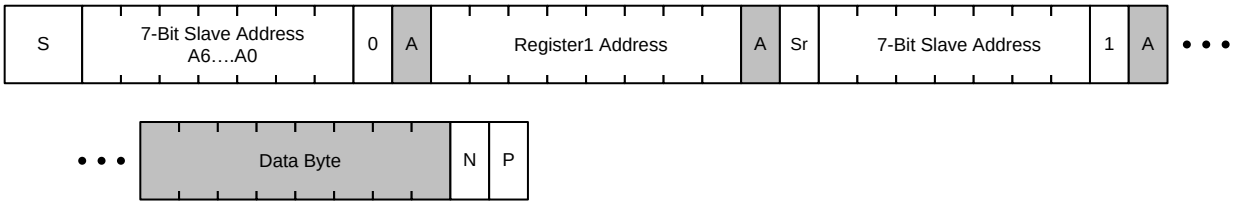


Figure 12. I²C Read Data Format

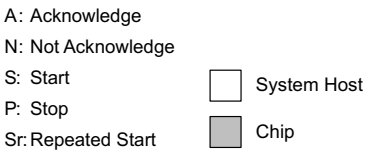


Figure 13. Legend

7.6 Register Map

The registers are listed in Table 2 and described in the following sections.

Table 2. Register Map

REGISTER / ADDRESS	7	6	5	4	3	2	1	0
Control Register 1 Address: 0x00H	I2C_CON	Reserved	TGATE	TMODE	EN	VSEL2	VSEL1	VSEL0
Control Register 2 Address: 0x01H	—	—	—	TONE_ POS1	TONE_ POS0	CL1	CL0	CL_EXT
Status Register 1 Address: 0x02H	—	T125	LDO_ON	Reserved	TSD	OCP	CABLE_ GOOD	VOUT_ GOOD

7.6.1 Control Register 1 - Address: 0x00H

Table 3. Control Register 1 - Address: 0x00H

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	I2C_CON	R/W	0	1: I^2C control enabled; 0: I^2C control disabled
6	Reserved	R/W	0	Reserved
5	TGATE	R/W	0	Tone Gate. Allows either the internal or external 22-kHz tone signals to be gated. 1: Tone Gate on use; 0: Tone gate off
4	TMODE	R/W	0	Tone mode. Select between the use of an external 22-kHz or internal 22-kHz signal. 1: internal; 0: external
3	EN	R/W	1	LNB output voltage Enable 1: output enabled; 0: output disabled
2	VSEL2	R/W	0	See Table 4 for output voltage selection
1	VSEL1	R/W	0	
0	VSEL0	R/W	0	

Table 4. Voltage Selection Bits

VSEL2	VSEL1	VSEL0	LNB(V)
0	0	0	13
0	0	1	13.4
0	1	0	13.8
0	1	1	14.2
1	0	0	18
1	0	1	18.6
1	1	0	19.2
1	1	1	19.8

7.6.2 Control Register 2 - Address: 0x01H

Table 5. Control Register 2 - Address: 0x01H

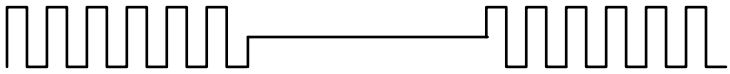
BIT	FIELD	TYPE	RESET	DESCRIPTION
7	—	R/W	—	—
6	—	R/W	—	—
5	—	R/W	—	—

Table 5. Control Register 2 - Address: 0x01H (continued)

BIT	FIELD	TYPE	RESET	DESCRIPTION
4	TONE_POS1	R/W	0	00: tone above Vout; 01: tone in the middle of Vout; 10: tone below Vout
3	TONE_POS0	R/W	1	
2	CL1	R/W	0	Current limit set bits
1	CL0	R/W	0	
0	CL_EXT	R/W	1	1: current limit set by external resistor; 0: current limit set by register

Some tone detection circuits in LNB are sensitive to the position of the tone on the output voltage. The TPS65233-1 provides options to select the position by setting the TONE_POS1 and TONE_POS0 bits, as illustrated below.

Option 1, TONE_POS1=0, TONE_POS0=0, Tone above VLNB



Option 2, TONE_POS1=0, TONE_POS0=1, Tone in the middle of VLNB

Option 2, TONE_POS1=1, TONE_POS0=0, Tone below VLNB

Figure 14. Tone Position Programmed by TONE_POS1, TONE_POS0 Bits

In addition to programming the LDO's current continuously via an external resistor, internal registers also provide options to program the current limit. There are four options that can be selected.

Table 6. Current Limit Selection Bits

CL1	CL0	CURRENT LIMIT (mA)
0	0	400
0	1	600
1	0	750
1	1	1000

7.6.3 Status Register 1 - Address: 0x02H

The TPS65233-1 has a full range of diagnostic flags for operation and debug. If any of the flags are triggered, the FAULT pin is pulled low sending an interrupt signal to processor. The processor then can read the status register to check the error conditions. The status bits are described in the following table. Among these bits, TSD and OCP are different from the others. Once TSD and OCP are set to 1, the FAULT pin logic is latched low and the processor must reset the bits in order to release the fault conditions. Other bits change as conditions change without latch.

Table 7. Status Register 1 - Address: 0x02H

BIT	FIELD	TYPE	RESET	DESCRIPTION
7	—	—	—	—
6	T125	R	0	1: if die temperature T > 125°C; 0: if die temperature T < 125°C
5	LDO_ON	R	0	1: internal LDO is turned on and boost converter is on; 0: Internal LDO is turned off but boost converter is on
4	Reserved	R	0	Reserved
3	TSD	R	0	1: thermal shutdown occurs; 0: thermal shutdown does not occur. FAULT pin pull low and latch, I^2C master need to read and release
2	OCP	R	0	Overcurrent protection. If over current conditions last for more than 48 ms. 1: Overcurrent protection triggered. 0: Overcurrent protection conditions released. FAULT pin pull low and latch, I^2C master need to read and release
1	CABLE_GOOD	R	0	Cable connection good. 1: Output current above 50 mA; 0: Output current less than 50 mA
0	VOUT_GOOD	R	0	LNB output voltage in range. 1: In range; 0: Out of range

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TPS65233-1 is a monolithic voltage regulator, specifically to provide the 13-V/18-V power supply and the 22-kHz tone signaling to the LNB down-converter, with I^2C interface. I^2C GUI software is shared with TPS65233 which is available on ti.com.

8.2 Typical Application

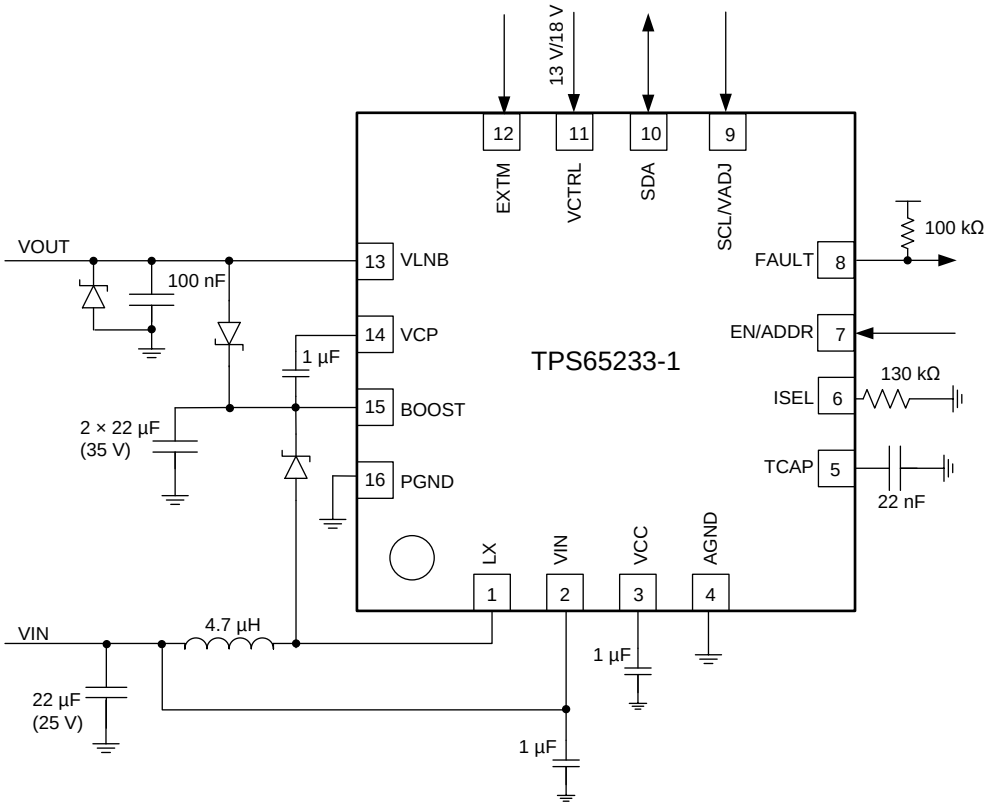


Figure 15. Application Schematic

8.2.1 Detailed Design Procedure

8.2.1.1 Capacitor Selection

In TPS65233-1, a 1-MHz non-synchronous boost converter is integrated and the boost converter features the internal compensation network. 4.7 µH and 10 µH boost inductor are recommended. TPS65233-1 works fine with both ceramic capacitor and electrolytic capacitor. The ceramic capacitors rated at least X7R, 1206 size are preferred for the lower LNB output ripple. Table 8 shows the recommended ceramic capacitors list for both 4.7 µH and 10 µH boost inductors. Minimum output capacitor at the output of the boost converter is 2 × 10-µF/25-V ceramic capacitor when 4.7-µH inductor is selected.

Boost converter is stable with both ceramic capacitor and electrolytic capacitor. If lower cost is demanded, a 100-µF electrolytic and a 1-µF/35-V ceramic capacitor work well, this solution provides lower system cost.

Table 8. Boost Inductor and Capacitor Selections

BOOST INDUCTOR	BOOST OUTPUT CAPACITOR (CERAMIC)
10 µH	2 × 22 µF, 25 V, 1206
	2 × 10 µF, 35 V, 1206
	1 × 22 µF, 35 V, 1206
	2 × 22 µF, 35 V, 1206
4.7 µH	2 × 10 µF, 25 V, 1206
	2 × 22 µF, 25 V, 1206
	1 × 22 µF, 35 V, 1206
	2 × 10 µF, 35 V, 1206
	2 × 22 µF, 35 V, 1206

8.2.2 Application Curves

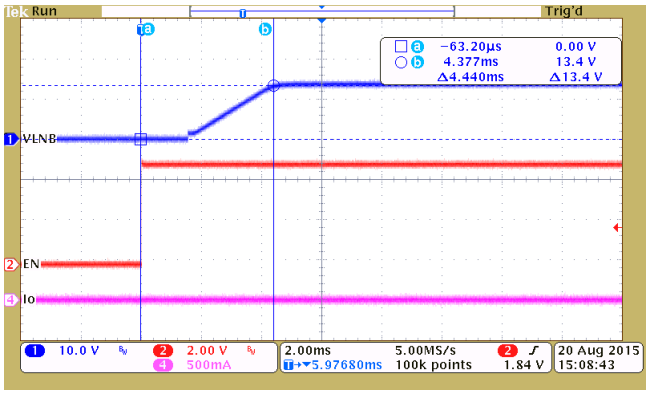


Figure 16. Soft Start, VLNB = 13.4 V, Delay from EN High to LNB Output High

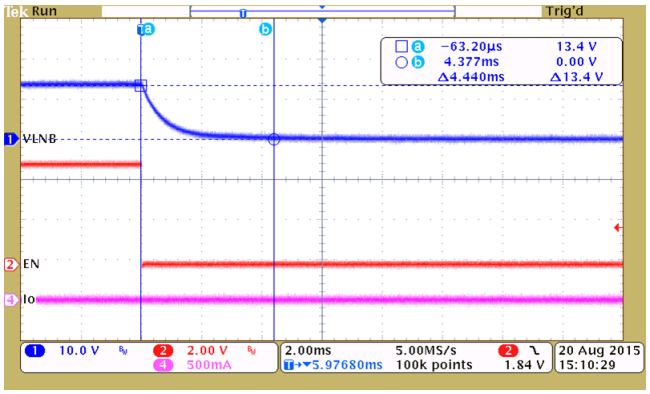


Figure 17. Power Off, VLNB = 13.4 V, Delay from EN Low to LNB Output Low

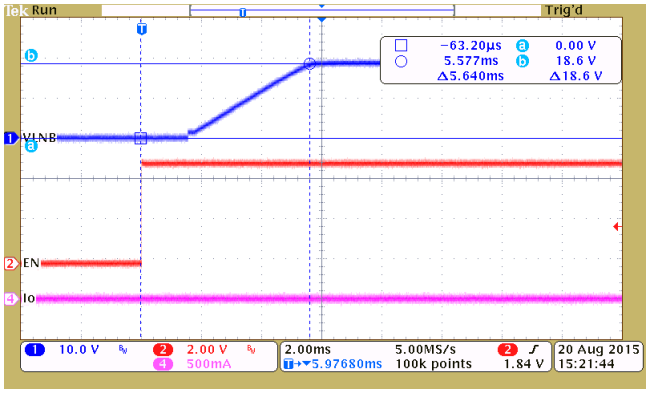


Figure 18. Soft Start, VLNB = 18.6 V, Delay from EN High to LNB Output High

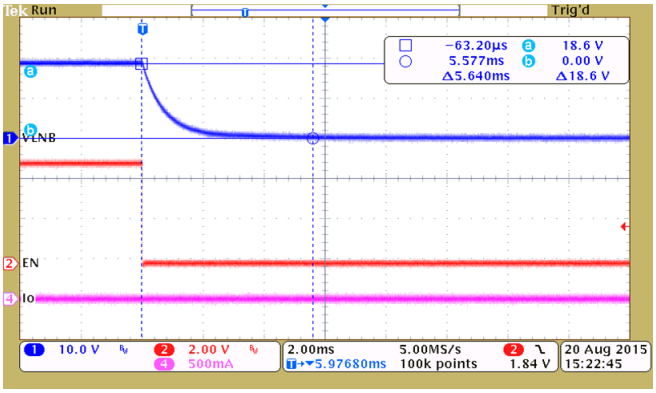


Figure 19. Power Off, VLNB = 18.6 V, Delay from EN Low to LNB Output Low

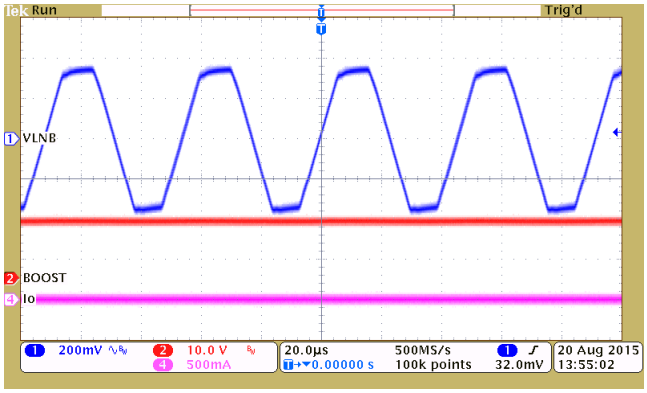


Figure 20. VLNB = 13.4 V, No Load, 22-kHz Tone

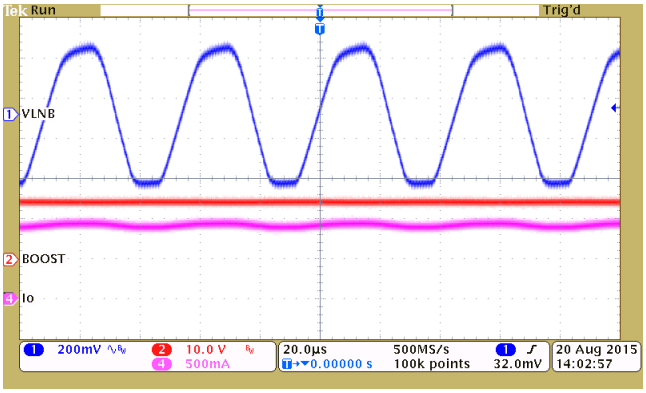


Figure 21. VLNB = 13.4 V, 950 mA, 22-kHz Tone

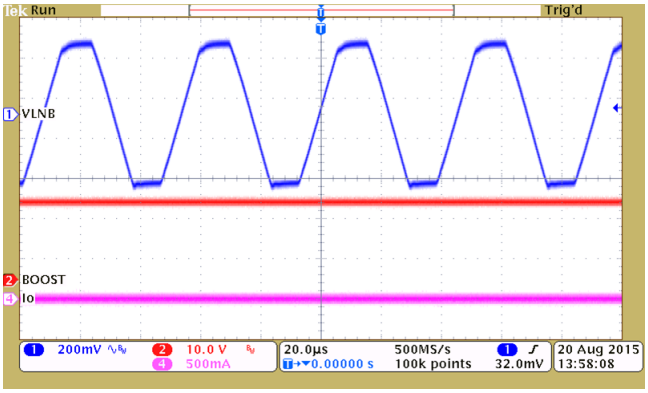


Figure 22. VLNB = 18.6 V, No Load, 22-kHz Tone

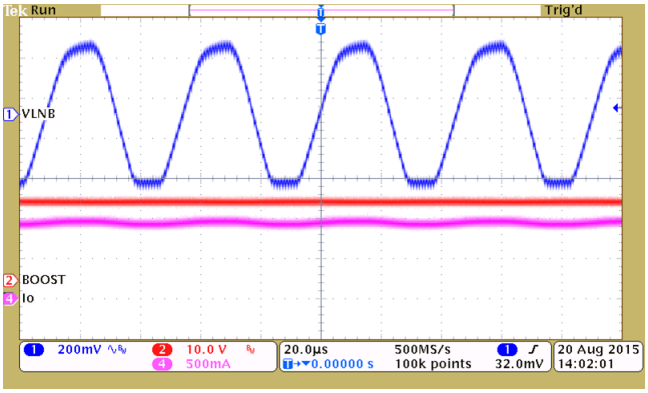


Figure 23. VLNB = 18.6 V, 950 mA, 22-kHz Tone

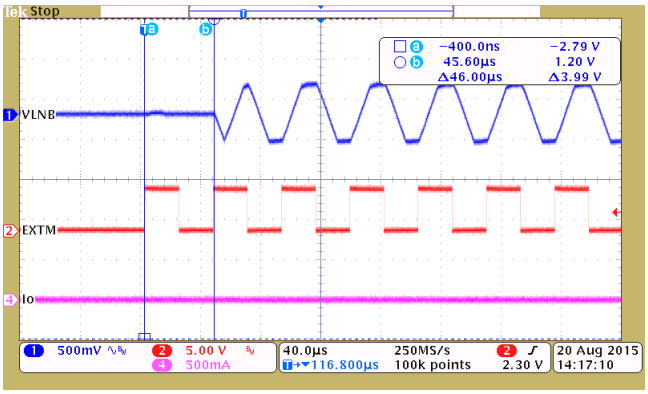


Figure 24. No Load, 22-kHz Tone Delay from EXTM Turns High to Output Tone, On

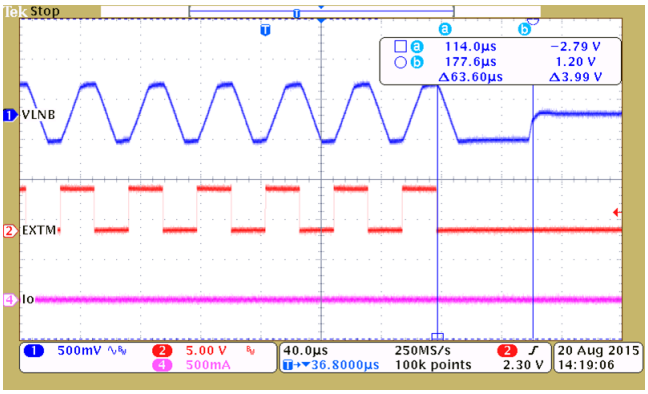


Figure 25. No Load, 22-kHz Tone Delay from EXTM Turns Low to Output Tone, Off

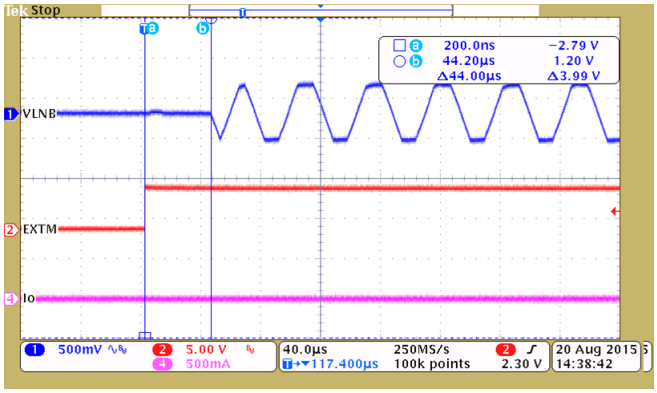


Figure 26. No Load, 22-kHz Tone Delay from EXTM Turns High to Output Tone, On

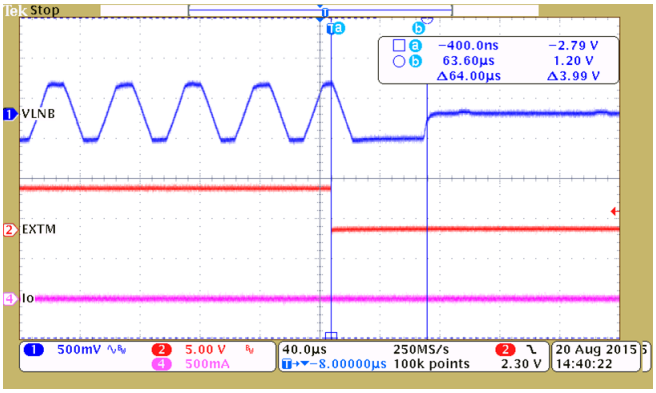


Figure 27. No Load, 22-kHz Tone Delay from EXTM Turns Low to Output Tone, Off

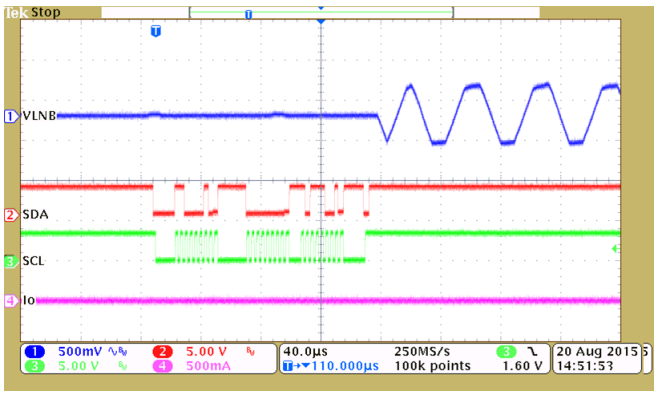


Figure 28. No Load, 22-kHz Tone Delay from I²C SDA to Output Tone, On

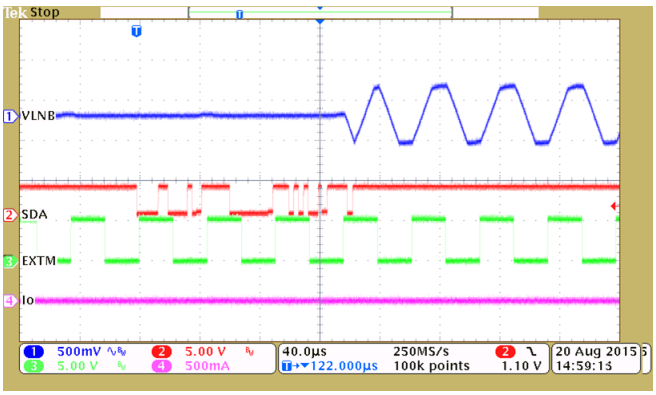


Figure 29. No Load, 22-kHz Tone Delay from I²C Gated, EXTM Provides 22 kHz to Output Tone, On

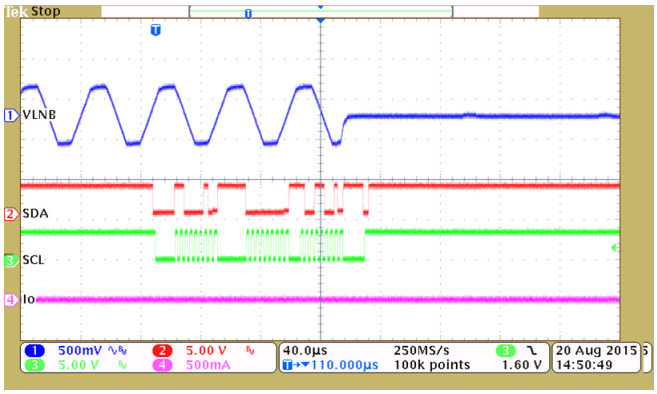


Figure 30. No Load, 22-kHz Tone Delay from I²C SDA to Output Tone, Off

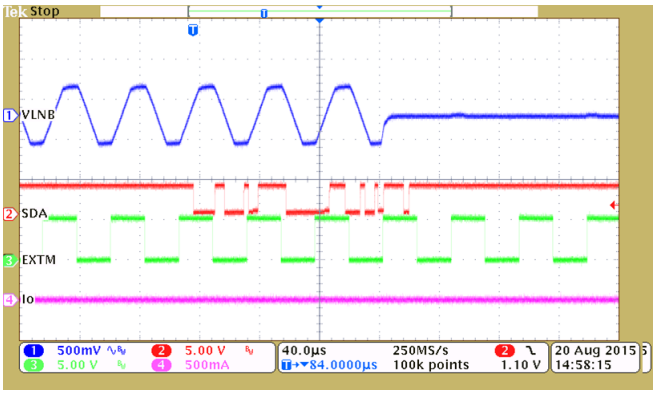


Figure 31. No Load, 22-kHz Tone Delay from I²C Gated, EXTM Provides 22 kHz to Output Tone, Off

9 Power Supply Recommendations

The devices are designed to operate from an input supply ranging from 4.5 V to 20 V. The input supply should be well regulated. If the input supply is located more than a few inches from the converter an additional bulk capacitance typically 100 µF may be required in addition to the ceramic bypass capacitors.

10 Layout

10.1 Layout Guidelines

The TPS65233-1 is designed to layout in a 2-layer PCB. Figure 32 shows the recommended layout practice. It is critical to make sure the GND of the input capacitor, output capacitor, and boost converter are connected at one point on the same layer as shown below. PGND and AGND are in different regions and are connected to the thermal pad. Other components are connected to AGND.

10.2 Layout Example

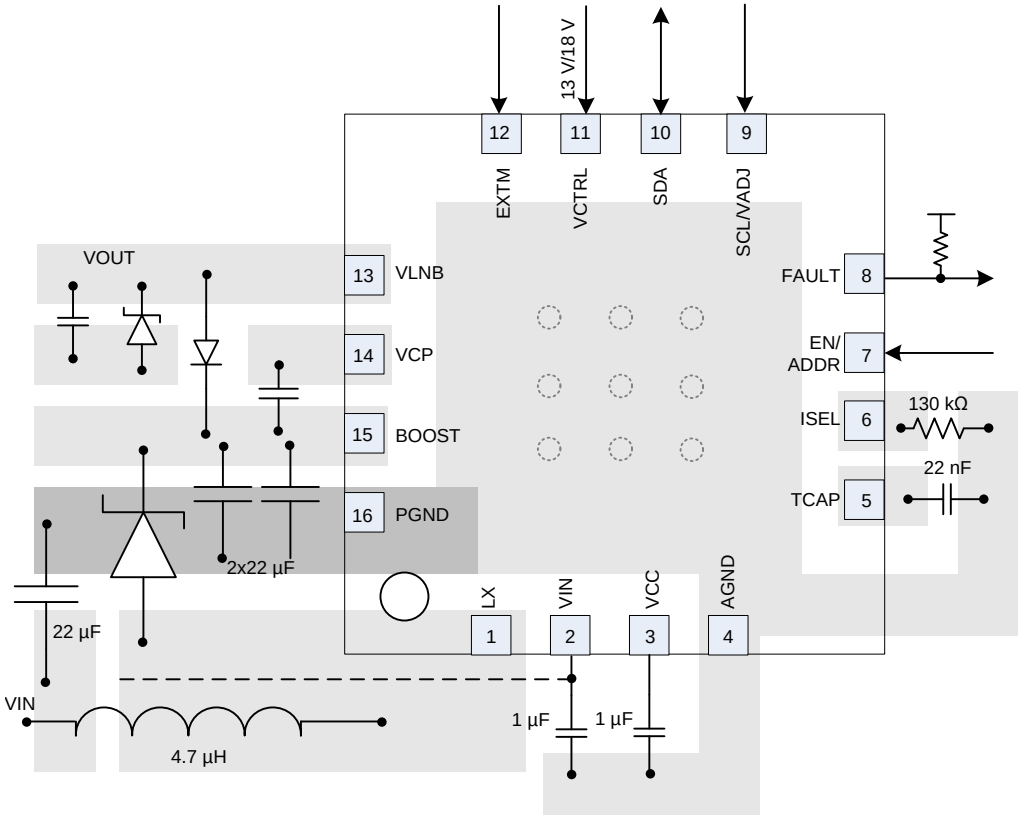


Figure 32. 2-Layer PCB Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65233-1RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	652331	Samples
TPS65233-1RTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	652331	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

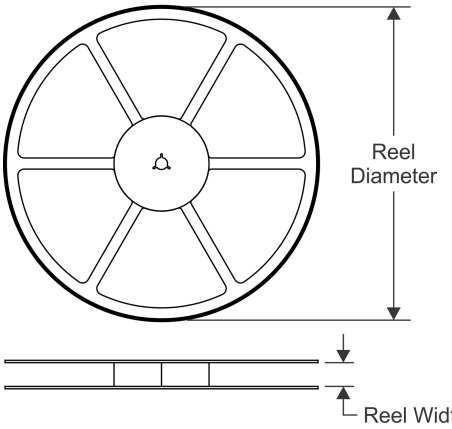
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

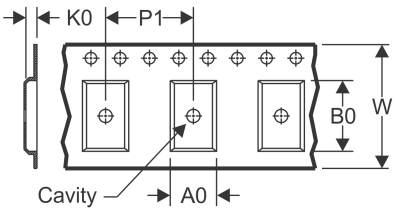
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

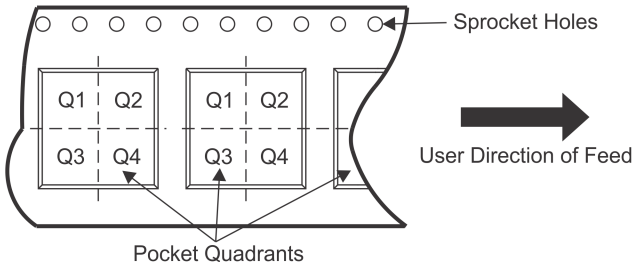


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

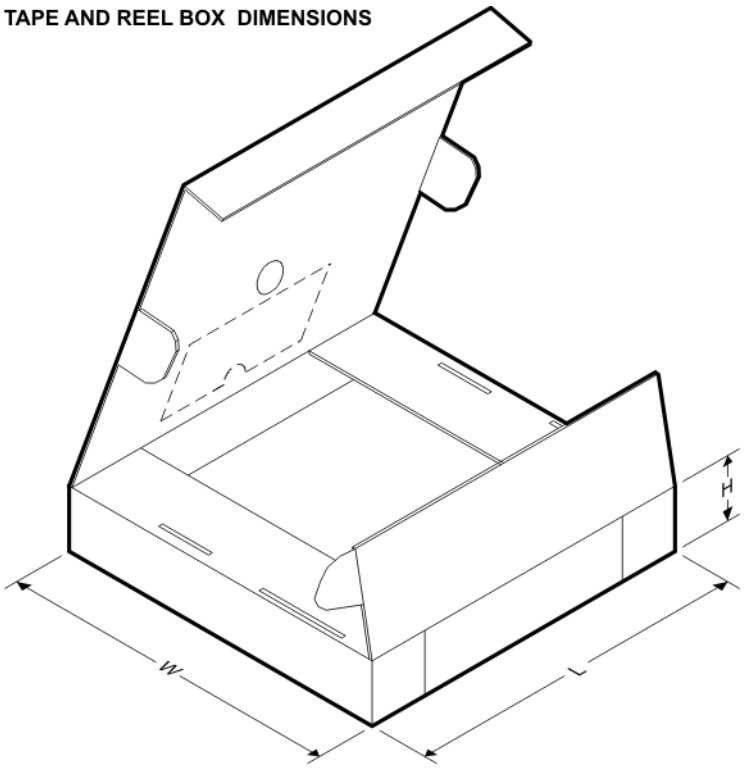
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65233-1RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS65233-1RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

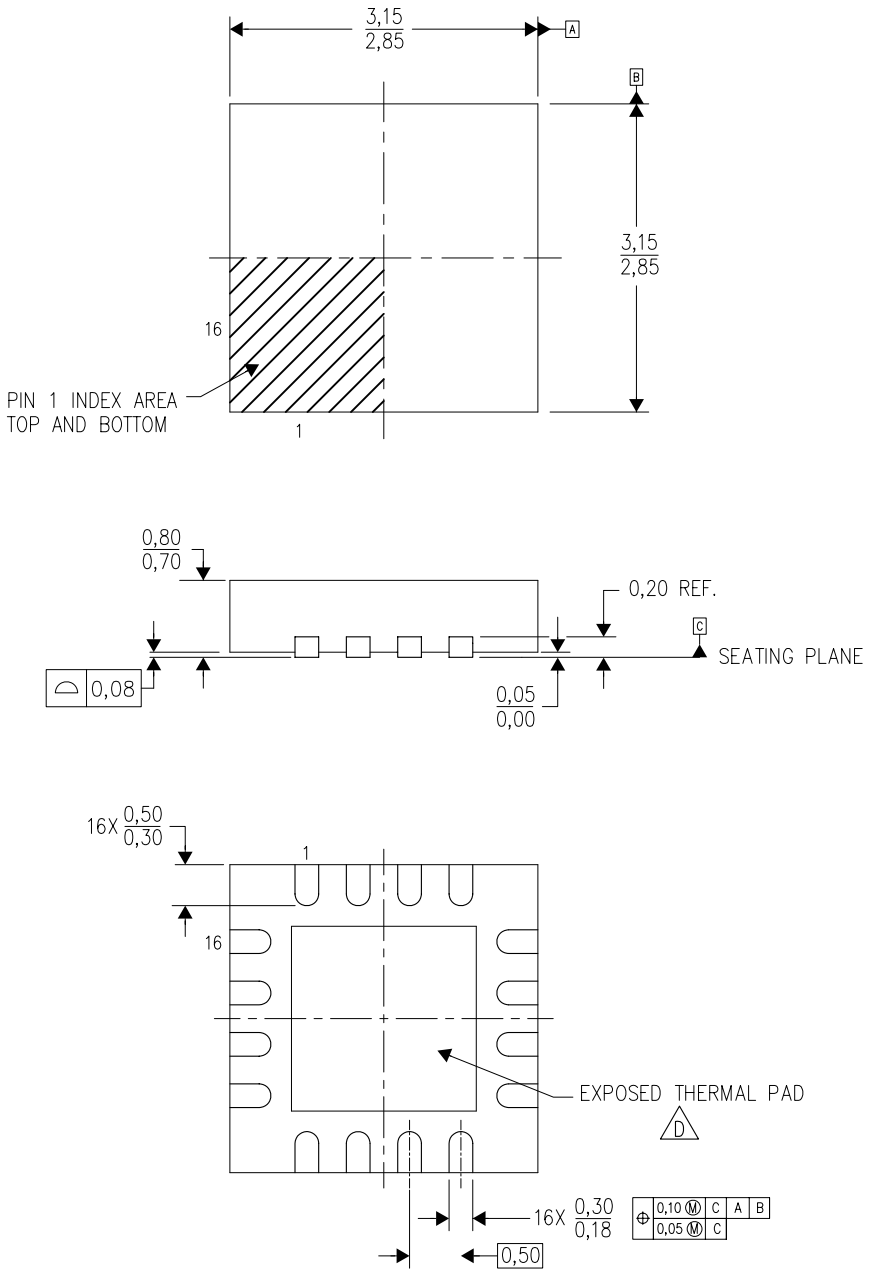
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65233-1RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS65233-1RTET	WQFN	RTE	16	250	210.0	185.0	35.0

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



4205254/D 01/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

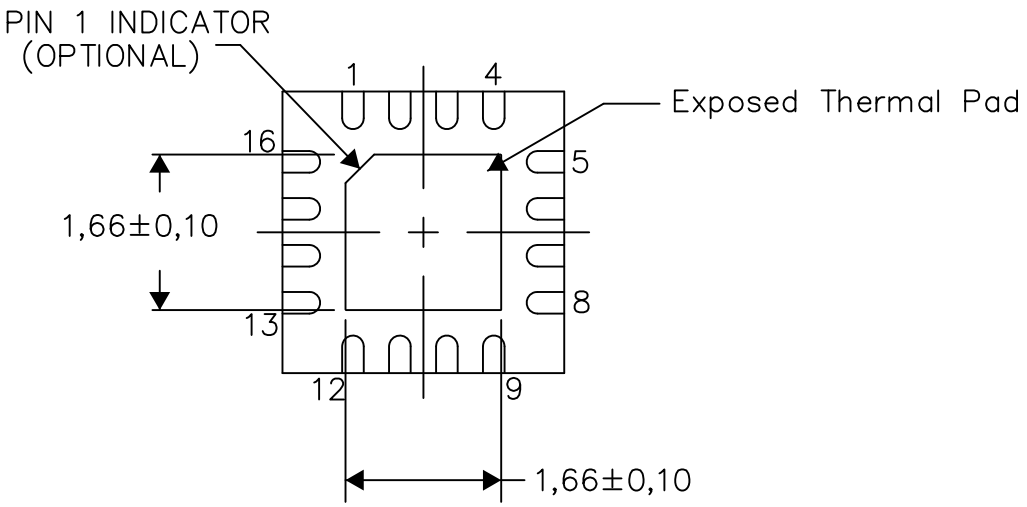
RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



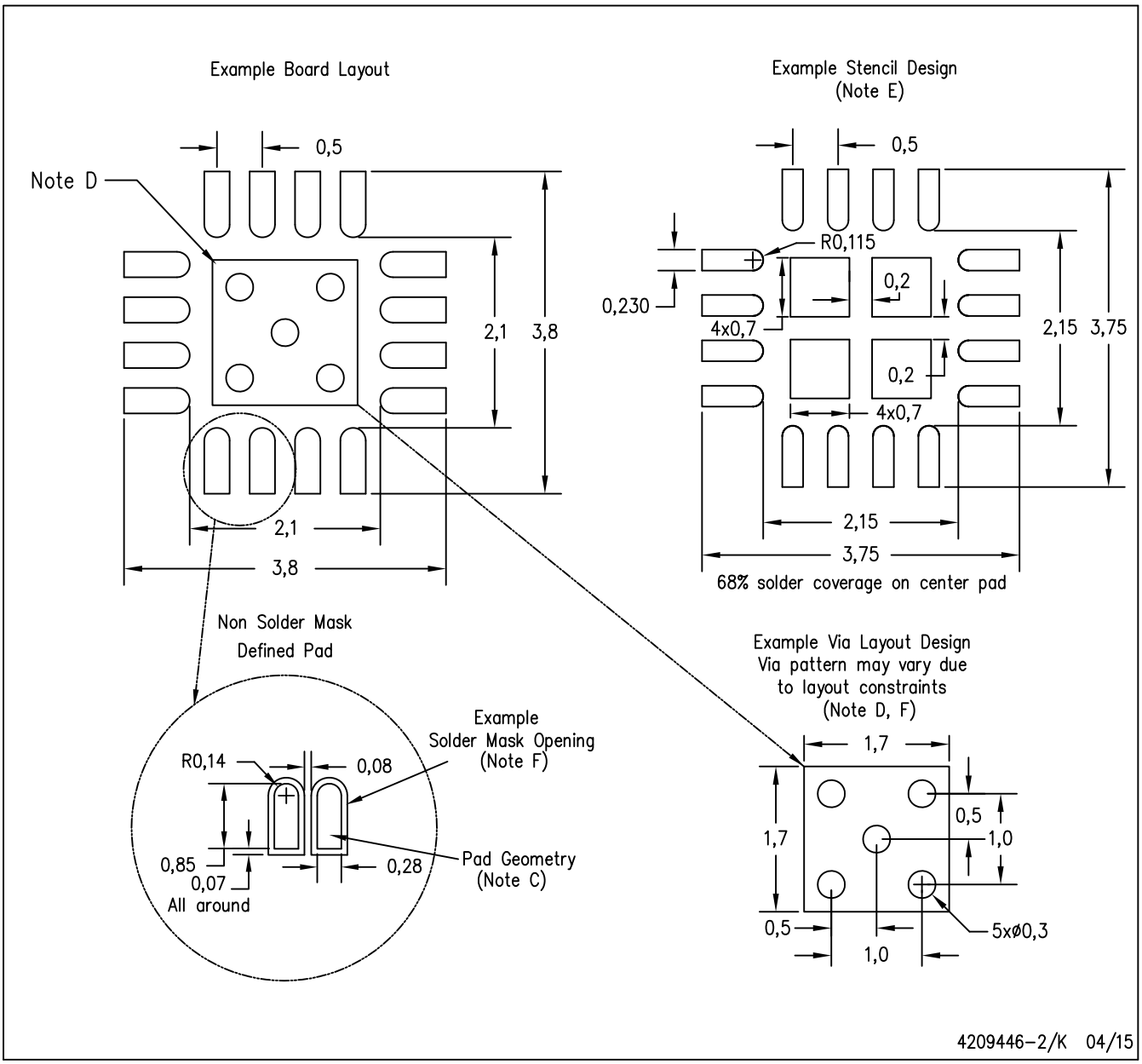
Bottom View

Exposed Thermal Pad Dimensions

4206446–8/U 08/15

NOTE: A. All linear dimensions are in millimeters

RTE (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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