

Automotive LED Driver Series

50 V 1.5 A 1ch LED Driver for 2 Wheeler Turn Indicator

BD18327EFV-M

General Description

BD18327EFV-M is 50 V-withstanding 1.5 A 1ch LED Driver for 2 Wheeler Turn Indicator. It has built-in CR Timer for LED blinking control. The IC provides high reliability because it has LED open detection, short circuit protection, over voltage protection. In case of LED open detection, output blinking rate is doubled. Under high input voltage condition, output PWM ON Duty reduces to control heat dissipation across the IC and protect the LED load.

Features

- AEC-Q100 Qualified^(Note 1)
- Functional Safety Supportive Automotive Products
- Flasher SW Resistance Detection
- Power Saving Mode
- Built-in CR Timer
- LED Open Detection
- Disable LED Open Detection Function at Reduced-voltage
- Short Circuit Protection (SCP)
- Over Voltage Protection (OVP)
- Output PWM ON Duty Control during High Input Voltage

(Note 1) Grade1

Applications

- 2 Wheeler Turn Indicator

Key Specifications

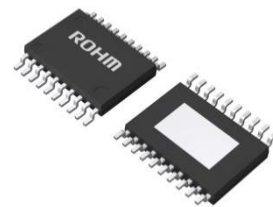
- Input Voltage Range: 6.0 V to 18.0 V
- OUT Pin Maximum Output Current: 1.5 A
- OUT Pin ON Resistance for High Mode: 0.8 Ω (Max)
- Circuit Current at Power Saving Mode: 100 μ A (Max)
- CR Timer Frequency Range: 150 Hz to 1 kHz
- Operating Temperature Range: -40 $^{\circ}$ C to 125 $^{\circ}$ C

Package

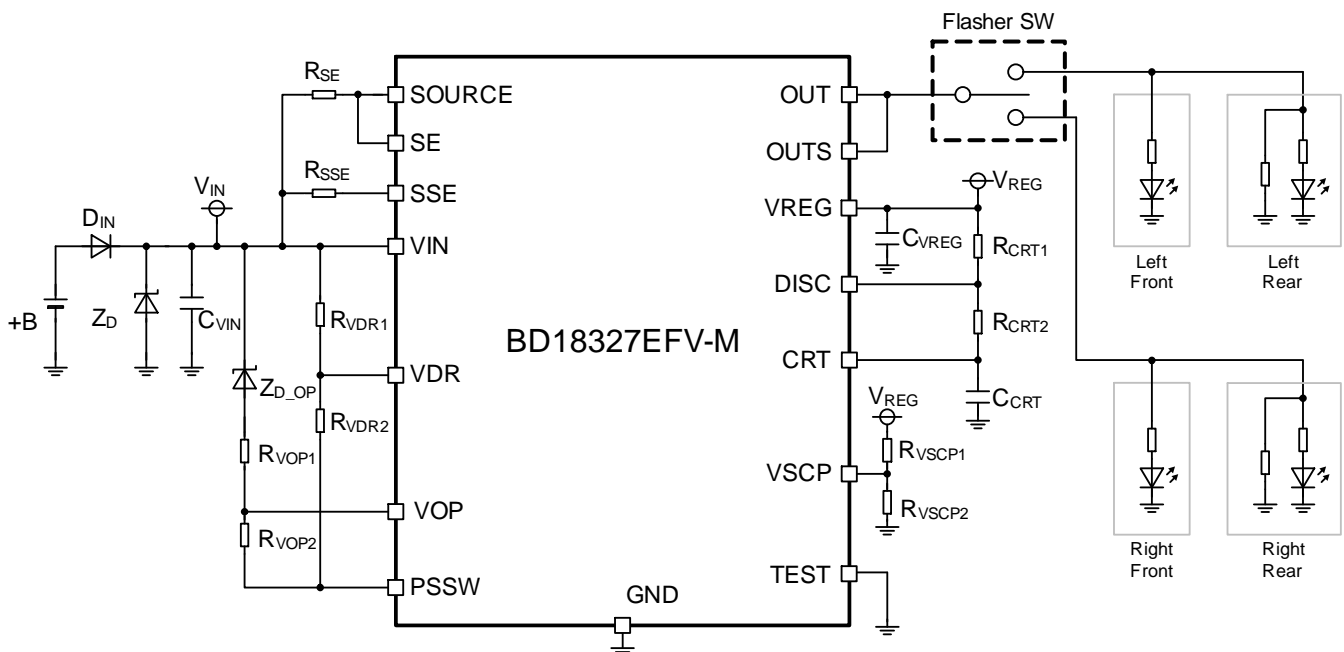
HTSSOP-B20

W (Typ) x D (Typ) x H (Max)

6.5 mm x 6.4 mm x 1.0 mm

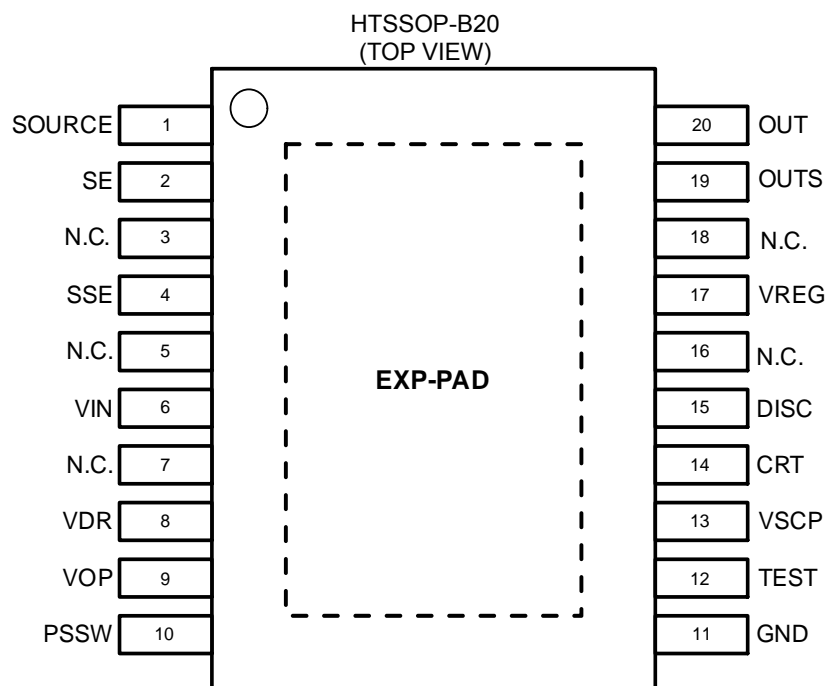


Typical Application Circuit



○Product structure : Silicon integrated circuit ○This product has no designed protection against radioactive rays.

Pin Configuration

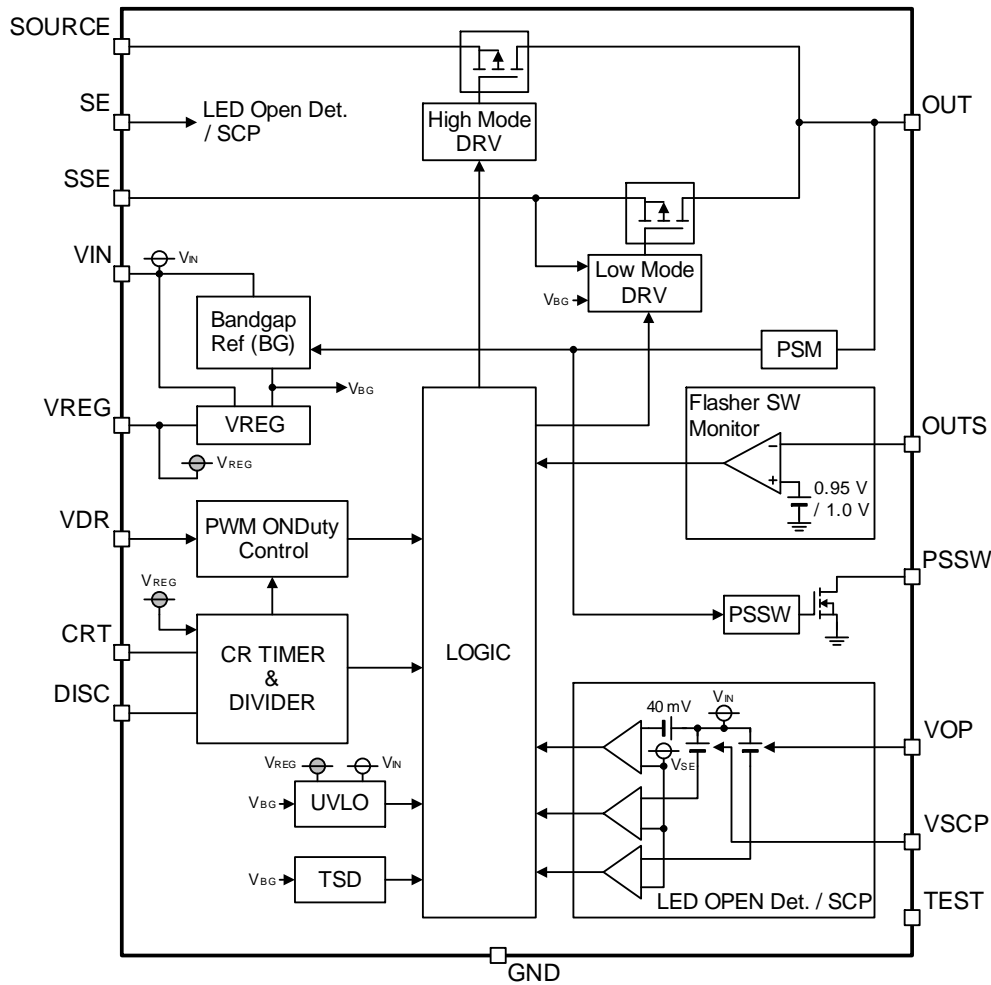


Pin Description

| Pin No. | Pin Name | Function |
|---------|----------|--------------------------------------------|
| 1 | SOURCE | Power PMOS source pin |
| 2 | SE | Output current sense input pin |
| 3 | N.C. | No internal connection ^(Note 1) |
| 4 | SSE | Output current sense input in Low Mode |
| 5 | N.C. | No internal connection ^(Note 1) |
| 6 | VIN | Power supply input |
| 7 | N.C. | No internal connection ^(Note 1) |
| 8 | VDR | PWM ON Duty setting |
| 9 | VOP | Open detection threshold setting pin |
| 10 | PSSW | Programmable ground pin |
| 11 | GND | GND |
| 12 | TEST | The test pin connects to GND |
| 13 | VSCP | Short detection threshold setting pin |
| 14 | CRT | CR timer setting1 |
| 15 | DISC | CR timer setting2 |
| 16 | N.C. | No internal connection ^(Note 1) |
| 17 | VREG | Regulated voltage pin |
| 18 | N.C. | No internal connection ^(Note 1) |
| 19 | OUTS | Output sense pin |
| 20 | OUT | Output pin |
| - | EXP-PAD | The EXP-PAD connect to GND. |

(Note 1) Leave this pin unconnected.

Block Diagram



Description of Blocks

(Unless otherwise specified, Ta = 25 °C, V_{IN} = 13 V, and numbers are “Typical” values.)

1 Operation mode description

1.1 Power Saving Mode (PS Mode)

After power on, the IC starts up in power saving mode. The current consumption of the IC is limited to 100 µA or less, and it is possible to reduce the power consumption when the Flasher SW is off. In the PS mode, the MOSFET built into the PSSW pin can be turned off to shut off the current flowing to the external resistor. When the Power Saving Mode is released, the IC monitors the VIN pin voltage, and when the UVLO VIN Release Voltage (5.0 V (Typ)) is exceeded, the IC shifts to Flasher SW Monitor Mode. The release condition for the power saving mode is expressed by the following equation.

$$I_{OUT_PSM} \times R_{PSM} \times > V_{PSM_REL}$$

and

$$V_{IN} > V_{UVLOR}$$

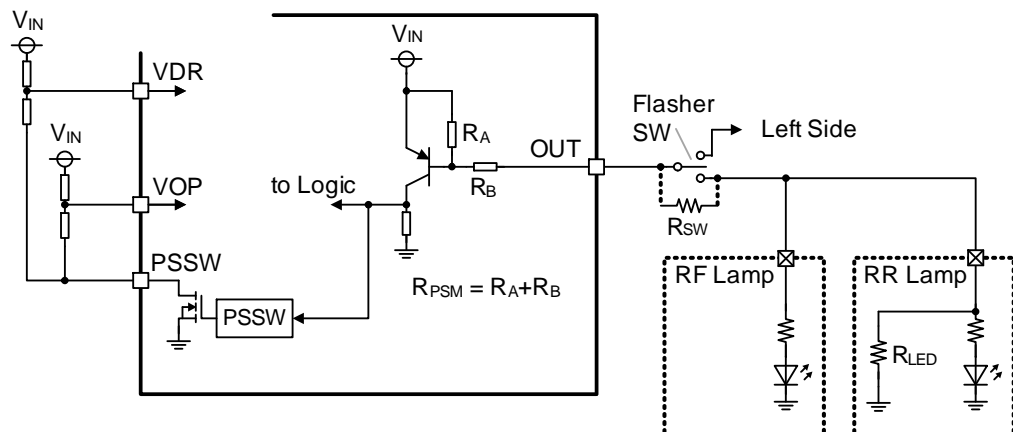
$$I_{OUT_PSM} = \frac{V_{IN}}{R_{PSM} + R_{SW} + R_{LED}}$$

where:

| | |
|----------------|-----------------------------------------------|
| I_{OUT_PSM} | is the OUT pin current in Power Saving Mode. |
| R_{PSM} | is the Power Saving Mode Internal Resistance. |
| V_{PSM_REL} | is the Power Saving Mode Release Threshold. |
| V_{IN} | is the VIN pin voltage. |
| V_{UVLOR} | is the UVLO VIN Release Voltage. |
| R_{LED} | is the LED board resistance. |
| R_{SW} | is the Flasher SW resistance. |

Solving above equation for R_{SW}

$$R_{SW} < R_{PSM} \times \frac{V_{IN}}{V_{PSM_REL}} - R_{PSM} - R_{LED}$$



1 Operation mode description – continued

1.2 Flasher SW Monitor Mode

When PS Mode is released, the IC shifts to Flasher SW Monitor Mode. When the IC shifts to Flasher SW monitor mode, the constant current source for SW resistance monitoring turns on and monitoring of the OUTS pin voltage starts. The constant current source turns ON only in the ON Duty section set by CR timer, and the judgment of the SW monitor also becomes only in this section. After switching from PS mode, if the OUTS pin voltage is V_{OUTS_ON} (0.95 V (Typ)) or more within 8 CLK cycle, the IC returns to PS mode again.

Condition for IC to go from Flasher SW Monitor Mode to Blinking High Mode:

After switching from PS mode, if the OUTS pin voltage falls below V_{OUTS_ON} (0.95 V (Typ)) within 8 CLK cycles, the IC shifts to the blinking High mode. The Blinking High Mode transition conditions are as follows.

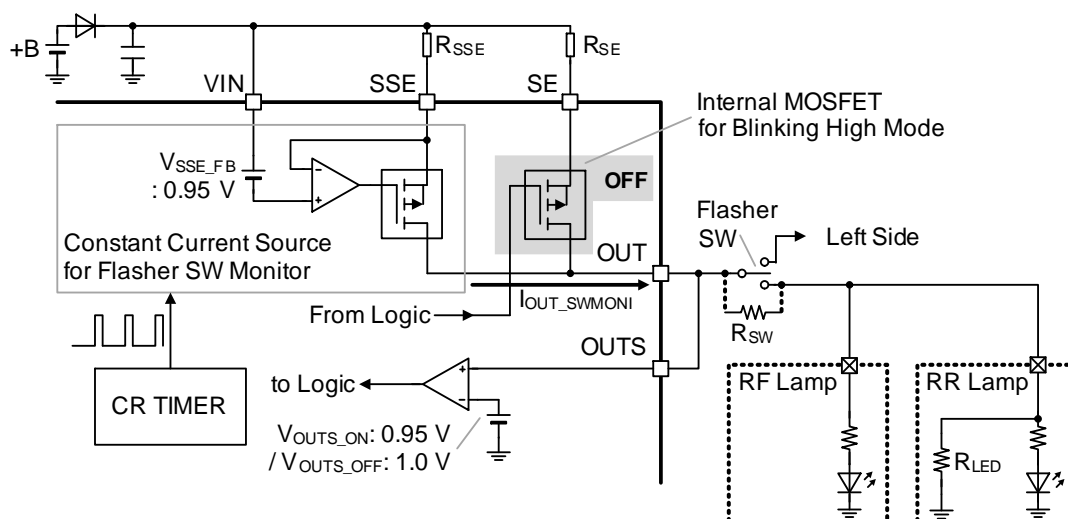
$$V_{OUTS} = I_{OUT\ SWMONI} \times (R_{SW} + R_{LED}) < V_{OUTS\ ON}$$

$$I_{OUT_SWMONI} = \frac{V_{SSE_FB}}{R_{SSE}}$$

$$\frac{(R_{SW}+R_{LED})}{R_{SSE}} < K_{BLON}$$

where:

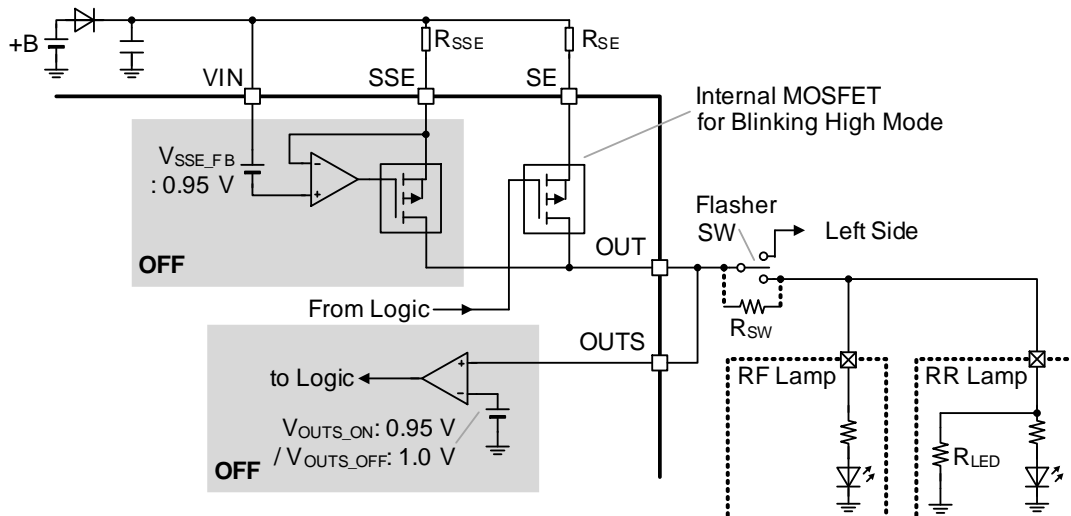
| | |
|-------------------|------------------------------------------------------------------------------------|
| V_{OUTS} | is the OUTS pin voltage. |
| I_{OUT_SWMONI} | is the OUT pin current in Flasher SW Monitor Mode. |
| V_{SSE_FB} | is the SSE pin Feedback Voltage. |
| R_{SSE} | is the Constant Current Setting Resistor. |
| R_{SW} | is the Flasher SW resistance. |
| R_{LED} | is the LED board resistance. |
| V_{OUTS_ON} | is the Blinking ON Threshold Voltage. |
| K_{RLON} | is the Blinking ON Threshold Constant. ($K_{BLON} = V_{OUTS_ON} / V_{SSE_FB}$) |



1 Operation mode description – continued

1.3 Blinking High Mode

The Blinking High mode continues for 256 CLK cycles. During Blinking High Mode, the constant current source for Flasher SW monitoring and the comparator built into the OUTS Pin turn off. During this period, the IC performs LED Open Detection, SW Open Detection and Short Circuit Protection. After 256 CLK cycles, the IC shifts to Blinking Low Mode.



1.4 Blinking Low Mode

When the IC enters Blinking Low Mode, the internal counter starts counting. After 256 CLK cycles, the IC shifts to Blinking High Mode. If the OUTS pin voltage reaches V_{OUTS_OFF} (1.0 V (Typ)) or more before 256 CLK cycles elapse, the IC returns to Flasher SW Resistance Monitor Mode again. The Flasher Switch Monitor Mode transition conditions are as follows.

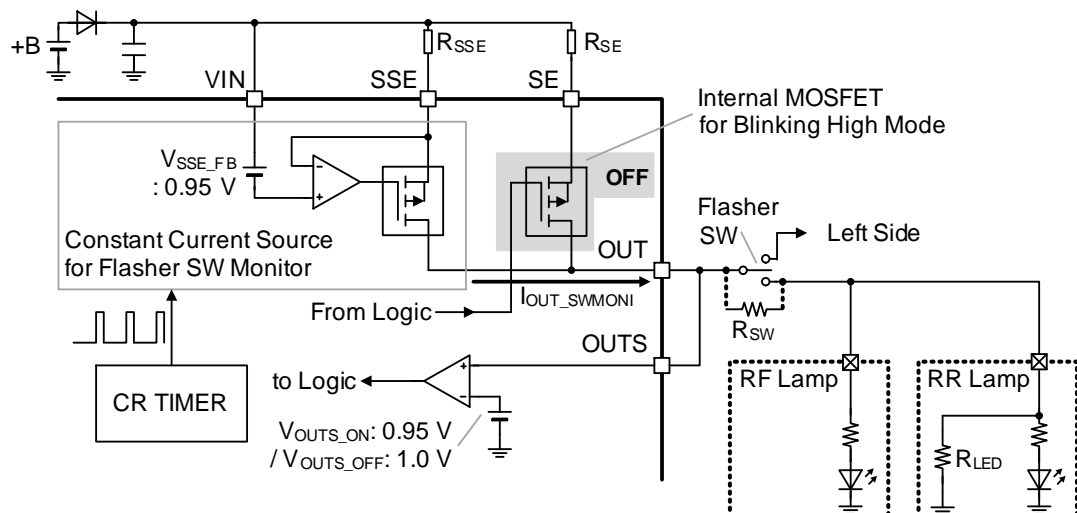
$$V_{OUTS} > V_{OUTS_OFF}$$

$$\frac{(R_{SW} + R_{LED})}{R_{SSE}} > K_{BLOFF}$$

where:

V_{OUTS_OFF} is the Blinking OFF Threshold Voltage.

K_{BLOFF} is the Blinking OFF Threshold Constant. ($K_{BLOFF} = V_{OUTS_OFF} / V_{SSE_FB}$)



1 Operation mode description – continued

1.5 Flasher SW Open Detection (SWOP)

If voltage drop across external resistance R_{SE} drops below a certain value, Flasher SW open is detected. When the Flasher SW open is detected, the IC shifts from Blinking High mode to Power Saving Mode. Flasher SW Open detection can only be detected in Blinking High Mode. The Flasher SW Open Detection condition can be calculated by the following formula.

$$V_{IN_SE} > V_{SWOP}$$

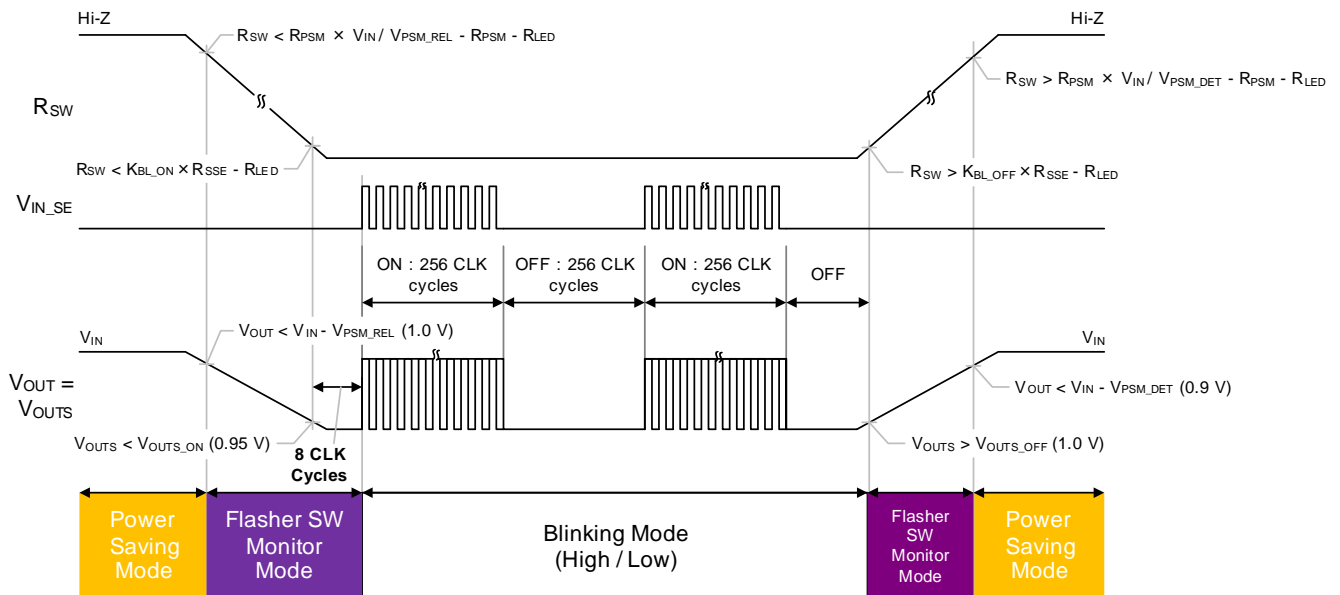
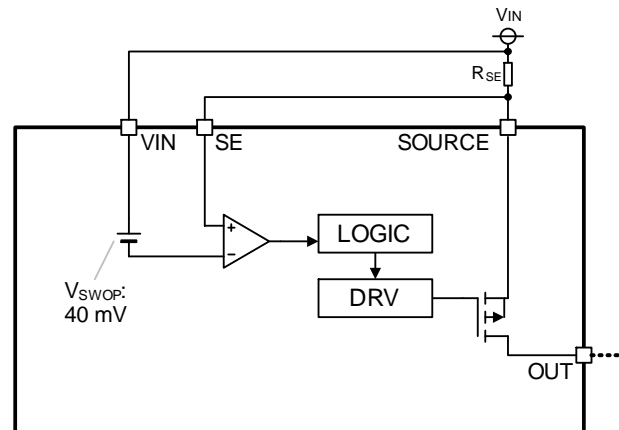
where:

V_{IN_SE}

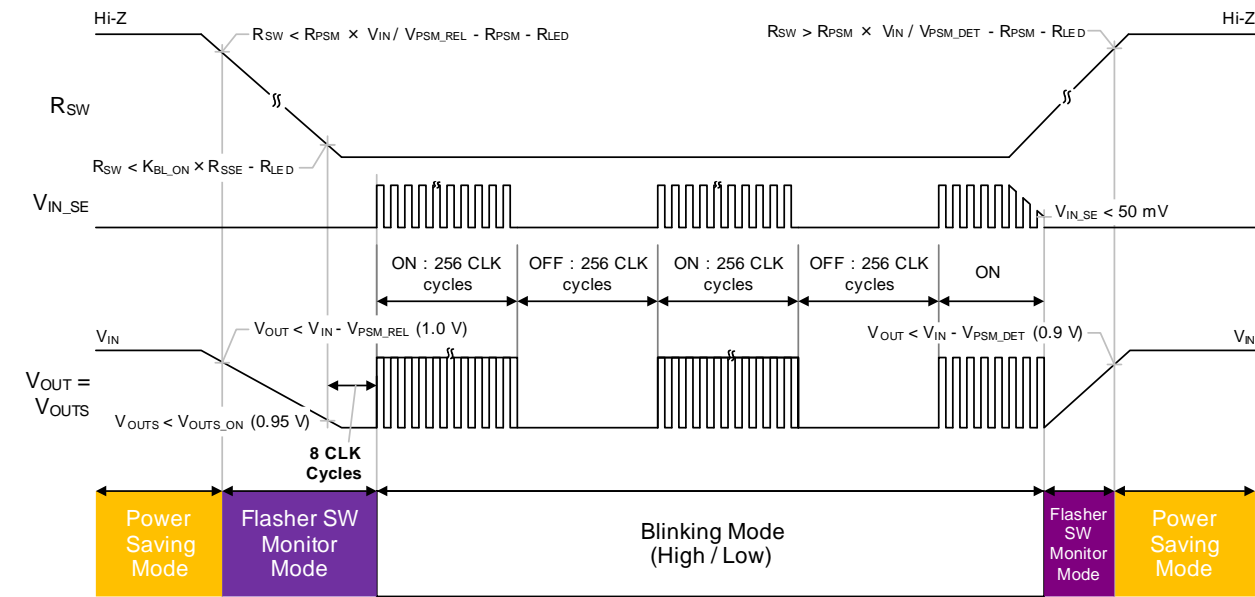
is the VIN to SE voltage.

V_{SWOP}

is the Flasher SW Open Detection Threshold.



1.5 Flasher SW Open Detection (SWOP) – continued



1 Operation mode description – continued

1.6 LED Open Detection Mode (LEDOP)

This LSI can detect LED open. In case of LED open inform the fault condition to user by double blinking. On detection of fault IC starts operating the outputs on almost 1/2 blinking period (double blink operation). If voltage drop across external resistance R_{SE} drops below a certain value, LED open is detected. The LED open detection condition can be calculated by the following formula.

$$V_{IN\ SE} < V_{OPEN} \ \& \ V_{IN} > V_{IN\ OPM}$$

$$V_{OPEN} = \frac{V_{OP}}{10}$$

$$V_{OP} = (V_{IN} - V_{ZD_OP}) \times \frac{R_{VOP2}}{R_{VOP1} + R_{VOP2}}$$

where:

 $V_{IN\ SE}$

is the VIN to SE voltage.

 V_{OPEN}

is the LED Open Detection Threshold Voltage.

 V_{IN}

is the VIN pin voltage.

 $V_{IN\ OPM}$

is the Disable LED Open Detection Function at Reduced-voltage.

 V_{OP}

is the VOP pin voltage.

$$V_{ZD \text{ OP}}$$

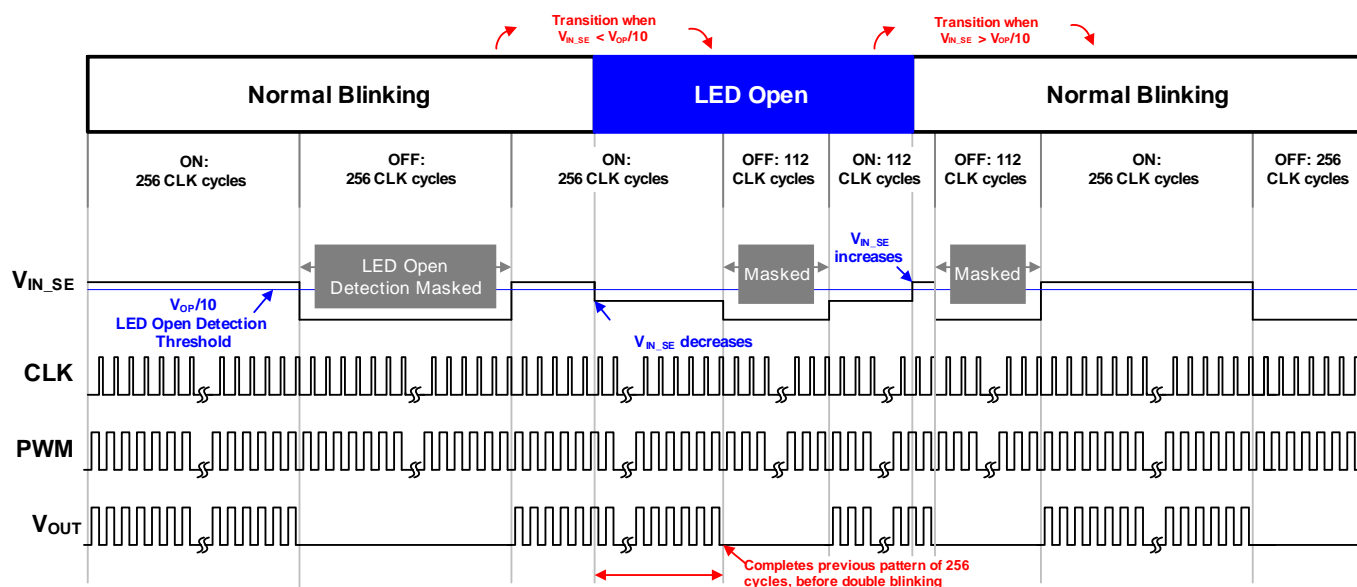
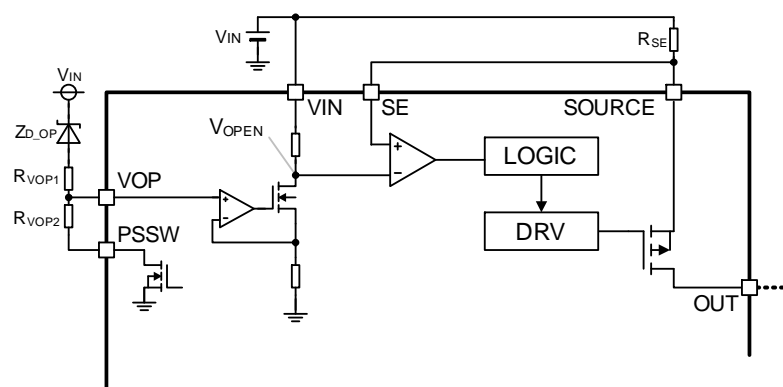
is the characteristic Zener voltage of diode Z_{D_OP} (chosen based on output voltage).

 R_{VOP1}

is the LED Open Detection Threshold Setting Resistor 1.

 R_{VOP2}

is the LED Open Detection Threshold Setting Resistor 2.



1 Operation mode description – continued

1.7 Short Circuit Protection Mode (SCP)

When voltage drop across R_{SE} rises above a certain value, short circuit is detected.

When short circuit is detected, the MOSFET connected to the OUT pin is turned off to prevent overcurrent from flowing into the IC. The Short Circuit Protection condition can be calculated by the following formula.

$$V_{IN_SE} > V_{SHORT}$$

$$V_{SHORT} = \frac{V_{SCP}}{2}$$

$$V_{SCP} = V_{REG} \times \frac{R_{VSCP2}}{R_{VSCP1} + R_{VSCP2}}$$

where:

V_{IN_SE}

is the VIN to SE voltage.

V_{SHORT}

is the Short Circuit Protection Threshold Voltage .

V_{SCP}

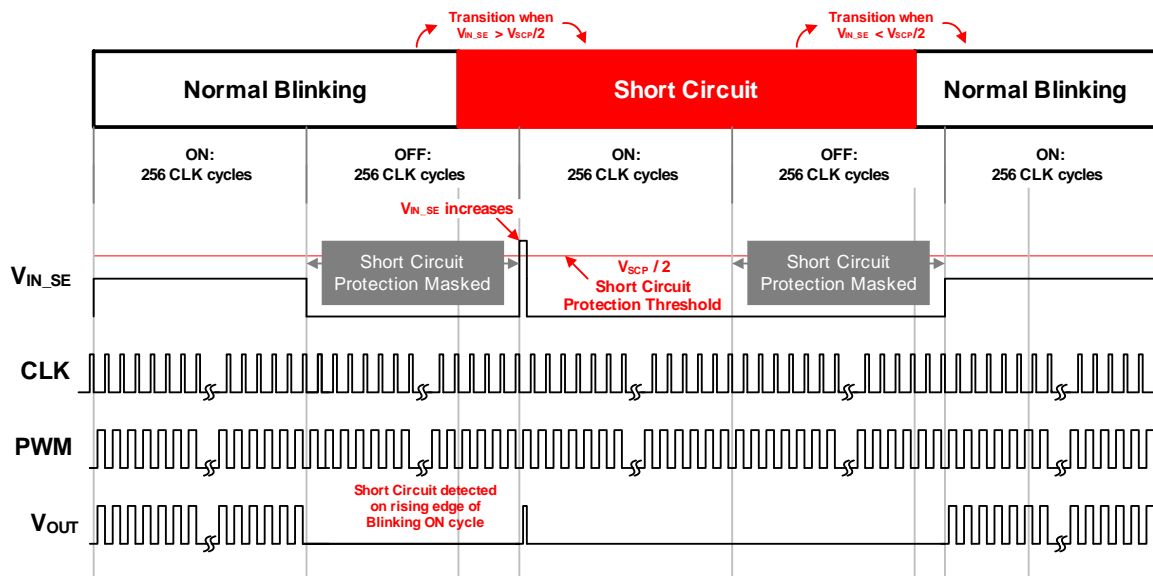
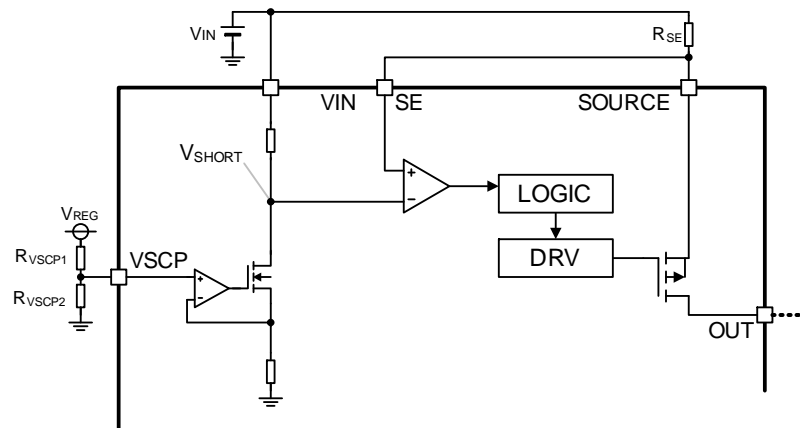
is the VSCP pin voltage.

R_{VSCP1}

is the SCP Threshold Setting Resistor 1.

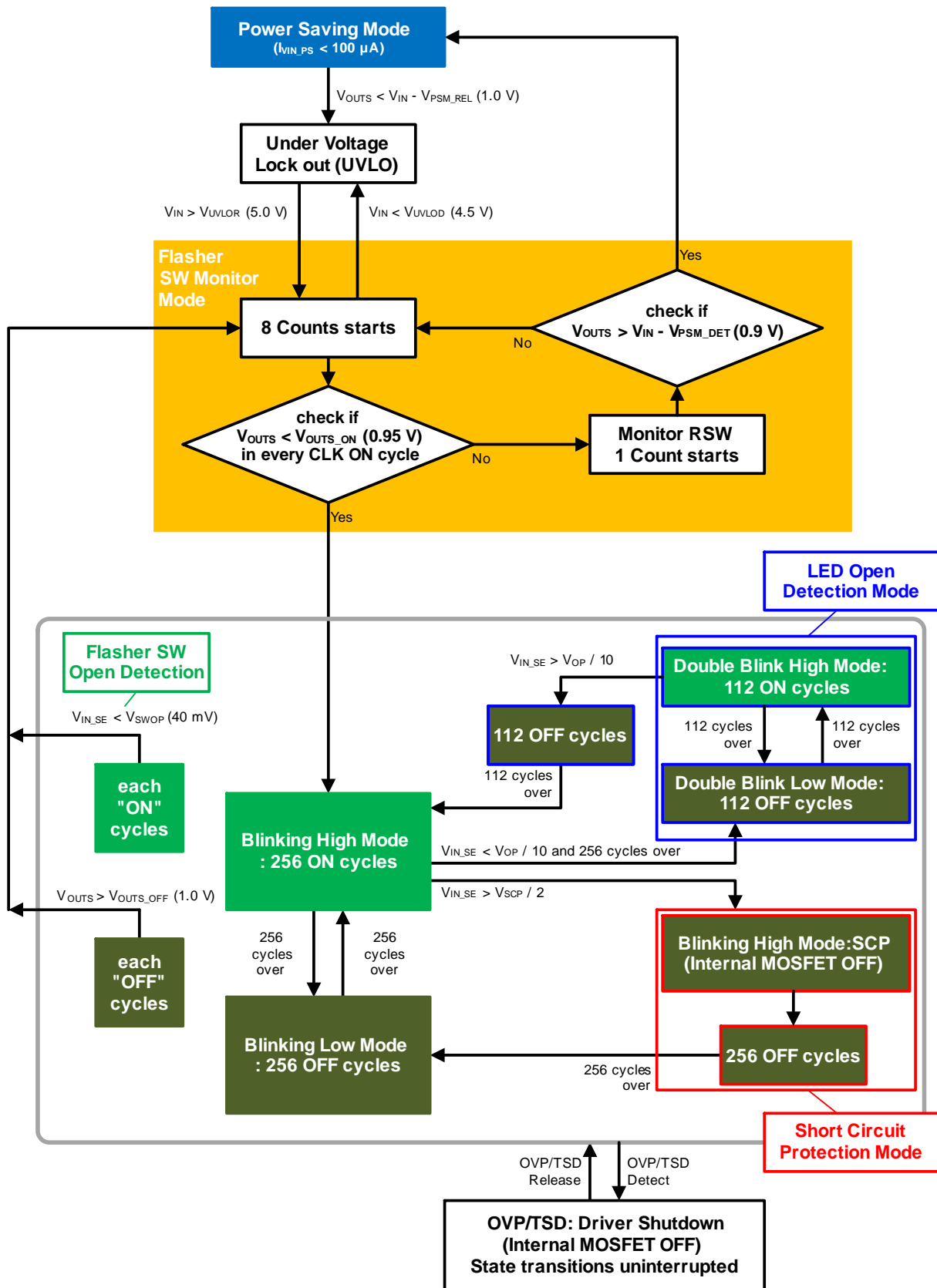
R_{VSCP2}

is the SCP Threshold Setting Resistor 2.



Description of Blocks – continued

2 State Transition Diagram



Description of Blocks – continued

3 CR Timer

This IC determines the flasher cycle from the internal clock generated by CR timer. The CR timer period, ON Duty, can be set by the external resistor R_{CRT1} , R_{CRT2} and the capacitance C_{CRT} .

- (1) CRT ramp up Time t_1 and CRT ramp down Time t_2
 CRT ramp up Time t_1 and CRT ramp down Time t_2 can be defined from the following equations.
 Make sure that t_2 is set PWM Minimum Pulse Width t_{MIN} (100 μ s) or more.

$$t_1 = \frac{(R_{CRT1} + R_{CRT2}) \times C_{CRT}}{N_{CHA}} \quad [s]$$

$$t_2 = \frac{(R_{CRT2} + R_D) \times C_{CRT}}{N_{DIS}} \quad [s]$$

When $R_{CRT2} \gg R_D$

$$t_2 = \frac{R_{CRT2} \times C_{CRT}}{N_{DIS}} \quad [s]$$

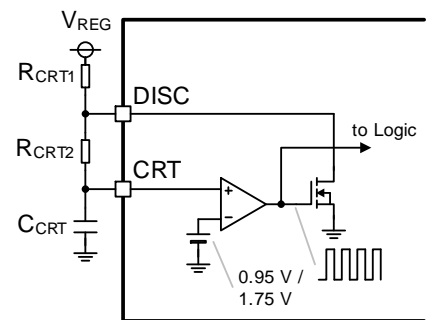
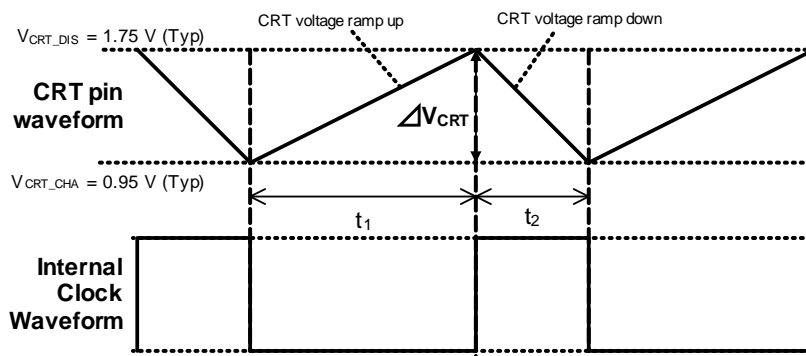
where:

R_{CRT1} is the CR Timer Time Setting Resistor 1.
 R_{CRT2} is the CR Timer Time Setting Resistor 1.
 R_D is the DISC Pin ON Resistance.
 C_{CRT} is the CR Timer Time Setting Capacitor.
 N_{CHA} is the CR Timer Charge Constant.
 N_{DIS} is the CR Timer Discharge Constant.

- (2) Internal clock frequency f_{CLK} and ON Duty D_{ON}
 Internal clock frequency and internal clock ON Duty is defined by t_1 and t_2 .

$$f_{CLK} = \frac{1}{t_1 + t_2} \quad [Hz]$$

$$D_{ON} = \frac{t_2}{t_1 + t_2} \quad [\%]$$



Description of Blocks – continued

4 Output PWM ON Duty Control during high input voltage

This IC has built in Output PWM ON Duty Control during high input voltage which protects the output LEDs. VDR pin voltage which is generated externally by dividing VIN pin voltage is compared with CRT pin voltage to generate PWM signal. When VDR > VCRT, the internal MOSFET for Blinking High Mode is turned off and the increase in average current flowing to the LED can be reduced.

Output PWM ON Duty D_{ON_PWM} is represented by following expression.

$$D_{ON} = \frac{V_{CRT_DIS} - V_{DR}}{V_{CRT_DIS} - V_{CRT_CHA}} [\%]$$

$$V_{DR} = V_{IN} \times \frac{R_{VDR2}}{R_{VDR1} + R_{VDR2}} [\%]$$

where:

V_{CRT_DIS} is the CRT Pin Discharge Voltage.

V_{CRT_CHA} is the CRT Pin Charge Voltage.

V_{DR} is the VDR pin voltage.

V_{IN} is the VIN pin voltage.

R_{VDR1} is the Output ON Duty Setting Resistor 1.

R_{VDR2} is the Output ON Duty Setting Resistor 2.

However,

$V_{DR} \leq V_{CRT_CHA}$: ON Duty = 100 %

$V_{DR} \geq V_{CRT_DIS}$: ON Duty = 0 %

Make sure to connect resistors for voltage division of VIN to fix the voltage on the VDR pin as shown in figure.

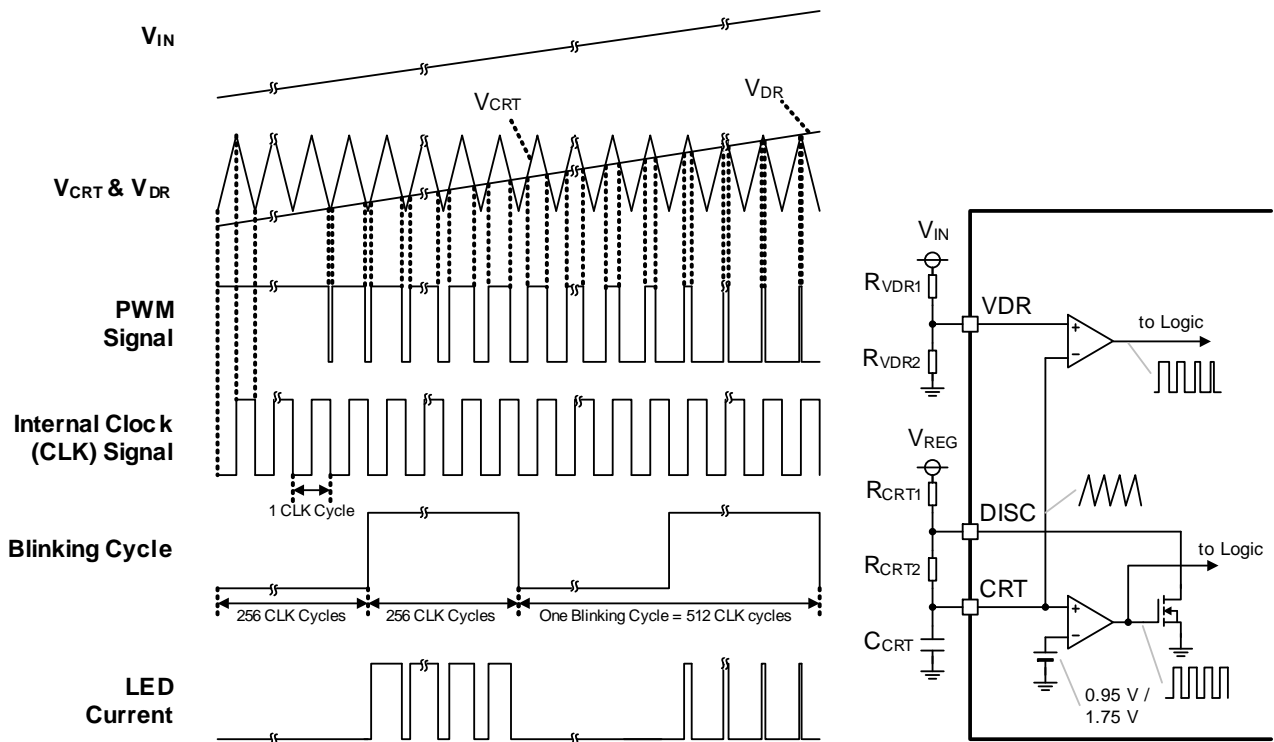
Example-

For $R_{VDR1} = 47 \text{ k}\Omega$ and $R_{VDR2} = 3.4 \text{ k}\Omega$

When $V_{IN} = 14 \text{ V}$, $V_{DR} = 0.944 \text{ V}$ & ON Duty = 100 %

When $V_{IN} = 18 \text{ V}$, $V_{DR} = 1.214 \text{ V}$ & ON Duty = 66 %

So as VIN increases the PWM duty cycle decreases.



Description of Blocks – continued**5 Reference Voltage (VREG)**

Reference voltage VREG 5.0 V (Typ) is generated from VIN input voltage. This voltage is used as power source for the internal circuit, and also used to fix the voltage of pins outside LSI to HIGH side. The VREG pin must be connected with $C_{VREG} = 1.0 \mu\text{F}$ to $10 \mu\text{F}$ to ensure capacity for the phase compensation. If C_{VREG} is not connected, the circuit behavior would become extraordinarily unstable, for example with the oscillation of the reference voltage.

The VREG pin voltage must not be used as power source for other devices than this LSI.

VREG circuit has a built-in UVLO function. The IC is activated when the VREG pin voltage rises to 3.5 V (Typ) or higher, and shuts down when the VREG pin voltage drops to 2.0 V (Typ) or lower.

6 Under Voltage Lock-Out (UVLO)

This IC has built-in under voltage lock-out function (UVLO).

For VIN ramp-up UVLO is active till VIN = 5.0 V (Typ). For VIN ramp down UVLO gets active when VIN = 4.5 V (Typ).

UVLO shuts down all circuit blocks other than regulator (VREG) block.

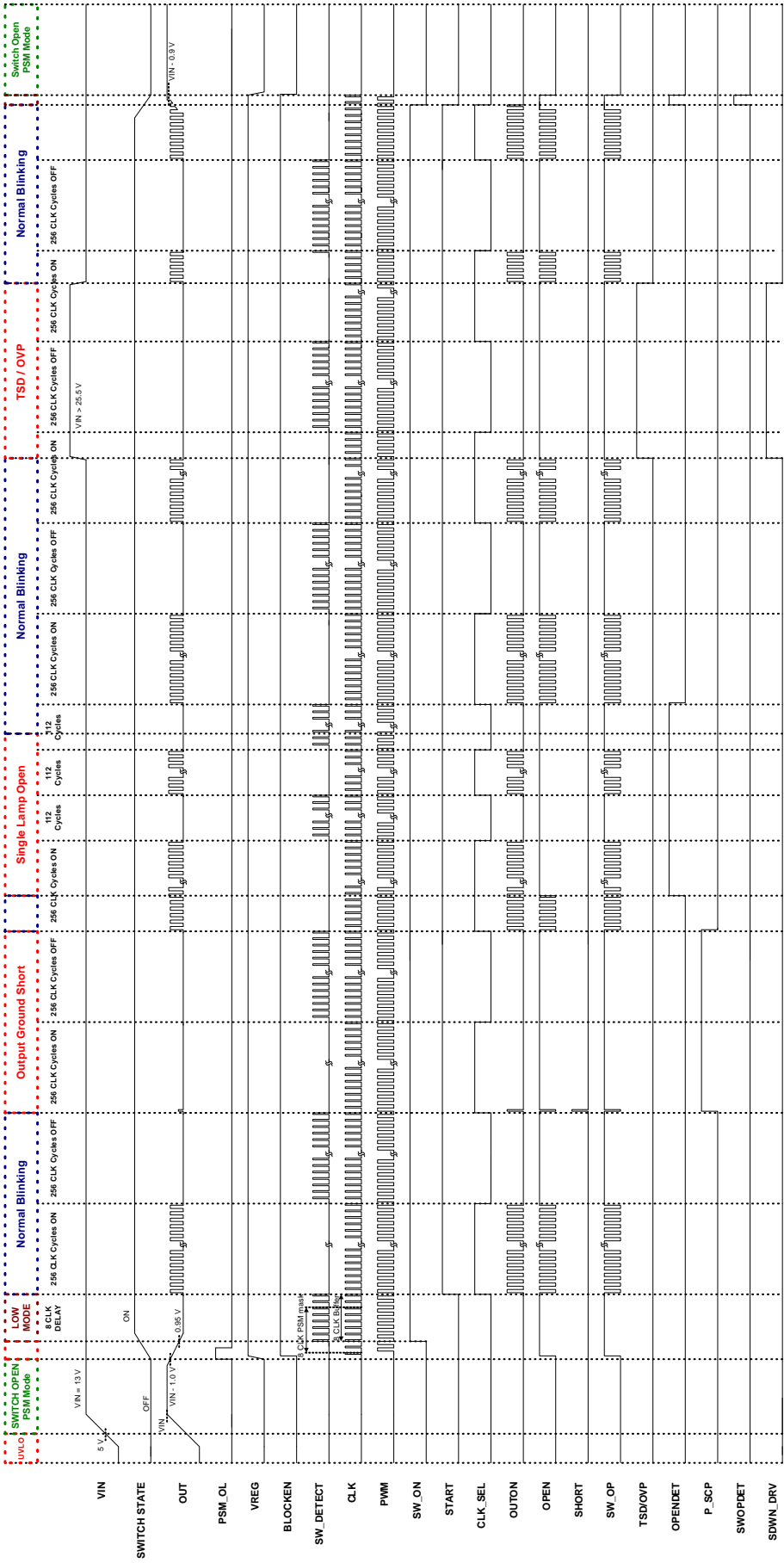
UVLO is also dependent on VREG voltage. At ramp-up UVLO is released when VREG > 3.5 V and at ramp down UVLO is enabled when VREG = 2.0 V.

7 Over Voltage protection (OVP)

This LSI has a function to turn off output and prevent deterioration of load when VIN Pin voltage exceeds 25.5 V (Typ).

When OVP is detected, after the supply voltage drops more than hysteresis width of 500 mV (Typ) below OVP, it returns to normal state.

Timing Chart



Absolute Maximum Ratings (Ta = 25 °C)

| Parameter | Symbol | Rating | Unit |
|----------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|------|
| VIN Voltage | V _{IN} | -0.3 to +50.0 | V |
| SOURCE, SE, SSE, OUT, OUTS, PSSW, VDR, VOP Voltage | V _{SOURCE} , V _{SE} , V _{SSE} , V _{OUT} , V _{OUTS} , V _{PSSW} , V _{DR} , V _{OP} | -0.3 to +V _{IN} +0.3 V | V |
| VIN to SOURCE, VIN to SE, VIN to SSE Voltage | V _{IN_SOURCE} , V _{IN_SE} , V _{IN_SSE} | -0.3 to +5.0 | V |
| VREG Voltage | V _{REG} | -0.3 to +7.0 | V |
| DISC, CRT, VSCP, TEST Voltage | V _{DISC} , V _{CRT} , V _{SCP} , V _{TEST} | -0.3 to V _{REG} +0.3 V | V |
| Storage Temperature Range | T _{stg} | -55 to +150 | °C |
| Maximum Junction Temperature | T _{jmax} | 150 | °C |

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance (Note 1)

| Parameter | Symbol | Thermal Resistance (Typ) | | Unit |
|----------------------------------------------------------------|---------------|--------------------------|--------------------------|------|
| | | 1s ^(Note 3) | 2s2p ^(Note 4) | |
| HTSSOP-B20 | | | | |
| Junction to Ambient | θ_{JA} | 103.50 | 31.40 | °C/W |
| Junction to Top Characterization Parameter ^(Note 2) | Ψ_{JT} | 10.00 | 4.00 | °C/W |

(Note 1) Based on JESD51-2A (Still-Air), using a BD18327 Chip.

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top centre of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-5, 7.

| Layer Number of Measurement Board | Material | Board Size |
|-----------------------------------|----------|-------------------------------|
| Single | FR-4 | 114.3 mm x 76.2 mm x 1.57 mmt |

| Top | |
|-----------------------|-----------|
| Copper Pattern | Thickness |
| Footprints and Traces | 70 μm |

| Layer Number of Measurement Board | Material | Board Size | Thermal Via ^(Note 5) | |
|-----------------------------------|----------|------------------------------|---------------------------------|----------|
| | | | Pitch | Diameter |
| 4 Layers | FR-4 | 114.3 mm x 76.2 mm x 1.6 mmt | 1.20 mm | Φ0.30 mm |

| Top | | 2 Internal Layers | | Bottom | |
|-----------------------|-----------|-------------------|-----------|-------------------|-----------|
| Copper Pattern | Thickness | Copper Pattern | Thickness | Copper Pattern | Thickness |
| Footprints and Traces | 70 μm | 74.2 mm x 74.2 mm | 35 μm | 74.2 mm x 74.2 mm | 70 μm |

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|------------------------------------|----------------------|-----|------|------|------|
| Supply Voltage ^(Note 1) | V _{IN} | 6.0 | 13.0 | 18.0 | V |
| OUT Pin Maximum Output Current | I _{OUT_MAX} | - | - | 1.5 | A |
| PWM Minimum Pulse Width | t _{MIN} | 100 | - | - | μs |
| PWM Frequency | f _{PWM} | 150 | - | 1000 | Hz |
| Operating Temperature | Topr | -40 | - | +125 | °C |

(Note 1) ASO should not be exceeded.

Recommended Setting Parts Range

| Parameter | Symbol | Min | Max | Unit |
|-------------------------------------------------|--------------------|-------|------|------|
| Power Supply Input Capacitor | C _{VIN} | 1.0 | 10.0 | μF |
| Reference Voltage Output Pin Capacitor | C _{VREG} | 1.0 | 10.0 | μF |
| Constant Current Setting Resistor | R _{SSE} | 0.04 | 10 | kΩ |
| Output Current Sense Resistor | R _{SE} | 0.065 | 10 | Ω |
| CR Timer Time Setting Resistor 1 | R _{CRT1} | 1.0 | 100 | kΩ |
| CR Timer Time Setting Resistor 2 | R _{CRT2} | 1.0 | 100 | kΩ |
| CR Timer Time Setting Capacitor | C _{CRT} | 0.01 | 1.00 | μF |
| SCP Threshold Setting Resistor 1 | R _{VSCP1} | 10 | 100 | kΩ |
| SCP Threshold Setting Resistor 2 | R _{VSCP2} | 4.7 | 100 | kΩ |
| LED Open Detection Threshold Setting Resistor 1 | R _{VOP1} | 10 | 100 | kΩ |
| LED Open Detection Threshold Setting Resistor 2 | R _{VOP2} | 4.7 | 100 | kΩ |
| Output PWM ON Duty Setting Resistor 1 | R _{VDR1} | 4.7 | 100 | kΩ |
| Output PWM ON Duty Setting Resistor 2 | R _{VDR2} | 4.7 | 100 | kΩ |

Electrical Characteristics

(Unless otherwise specified $V_{IN} = 13\text{ V}$ $T_a = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $C_{VREG} = 4.7\text{ }\mu\text{F}$)

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|------------------------------------------------------|-----------------|--------------------------|--------------------------|--------------------------|------------------|-------------------------------------------|
| Circuit Current at Normal Mode | I_{VIN_NOM} | - | - | 10 | mA | |
| Circuit Current at Power Saving Mode | I_{VIN_PS} | - | - | 100 | μA | OUT: OPEN |
| [VREG] | | | | | | |
| Reference Voltage | V_{REG} | 4.750 | 5.000 | 5.250 | V | $I_L = 2\text{ mA}$ |
| [Current Driver for Low Mode] | | | | | | |
| SSE Pin Feedback Voltage | V_{SSE_FB} | - | 0.95 | - | V | |
| [Flasher SW Resistance Monitor Mode] | | | | | | |
| Blinking ON Threshold Voltage | V_{OUTS_ON} | - | 0.95 | - | V | $V_{OUTS} = \text{Sweep down}$ |
| Blinking OFF Threshold Voltage | V_{OUTS_OFF} | - | 1.00 | - | V | $V_{OUTS} = \text{Sweep up}$ |
| Blinking ON Threshold Constant | K_{BLON} | 0.95 | 1.00 | 1.05 | - | $K_{BLON} = V_{OUTS_ON} / V_{SSE_FB}$ |
| Blinking OFF Threshold Constant | K_{BLOFF} | 1.00 | 1.05 | 1.11 | - | $K_{BLOFF} = V_{OUTS_OFF} / V_{SSE_FB}$ |
| [Power Saving Mode] | | | | | | |
| Power Saving Mode Release Threshold | V_{PSM_REL} | 0.5 | 1.0 | 1.5 | V | $V_{OUT} = \text{Sweep down}$ |
| Power Saving Mode Detect Threshold | V_{PSM_DET} | 0.4 | 0.9 | 1.4 | V | $V_{OUT} = \text{Sweep up}$ |
| Power Saving Mode Internal Resistance | R_{PSM} | 8 | 15 | 21 | $\text{k}\Omega$ | |
| [Output Section] | | | | | | |
| OUT Pin ON Resistance for High Mode | R_{ON_OUT} | - | 0.4 | 0.8 | Ω | $I_{OUT} = 0.5\text{ A}$ |
| OUT Pin ON Resistance for Low Mode | R_{LON_OUT} | - | 10 | - | Ω | $I_{OUT} = 20\text{ mA}$ |
| OUT Pin Leakage Current | I_{LEAK_OUT} | - | - | 10 | μA | $V_{OUT} = 13\text{ V}$ |
| [CR Timer Section] | | | | | | |
| CRT Pin Charge Voltage | V_{CRT_CHA} | $V_{REG} \times 0.18$ | $V_{REG} \times 0.19$ | $V_{REG} \times 0.20$ | V | $V_{CRT} = \text{Sweep down}$ |
| CRT Pin Discharge Voltage | V_{CRT_DIS} | $V_{REG} \times 0.33$ | $V_{REG} \times 0.35$ | $V_{REG} \times 0.37$ | V | $V_{CRT} = \text{Sweep up}$ |
| DISC Pin ON Resistance | R_D | - | 10 | 20 | Ω | $I_L = 10\text{ mA}$ |
| CR Timer Charge Constant | N_{CHA} | 4.31 | 4.54 | 4.77 | - | |
| CR Timer Discharge Constant | N_{DIS} | 1.55 | 1.64 | 1.73 | - | |
| [COUNTER Section] | | | | | | |
| Flasher SW Resistance Detection Circuit Count Number | N_{COUNT} | 7 | - | 10 | - | |
| Blinking Cycle Time at Normal Mode | T_{BL_NOM} | $1 / f_{CLK} \times 511$ | $1 / f_{CLK} \times 512$ | $1 / f_{CLK} \times 513$ | s | |
| Blinking Cycle Time at LED Open Detection | T_{BL_LEDOP} | $1 / f_{CLK} \times 223$ | $1 / f_{CLK} \times 224$ | $1 / f_{CLK} \times 225$ | s | |
| Blinking ON Duty | D_{ON} | 49 | 50 | 51 | % | |

Electrical Characteristics - continued

(Unless otherwise specified $V_{IN} = 13\text{ V}$ $T_a = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $C_{VREG} = 4.7\text{ }\mu\text{F}$)

| Parameter | Symbol | Min | Typ | Max | Unit | Condition |
|--------------------------------------------------------|------------------|---------------------|-------------|---------------------|----------|----------------------------------------------------------------|
| [PSSW Section] | | | | | | |
| PSSW ON Resistance | R_{PSSW} | - | 4 | 10 | Ω | $I_{PSSW} = 30\text{ mA}$ |
| [LED Open Detection/ Short Circuit Protection] | | | | | | |
| Disable LED Open Detection Function at Reduced-voltage | V_{IN_OPM} | 7.85 | 8.25 | 8.65 | V | $V_{IN} = \text{Sweep down Detect}$ |
| | | 8.00 | 8.45 | 8.90 | V | $V_{IN} = \text{Sweep up Release}$ |
| | | - | 0.20 | - | V | V_{IN} Hysteresis |
| VOP Pin Input Voltage Range | V_{OP_RANGE} | 1.0 | - | $V_{IN} - 4.0$ | V | $V_{IN} < 14\text{ V}$ |
| | | 1.0 | - | 10.0 | V | $V_{IN} > 14\text{ V}$ |
| VSCP Pin Input Voltage Range | V_{SCP_RANGE} | 1.0 | - | 2.5 | V | |
| LED Open Detection Threshold Voltage 1 | V_{OPEN1} | $(V_{OP}/10) - 5$ | $V_{OP}/10$ | $(V_{OP}/10) + 5$ | mV | $V_{IN_SE} = \text{Sweep down}$ $V_{OP} \leq 2.5\text{ V}$ |
| LED Open Detection Threshold Voltage 2 | V_{OPEN2} | $(V_{OP}/10) - 6.5$ | $V_{OP}/10$ | $(V_{OP}/10) + 6.5$ | mV | $V_{IN_SE} = \text{Sweep down}$ $V_{OP} > 2.5\text{ V}$ |
| Flasher SW Open Detection Threshold Voltage | V_{SWOP} | 27 | 40 | 53 | mV | $V_{IN_SE} = \text{Sweep down}$ |
| Short Circuit Protection Threshold Voltage | V_{SHORT} | $V_{SCP}/2 - 0.100$ | $V_{SCP}/2$ | $V_{SCP}/2 + 0.100$ | V | $V_{IN_SE} = \text{Sweep up}$ |
| [VIN UVLO] | | | | | | |
| UVLO VIN Detect Voltage | V_{UVLOD} | 4.0 | 4.5 | 5.0 | V | $V_{IN} = \text{Sweep down}$ |
| UVLO VIN Release Voltage | V_{UVLOR} | 4.5 | 5.0 | 5.5 | V | $V_{IN} = \text{Sweep up}$, $V_{REG} > 3.5\text{ V}$ |
| [Overvoltage Protection] | | | | | | |
| Over Voltage Protection Threshold Voltage | V_{OVP} | 22.95 | 25.50 | 28.05 | V | $V_{IN} = \text{Sweep up}$ |
| Over Voltage Protection Hysteresis Voltage | V_{OVPHYS} | 250 | 500 | 750 | mV | $V_{IN} = \text{Sweep down}$ |

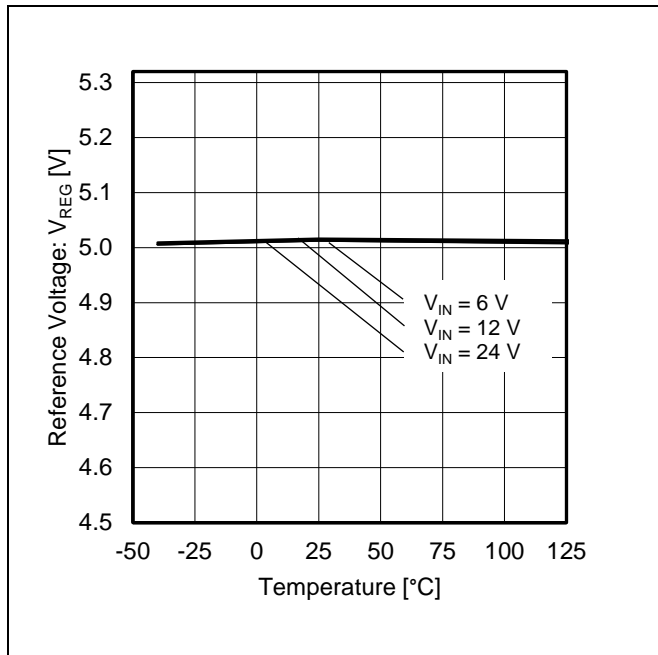
Typical Performance Curve(Unless otherwise specified $V_{IN} = 13\text{ V}$, $T_a = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $C_{VREG} = 4.7\text{ }\mu\text{F}$)

Figure 1. Reference Voltage vs Temperature

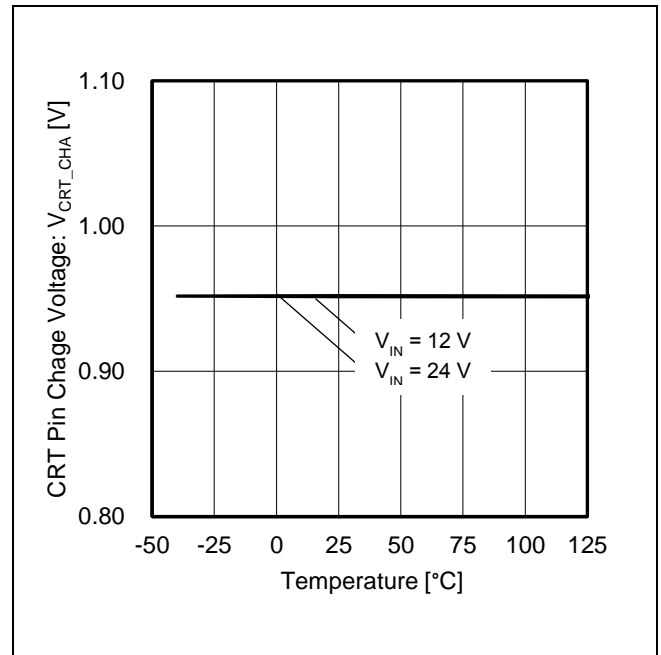


Figure 2. CRT Pin Charge Voltage vs Temperature

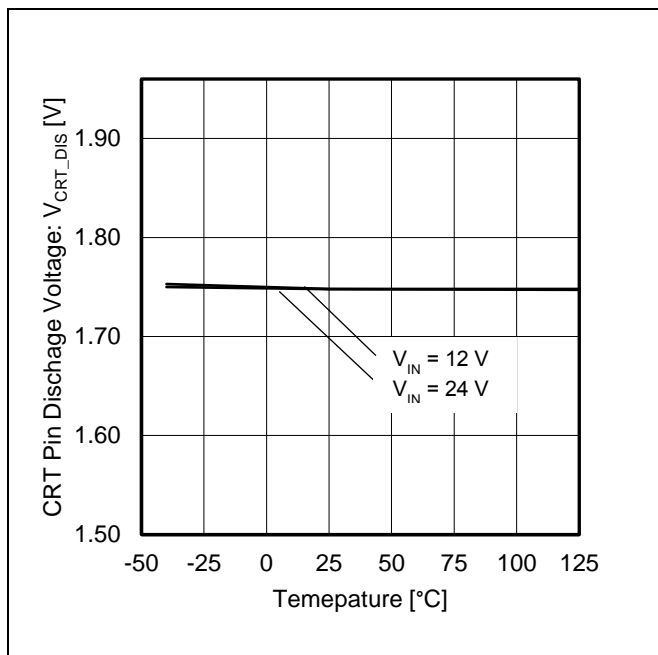


Figure 3. CRT Pin Discharge Voltage vs Temperature

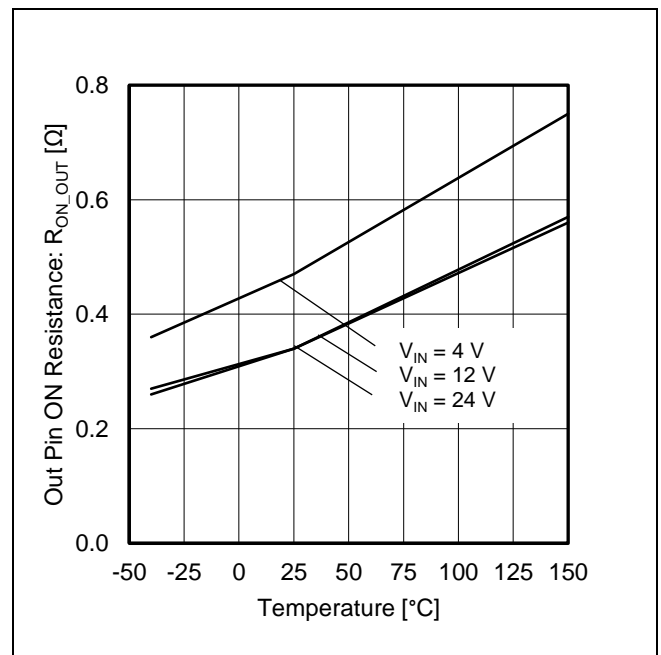


Figure 4. Out Pin ON Resistance for High Mode vs Temperature

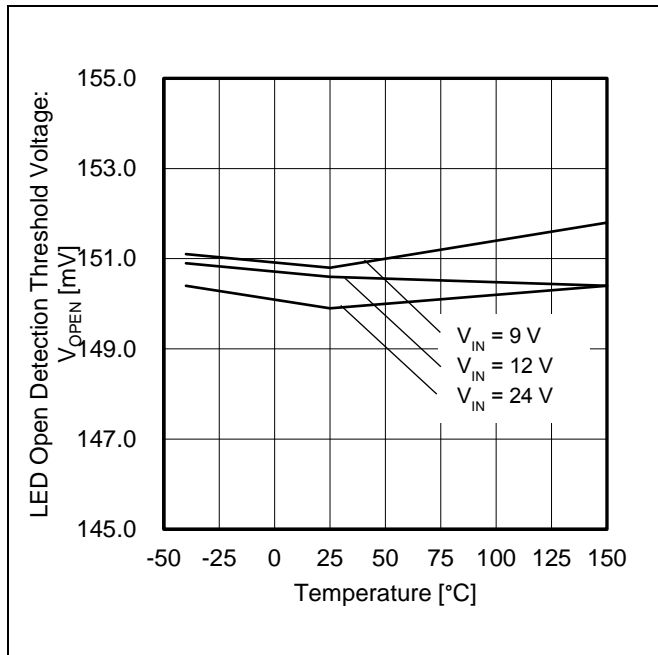
Typical Performance Curve - continued(Unless otherwise specified $V_{IN} = 13\text{ V}$, $T_a = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $C_{VREG} = 4.7\text{ }\mu\text{F}$)

Figure 5. LED Open Detection Threshold Voltage
at $V_{OP} = 1.5\text{ V}$, $V_{OPEN} = 150\text{ mV}$
vs Temperature

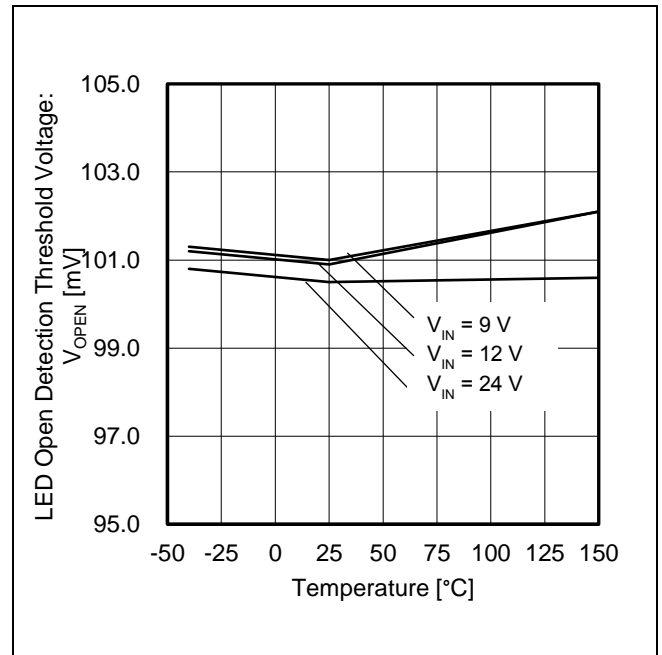


Figure 6. LED Open Detection Threshold Voltage
at $V_{OP} = 1.0\text{ V}$, $V_{OPEN} = 100\text{ mV}$
vs Temperature

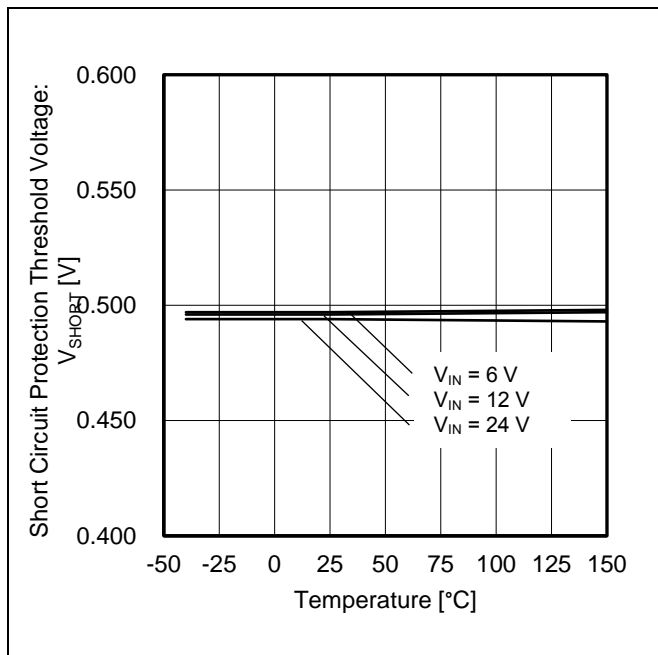


Figure 7. Short Circuit Protection Threshold Voltage
at $V_{SCP} = 1.0\text{ V}$, $V_{SHORT} = 0.500\text{ V}$
vs Temperature

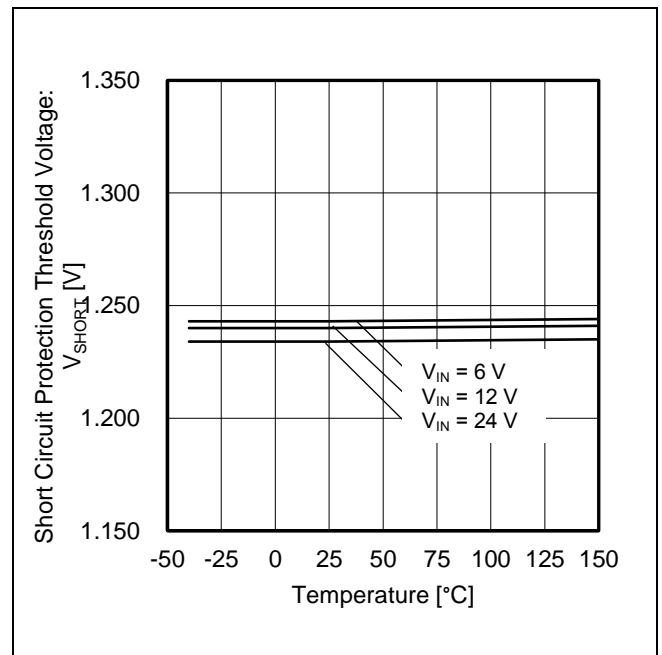
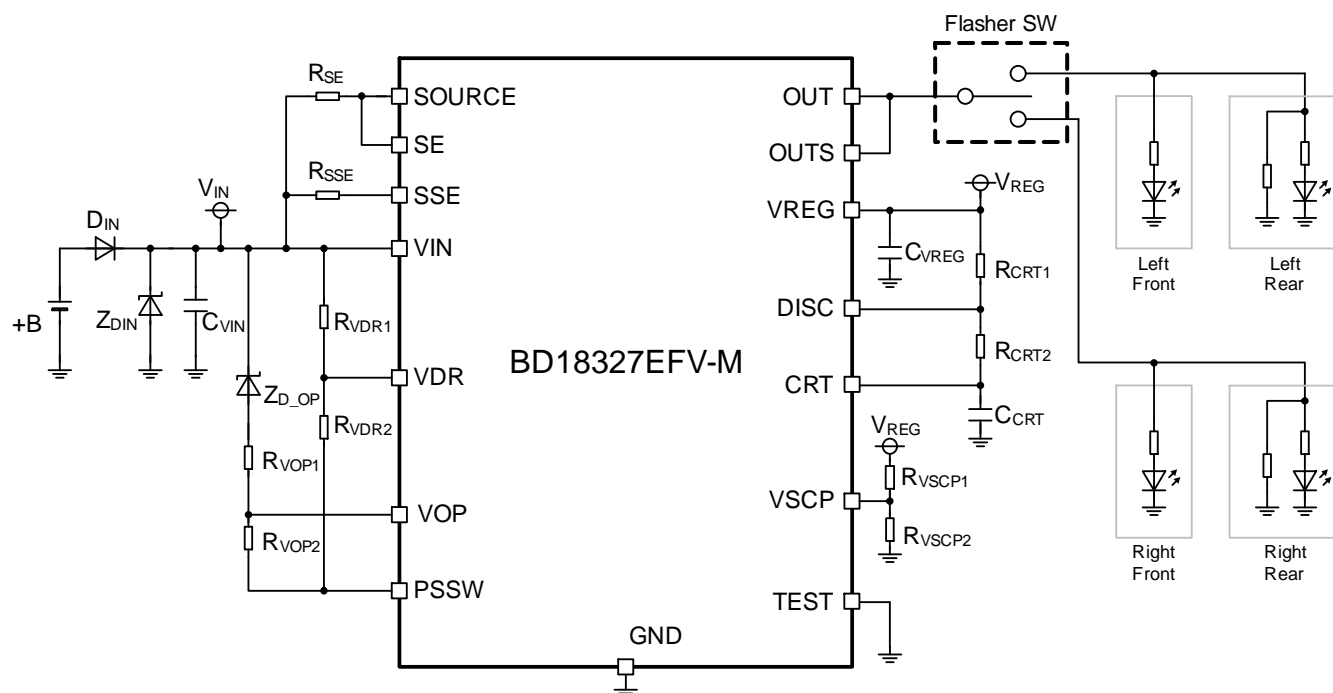


Figure 8. Short Circuit Protection Threshold Voltage
at $V_{SCP} = 2.5\text{ V}$, $V_{SHORT} = 1.250\text{ V}$
vs Temperature

Application Example

VIN = 13 V, CLK frequency 763 Hz (duty = 100 %), Blinking frequency: 1.49 Hz, IOUT = 687 mA



Recommended Parts List:

| Parts | No | Parts Name | Value | UNIT | Product Maker |
|-----------|--------------------|--------------------|-------|------|-----------------|
| IC | U1 | BD18327EFV-M | - | - | ROHM |
| Diode | D _{IN} | RFN2LAM6STFTR | - | - | ROHM |
| | Z _{DIN} | TND12H-220KB00AAA0 | 43 | V | NIPPON CHEMICON |
| | Z _{D_OP} | EDZVFH3.6B | 3.6 | V | ROHM |
| Resistor | R _{SE} | LTR100JZPFLR510 | 0.51 | Ω | ROHM |
| | R _{SSE} | MCR03EZPFX3600 | 360 | Ω | ROHM |
| | R _{VDR1} | MCR03EZPFX6802 | 68 | kΩ | ROHM |
| | R _{VDR2} | MCR03EZPFX5101 | 5.1 | kΩ | ROHM |
| | R _{CRT1} | MCR03EZPFX4702 | 47 | kΩ | ROHM |
| | R _{CRT2} | MCR03EZPFX3301 | 3.3 | kΩ | ROHM |
| | R _{VSCP1} | MCR03EZPFX3002 | 30 | kΩ | ROHM |
| | R _{VSCP2} | MCR03EZPFX1002 | 10 | kΩ | ROHM |
| | R _{VOP1} | MCR03EZPFX2402 | 24 | kΩ | ROHM |
| | R _{VOP2} | MCR03EZPFX1002 | 10 | kΩ | ROHM |
| Capacitor | C _{VIN} | GCM31CC71H475KA03 | 4.7 | μF | murata |
| | C _{VREG} | GCM188C71A225KE01 | 2.2 | μF | murata |
| | C _{CRT} | GCM155R11A104KA01 | 0.1 | μF | murata |

Precautions for board design

- ① Place C_{VIN}, C_{VREG} in the immediate vicinity of the IC pin. If necessary, connect a bypass capacitor (0.1 μF) close to the IC.
- ② Select the optimum one for D1 according to the output current.

I/O Equivalence Circuit

| | | |
|-----------|----------|----------|
| 1. SOURCE | 2. SE | 4. SSE |
| | | |
| 8. VDR | 9. VOP | 10. PSSW |
| | | |
| 12. TEST | 13. VSCP | 14. CRT |
| | | |
| 15. DISC | 17. VREG | 19. OUTS |
| | | |
| 20. OUT | | |
| | | |

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin\ A$ and $GND > Pin\ B$, the P-N junction operates as a parasitic diode.

When $GND > Pin\ B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

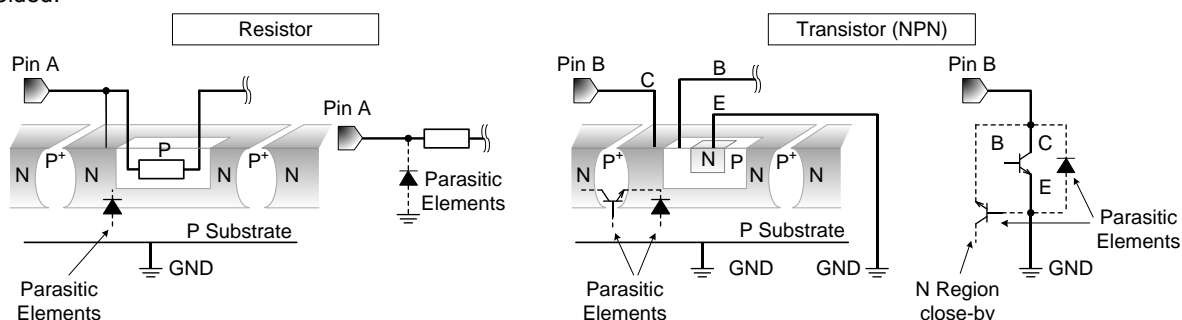


Figure 9. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Functional Safety

"ISO 26262 Process Compliant to Support ASIL-*

A product that has been developed based on an ISO 26262 design process compliant to the ASIL level described in the datasheet.

"Safety Mechanism is Implemented to Support Functional Safety (ASIL-*)"

A product that has implemented safety mechanism to meet ASIL level requirements described in the datasheet.

"Functional Safety Supportive Automotive Products"

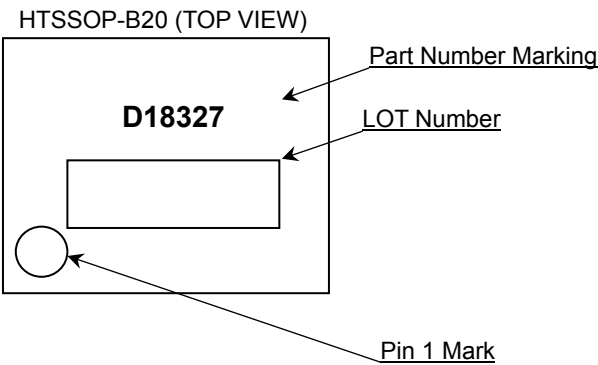
A product that has been developed for automotive use and is capable of supporting safety analysis with regard to the functional safety.

Note: "ASIL-*" is stands for the ratings of "ASIL-A", "-B", "-C" or "-D" specified by each product's datasheet.

Ordering Information

| | | | | | | | | | | | | |
|---------------------|--|--|--|--|--|--|--|--|--|----------------------------|------|--------------------------------------------------------------------------------------|
| B D 1 8 3 2 7 E F V | | | | | | | | | | - | M E2 | |
| Part Number | | | | | | | | | | Package EFV: HTSSOP-B20 | | Packing and Forming Specification M: For Automotive E2: Embossed Tape and Reel |

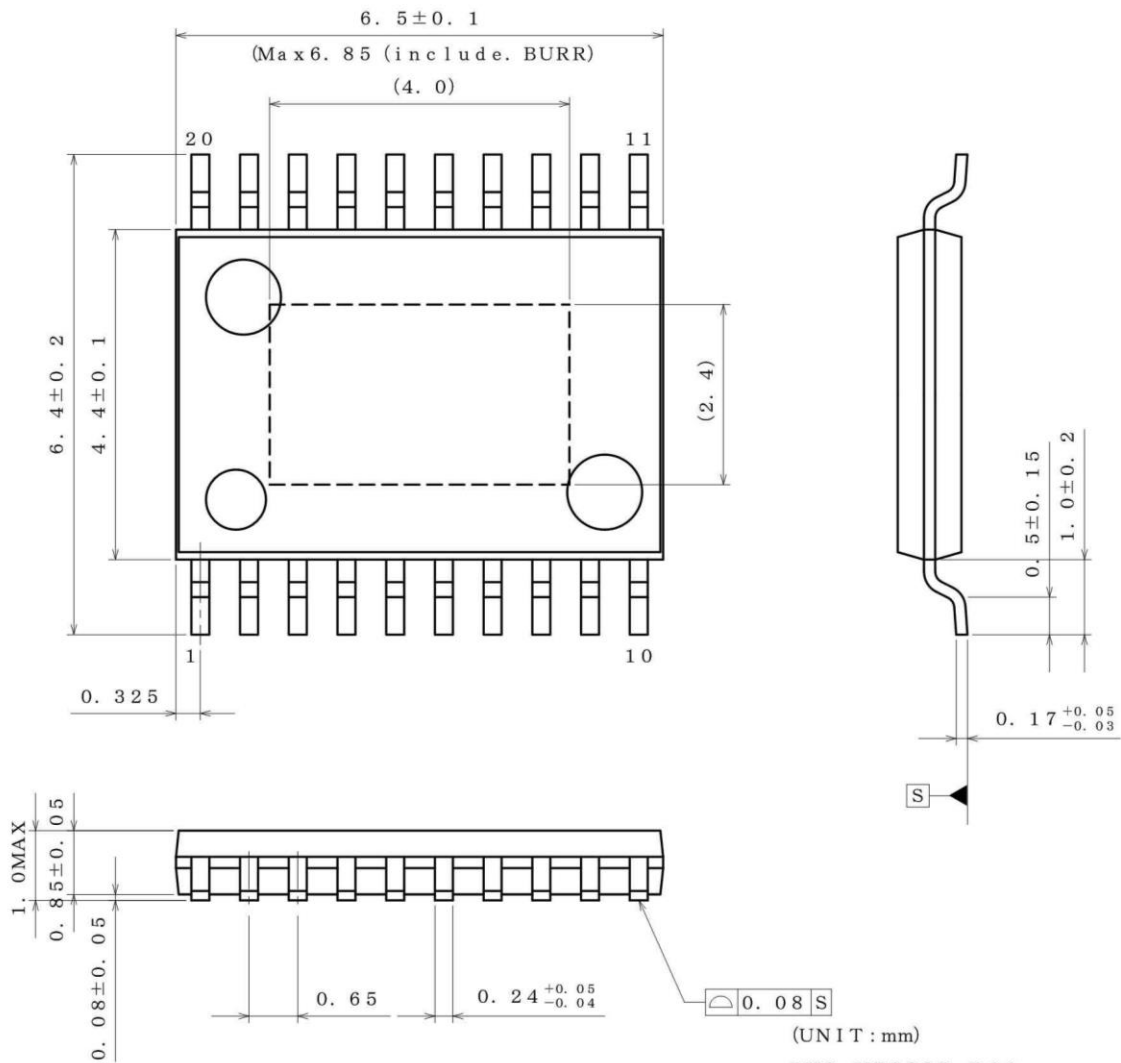
Marking Diagram



Physical Dimension and Packing Information

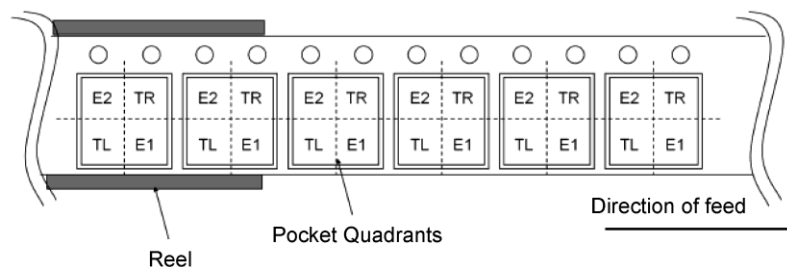
Package Name

HTSSOP-B20



< Tape and Reel Information >

| | |
|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------|
| Tape | Embossed carrier tape |
| Quantity | 2500pcs |
| Direction of feed | E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand |



Revision History

| Date | Version | Changes |
|-------------|---------|-------------|
| 26.Apr.2021 | 001 | New Release |

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV | | CLASS III | |

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 - [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - [f] Sealing or coating our Products with resin or other coating materials
 - [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - [h] Use of the Products in places subject to dew condensation
4. The Products are not subject to radiation-proof design.
5. Please verify and confirm characteristics of the final or mounted products in using the Products.
6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
8. Confirm that operation temperature is within the specified range described in the product specification.
9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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