Bluetooth TM HCI module Data Sheet

Texas Instruments Chipset
for Bluetooth 4.0 + FM(Tx/Rx)

Tentative P/N : LBMA1BGUG2-TEMP

The revision history of the product specification

Issued Date	Revision Code	Revision Page	Changed Items	Change Reason
2012/Oct/16	-		Issued as Product Specification.	

TABLE OF CONTENTS

 Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

1. SCOPE

This specification is applied to the Bluetooth ™ HCI module (Blue Module ™)

2. KEY FEATURES

- Full compliant with Bluetooth specification v4.0 up to HCI level
- Flexibility for easy stack integration and validation into various microcontrollers such as TI platform (Stellaris®, MSP430™)
- Best-in-class Bluetooth (RF) performance (Tx power, Rx sensitivity, Blocking)
- Texas Instruments CC2564 inside (65nm CMOS process integrating Bluetooth BR/EDR/LE functions)
- Advanced power management design for extend battery life and ease of use
- On chip power management, including direct connection to battery or DC/DC
- Internal crystal oscillator (38.4MHz)
- Full Bluetooth data rate up to 2178kbps asymmetric
- Support for Bluetooth power saving modes (Sniff, Hold)
- Support for very low-power modes (deep sleep, power down)
- Standard HCI over H4 UART with maximum rate of 4Mbps
- Fully programmable digital PCM codec interface
- Surface mount type 5.8 x 4.8 x 1.0mm^3, 0.6g weight
- Compliant with RoHS

3. ORDERING INFORMATION

Ordering Part Number	Description
LBMA1BGUG2-TEMP	In case of sample order
LBMA1BGUG2-TEMP-D	EVK
LBMA1BGUG2-TEMP-AA	Motherboard

4. ABSOLUTE MAXIMUM RATINGS

		min.	max.	unit
Storage Temperature		-40	+85	deg.C
Supply Voltage	VDD_IN / MLDO_IN	-0.5	5.2	V
	VDD_IO	-0.5	2.0	V

5. OPERATING CONDITION

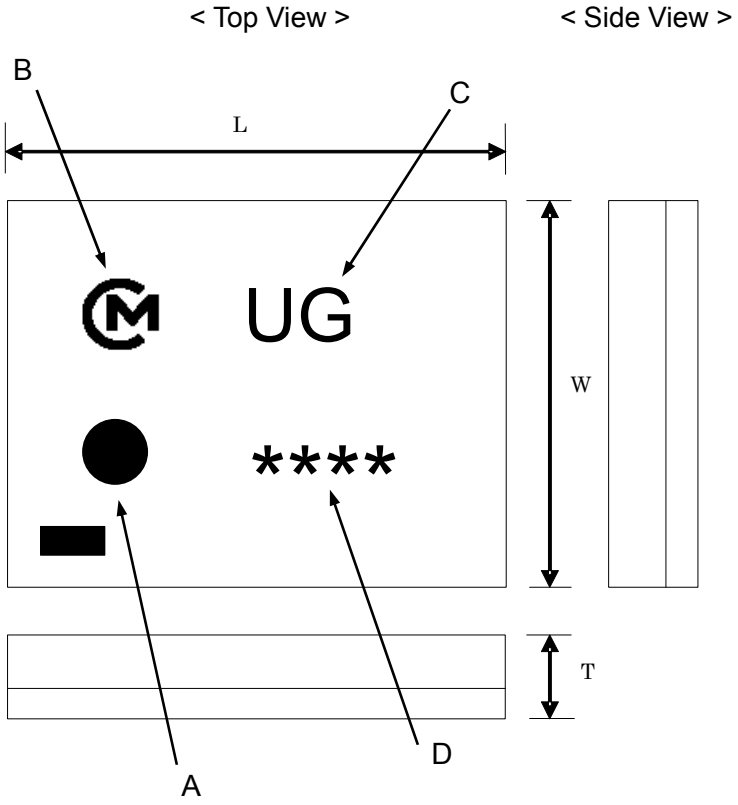
		min.	typ.	max.	Unit
Operating Temperature Range		-40	-	+85	deg.C
Specification Temperature Range		-20	+25	+70	deg.C
Supply Voltage	VDD_IN / MLDO_IN	2.2	3.6	4.8	V
	VDD_IO	1.7	1.8	1.9	V

[Note] All RF characteristics in this datasheet are defined by Specification Temperature Range

6. ROHS COMPLIANCE

This component can meet with RoHS compliance.

7. DIMENSIONS, MARKING AND TERMINAL CONFIGURATIONS



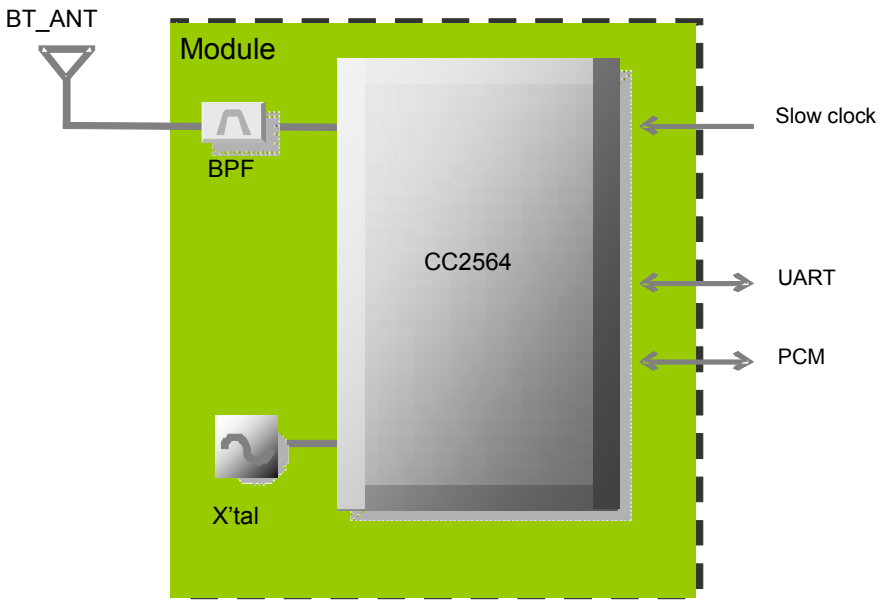
Dimensions (unit : mm)

Mark	Dimensions	Mark	Dimensions	Mark	Dimensions
L	5.8 +/- 0.2	W	4.8 +/- 0.2	T	1.0 (max.)

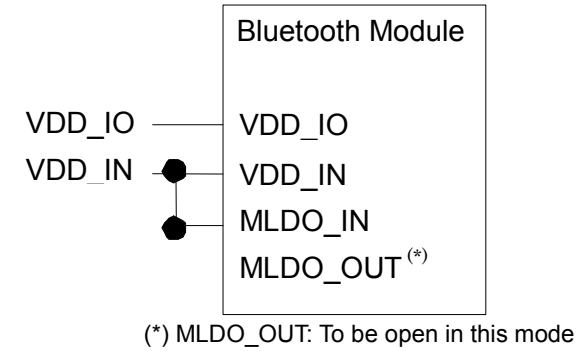
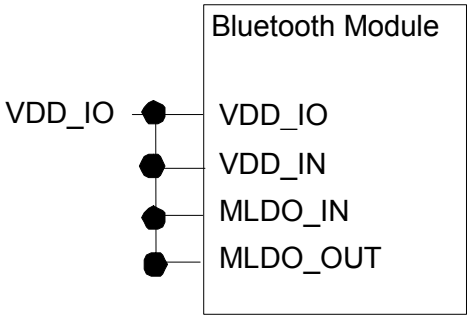
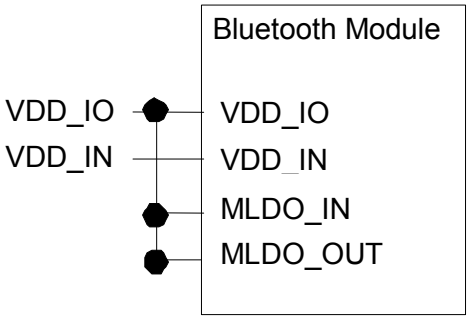
Marking	Meaning
A	Pin 1 Marking
B	Murata Logo
C	Module Type
D	Production Control Number

8. BLOCK DIAGRAM

Block Diagram



9. POWER SUPPLY OPTION

(a) Full VBAT power mode	 (*) MLDO_OUT: To be open in this mode VDD_IO:1.8V, VDD_IN:3.6V
(b) Full DCDC power mode	 VDD_IO:1.8V
(c) Mixed VBAT and DCDC mode	 VDD_IO:1.8V, VDD_IN: 3.6V

10. Slow Clock

Characteristics	Condition	Sym	Min	Typ	Max	Unit
Input slow clock frequency				32768		Hz
Input slow clock accuracy (Initial + temp + aging)					±250	ppm
Input transition time t_r/t_f – 10% to 90%		t_r/t_f			100	nsec
Frequency input duty cycle			15	50	85	%
Phase noise	At 1 kHz				-125	dBc/Hz
Jitter	Integrated over 300 to 15000 Hz				1	Hz
Slow clock input voltage limits	Square wave, DC coupled	V_{IH}			VDD_IO	V peak
		V_{IL}			0.35 x VDD_IO	V peak
Input impedance			1			MΩ
Input capacitance					5	pF

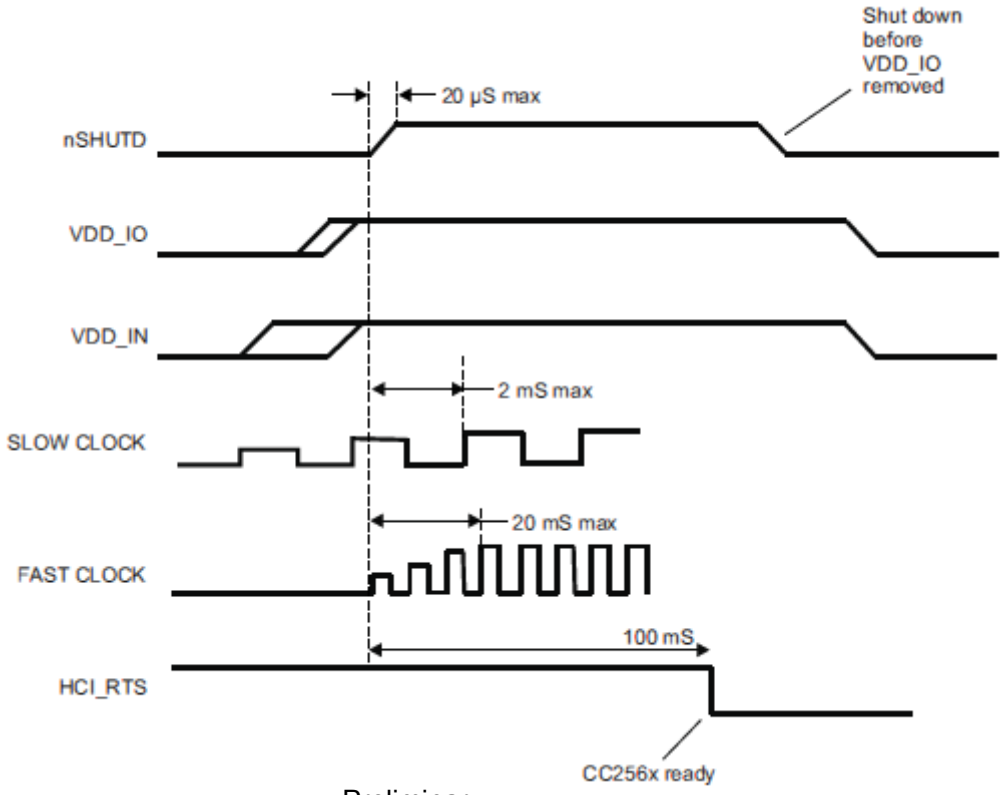
11. POWER-UP SEQUENCE

Power up requirements (see Figure11)

1. nSHUTD must be low. VDD_IN and VDD_IO are don't care when nSHUTD is low. However, no signals are SLOW_CLK_IN and AUD_xxx, which are fail-safe and can tolerate external voltages with no VDD_IO and VDD_IN.
2. VDD_IO and VDD_IN must be stable before releasing nSHUTD.
3. Fast clock must be stable maximum 20 ms after nSHUTD goes high.
4. Slow clock must be stable within 2 ms of nSHUTD going high.

The module indicates that the power-up sequence is complete by asserting RTS low. This occurs up to 100 ms after nSHUTD goes high.

Figure 11 Power-up sequence



12. HOST CONTROLLER INTERFACE

The module incorporates one UART dedicated to the HCI transport layer. The HCI interface transports commands, events, ACL, and synchronous data between the device and the host using HCI data packets.

The UART module supports H4 (4-wire) protocol with maximum baud rate of 4Mbps for all fast-clock frequencies.
After power up the baud rate is set for 115.2kbps, irrespective of fast clock frequency.
The baud rate can thereafter be changed with a vendor-specific command. The module responds with a Command Complete event (still at 115.2kbps), after which the baud rate change occurs.

HCI hardware includes the following features:
- Receiver detection of break, idle, framing, FIFO overflow, and parity error conditions
- Transmitter underflow detection
- CTS/RTS hardware flow control

Table12-1 shows the UART module default settings.

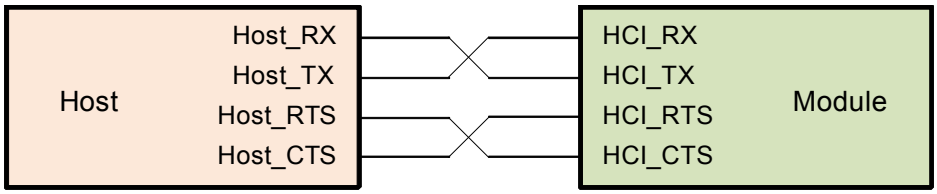
Table12-1 UART Default setting

Parameter	Value
Bit rate	115.2kbps
Data length	8 bits
Stop bit	1
Parity	None

12.1. UART 4-wire Interface – H4

The interface includes four signals: TX, RX, CTS, and RTS. Flow control between the host and the module is byte-wise by hardware.
Flow control is obtained as shown in Figure12-2.

Figure12-2 UART Interface Connection



When the UART RX buffer of the module passes the flow control threshold, it sets the UART_RTS signal high to stop transmission from the host.

When the UART_CTS signal is set high, the module stops its transmission on the interface. If HCI_CTS is set high in the middle of transmitting a byte, the module finishes transmitting the byte and stops the transmission.

12.2. Digital Codec Interface

The codec interface is a fully programmable port to support seamless interfacing with different PCM codec devices. The interface includes the following features:
- Two voice channels
- Master and slave modes
- All voice coding schemes defined by the Bluetooth specification – linear, A-Law, μ-Law
- Long and short frames

- Different data sizes, orders, and positions
- High-rate interface for EDR connection
- High flexibility to support variety of codecs
- Bus sharing – Data_Out is in high-Z mode when interface doesn't transmit voice data

BTIP Vendor Specific HCI Commands User's Guide (SWRU193) describes all configuration options.

12.2.1. Hardware Interface

The interface includes four signals:
- Clock – configurable direction (input or output)
- Frame_Sync/Word_Sync – configurable direction (input or output)
- Data_In – Input
- Data_Out – Output/3-state

The module can be either the master of the interface where it generates the clock and the frame-sync signals, or the slave where it receives these two signals.

For slave mode, clock input frequencies of up to 16MHz are supported. At clock rate above 12MHz, the maximum data burst size is 32bits.

For master mode, the module can generate any clock frequency between 64kHz and 6MHz.

12.2.2. Data Format

The data format is fully configurable:
- The data length can be from 8 to 320bits, in 1-bit increments, when working with 2 channels, or up to 640bits when using 1 channel. The data length can be set independently for each channel.
- The data position within a frame is also configurable in with 1 clock (bit) resolution and can be set independently(relative to the edge of the Frame_Sync signal) for each channel.
- The Data_In and Data_Out bit order can be configured independently. For examples; Data_In can start with the MSB while Data_Out starts with LSB. Each channel is separately configurable. The inverse bit order (that is, LSB first) is supported only for sample size up to 24bits.
- It is not necessary for the size of the Data_In and Data_Out to be the same length.
- The Data_Out line if configured to high-Z output between data worodsl Data_Out can also be set for permanent. At power up, Data_Out is configured as high-Z.

12.2.3. Frame Idle Period

The codec interface has the capability for frame idle periods, where the clock can "take a break" and become 0 at the end of the frame, after all data are transferred.

The module is the master of the interface, the frame idle period is configurable. There are two configurable parameters:
- Clk_Idle_Start – Indicates the number of clock cycles from the beginning of the frame until the beginning of the idle period. After Clk_Idle_Start clock cycles, the clock becomes 0.
- Clk_Idle_End – Indicates the time from the beginning of the frame till the end of the idle period. This time is given in multiples of clock periods.

The delta between Clk_Idle_Start and Clk_Idle_End is the clock idle period.

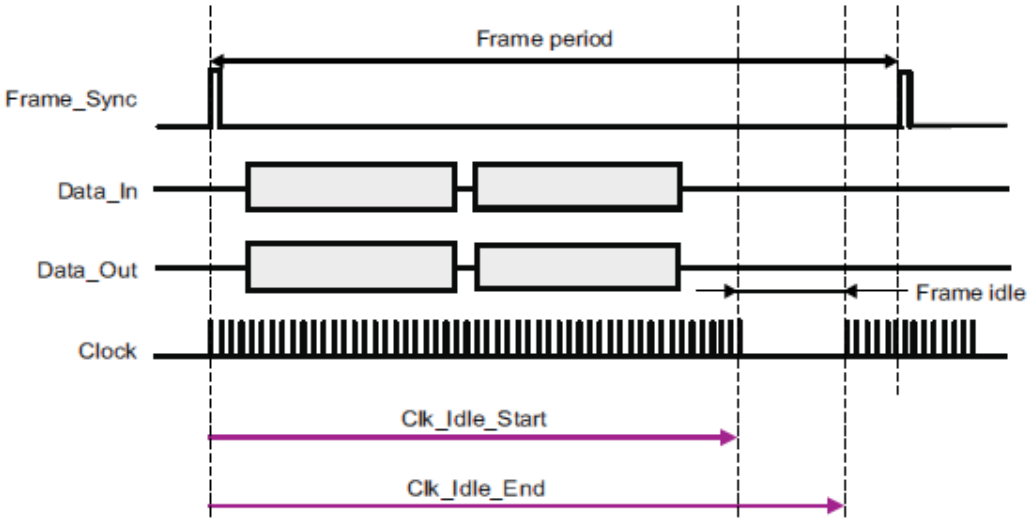
For example, for clock rate = 1MHz, frame sync period = 10kHz, Clk_Idle_Start = 60, Clk_Idle_End = 90.

Between both frame-sync signals there are 70 clock cycles (instead of 100). The clock idle period starts 60 clock cycles after the beginning of the frame, and lasts 90 – 60 = 30 clock cycles. This means that

the idle period ends 100 – 90 = 10 clock cycles before the end of the frame. The data transmission must end before the beginning of the idle period.

Figure12-3 shows the frame idle timing.

Figure12-3 PCM Interface



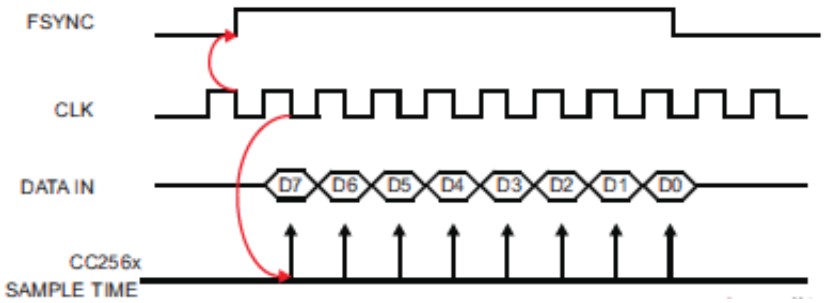
12.2.4. Clock-Edge Operation

The codec interface of the module can work on the rising or the falling edge of the clock. It can also sample the frame-sync signal and the data at inversed polarity.

Figure12-4 shows the operation of a falling-edge-clock type of codec. The codec is the master of the bus.

The frame-sync signal is updated (by the codec) on the falling edge of the clock and is therefore sampled (by the module) on the next rising clock. The data from the codec is sampled (by the module) on the edge of the clock.

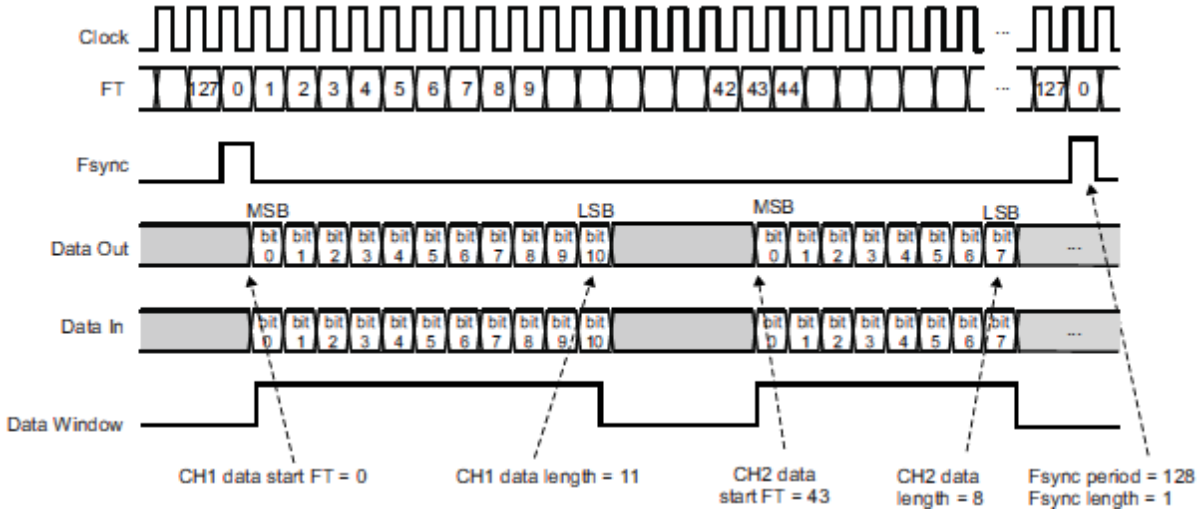
Figure12-4 Clock-Edge Operation



12.2.5. Two-Channel Bus Example

In Figure12-5, a 2-channel bus is shown where the two channels have different word sizes and arbitrary positions in the bus frame. (FT stands for frame timer)

Figure12-5 Two-Channel Bus



12.2.6. Improved Algorithm For Lost Packets

The module features an improved algorithm for improving voice quality when received voice data packets are lost. There are two options:

- Repeat the last sample – possible only for sample sizes up to 24bits. For sample sizes larger than 24bits, the last byte is repeated.
- Repeat a configurable sample of 8 to 24bits (depending on the real sample size) to simulate silence (or anything else) in the bus. The configured samples are written in a specific register for each channel.

The choice between those two options is configurable separately for each channel.

12.2.7. Bluetooth/Codec Clock Mismatch Handling

In Bluetooth RX, the module receives RF voice packets and writes them to the codec interface. If the module receives data faster than the codec interface output allows, an overflow occurs. In this case, the Bluetooth has two possible behavior modes:

- Allow overflow: If overflow is allowed, the Bluetooth continues receiving data and overwrites any data not yet to the codec.
- Don't allow overflow: If overflow is not allowed, RF voice packets received when the buffer is full are discarded.

13. DC/RF CHARACTERISTICS FOR BLUETOOTH (BD/EDR)

25deg.C, VDD_IN=3.6V, VDD_IO_1.8V unless otherwise specified.

Items	Contents			
Bluetooth specification	Ver 4.0			
Channel spacing	1MHz			
Number of RF channel	79			
Power class	1			
Operation mode (Rx/Tx)	Time division multiplex either transmit or receive Frequency hopping after one Rx/Tx cycle			
- DC Characteristics -	min.	typ.	max.	Unit
1. DC Current				
1) DH1 Packet 50% Rx/Tx slot duty cycle	-	52	65	mA
2) DH3 Packet 50% Rx/Tx slot duty cycle	-	56	75	mA
3) DH5 Packet 50% Rx/Tx slot duty cycle	-	58	75	mA
- TX characteristics -	min.	typ.	max.	unit
2. Output Power	5	8.5	12	dBm
3. Power Control Step	2	-	8	dB
4. Frequency range (Rx/Tx)	2402 – 2480MHz			
5. -20dB bandwidth	-	0.92	1	MHz
6. Adjacent Channel Power *1				
5.1 [M-N] = 2	-	-45	-20	dBm
5.2 [M-N] ≧ 3	-	-45	-40	dBm
7. Modulation characteristics				
6.1 Modulation δf1avg	140	159	175	kHz
6.2 Modulation δf2max	115	130	-	kHz
6.3 Modulation δf2avg/δf1avg	0.8	0.9	-	-
8. Initial Carrier Frequency Tolerance	-75	-	+75	kHz
9. Carrier Frequency Drift				
8.1 1slot	-25	-	+25	kHz
8.2 3slot	-40	-	+40	kHz
8.3 5slot	-40	-	+40	kHz
8.4 Maximum drift rate	-20	-	+20	kHz/50μs
10. Out-of-Band Spurious Emissions				
9.1 30-1000MHz (Operation Mode)	-	-	-36	dBm
9.2 1000-12750MHz (Operation Mode)	-	-	-30	dBm
11. EDR Relative Power (DQPSK / 8DPSK)	-4	-	1	dBm
12. EDR Carrier Frequency Stability and Modulation Accuracy				
12.1 ω_i (DQPSK and 8DPSK)	-75	-	75	kHz
12.2 $\omega_i+\omega_0$ (DQPSK and 8DPSK)	-75	-	75	kHz
12.3 ω_o (DQPSK and 8DPSK)	-10	-	10	kHz
12.4 RMS DEVM (DQPSK)	-	0.045	0.20	-
12.5 99% DEVM (DQPSK)	-	0.10	0.30	-
12.6 Peak DEVM (DQPSK)	-	0.12	0.35	-
12.7 RMS DEVM (8DPSK)	-	0.045	0.13	-
12.8 99% DEVM (8DPSK)	-	0.10	0.20	-
12.9 Peak DEVM (8DPSK)	-	0.12	0.25	-
13. EDR Differential Phase Encoding (PER / DQPSK and 8DPSK)	-	0	1	%
14. EDR In-band Spurious Emission				
14.1 |M-N|=1 ($P_{TX-26dB}$) (DQPSK and 8DPSK)	-	-	-26	dB
14.2 |M-N|=2 (DQPSK and 8DPSK)	-	-	-20	dBm

14.3 |M-N|≥3 (DQPSK and 8DPSK)	-	-	-40	dBm
- RX characteristics -	min	typ	max	unit
15. Sensitivity (BER ≤ 0.1%)				
15.1 2402MHz	-	-91	-70	dBm
15.2 2441MHz	-	-91	-70	dBm
15.3 2480MHz	-	-91	-70	dBm
16. C/I Performance (BER ≤ 0.1%) *2				
16.1 co-channel ratio (-60dBm input)	-	7	11	dB
16.2 1MHz ratio (-60dBm input)	-	-10	0	dB
16.3 2MHz ratio (-60dBm input)	-	-46	-30	dB
16.4 3MHz ratio (-67dBm input)	-	-48	-40	dB
16.5 image +/- 1MHz ratio (-67dBm input)	-	-30	-20	dB
17. Blocking performance (BER ≤ 0.1%) *3				
17.1 30MHz-2000MHz	-10	-	-	dBm
17.2 2000MHz-2400MHz	-27	-	-	dBm
17.3 2500MHz-3000MHz	-27	-	-	dBm
17.4 3000MHz-12750MHz	-10	-	-	dBm
18. Intermodulation performance (BER ≤ 0.1%, -64dBm input)	-39	-30	-	dBm
19. Maximum Input Level	-20	-	-	dBm
20. EDR Sensitivity ($BER \leq 7x10^{-5}$ or $BER \leq 10^{-4}$)				
20.1 2402MHz (DQPSK)	-	-91	-70	dBm
20.2 2402MHz (8DPSK)		-84	-70	dBm
20.3 2441MHz (DQPSK)	-	-91	-70	dBm
20.4 2441MHz (8DPSK)		-84	-70	dBm
20.5 2480MHz (DQPSK)	-	-91	-70	dBm
20.6 2480MHz (8DPSK)		-84	-70	dBm
21. EDR BER Floor Performance ($BER \leq 7x10^{-6}$ or $BER \leq 10^{-5}$)				
21.1 2402MHz (DQPSK and 8DPSK)	-	-	-60	dBm
21.2 2441MHz (DQPSK and 8DPSK)	-	-	-60	dBm
21.3 2480MHz (DQPSK and 8DPSK)	-	-	-60	dBm
22. EDR C/I Performance (DQPSK)				
22.1 co-channel ratio (-60dBm input)	-	9	13	dB
22.2 1MHz ratio (-60dBm input)	-	-13	0	dB
22.3 2MHz ratio (-60dBm input)	-	-48	-30	dB
22.4 3MHz ratio (-67dBm input)	-	-50	-40	dB
22.5 image +/-1MHz ratio (-67dBm input)	-	-30	-20	dB
23. EDR C/I Performance (8DPSK)				
23.1 co-channel ratio (-60dBm input)	-	15	21	dB
23.2 1MHz ratio (-60dBm input)	-	-7	5	dB
23.3 2MHz ratio (-60dBm input)	-	-41	-25	dB
23.4 3MHz ratio (-67dBm input)	-	-45	-33	dB
23.5 image +/-1MHz ratio (-67dBm input)	-	-23	-13	dB
24. EDR Maximum Input Level ($BER \leq 10^{-3}$) (DQPSK and 8DPSK)	-20	-	-	dBm

*1 Up to three spurious responses within Bluetooth limits are allowed.
*2 Up to five spurious responses within Bluetooth limits are allowed.
*3 Up to twenty-four spurious responses within Bluetooth limits are allowed.

14. DC/RF CHARACTERISTICS FOR BLUETOOTH (LE)

25deg.C, VDD_IN=3.6V, VDD_IO_1.8V unless otherwise specified.

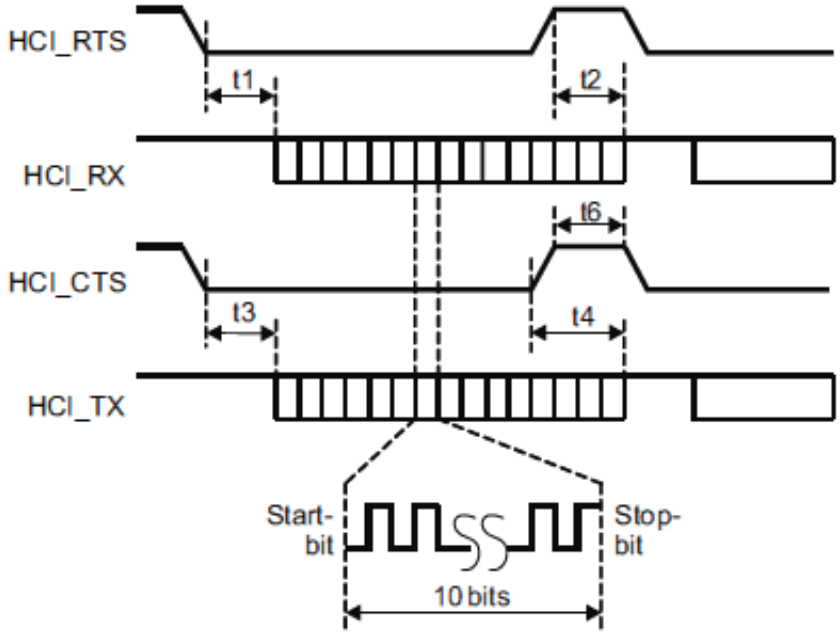
Item / Conditions	Spec.			Unit
	MIN	TYP	MAX	
Center frequency	2402	-	2480	MHz
Channel Spacing	-	2	-	MHz
Number of RF Channels	-	40	-	-
Output power	-4	0	+4	dBm
Modulation characteristics				
1) $\Delta f1_{avg}$	225	-	275	kHz
2) $\Delta f2_{max}$ (at 99.9%)	185	-	-	kHz
3) $\Delta f2_{avg} / \Delta f1_{avg}$	0.8	-	-	-
Carrier frequency offset and drift				
1) Frequency offset: $\lvert f_n - f_{TX} \rvert$	-	-	150	kHz
2) Frequency drift: $\lvert f_0 - f_n \rvert$	-	-	50	kHz
3) Drift rate #0: $\lvert f_1 - f_0 \rvert$	-	-	20	kHz
4) Drift rate #n: $\lvert f_n - f_{n-5} \rvert$	-	-	20	kHz
Receiver sensitivity (PER < 30.8%)	-	-	-70	dBm
Maximum input signal level (PER < 30.8%)	-10	-	-	dBm
PER Report Integrity (-30dBm input)	50	-	65.4	%

15. INTERFACE SPECIFICATIONS

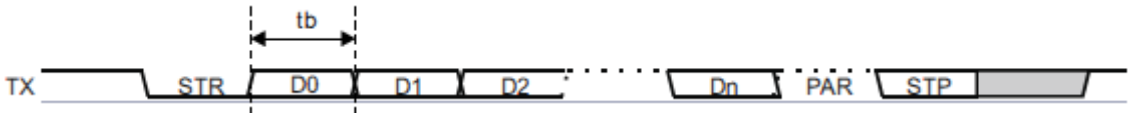
15.1. UART

Figure15-1 shows the UART timing diagram.

Figure15-1 UART Timing Diagram



Symbol	Characteristics	Condition	Min	Typ	Max	Unit
	Baud rate		37.5		4000	kbps
	Baud rate accuracy		-2.5		1.5	%
t3	CTS low to TX_DATA on		0	2		μ sec
t4	CTS high to TX_DATA off	Hardware flow control			1	byte
t6	CTS high pulse width		1			bit
t1	RTS low to RX_DATA on		0	2		μ sec
t2	RTS high to RX_DATA off	Interrupt set to 1/4 FIFO			16	byte

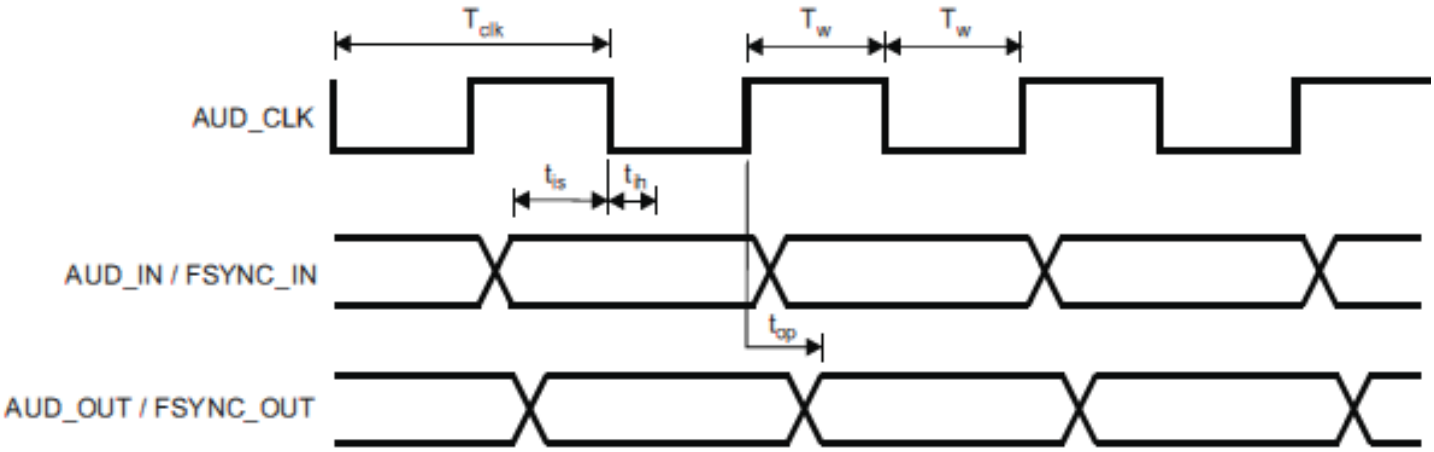


Symbol	Description
STR	Start bit
D0…Dn	Data bit (LSB first)
PAR	Parity bit (optional)
STP	Stop bit

15.2. PCM

Figure15-2 shows the PCM timing diagram.

Figure15-2 PCM Timing Diagram



PCM Master

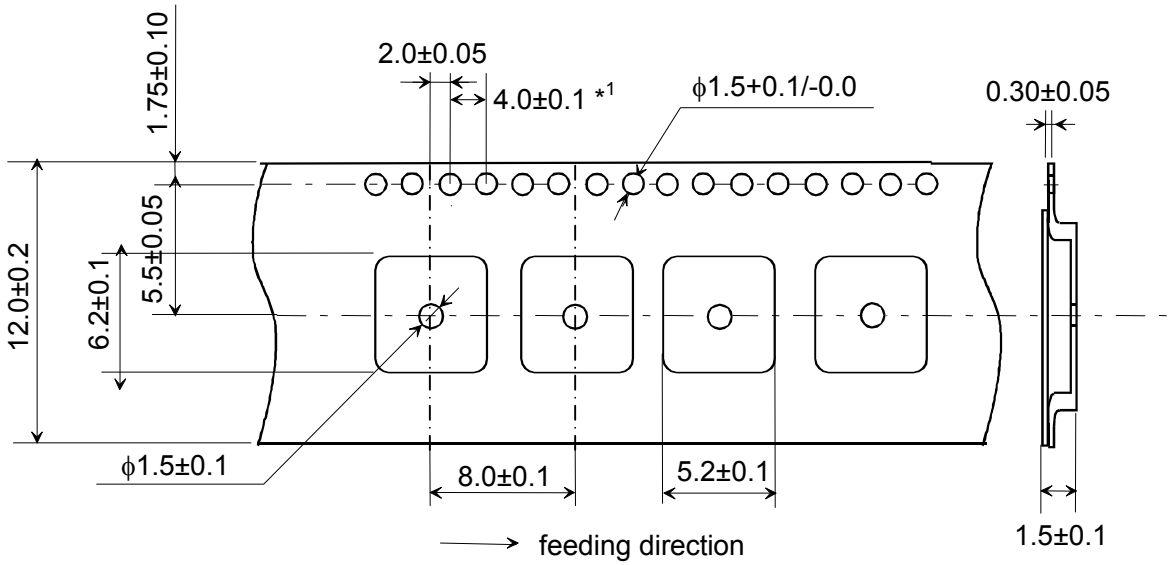
Symbol	Parameter	Condition	Min	Max	Unit
T_{clk}	Cycle time		166.67 (6MHz)	15625 (64kHz)	nsec
T_w	High or low pulse width		50% of T_{clk} min		
t_{is}	AUD_IN setup time		25		
t_{ih}	AUD_IN hold time		0		
t_{op}	AUD_OUT propagation time	40pF load	0	10	
t_{op}	FSYNC_OUT propagation time	40pF load	0	10	

PCM Slave

Symbol	Parameter	Condition	Min	Max	Unit
T_{clk}	Cycle time		62.5 (16MHz)		nsec
T_w	High or low pulse width		40% of T_{clk}		
T_{is}	AUD_IN setup time		8		
T_{ih}	AUD_IN hold time		0		
t_{is}	AUD_FSYNC setup time		8		
t_{ih}	AUD_FSYNC hold time		0		
t_{op}	AUD_OUT propagation time	40pF load	0	21	

16. TAPE AND REEL PACKING

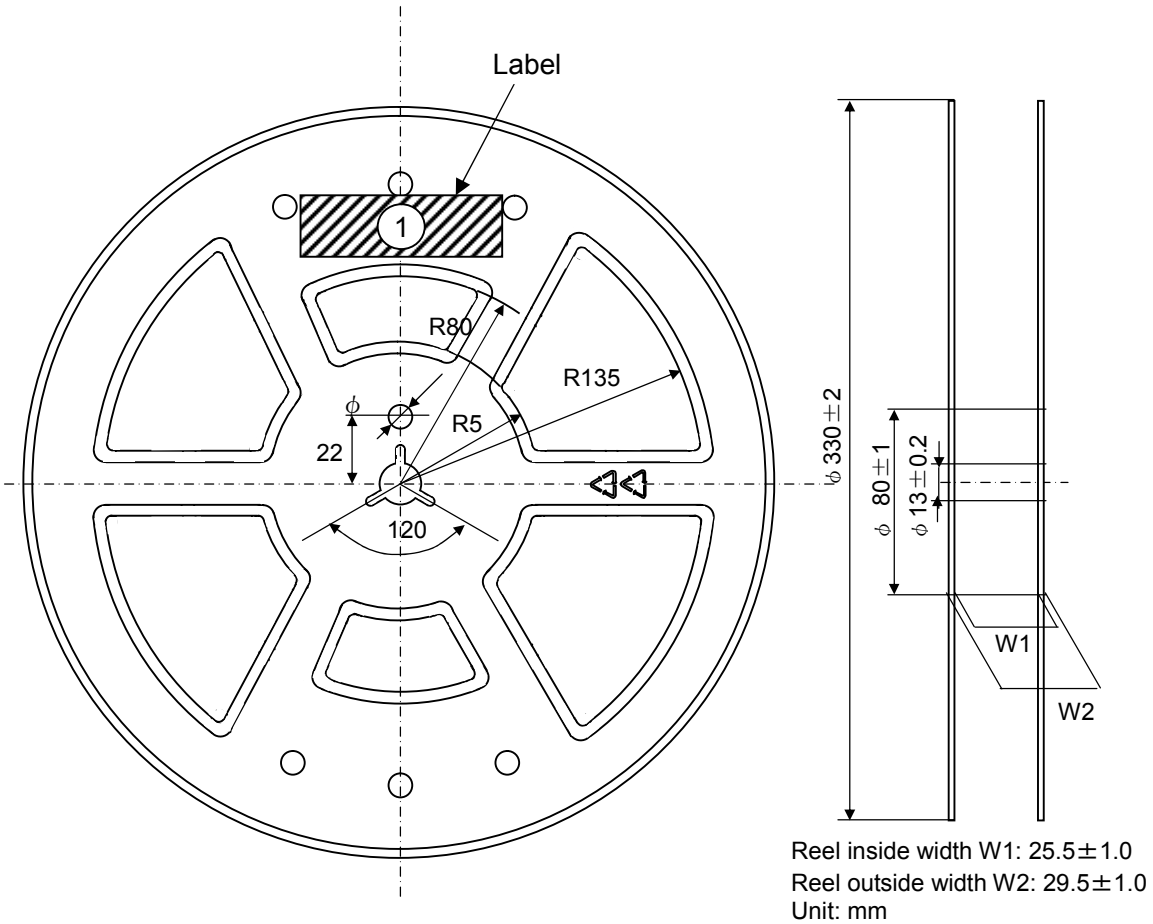
(1) Dimensions of Tape (Plastic tape)



*1 Cumulative tolerance of max. ± 0.15 every 10 pitches

(unit : mm)

(2) Dimensions of Reel



Reel inside width W1: 25.5±1.0
Reel outside width W2: 29.5±1.0
Unit: mm

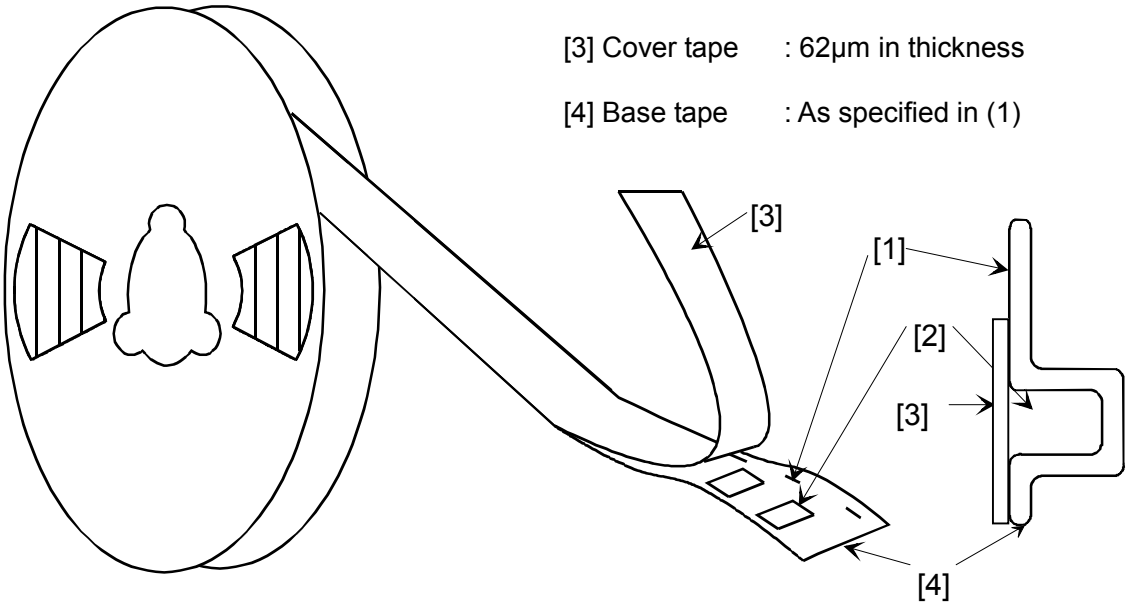
(3) Taping Diagrams

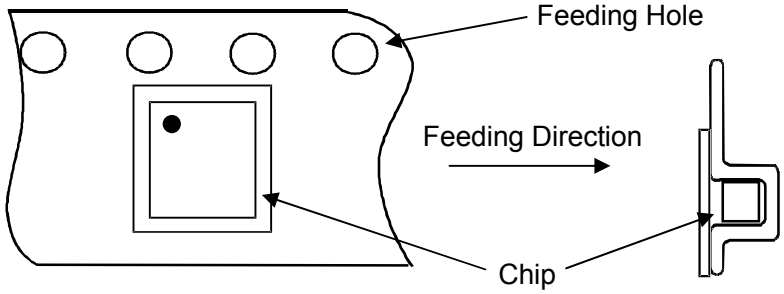
[1] Feeding Hole : As specified in (1)

[2] Hole for chip : As specified in (1)

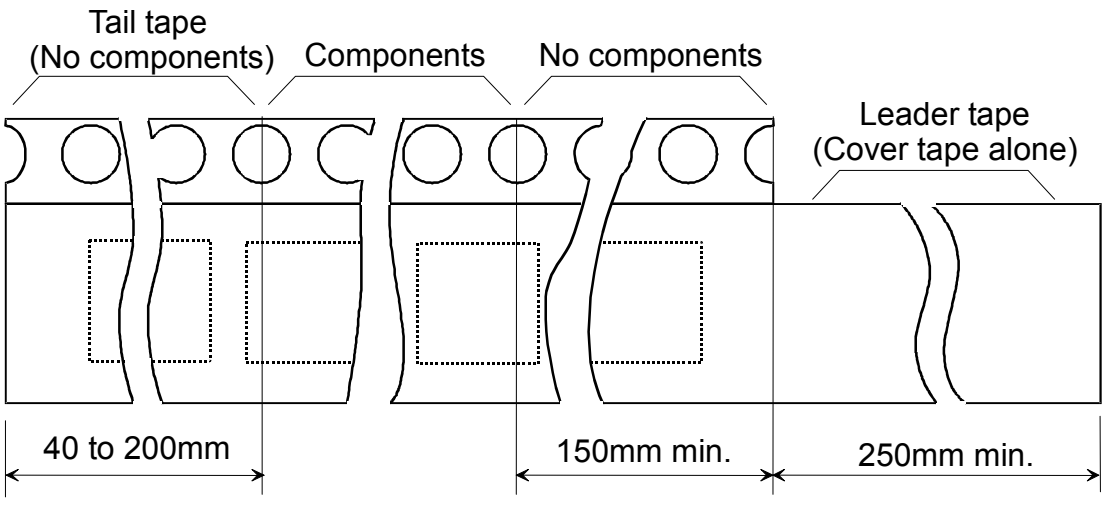
[3] Cover tape : 62μm in thickness

[4] Base tape : As specified in (1)





(4) Leader and Tail tape



Feeding direction

(5) The tape for chips are wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.

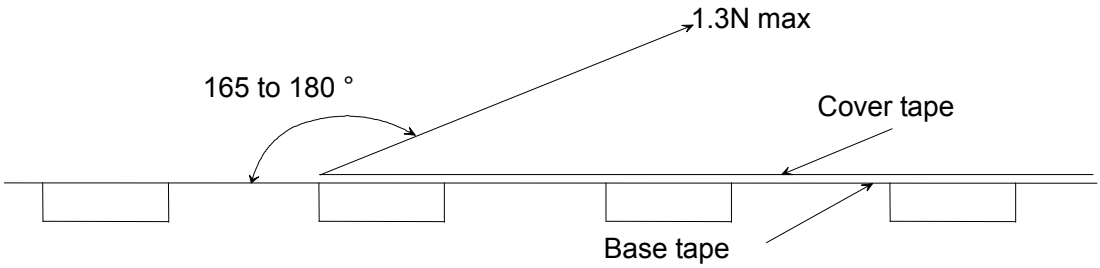
(6) The cover tape and base tape are not adhered at no components area for 250mm min.

(7) Tear off strength against pulling of cover tape : 5N min.

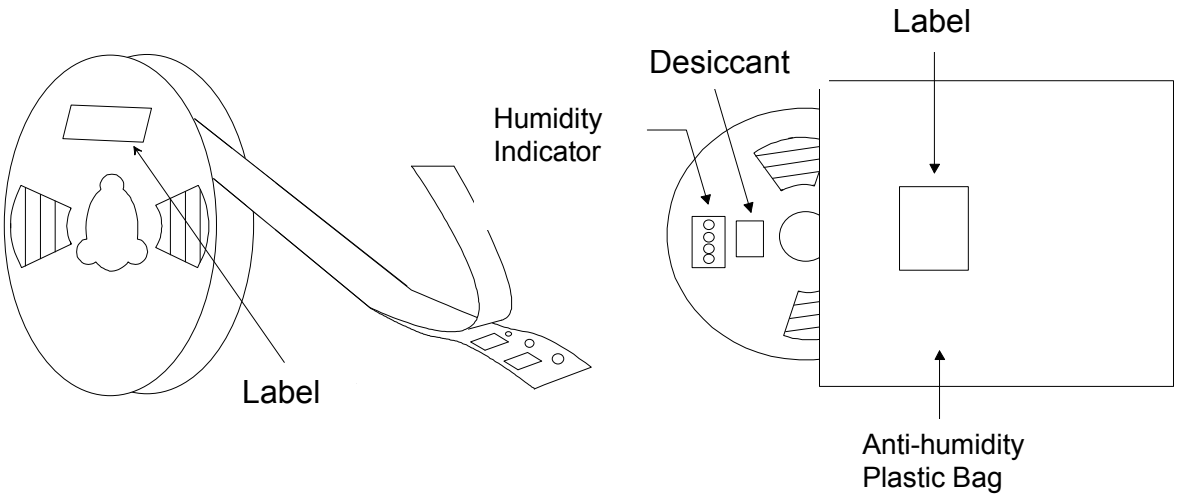
(8) Packaging unit : 1000pcs./ reel

(9) material : Base tape : Plastic
Real : Plastic
Cover tape, cavity tape and reel are made the anti-static processing.

(10) Peeling of force : in the direction of peeling as shown below.
Peeling speed : 300mm/min ±10mm/min



(11) Packaging (Humidity proof Packing)



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

17. NOTICE

17.1. Storage Conditions:

Please use this product within 6month after receipt.
- The product shall be stored without opening the packing under the ambient temperature from 5 to 35deg.C and humidity from 20 to 70%RH.
(Packing materials, in particular, may be deformed at the temperature over 40deg.C.)
- The product left more than 6months after reception, it needs to be confirmed the solderbility before used.
- The product shall be stored in non corrosive gas (Cl_2, NH_3, SO_2, No_x, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.

This product is applicable to MSL3 (Based on JEDEC Standard J-STD-020)
- After the packing opened, the product shall be stored at ≦30deg.C / ≦60%RH and the product shall be used within 168hours.
- When the color of the indicator in the packing changed, the product shall be baked before soldering.

Baking condition: 125+5/-0deg.C, 24hours, 1time

The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

17.2. Handling Conditions:

Be careful in handling or transporting products because excessive stress or mechanical shock may break products.

Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bear hands that may result in poor solder ability and destroy by static electrical charge.

17.3. Standard PCB Design (Land Pattern and Dimensions):

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

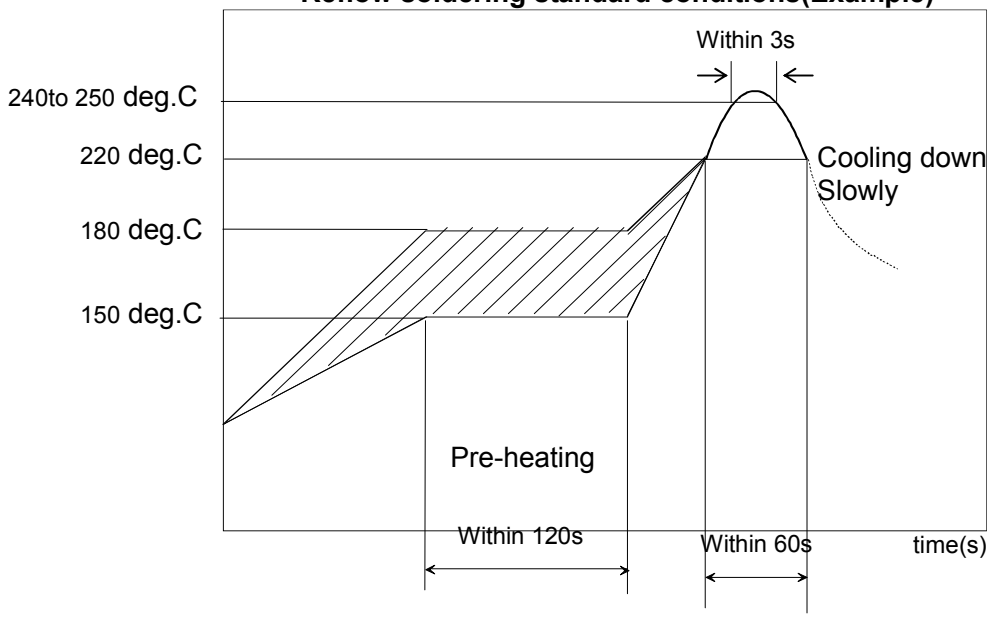
17.4. Notice for Chip Placer:

When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

17.5. Soldering Conditions:

The recommendation conditions of soldering are as in the following figure.
When products are immersed in solvent after mounting, pay special attention to maintain the temperature difference within 100 °C. Soldering must be carried out by the above mentioned conditions to prevent products from damage. Contact Murata before use if concerning other soldering conditions.

Reflow soldering standard conditions(Example)



Please use the reflow within 2 times.
Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt % or less.

17.6. Cleaning:

Since this Product is Moisture Sensitive, any cleaning is not permitted.

17.7. Operational Environment Conditions:

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl_2, NH_3, SO_x, NO_x etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

As it might be a cause of degradation or destruction to apply static electricity to products, do not apply static electricity or excessive voltage while assembling and measuring.

17.8. Input Power Capacity:

Products shall be used in the input power capacity as specified in this specifications.
Inform Murata beforehand, in case that the components are used beyond such input power capacity range.

18. PRECONDITION TO USE OUR PRODUCTS

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.
All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.
Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.
WE HEREBY DISCLAIMS ALL OTHER WARRANTIES REGARDING THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION ANY WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, THAT THEY ARE DEFECT-FREE, OR AGAINST INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS.
The product shall not be used in any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property. You acknowledge and agree that, if you use our products in such applications, we will not be responsible for any failure to meet such requirements. Furthermore, YOU AGREE TO INDEMNIFY AND DEFEND US AND OUR AFFILIATES AGAINST ALL CLAIMS, DAMAGES, COSTS, AND EXPENSES THAT MAY BE INCURRED, INCLUDING WITHOUT LIMITATION, ATTORNEY FEES AND COSTS, DUE TO THE USE OF OUR PRODUCTS IN SUCH APPLICATIONS.

- Aircraft equipment. - Aerospace equipment - Undersea equipment.
- Power plant control equipment - Medical equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Traffic signal equipment. - Disaster prevention / crime prevention equipment.
- Burning / explosion control equipment
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.

We expressly prohibit you from analyzing, breaking, reverse-engineering, remodeling altering, and reproducing our product. Our product cannot be used for the product which is prohibited from being manufactured, used, and sold by the regulations and laws in the world.
We do not warrant or represent that any license, either express or implied, is granted under any our patent right, copyright, mask work right, or our other intellectual property right relating to any combination, machine, or process in which our products or services are used. Information provided by us regarding third-party products or services does not constitute a license from us to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from us under our patents or other intellectual property.
Please do not use our products, our technical information and other data provided by us for the purpose of developing of mass-destruction weapons and the purpose of military use.
Moreover, you must comply with "foreign exchange and foreign trade law", the "U.S. export administration regulations", etc.
Please note that we may discontinue the manufacture of our products, due to reasons such as end of supply of materials and/or components from our suppliers.
By signing on specification sheet or approval sheet, you acknowledge that you are the legal representative for your company and that you understand and accept the validity of the contents herein. When you are not able to return the signed version of specification sheet or approval sheet within 30 days from receiving date of specification sheet or approval sheet, it shall be deemed to be your consent on the content of specification sheet or approval sheet. Customer acknowledges that engineering samples may deviate from specifications and may contain defects due to their development status. We reject any liability or product warranty for engineering samples. In particular we disclaim liability for damages caused by

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- deviation or lapse in function of engineering sample,
- improper use of engineering samples.

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