Internal FET Abnormality Detection Function

High Efficiency / Low Standby Power 2-Channel Secondary Side Synchronous Rectification Control IC

BD85506F

General Description

BD85506F is a 2-channel secondary side Synchronous Rectification (SR) controller for LLC with enhanced abnormality detection function on the secondary side.
This IC has a function to detect FET abnormalities such as body diode rectification operation.
In addition, it incorporates a high-accuracy overvoltage detection circuit, contributing to improved safety and reduction of external components.
For efficiency, the OFF threshold voltage of the synchronous rectifier FET can be adjusted with a resistor.
Moreover, by providing the Source monitor pin of each FET, it is possible to monitor the voltage between Drain and Source, and further improvement in efficiency is possible.
In the burst operation at light load of the primary side controller, the synchronous rectification operation is automatically placed in the standby state, suppressing the switching power and the circuit current of the IC itself and reducing standby power consumption.
The built-in multipurpose comparator can also be used as a low consumption shunt regulator in addition to the abnormality detection comparator.
The operating power supply voltage ranges from 5.0 V to 32 V, covering various output voltage lineups.
Additionally, by adopting a process with a high withstand voltage of 120 V(Max), it is possible to directly monitor the Drain voltage.

Features

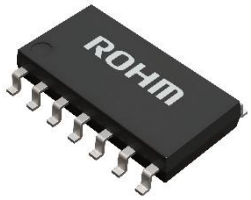
- Internal FET Abnormality Detection Function for Secondary Side Synchronous Rectification.
- Internal Overvoltage Detection Circuit (OVP). (Externally adjustable, high accuracy: 2 %)
- Efficiency Improvement by FET OFF Threshold Voltage is Adjustable.
- Source of each FET can be individually monitored.
- Internal Standby Mode Automatic Determination Function.
- Internal Multipurpose Comparator. (It can also be used as a shunt regulator)
- With the Slow Start Function, it is possible to set the FET Abnormality Detection Function at startup and the during the start of Switching Operation
- Wide Input Voltage Range 5.0 V to 32 V
- D1, D2 Pin 120 V (Max) Breakdown Voltage
- Flow Compatible SOP14 Package

Key Specifications

- Input Voltage Range: 5.0 V to 32 V
- Operating Circuit Current (SW Stopped Mode): 800 µA(Typ)
- Standby Circuit Current: 300 µA(Typ)
- Drain Monitor Pin Absolute Voltage: 120 V(Max)
- Operating Temperature Range: -40 °C to +105 °C

Package

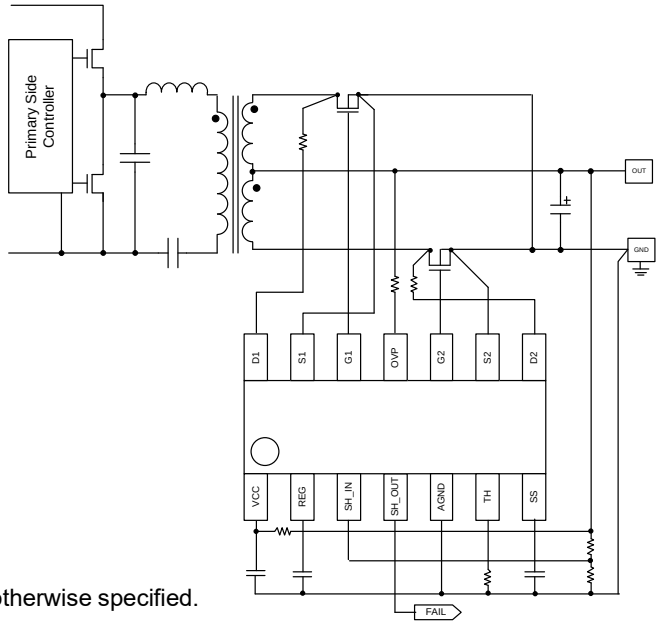
Package	W(Typ) x D(Typ) x H(Max)
SOP14	8.70 mm x 6.20 mm x 1.71 mm



Applications

Isolated LLC Type AC/DC Power Supply.
Adapter, TV, Printer, Office Equipment, etc.

Typical Application Circuits



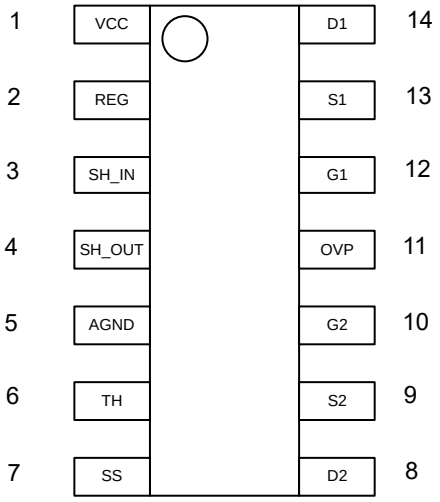
(Remark) The values in the datasheet are typical unless otherwise specified.

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Pin Configuration

(TOP VIEW)



Pin Configuration

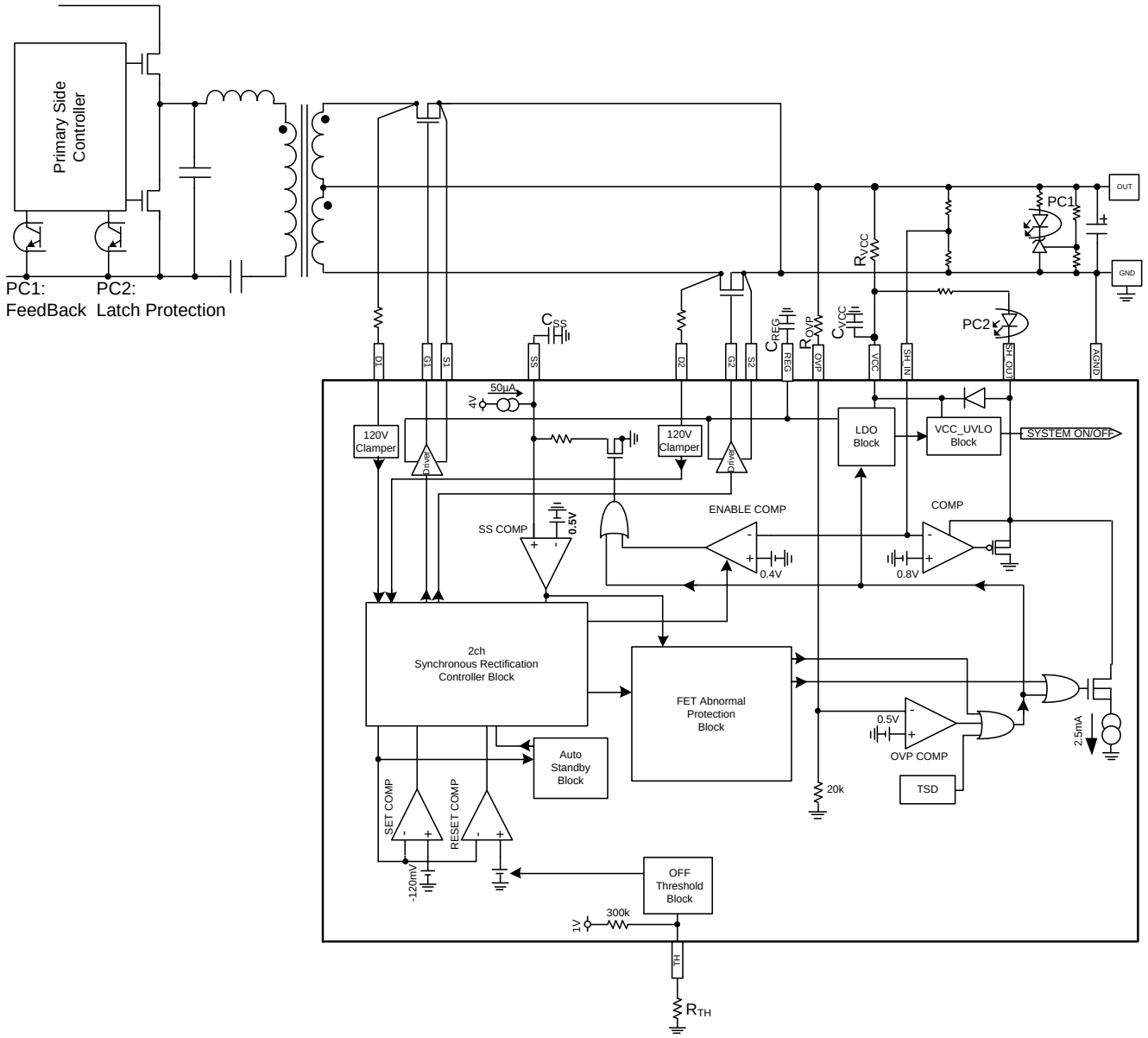
Pin Descriptions

Pin No.	Pin Name	Function
1	VCC	Power supply input pin
2	REG	Regulator output pin for driver
3	SH_IN	Multi-purpose comparator input pin/ENABLE input pin
4	SH_OUT	Multi-purpose comparator output pin/FAIL output pin when abnormality is detected
5	AGND	Analog GND
6	TH	FET OFF Threshold setting pin
7	SS	Mask time setting pin of drive and FET abnormality detection function at start up.
8	D2	Channel 2 Drain signal input pin
9	S2	Channel 2 Source signal input pin
10	G2	Channel 2 Gate drive signal output pin
11	OVP	Overvoltage detection setting pin
12	G1	Channel 1 Gate drive signal output pin
13	S1	Channel 1 Source signal input pin
14	D1	Channel 1 Drain signal input pin

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Block Diagram



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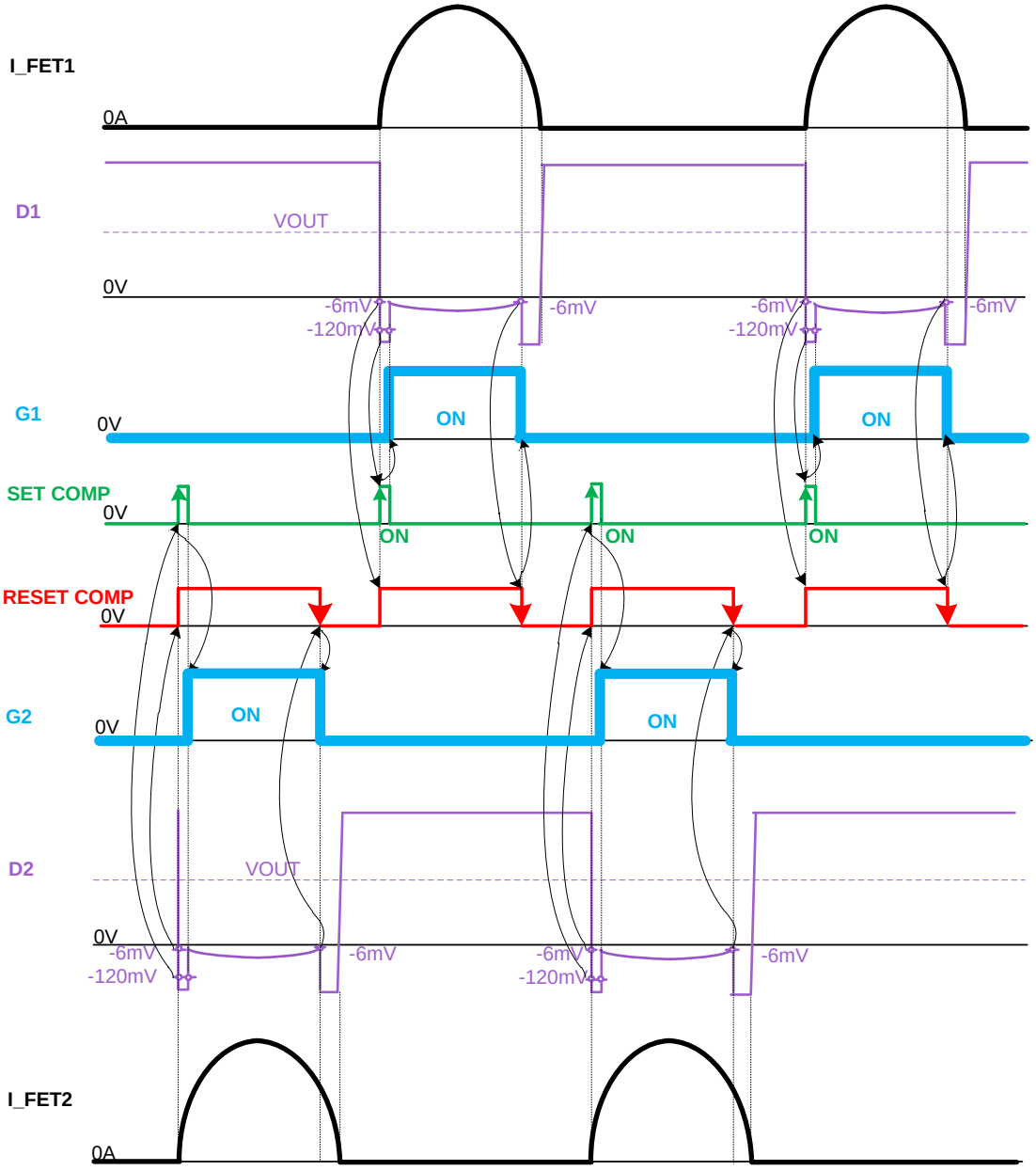
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Description of Blocks

1. SET COMP Block
Monitors D1 and D2 pin voltages and outputs a signal to turn ON the FET by detecting -120 mV or less.

2. RESET COMP Block
Monitors D1 and D2 pin voltages and outputs a signal to turn OFF the FET by detecting a voltage greater than the set voltage at the TH pin.

3. OFF Threshold Block
Sets the D1 and D2 voltages to turn OFF the FET by setting the TH pin resistance. (D1 and D2 become the same setting)
The ON/OFF sequence of secondary side synchronous rectification is shown below. (Shown in the example below is for setting the TH pin to 200 kΩ, -6 mV setting)



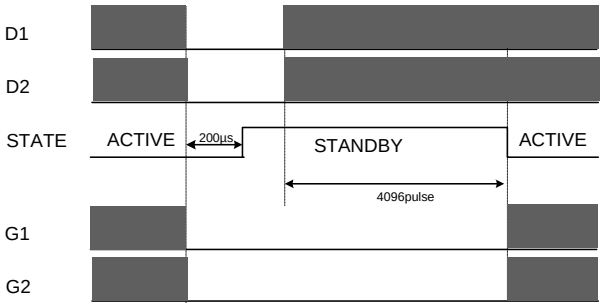
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Description of Blocks – continued

4. Auto Standby Block

By detecting the presence or absence of the D1 and D2 pin pulses, the synchronous rectification operation is automatically operated or stopped, respectively. If a pulse is not detected on the D1 and D2 pins within 200 µs, the chip enters its standby state and the synchronous rectification operation is stopped. After a total of 4096 pulses is detected on the D1 and D2 pins, the chip becomes active and resumes the synchronous rectification action.



5.COMP Block

This is a multipurpose comparator. It can be used as a comparator in various voltage detection applications such as set temperature monitoring and voltage monitoring. It can also be used as a low-consumption shunt regulator via feedback operation.

6. ENABLE COMP Block

This comparator is for turning ON or OFF the synchronous rectification. When the SH_IN pin goes below or equal to 0.4 V, the SS pin capacitor is discharged and the synchronous rectification operation, G pin OPEN detection, and D pin OPEN detection functions are also stopped.

7. OVP Block

This is the overvoltage detection block for the output voltage. Since the lower 20 kΩ resistor is built-in, the detection voltage can be adjusted by connecting a resistor between the detection node and the OVP pin. After OVP is detected, a FAIL signal (constant current sink of 2.5 mA) is output from the SH_OUT pin. When the OVP release voltage is reached or when VCC_UVLO is detected, the constant current sink from SH_OUT is stopped.

8. LDO Block

This is the IC internal power supply generation block. The driver power supply is output at the REG pin, and stable operation is obtained by connecting a ceramic capacitor on its output.

9. SS COMP Block

Slow start block that sets the operation start time for startup, synchronous rectification, G pin OPEN detection, and D pin OPEN detection functions. When VCC UVLO has been cancelled, a constant current of 50µA is output from the SS pin and its capacitor is charged. When the SS pin voltage reaches at least 0.5V, the following operation takes place:

(a) If the SH_IN pin voltage≥0.4 V then the SS pin capacitor continues charging. Synchronous rectification and G, D pin OPEN detection functions start operating.
(b) If the SH_IN pin voltage < 0.4 V then the SS pin capacitor discharges. Charging of the SS pin capacitor starts again after the SH_IN pin voltage≥0.4 V. If the SS pin reaches SS≥0.5V, synchronous rectification and G and D pin OPEN detection functions start operating.

For more details, refer to "The SS pin discharge function by SH_IN voltage" in "Application Part Selection Method".

10. FET Abnormal Protection Block

This block is for the detection of any of the abnormal FET conditions listed below.

(a) One of the G1 and G2 pins is OPEN and the FET is Body Diode rectified;
(b) One of the D1 and D2 pins is OPEN and the FET is Body Diode rectified;
(c) One of the S1 and S2 pins is set to OPEN, and the OFF timing of the FET is abnormal.

When detecting these conditions, the FAIL signal (constant current sink of 2.5 mA) is output from the SH_OUT pin.
For details of each abnormality detection operation, refer to "Abnormality detection function" of "Application circuit".

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Absolute Maximum Ratings (Ta=25 °C)

Parameter	Symbol	Rating	Unit
VCC Pin	V_{MAX_VCC}	-0.3 to +40	V
OVP Pin	V_{MAX_OVP}	-0.3 to +40	V
SH_IN Pin	$V_{MAX_SH_IN}$	-0.3 to +40	V
SH_OUT Pin	$V_{MAX_SH_OUT}$	-0.3 to +VCC	V
G1, G2 Pin	V_{MAX_G1}, V_{MAX_G2}	-0.3 to +15	V
D1, D2 Pin	V_{MAX_D1}, V_{MAX_D2}	+120*(Note 1)*	V
REG Pin	V_{MAX_REG}	-0.3 to +15	V
SS Pin	V_{SS}	-0.3 to +5.5	V
TH Pin	V_{MAX_TH}	-0.3 to +5.5	V
Maximum Junction Temperature	Tjmax	+150	°C
Storage Temperature Range	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) When negative voltage is applied, current flows through the ESD protection element. A current limiting resistor is required for D1 and D2 pins so that the current through these pins is 6 mA or less.

Thermal Resistance *(Note 2)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 4)*	2s2p*(Note 5)*	
SOP14				
Junction-to-Ambient	θ_{JA}	166.5	108.1	°C/W
Junction-to-Top Characterization Parameter*(Note 3)*	Ψ_{JT}	26	22	°C/W

(Note 2) Based on JESD51-2A (still air).
(Note 3) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 4) Using a PCB board based on JESD51-3.
(Note 5) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

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Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range	V_{CC}	5.0	20	32	V
Operating Temperature	Topr	-40	+25	+105	°C
VCC Capacitor Range*(Note 6)*	C_{VCC}	2.2	4.7	-	µF
VCC Resistor Range	R_{VCC}	100	200	-	Ω
TH Resistor Range	R_{TH}	12	200	330	kΩ
REG Capacitor Range*(Note 6)*	C_{REG}	0.47	1.0	2.2	µF

(Note 6) Determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others

Electrical Characteristics

(Unless otherwise specified V_{CC}=20 V, V_{SH_IN}=0.6 V, Ta=25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Circuit Current Item						
Switching Operation Circuit Current	I_{ON}	0.5	1	2	mA	fsw=50 kHz Switching State Gx=OPEN
Standby Circuit Current	I_{STB}	180	300	480	µA	Standby State
Switching Stopped Circuit Current	I_{ACT}	450	800	1400	µA	Switching Stop State
Circuit Current at VCC UVLO Detection	I_{OFF}	120	180	300	µA	V_{CC}=3.5 V
VCC UVLO BLOCK						
VCC UVLO Threshold Voltage 1	V_{UVLO1}	4.1	4.5	4.9	V	VCC Sweep Up
VCC UVLO Threshold Voltage 2	V_{UVLO2}	3.9	4.3	4.7	V	VCC Sweep Down
Slow Start BLOCK						
Slow Start Completion Voltage	V_{SS}	0.4	0.5	0.6	V	V_{SS}=0 V→1 V, V_{SH_IN}=0.6 V
Slow Start Charge Current	I_{SS}	-60	-50	-40	µA	V_{SS}=0.3 V, V_{SH_IN}=0.6 V
ENABLE Voltage	V_{EN}	0.32	0.40	0.48	V	V_{SH_IN}=0.3 V→0.5 V
Synchronous Rectifier Controller BLOCK						
GATE ON Threshold Voltage	V_{GON}	-180	-120	-60	mV	V_{Dx}=+300 mV→-600 mV
GATE OFF Threshold Voltage	V_{GOFF}	-10	-6	-1	mV	V_{Dx}=-600 mV→+300 mV R_{TH}=200 kΩ
Standby State Automatic Detection BLOCK						
Standby State Detection Time	t_{STB}	100	200	300	µs	D1, D2 Stop Pulse
Number of Waiting State Release Pulses	P_{ACT}	-	4096	-	Pulse	D1, D2 total Pulse Number
DRAIN Monitor BLOCK						
D1, D2 Pin Sink Current	I_{D_SINK}	120	270	450	µA	V_{Dx}=120 V
D1, D2 Pin Source Current	I_{D_SO}	-8	-5	-1	µA	V_{Dx}=-0.6 V→-0.05 V
Driver BLOCK						
REG Pin Output Voltage	V_{REG}	11	12	13	V	Switching Stop State
REG Pin Maximum Output Current	I_{MAX_REG}	20	-	-	mA	V_{CC}=20 V, V_{REG}=0 V
High Side FET ON Resistance	R_{HONR}	0.7	1.5	3.0	Ω	I_{OUT}= -10 mA
Low Side FET ON Resistance	R_{LONR}	0.5	0.9	1.6	Ω	I_{OUT}= +10 mA
G1, G2 Pin Turn On Delay Time	t_{DELAY_ON}	-	90	-	ns	V_{Dx}=5 V→-0.3 V
G1, G2 Pin Turn Off Delay Time	t_{DELAY_OFF}	-	100	-	ns	V_{Dx}=-0.3 V→5 V

(Gx, Dx, Sx means x = 1 or 2)

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Electrical Characteristics – continued

(Unless otherwise specified V_{CC}=20 V, V_{SH_IN}=0.6 V, Ta=25 °C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
COMP BLOCK						
Reference Voltage	V_{SH_REF}	0.792	0.8	0.808	V	
Reference Voltage Temperature Change	V_{SHTEMP}	-	-8	-	mV	Ta=25 °C→105 °C
Reference Input Current	I_{SH_IN}	-0.2	0	+0.2	µA	V_{SH_IN}=2 V
SH_OUT Pin Current at SH_IN=L	I_{SH_OUT}	5	10	20	µA	V_{SH_OUT}=20 V, V_{SH_IN}=0 V
SH_OUT Sink Current	I_{SH_SINK}	10	-	-	mA	V_{SH_IN}=0.85 V, V_{SH_OUT}=5.0 V
Abnormality Detection BLOCK						
Overvoltage Detection Voltage	V_{OVP_TH1}	20.58	21.0	21.42	V	R_{OVP}=820 kΩ V_{CC} Sweep Up
Overvoltage Release Voltage	V_{OVP_TH2}	9	10	11	V	R_{OVP}=820 kΩ V_{CC} Sweep Down
G Pin OPEN Detection Voltage	V_{GOP_TH}	-405	-325	-245	mV	V_{Dx}=0 mV→-500 mV
G Pin OPEN Detection Timing	t_{GOP}	2	2.5	3.5	µs	
G Pin OPEN Count Complete Pulse Number	P_{GOP}	-	2048	-	Pulse	D1 and D2 Pin Number of Pulses
D Pin OPEN Detection Voltage	V_{DOP_TH}	1.7	2.0	2.3	V	V_{Dx}=3 V→1 V
D Pin OPEN Count Complete Pulse Number	P_{DOP}	-	128	-	Pulse	Dx Pin Connected Number of Pulses.
S Pin OPEN Detection Voltage	V_{SOP_TH}	200	300	400	mV	V_{Sx}=0 mV→500 mV
SH_OUT Sink Current at Abnormality Mode	$I_{SH_OUT_PRO}$	1.2	2.5	4.2	mA	V_{SH_OUT}=5 V, V_{SH_IN}=0.6 V
REG Pin Discharge Resistance	R_{REG_DIS}	1.2	2.2	3.2	kΩ	V_{REG}=1 mA

(Gx, Dx, Sx means x = 1 or 2)

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Typical Performance Curves
(Reference Data)

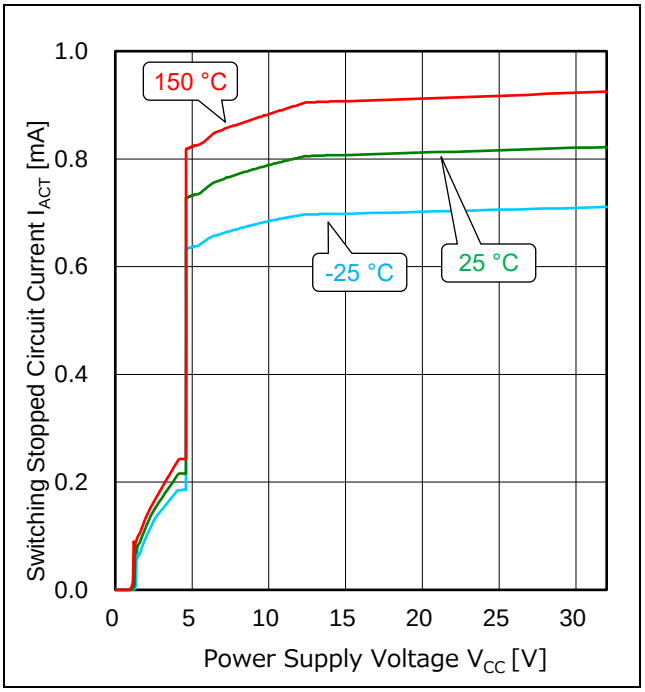


Figure 1. Switching Stopped Circuit Current vs Power Supply Voltage

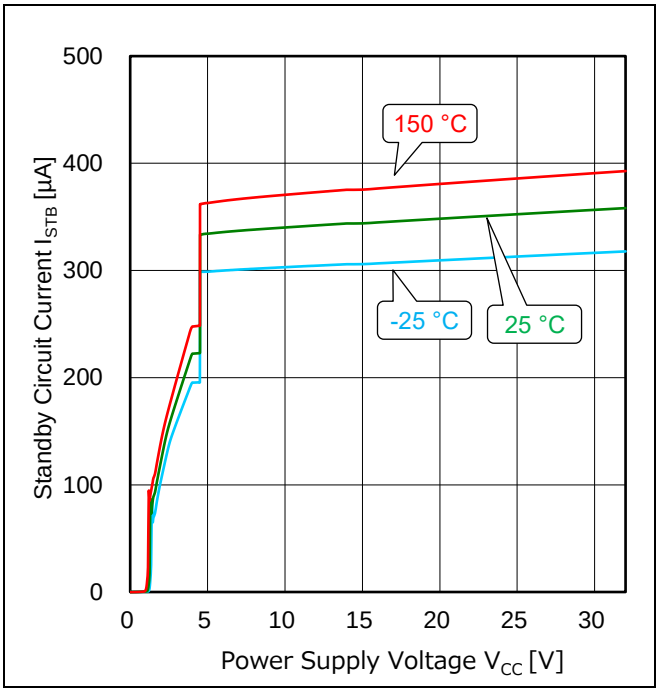


Figure 2. Standby Circuit Current vs Power Supply Voltage

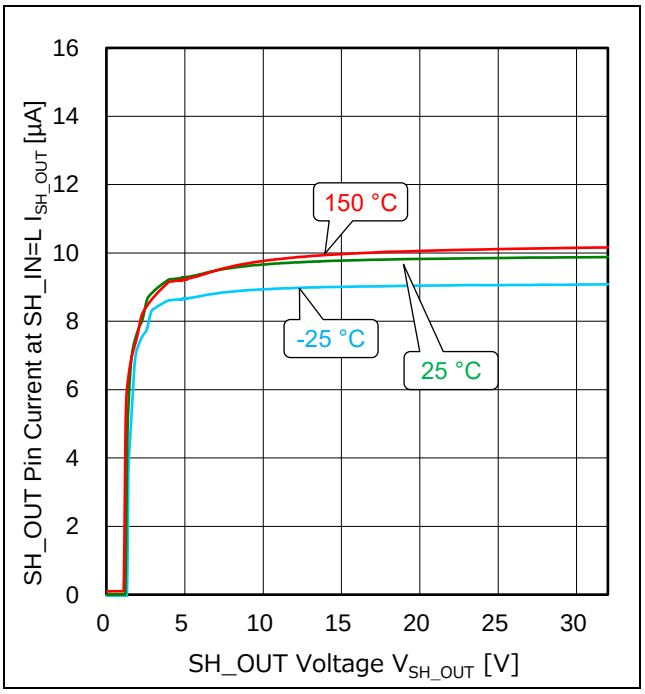


Figure 3. SH_OUT Pin Current at SH_IN=L vs SH_OUT Voltage (VCC=SHOUT, V_{SH_IN}=0 V)

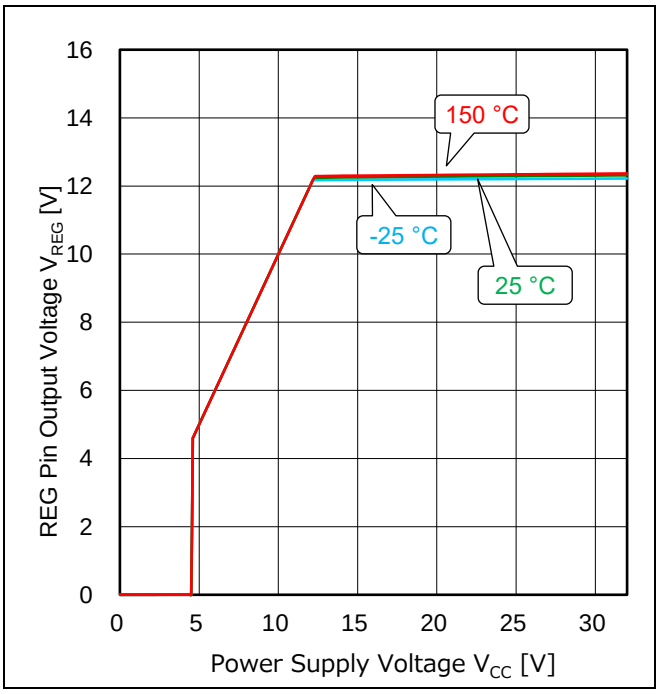


Figure 4. REG Pin Output Voltage vs Power Supply Voltage (V_{SH_IN}=0 V)

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Typical Performance Curves – continued
(Reference Data)

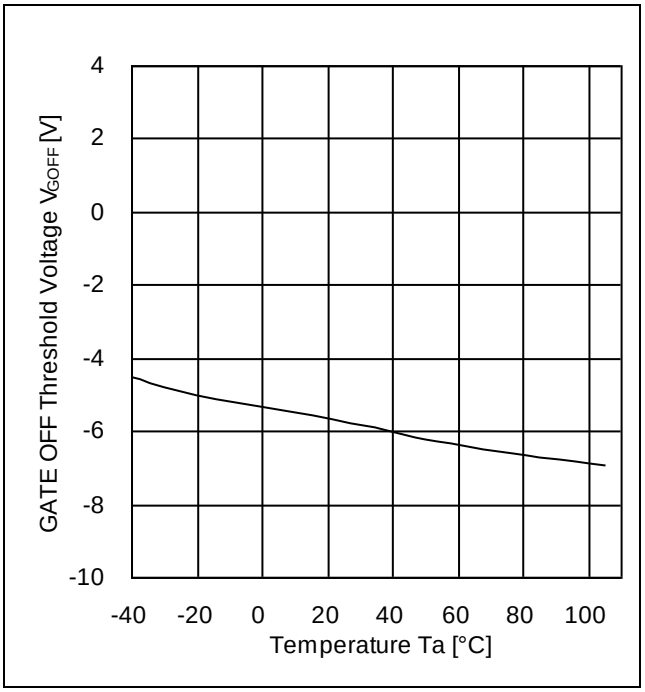


Figure 5. GATE OFF Threshold Voltage vs Temperature
(V_{CC}=20 V, DRAIN Sweep Up)

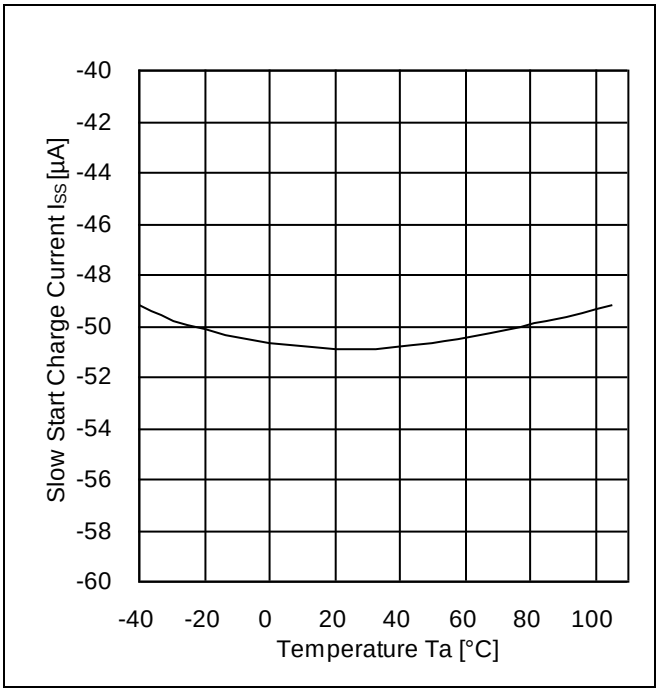


Figure 6. Slow Start Charge Current vs Temperature
(V_{CC}=20 V, V_{SS}=0.3 V)

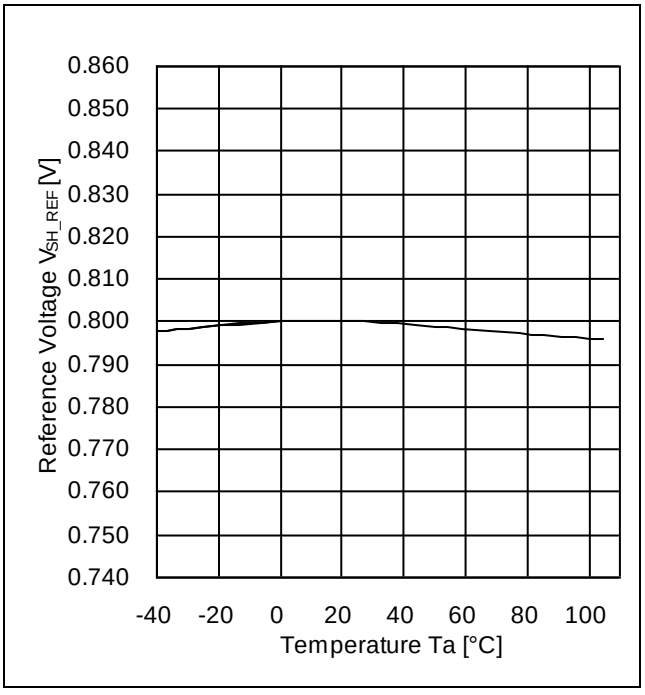


Figure 7. Reference Voltage vs Temperature
(V_{CC}=20 V)

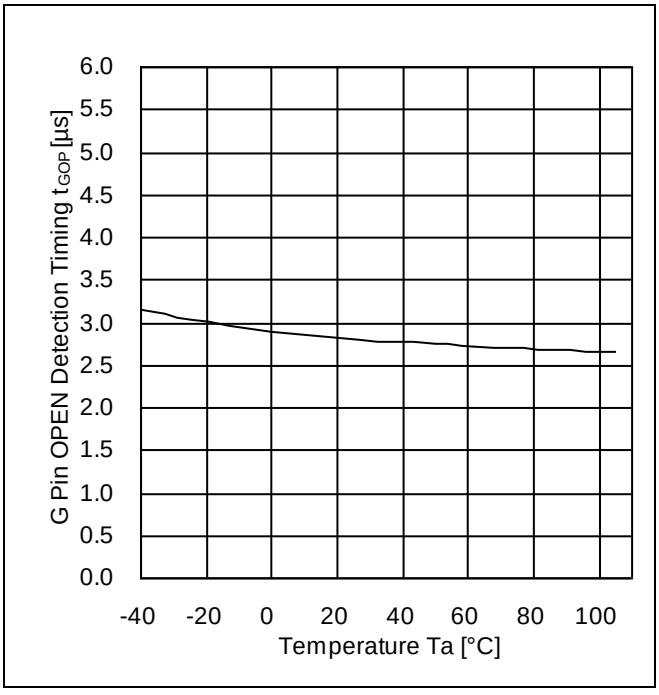


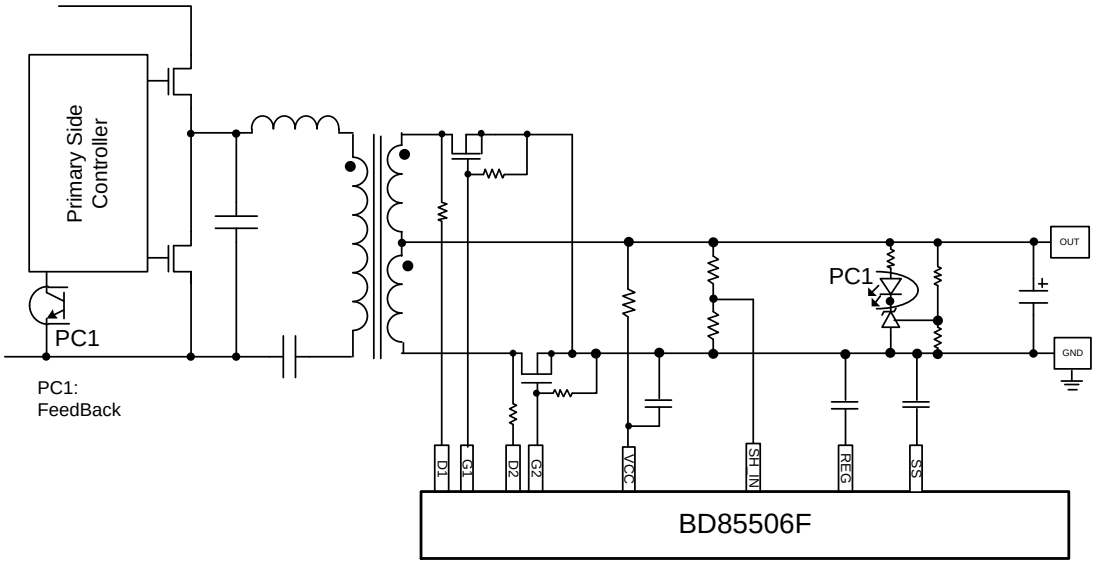
Figure 8. G Pin OPEN Detection Timing vs Temperature
(V_{CC}=20 V)

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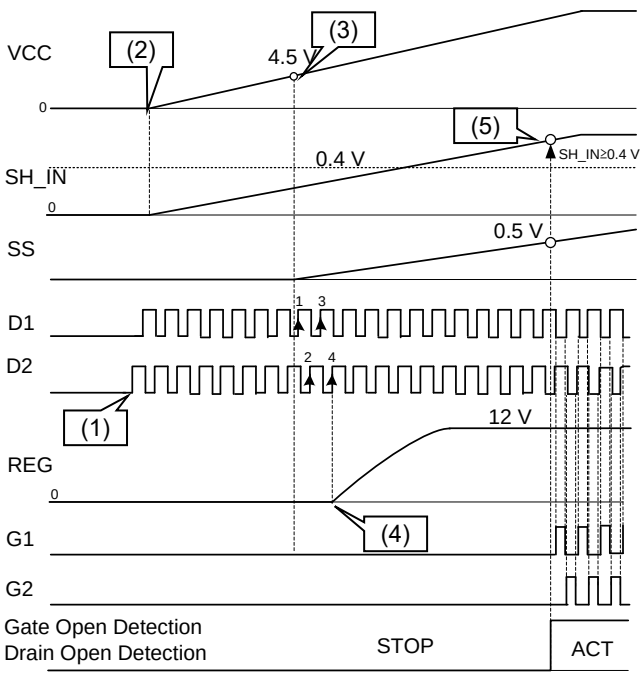
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Timing Chart

The startup sequence is shown below.

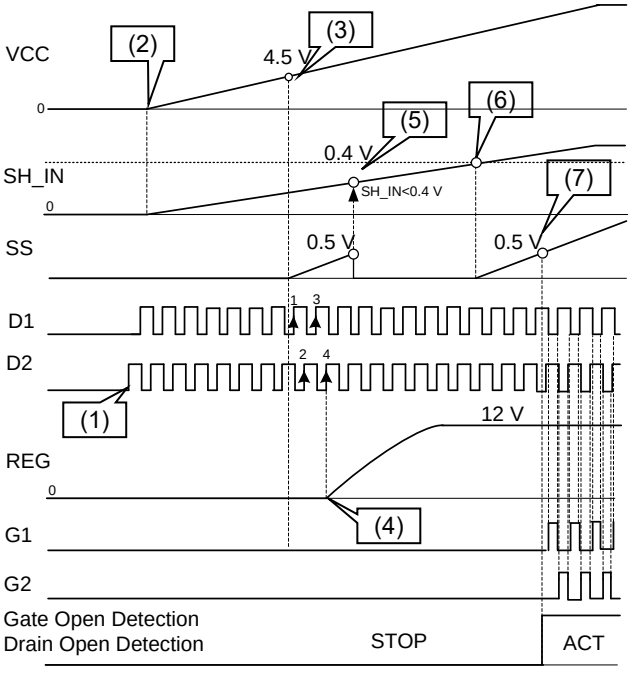


Startup Sequence SH_IN≥0.4 V at SS≥0.5 V



(1) Primary side controller starts, pulses input to pins D1, D2 secondary side.
(2) VCC(=VOUT)Voltage is boosted.
(3) When VCC reaches 4.5 V, VCC_UVLO is released and SS pin capacitor starts charging.
(4) After VCC_UVLO is released, Startup REG outputs by inputting four pulses to D1 and D2.
(5) When SS reaches 0.5 V, if SH_IN≥0.4 V, SR control, Gate Open detection and Drain Open detection functions start.

Startup Sequence SH_IN<0.4 V at SS≥0.5 V



(1) Primary side controller starts, pulses input to pins D1, D2 secondary side.
(2) VCC(=VOUT)Voltage is boosted
(3) When VCC reaches 4.5 V, VCC_UVLO is released and SS pin capacitor starts charging.
(4) After VCC_UVLO is released, Startup REG outputs by inputting four pulses to D1 and D2.
(5) When SS reaches 0.5 V, if SH_IN<0.4 V, SS pin capacitor discharges.
(6) When SH_IN reaches 0.4 V, SS pin capacitor starts charging again.
(7) After reaching SS≥0.5 V, SR control, Gate Open detection and Drain Open detection functions start.

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Application Examples

1. Abnormality Detection Function

In secondary side synchronous rectification, if the connection between the IC and the FET becomes OPEN due to mounting failure or similar conditions wherein the FET cannot be driven, and even if the FET cannot be operated through switching, the FET can still be rectified by its body diode and output. However, when a heavy load is applied, the power loss increases in the body diode, causing abnormal heat generation. In order to prevent this abnormal heat generation, the safety of the circuit can be secured by the FET abnormality detection function built-in this IC.
(Body diode rectification operation is a failure mode which is difficult to detect because both voltage and current are output normally)
In addition, OVP comparators and multipurpose comparators are also built-in, so it is possible to detect abnormality on the secondary side.

List of Abnormality Detection Function and Purpose

No.	Abnormality Detection Function Name	Detection State	Abnormal Operation	Detection Purpose
1	G Pin OPEN Detection	Either G1 or G2 in is disconnected from secondary side SR FET	FET body diode rectification due to stoppage of FET drive	Prevent abnormal heat generation of rectifier FET
2	D Pin OPEN Detection	Either of D1 or D2 pin is disconnected from secondary side SR FET	FET body diode rectification due to stoppage of FET drive	Prevent abnormal heat generation of rectifier FET
3	S Pin OPEN Detection	Either S1 or S2 pin is disconnected from secondary side SR FET	Reverse FET current due to off threshold fluctuation	FET destruction protection
4	OVP Detection	Overvoltage	Abnormal boost up	Breakdown voltage failure protection
5	COMP Detection	multi-purpose	-	-

Detection method and return method of each abnormality detection function

No.	Abnormality Detection Function Name	Detection Condition	Mask Condition of Abnormality Detection	Action of after Confirming Abnormality Detection	Reset Condition
1	G Pin OPEN Detection	*2.5 µs after Gx=ON *Dx voltage <-0.325 V	*SS<0.5 V *Total D1+D2 =2048 pulse continuously	*2.5 mA sink from SH_OUT	VCC_UVLO detection
2	D Pin OPEN Detection	Dx<2.0 V	*SS<0.5 V *Continuous detection while Dx=128 pulse	*2.5 mA sink from SH_OUT *Driver stop *SS discharge *REG discharge	VCC_UVLO detection
3	S Pin OPEN Detection	Sx>0.3 V	Continuous for 9 µs	*2.5 mA sink from SH_OUT *Driver stop *SS discharge *REG discharge	VCC_UVLO detection
4	OVP Detection	Over OVP detection setting voltage	Continuous for 25 µs	*2.5 mA sink from SH_OUT *SS, REG discharge and SR stop	Reach OVP cancel voltage or VCC UVLO detection
5	COMP Detection	SH_IN>0.8 V	-	*Sink current from SH_OUT	Restore

(Gx, Dx, Sx means x = 1 or 2)

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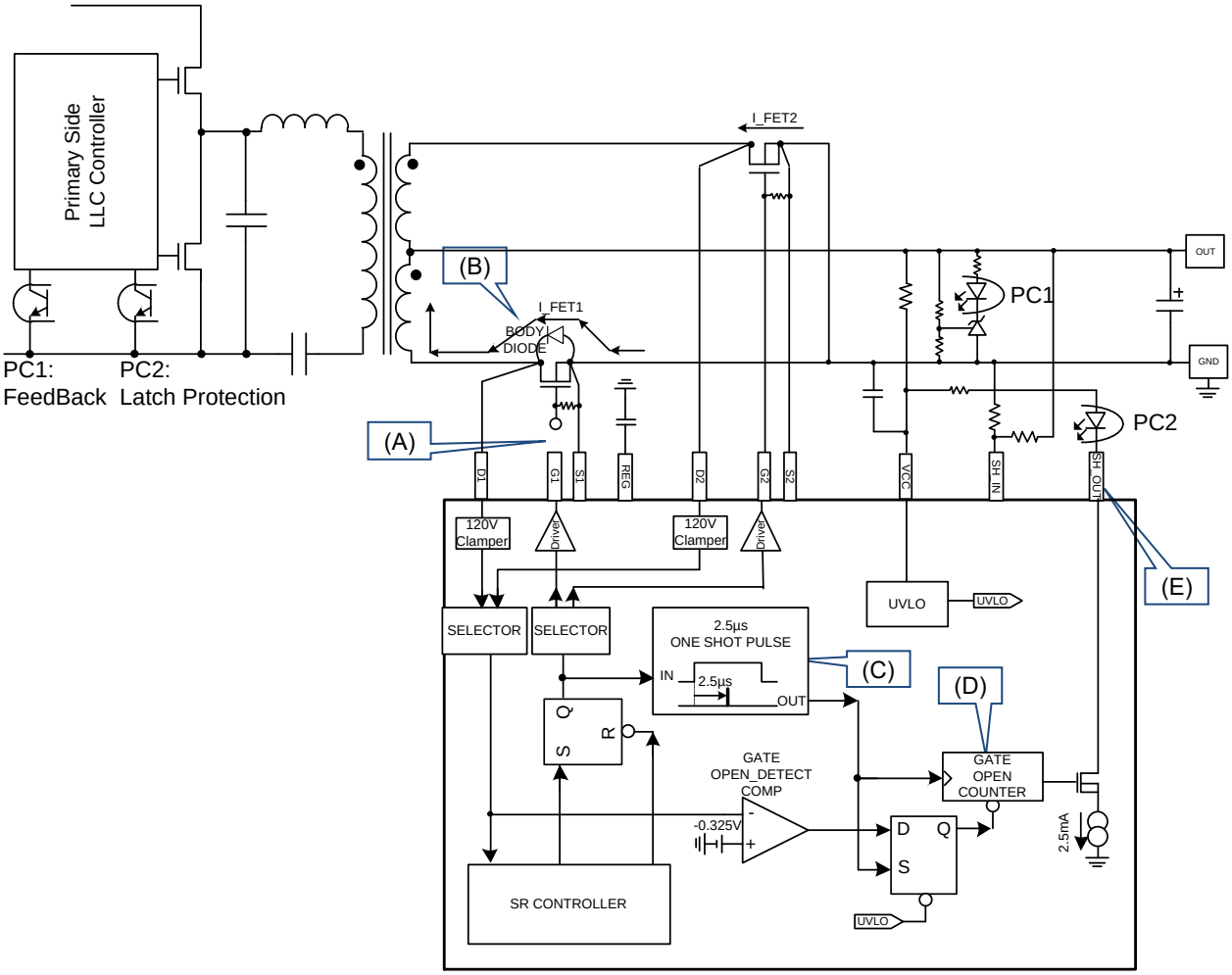
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Abnormality Detection Function – continued

(1) Detection method of G1, G2 OPEN

When one of the G1 and G2 pins of the IC becomes OPEN or when the parts connected to the FET are disconnected, and even if the FET cannot be operated through switching, the FET will still be able to output normally through Body diode rectification operation. However, when heavy load is applied, the power loss at body diode increases and may cause abnormal heat generation. This condition can be detected through the G pin OPEN detection function.

Below is a block diagram with an example for G pin OPEN detection operation.



Example of abnormality detection operation

Circuit configuration: A circuit that causes the PC2 to latch and stop on the primary side after detection of abnormality.

Abnormal condition: G1 is OPEN.

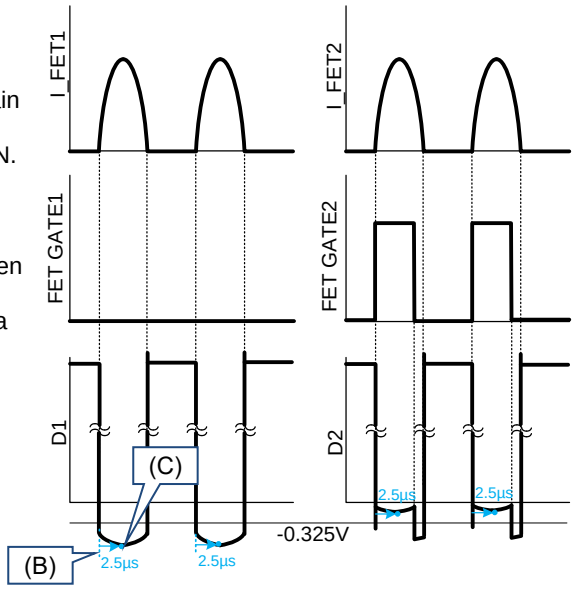
A: G1=OPEN

B: The FET is always turned OFF and its body diode performs rectification. When I_FET1 flows, the voltage between the Drain and Source of the FET becomes Vf.

C: D1 voltage is monitored after 2.5 µs from the time G1 turns ON. Detected G1 OPEN state at less than -0.325 V.

D: G1 OPEN detection confirmed when 2048 pulses are continuously detected.
(Count resets when D1 voltage becomes -0.325 V or more even at 1 pulse)

E: Sinks the current from SH_OUT and stops the primary side via the photo coupler (PC2).
(In case of G pin OPEN detection, synchronous rectification operation is not stopped)



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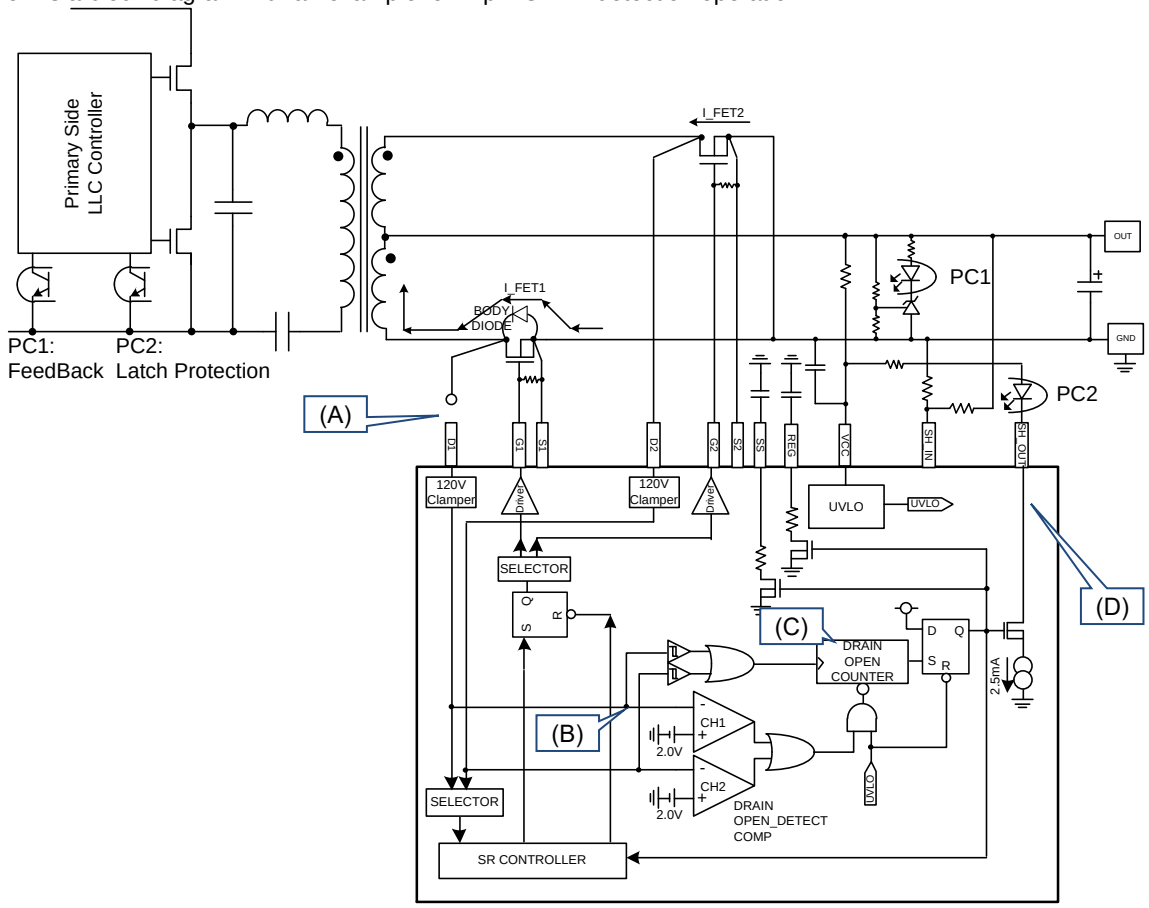
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Abnormality Detection Function – continued

(2) Detection method of D1, D2 OPEN

Likewise, if one of the D1 and D2 pins of the IC becomes OPEN or when the parts connected to the FET are disconnected, the FET cannot be operated through switching, causing abnormal heat generation. But this IC is able to detect such abnormalities through its D pin OPEN detection function.

Below is a block diagram with an example for D pin OPEN detection operation.



Example of abnormality detection operation

Circuit configuration: A circuit that causes the PC2 to latch and stop on the primary side after detection of abnormality.

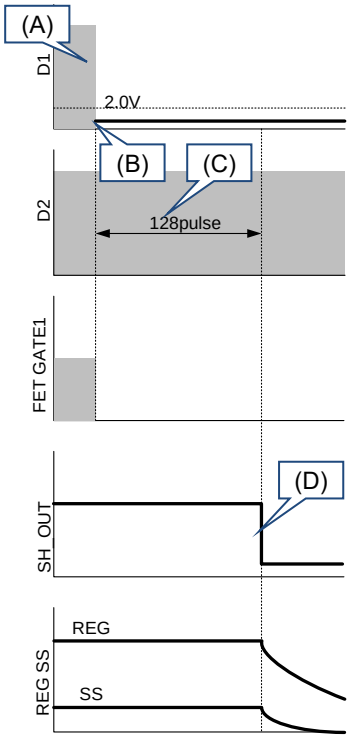
Abnormal condition: D1 is OPEN.

A: No signal input when D1 = OPEN.

B: D1<2.0 V, chip detects D1 OPEN and starts counting.

C: D1 OPEN detection is confirmed when D1<2.0 V continuously when the input pulse count at D2 reaches 128. (Count resets when D1 becomes 2.0 V or more even at 1 pulse)

D: Sinks the current from SH_OUT and stops the primary side via the photo coupler (PC2).
Synchronous rectification drive is stopped, discharging the REG and SS pin capacitor.



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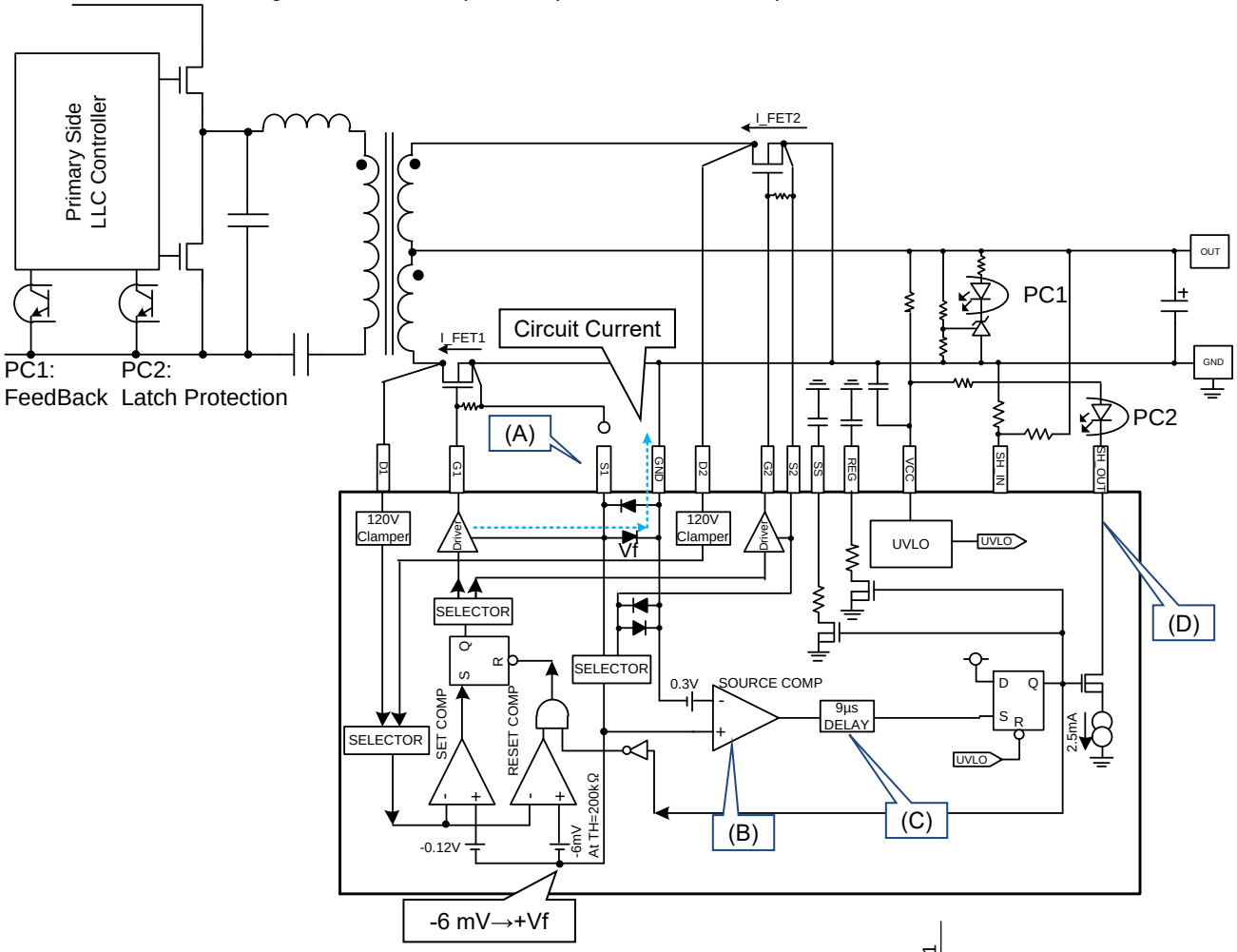
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Regarding Abnormality Detection Function – continued

(3) Detection method of S1, S2 OPEN

When either S1 or S2 pin becomes OPEN, the S pin voltage rises by +Vf due to the circuit current. Therefore, since the reference voltage of RESET COMP is also +Vf, it is not able to turn OFF the FET, which may lead to breakdown due to FET reverse current. With this IC, S pin OPEN detection function prevents this FET from being destroyed, ensuring safety of the circuit.

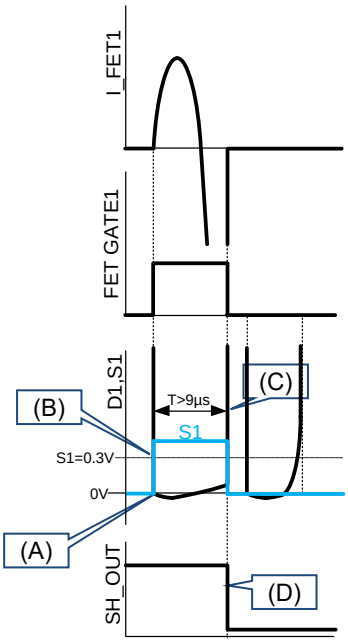
Below is a block diagram with an example for S pin OPEN detection operation.



Example of abnormality detection operation
Circuit configuration: A circuit that causes the PC2 to latch and stop on the primary side after detection of abnormality.
Abnormal state: When S1 is set to OPEN.

A: When S1=OPEN, S1 voltage increases for +Vf when G1=H.
The voltage becomes S1≥0.3 V. (OFF threshold= - 6 mV should also add +Vf. G1 cannot be turned off)
B: S1 OPEN is detected and counting starts.
C: After 9 µs of continuous detection, the S1 open state is confirmed.
D: Sinks the current from SH_OUT and stops the primary side via the photo coupler (PC 2). Synchronous rectification drive is stopped, discharging the REG and SS pin capacitors.

In the S1, S2 OPEN state, FET may be destroyed by current backflow. This is the system to stop the switching operation quickly. Therefore, there is no pulse count, and the protection function is independent of the slow start function.



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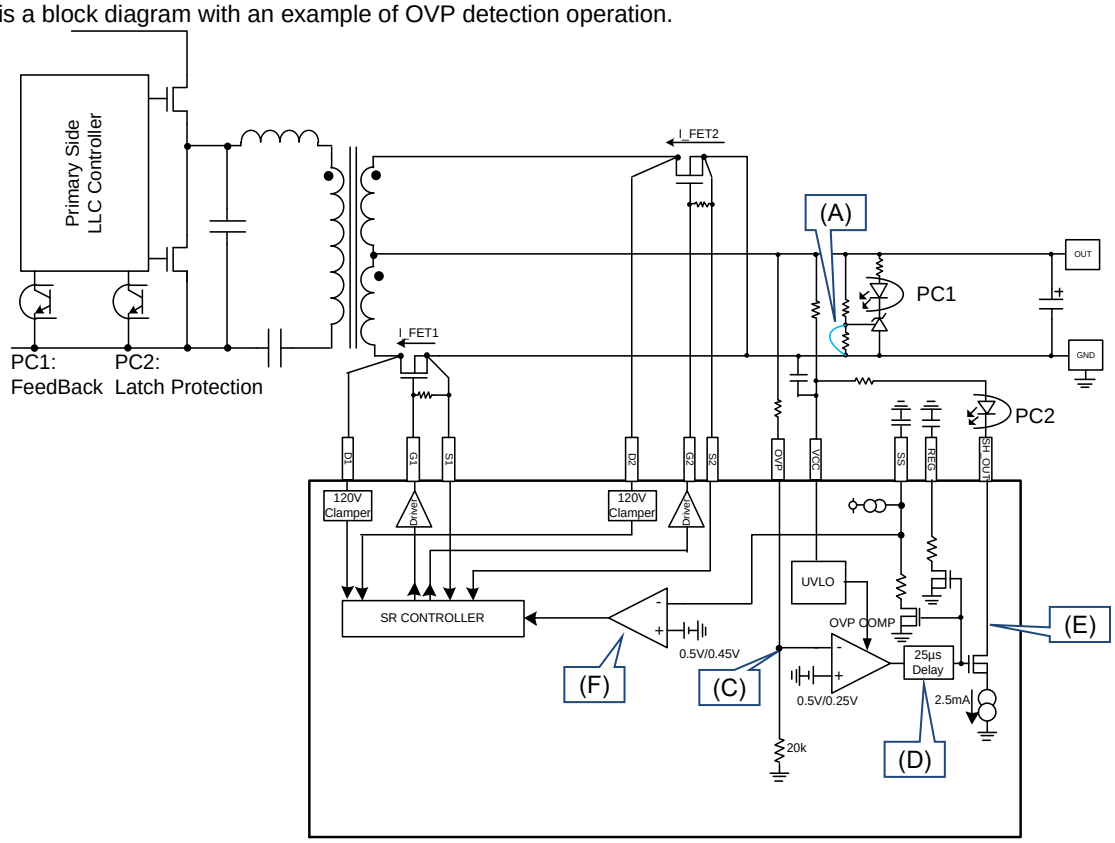
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Regarding Abnormality Detection Function – continued

(4) Detection method of overvoltage (OVP)

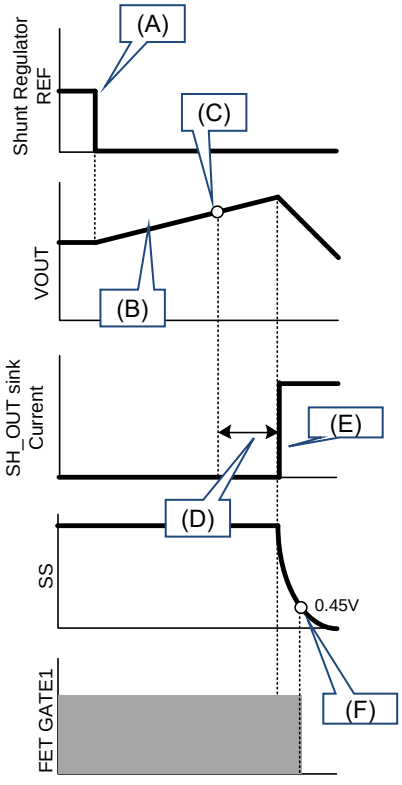
It is possible to detect when overvoltage has occurred due to abnormal feedback operation. The accuracy is within 2 %, with high precision, and the mask period is set to 25 µs. Overvoltage detection can be set only by adjusting the upper resistance since the lower resistor is built-in.

Below is a block diagram with an example of OVP detection operation.



Example of abnormality detection operation
Circuit configuration: A circuit that causes the PC2 to latch and stop on the primary side after detection of abnormality.
Abnormal state: When abnormally boosted.

A: The lower resistor of the shunt regulator shorts to GND.
B: The output voltage abnormally boosts.
C: The OVP detection voltage is reached.
D: OVP state is confirmed if abnormality persists for 25 µs.
E: Stops the primary side by current sink from SH_OUT, and discharges REG and SS pin capacitors.
F: SR Driver is stopped when SS voltage reach SS≤0.45 V.



OVP detection has hysteresis, and it is canceled with 1/2 of the OVP detection voltage. However, if VCC_UVLO is detected first, VCC_UVLO takes precedence and OVP detection is canceled. OVP detection is controlled independently of the slow start function.

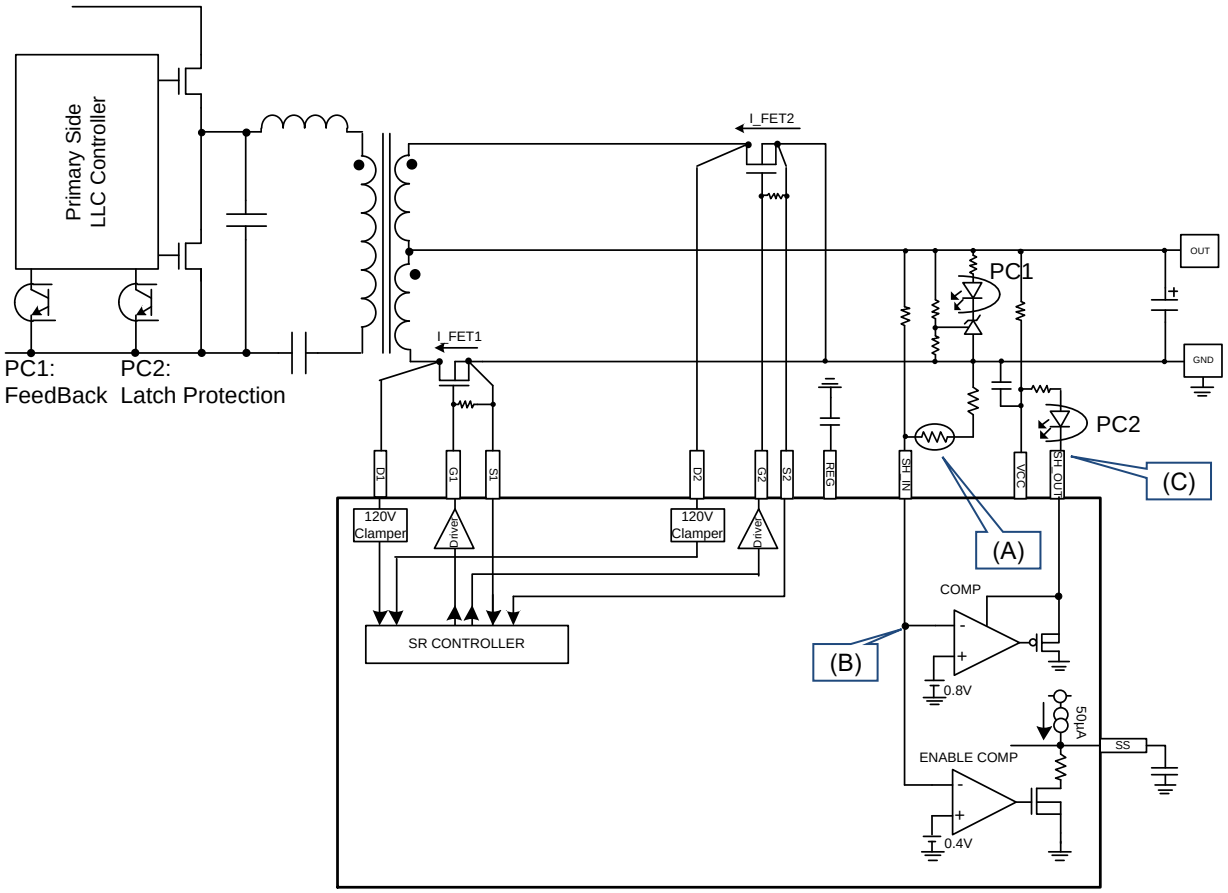
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Regarding Abnormality Detection Function – continued

(5) Multipurpose COMP detection method

The multipurpose comparator can use the SH_IN pin as an input pin. In the example below, it forms a circuit that detects temperature abnormality of a set using a positive characteristic thermistor.
Below is a block diagram with an example of detection operation by COMP.



Example of abnormality detection operation
Circuit configuration: A positive characteristic thermistor is used as a heat detecting element. An example of a circuit is also shown for latching stop on the primary side by PC2 after detection of abnormality.
Abnormal condition: Abnormal heat generation.

A: The temperature rises and the positive characteristic thermistor resistance value rises. The SH_IN voltage rises.
B: The SH_IN pin voltage reaches 0.8 V or more.
C: Comparator output drives the photo coupler (PC2) and stops the primary side.

The detection precision of COMP is as high as 1 %, there is no mask period and no hysteresis. Since the SH_IN pin is also used as ENABLE, input setting should be made so that SH_IN≥0.48 V during normal operation.
And COMP is controlled independently of the slow start function.

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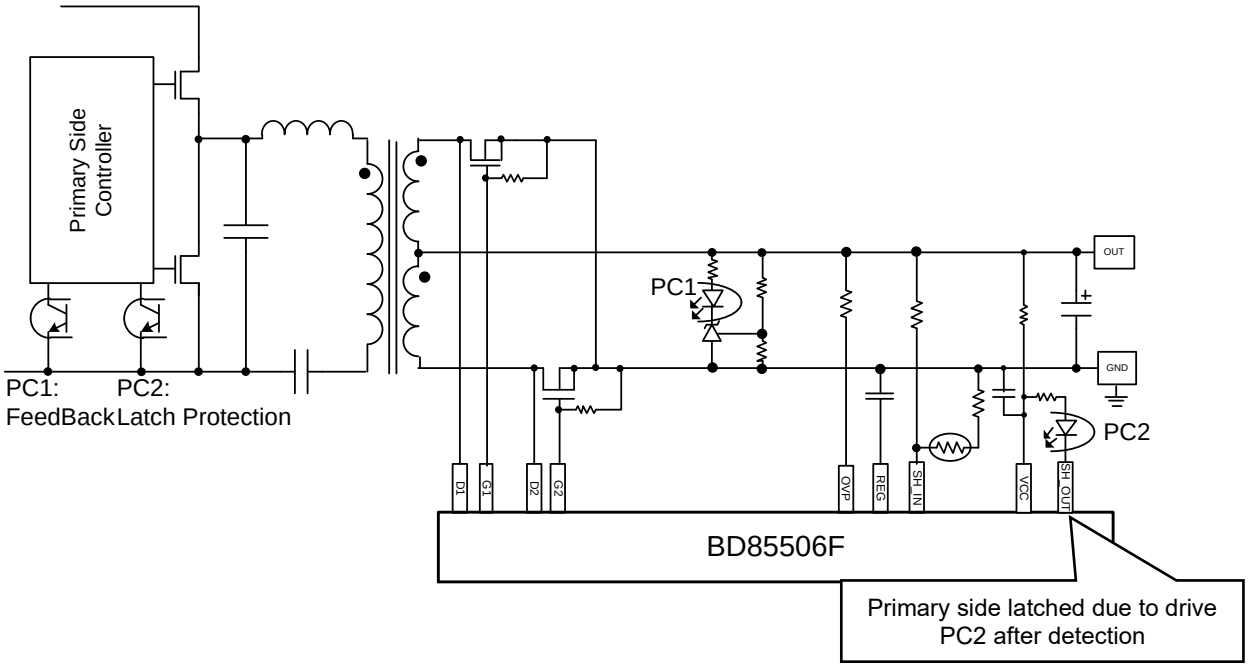
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2.Setting After Abnormality Detection

Depending on the application, operation after abnormality detection can be in any of the following: latch protection, auto restart protection, judgment only signal output, or unused.
These application circuits and operation methods will be explained in the following sections.

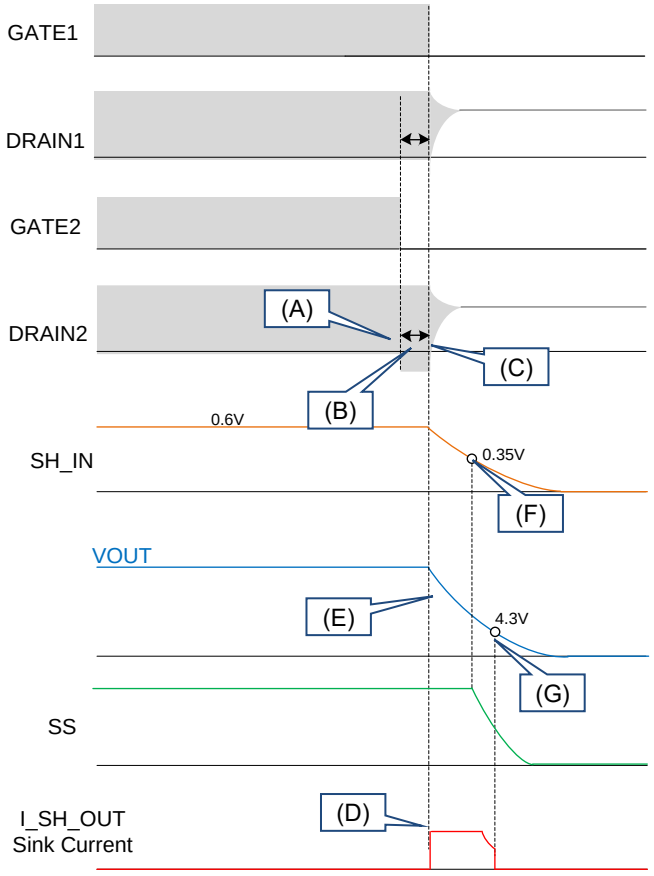
(1) Example of latch protection application

If there is a latch stop protection function on the primary side, the circuit sends a signal to the primary side via the photo coupler and stops the primary side.
Below is a latch protection application circuit and a sequence example.



G2 Example of OPEN protection operation sequence

A: G2 is OPEN.
B: Count for G2 OPEN detection state.
C: Count of 2048 pulses completes.
D: Constant current sink from SH_OUT.
E: VOUT drops with primary side latch stop by PC2.
F: SH_IN≤0.35 V, discharge SS and REG.
G: VCC_UVLO is detected at VCC ≤ 4.3 V and secondary side stops.



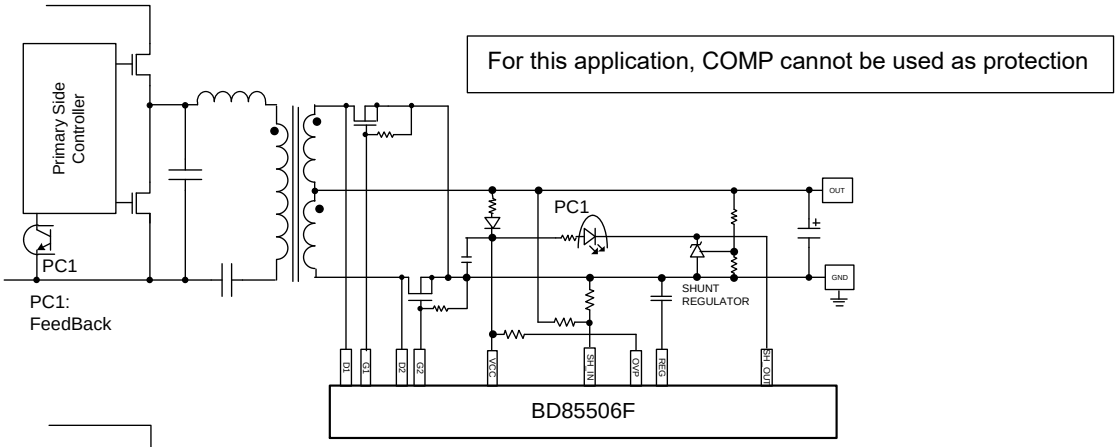
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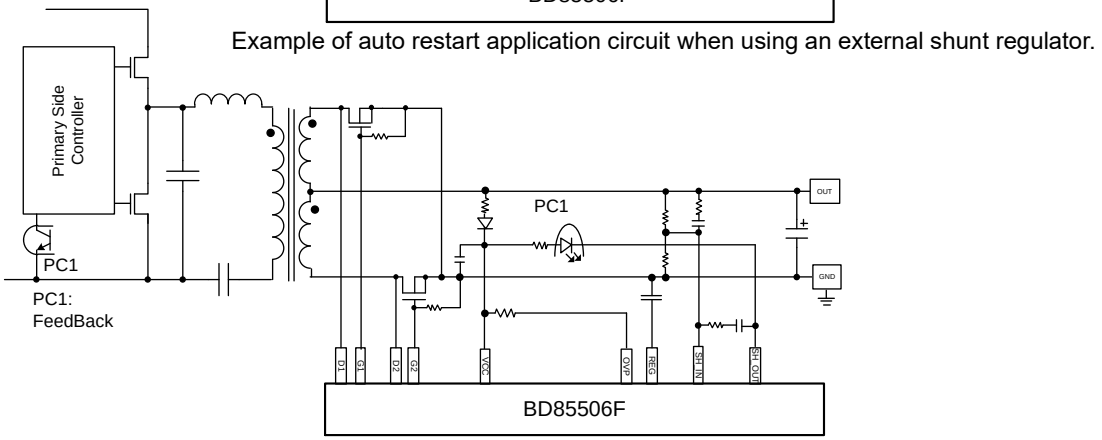
Setting After Abnormality Detection – continued

(2) Auto restart application example

In this method, function does not stop completely after abnormality detection. In the detection period, the output toggles between ON and OFF, and if the state returns to normal, the circuit resumes normal operation after detection of UVLO. Below are examples of application circuits and sequence examples for auto restart protection. (Below is an example of use of the primary side control IC which completely stops when current is forcibly passed to the feedback photo coupler PC1)



Example of auto restart application circuit when using an external shunt regulator.



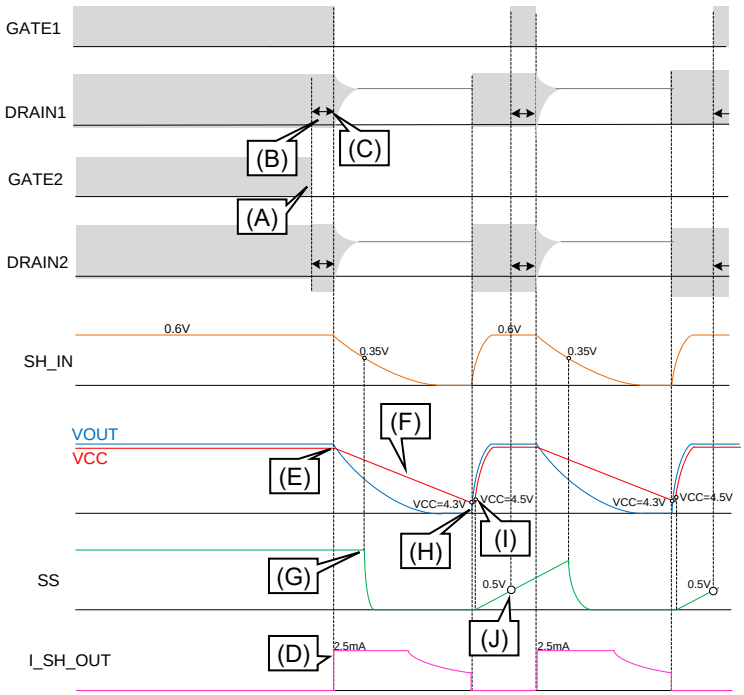
Example of auto restart application circuit when COMP is used as shunt regulator.

Example for G2 OPEN protection

operation sequence

A: G2 is OPEN.
B: Count for G2 OPEN detection state starts.
C: Count of 2048 pulses completes.
D: Constant current sink from SH_OUT.
E: PC1 stops primary side and VOUT drops.
F: VCC holds voltage by Diode and capacitor and secures stop time (heat dissipation time).
G: SH_IN≤0.35 V, discharge SS and REG.
H: VCC≤VCC_UVLO is detected at 4.3 V. SH_OUT Sink current stops, primary side restarts.
I: VCC≥4.5 V, Releases VCC_UVLO and starts SS charging.
J: SS reaches 0.5 V, synchronous rectification, G, D pin open detection function, operation starts.

Return to B.



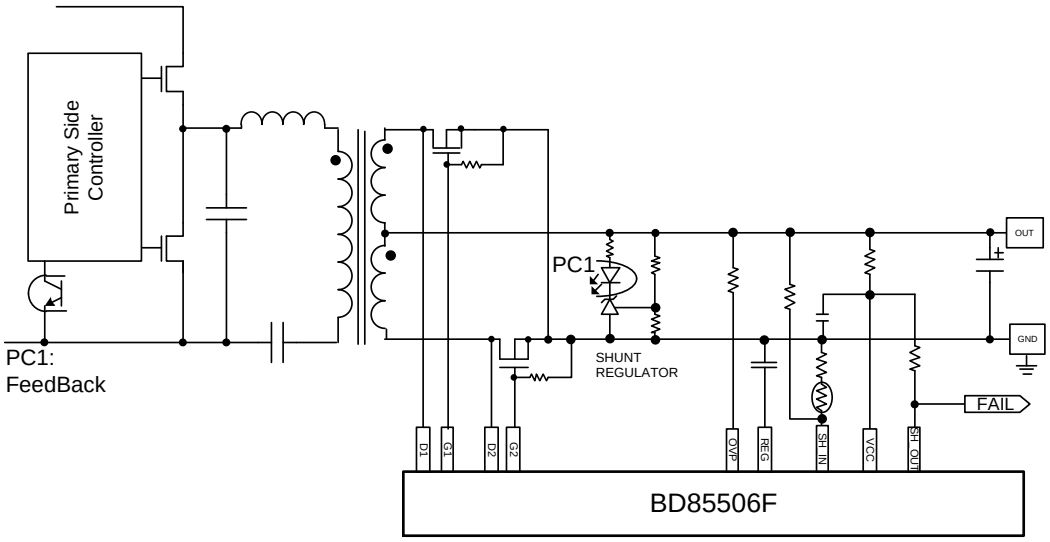
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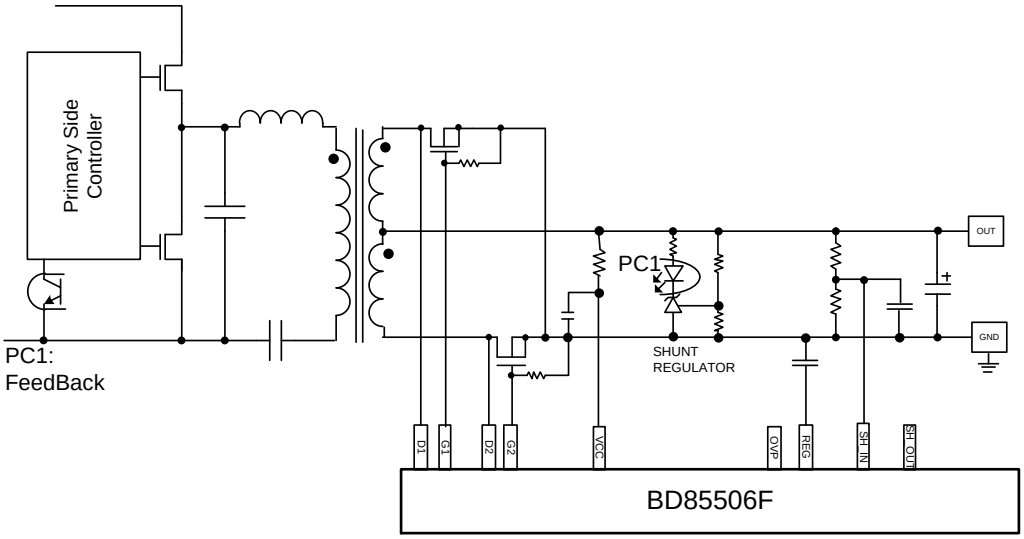
Setting After Abnormality Detection – continued

(3) Application example using only judgment signal

Shown below is an example of application to output a FAIL signal to be used in making a High or Low judgment for shipment inspection, etc.



(4) Example of application not using the abnormality detection signal



When the abnormality detection signal is not used:
* OPEN the SH_OUT pin
* Open the OVP pin
* For the SH_IN pin, input a voltage between 0.48 V (Max) and 0.792 V (Min) by a resistor divider on the VOUT or REG pin.

By doing this, FAIL output of G pin OPEN detection, OVP detection, COMP detection is disabled.
However, when the D pin OPEN and the S pin OPEN are detected, the secondary side synchronous rectification operation is stopped.

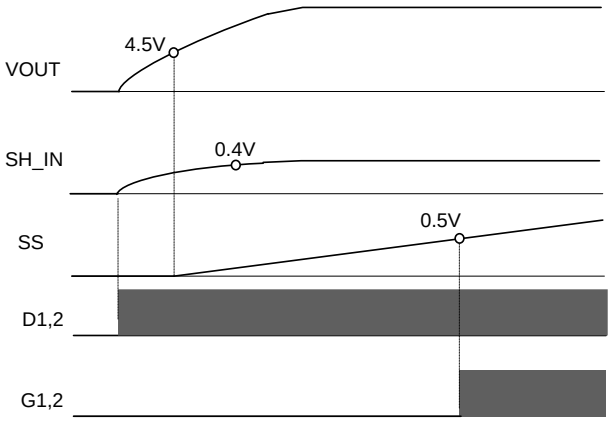
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Selection of External Components

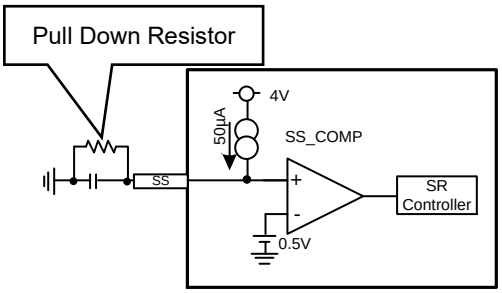
1. SS Pin Setting

Set the operation start time of the G pin OPEN detection, D pin OPEN detection, and secondary side synchronous rectification at the startup time by the capacitance value connected to the SS pin. When the SH_IN pin voltage reaches VCC≥4.5 V, charging starts with a constant current of 50 µA to the SS pin capacitor. When the SS pin voltage V_{SS}≥0.5 V is reached, secondary side synchronous rectification operation and G, D pin OPEN detection function start operating.



The formula for setting SS time t_{SS} and capacitance C_{SS} is

$$C_{SS} = 50 \times 10^{-6}(A) \times \frac{t_{SS}(s)}{0.5(V)} \quad [\text{F}]$$



As an example, the capacitance value for canceling slow start after 5 ms:

$$C_{SS} = 50 \times 10^{-6}(A) \times \frac{5\times10^{-3}(s)}{0.5(V)} = 0.5 \ [\mu\text{F}]$$

In addition, it is also effective to connect a pull-down resistor to make the slow start time longer. The slow start time for this is expressed by the following formula.

$$C_{ss} = -\frac{t_{SS}(s)}{R_{SS}(\Omega)\times ln\left(1-\frac{V_{SS}(V)}{R_{SS}(\Omega)\times I_{SS}(A)}\right)} \ [\text{F}]$$

Calculation example

The C_{SS} capacitance for t_{SS}=140 ms, R_{SS}=20 kΩ, V_{SS}=0.5 V, I_{SS}=50 µA is:

$$C_{ss} = -\frac{0.14(s)}{20\times10^{3}(\Omega)\times ln\left(1-\frac{0.5(V)}{20\times10^{3}(\Omega)\times50\times10^{-6}(A)}\right)} \cong 10 \ [\mu\text{F}]$$

However, please set the resistance value of R_{SS} so as to exceed the slow start completion voltage V_{SS} taking to account tolerances of values.

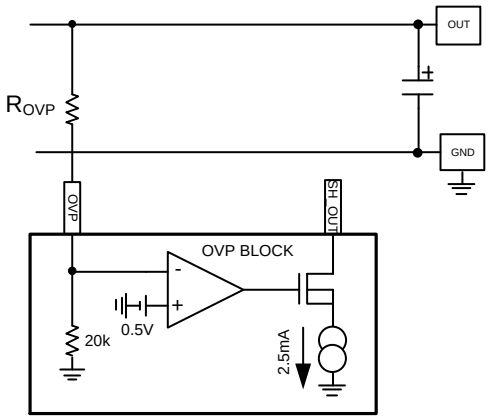
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Application Part Selection Method – continued

2. OVP Pin Setting

Since the lower resistor (20 kΩ) is built-in the OVP pin, it is possible to set the detection voltage by adjusting the resistance between the detection node and OVP pin. After OVP detection, current sinks from SH_OUT.



OVP detection theoretical voltage formula

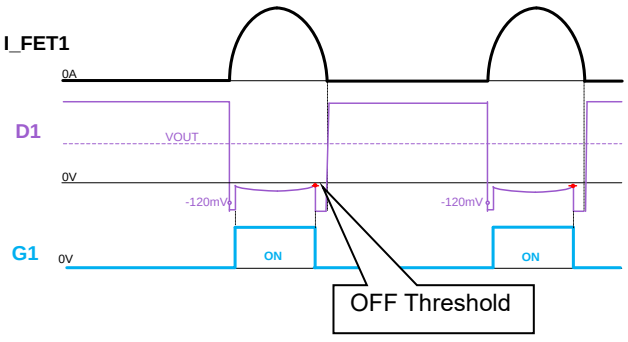
$$R_{OVP} = \frac{V_{OVP_TH1}(V)}{0.5(V)} \times 20(k\Omega) - 20(k\Omega) \text{ [kΩ]}$$

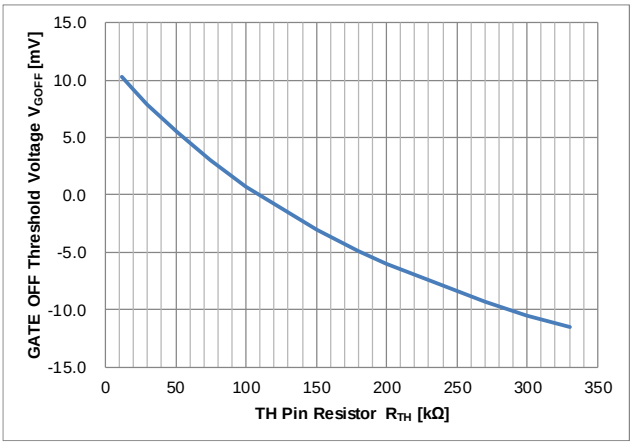
Calculation example
The set resistance value R_{OVP} when V_{OVP_TH1} = 20 V is

$$R_{OVP} = \frac{20(V)}{0.5(V)} \times 20(k\Omega) - 20(k\Omega) = 780 \text{ [kΩ]}$$

3. TH Pin Setting

By adjusting the resistance at the TH pin, the OFF threshold voltage of secondary side synchronous rectification can be changed.





Be careful that OFF threshold accuracy changes depending on the resistor value

The relationship between the GATE OFF threshold voltage V_{GOFF} and the adjustment resistor R_{TH} is as follows.

$$V_{GOFF} = 12(mV) - \frac{45 \times R_{TH}(k\Omega)}{(300(k\Omega) + R_{TH}(k\Omega))} \text{ [mV]}$$

Calculation example
The set GATE OFF Threshold value V_{GOFF} when R_{TH} = 200 kΩ is

$$V_{GOFF} = 12(mV) - \frac{45 \times 200k\Omega}{(300(k\Omega) + 200(k\Omega))} = -6 \text{ [mV]}$$

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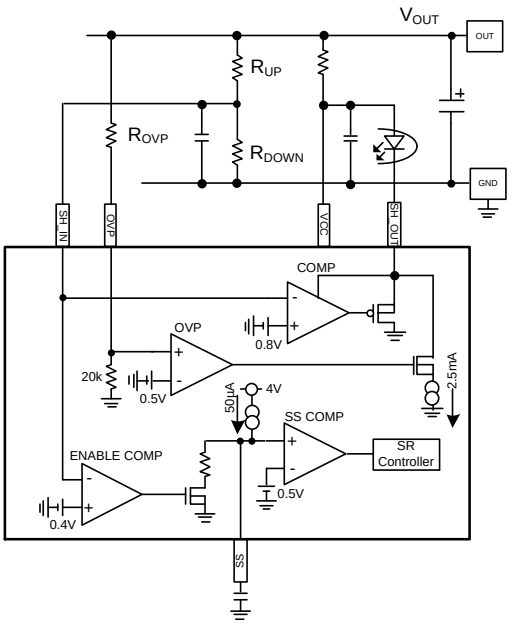
Application Part Selection Method – continued

4. SH_IN Pin Setting

The SH_IN pin is the input pin of the multipurpose comparator with 0.8 V reference and SH_OUT as the output. Typical uses are:
A. Overvoltage detection (double detection together with the OVP pin);
B. Circuit overheat detection; and
C. Shunt Regulator
However, since the SH_IN pin is also used as the ENABLE function, it is necessary to input a voltage to the SH_IN pin greater than or equal to 0.48 V (Max) during normal operation.

(1) For overvoltage detection

Normally, the OVP pin is used for overvoltage detection, but double detection can be made by using multipurpose COMP for additional safety improvement.



The method on how to set values is shown below. The setting of the resistance dividers R_{UP} and R_{DOWN} when the output voltage is V_{OUT} and the overvoltage output to be detected is V_{SH_OVP} are as follows.

$$R_{UP} = R_{DOWN}(k\Omega) \times \frac{\left(V_{SH_OVP}(V) - V_{SH_REF}(V)\right)}{V_{SH_REF}(V)} \text{ [kΩ]}$$

However, during normal operation, the SH_IN pin voltage V_{SH_IN} must satisfy the following conditions.

$$V_{SH_IN} = 0.48V \leq V_{OUT}(V) \times \frac{R_{DOWN}(k\Omega)}{\left(R_{UP}(k\Omega) + R_{DOWN}(k\Omega)\right)} \text{ [V]}$$

Calculation example
When setting V_{OUT}=24 V for normal operation and V_{SH_OVP}=28.8 V for OVP detection voltage, the R_{UP} resistance value when R_{DOWN}=12 kΩ is:

$$R_{UP} = 12(k\Omega) \times \frac{\left(28.8(V) - 0.8(V)\right)}{0.8(V)} = 420 \text{ [kΩ]}$$

Also, the SH_IN pin voltage during stable operation is

$$V_{SH_IN} = 24(V) \times \frac{12(k\Omega)}{\left(420(k\Omega) + 12(k\Omega)\right)} = 0.667V \geq 0.48 \text{ [V]}$$

The above values meet the condition for operation.

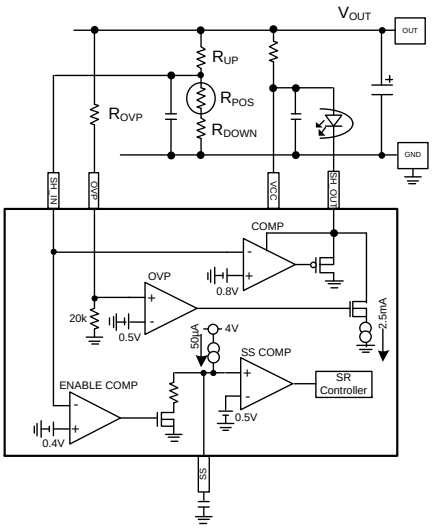
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SH_IN Pin Setting – continued

(2) For overheating detection

By using a positive characteristic thermistor for resistance division at the SH_IN pin, circuit overheat detection is possible. The characteristics of the positive temperature coefficient thermistor are almost constant resistance value at around room temperature. But when a certain temperature (Curie point) is exceeded, the resistance value increases sharply. It is possible to detect the temperature by using this characteristic.



If the output voltage during normal operation is V_{OUT}, the positive characteristic thermistor resistance value of the temperature to be detected is R_{POS1}, and the lower resistance value of the resistor divider is R_{DOWN}, the upper resistance value R_{UP} is set as shown below.

$$R_{UP} = V_{OUT}(V) \times \frac{\left(R_{DOWN}(k\Omega)+R_{POS1}(k\Omega)\right)}{V_{SH_REF}(V)} - \left(R_{DOWN}(k\Omega) + R_{POS1}(k\Omega)\right) \text{ [kΩ]}$$

However, the following condition must be satisfied for the positive characteristic thermistor resistance value R_{POS2} at the normal temperature and the SH_IN pin voltage V_{SH_IN}.

$$V_{SH_IN} = 0.48(V) \leq V_{OUT}(V) \times \frac{R_{DOWN}(k\Omega)+R_{POS2}(k\Omega)}{\left(R_{UP}(k\Omega)+R_{DOWN}(k\Omega)+R_{POS2}(k\Omega)\right)} \quad \text{[V]}$$

Calculation example

For example, using Murata PRF15BB102RB6RC *(Note 7)* as a positive characteristic thermistor:

(Note 7) Please refer to the data sheet published by Murata Co. for product information.

When setting the positive characteristic thermistor temperature to detect at 115 °C,
During normal operation V_{OUT}=24 V,
The positive characteristic thermistor resistance value at the detection temperature of 115 °C is R_{POS1}=10 kΩ
The R_{UP} resistance value when R_{DOWN}=22 kΩ is

$$R_{UP} = 24(V) \times \frac{\left(22(k\Omega)+10(k\Omega)\right)}{0.8(V)} - \left(22(k\Omega) + 10(k\Omega)\right) = 928 \text{ [kΩ]}$$

Also, the positive characteristic thermistor resistance value at 25 °C is R_{POS2}=0.5 kΩ (Min) in consideration of tolerances,

$$V_{SH_IN} = 0.48(V) \leq 24(V) \times \frac{22(k\Omega)+0.5(k\Omega)}{\left(928(k\Omega)+22(k\Omega)+0.5(k\Omega)\right)} = 0.568 \text{ [V]}$$

This meets the condition.

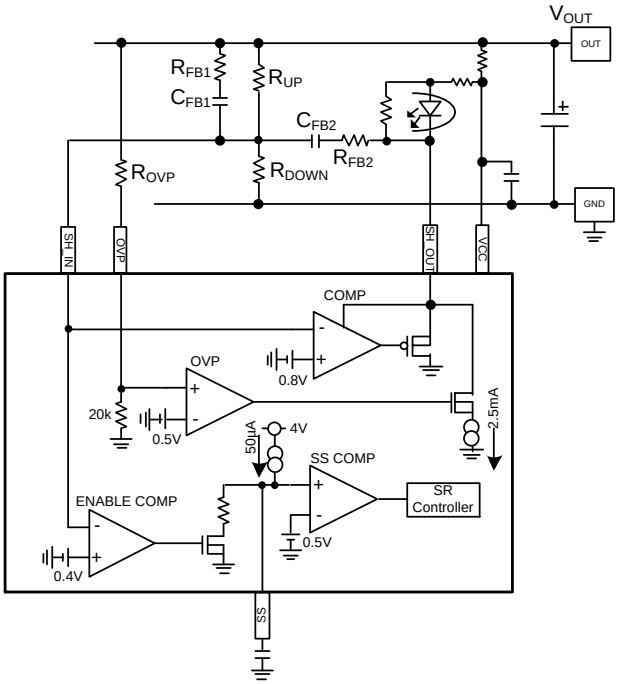
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SH_IN Pin Setting – continued

(3) As a shunt regulator

Connecting a feedback resistor to the SH_IN pin makes it usable as a shunt regulator. Since the current consumption from SH_OUT is as small as 10 μA, it is possible to reduce standby power consumption at no load.



In normal operation, the output voltage is V_{OUT}, the feedback resistance divides R_{UP}, R_{DOWN} values are as follows.

$$R_{UP} = R_{DOWN}(k\Omega) \times \frac{\left(V_{OUT}(V) - V_{SH_REF}(V)\right)}{V_{SH_REF}(V)} \text{ [kΩ]}$$

Calculation example

The R_{UP} resistance value when V_{OUT}=24 V in normal operation and the lower side resistance R_{DOWN} is 80 kΩ,

$$R_{UP} = 80(k\Omega) \times \frac{\left(24(V) - 0.8(V)\right)}{0.8(V)} = 2320 \text{ [kΩ]}$$

However, it is necessary to reset the phase compensation of R_{FB1}, R_{FB2}, C_{FB1}, and C_{FB2}. Therefore, it is recommended to check with FRA or other instruments, to ensure that the oscillation margin is enough after setting.

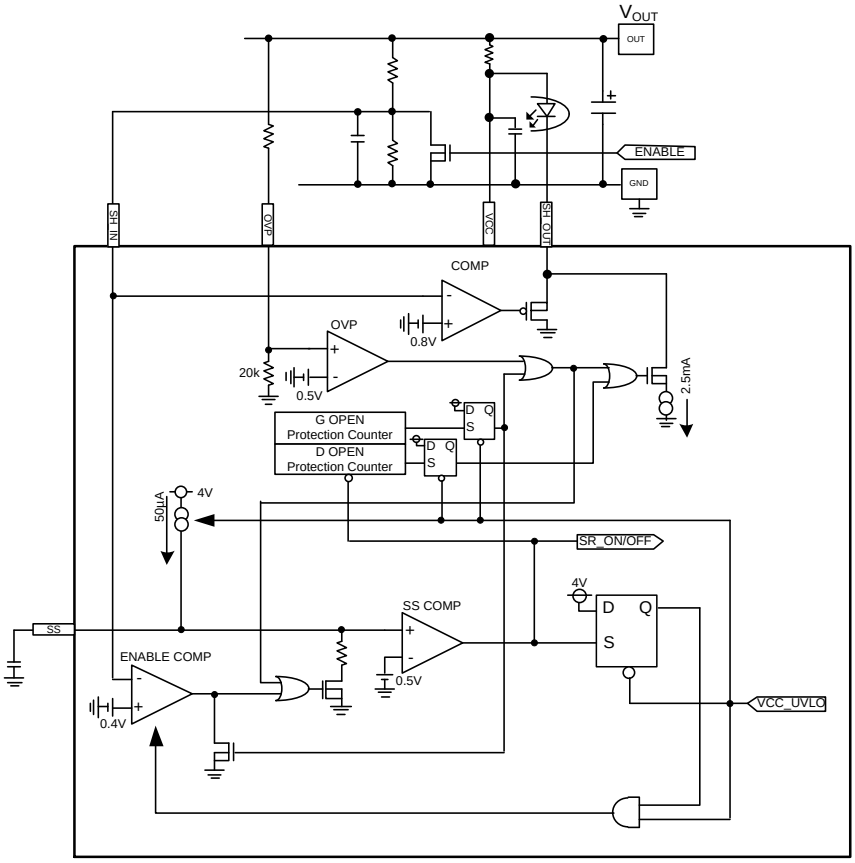
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Application Part Selection Method – continued

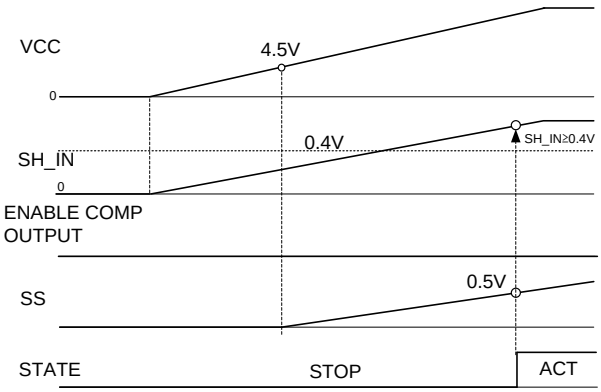
5.The SS pin discharge function by SH_IN voltage

When the SH_IN pin is set to 0.4 V or less, the SS pin capacitor is discharged. With this function, synchronous rectification and G, D pin OPEN protection can be stopped arbitrarily by an external signal.
However, this function cannot be used as a reset after error detection.

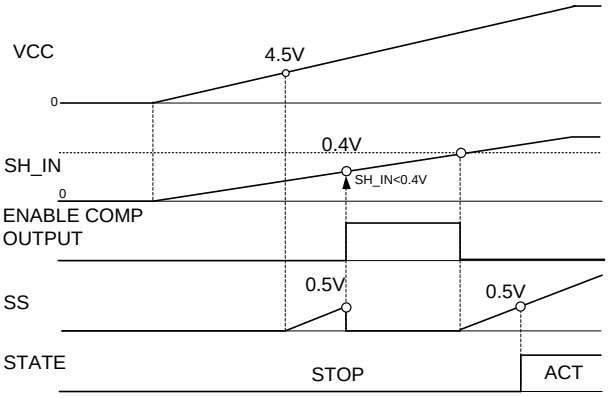


Also, at startup, a large amount of rush current flows and operation may become unstable. Therefore, after set voltage had been reached (SH_IN voltage≥0.4 V), SR control and G, D pin OPEN detection starts operation.

In the case of SH_IN≥0.4 V at SS≥0.5 V, Startup sequence



In the case of SH_IN<0.4 V at SS≥0.5 V, Startup sequence

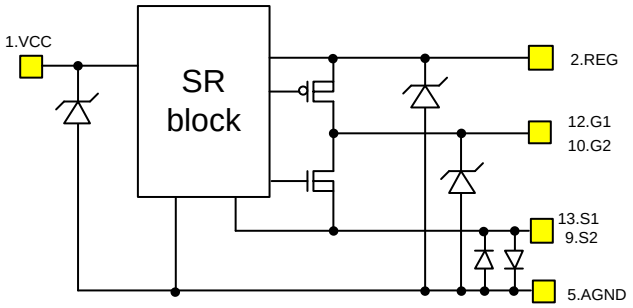
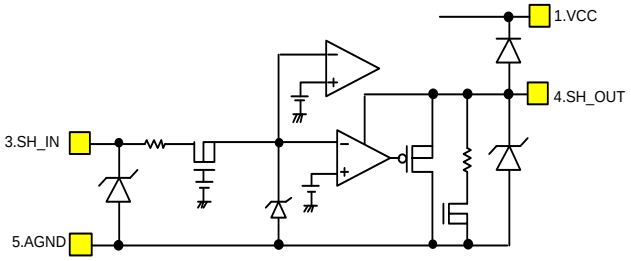
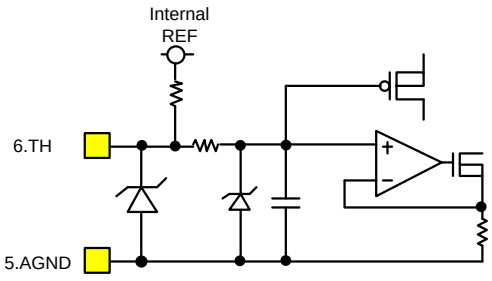
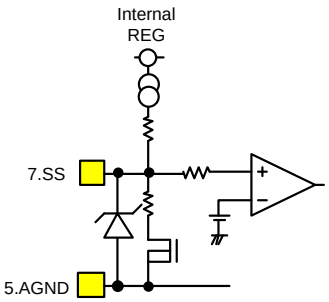
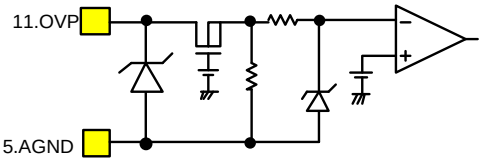
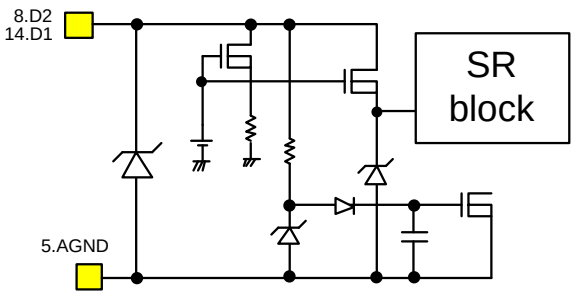


If SS≥0.5 V, when SH_IN≥0.4 V, it is judged that the set output has been reached and the SS pin capacitor continues charging.
But if SS≥0.5 V, when SH_IN<0.4 V, it is judged that the set voltage has not been reached and the SS pin capacitor is discharged. And when the voltage reaches SH_IN≥0.4 V, charging of the SS pin capacitor restarts.

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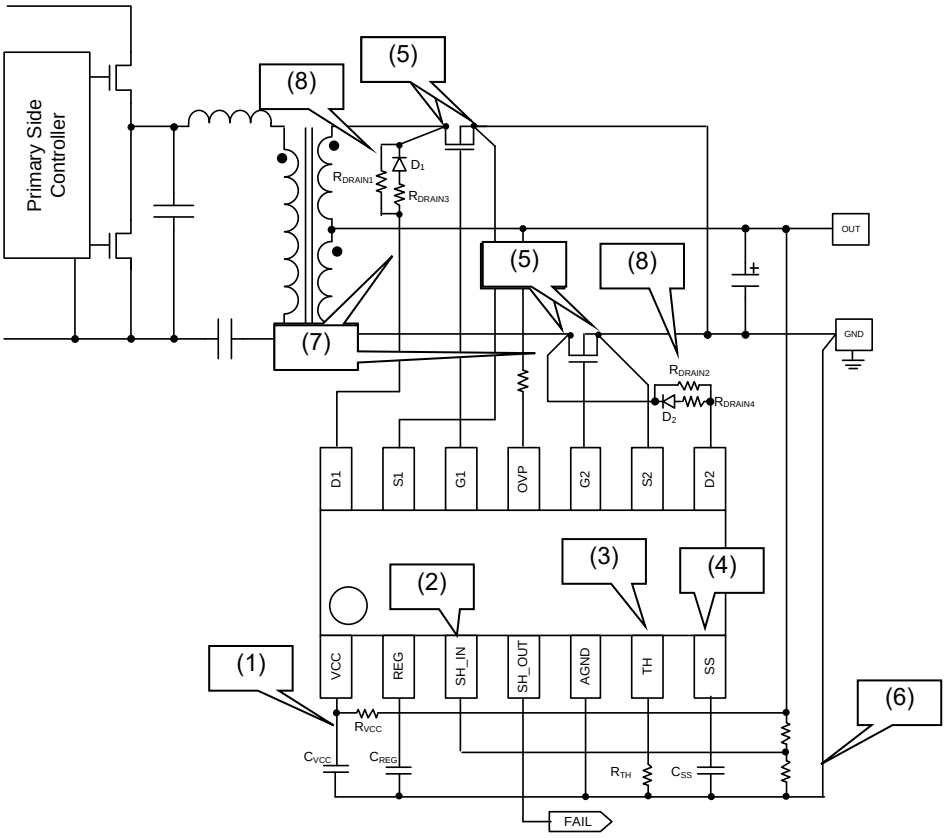
I/O Equivalence Circuits

1pin VCC / 2pin REG / 9pin S2 / 10pin G2 12pin G1 / 13pin S1	3pin SH_IN / 4pin SH_OUT
	
6pin TH	**7pin SS**
	
11pin OVP	**8pin D2 / 14pin D1**
	

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Layout Notes



LLC Application Circuit

(1) The VCC line may malfunction under the influence of switching noise.
Therefore, it is recommended to connect the noise suppression capacitor C_{VCC} (2.2 µF or more including temperature characteristics, DC bias characteristics, and tolerances) and resistor R_{VCC} (100 Ω or more) between near by the VCC pin and the AGND pin. At this time, the supply voltage drops due to the R_{VCC} resistance, but please set the resistance value so that the FET Driver voltage can be sufficiently secured.

(2) The SH_IN pin is a high-impedance line. Layout its wiring as short as possible and make sure it does not run parallel to a switching line.

(3) The TH pin is OFF threshold setting pin. When the OFF timing is affected by switching, it is recommended to connect resistor R_{TH} to the TH Pin and AGND as near to the TH pin as possible.

(4) The SS pin is the slow start time setting pin. It is recommended that the capacitor C_{SS} is connected as closest to the AGND line as possible.

(5) Since the synchronous rectification controller IC needs to accurately monitor the V_{DS} generated in the FET, ensure to connect the D1 and D2 pins of the IC to the Drain of the FET and the S1 and S2 pins to the Source of the FET independently.
It is recommended to set the DRAIN monitoring point of the FET considering the influence of the parasitic inductor due to the substrate wiring of the current path.

(6) It is recommended that the GND of the different parts connected to the IC is connected to the output GND through independent wiring.

(7) Because the Drain wiring is a switching line, it should be wired as short as possible and be wire thinly.

(8) Since the D1 and D2 pins detect a very small voltage, it may toggle between ON and OFF depending on the surge voltage.
Therefore, it is recommended to connect a filter circuit as a measure to absorb surge.

Value setting reference example*(Note 8)*:
Schottky barrier diode D_1 D_2: RB751G-40 (ROHM)
FET turn off filter resistance R_{DRAIN1} R_{DRAIN2}: 0.3 k to 2 kΩ
Drain pin current limit resistor R_{DRAIN3} R_{DRAIN4}: 150 Ω
(Note 8) Constants are reference values and not guaranteed values. Please verify on the actual application and set optimum values for the constants.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

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Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

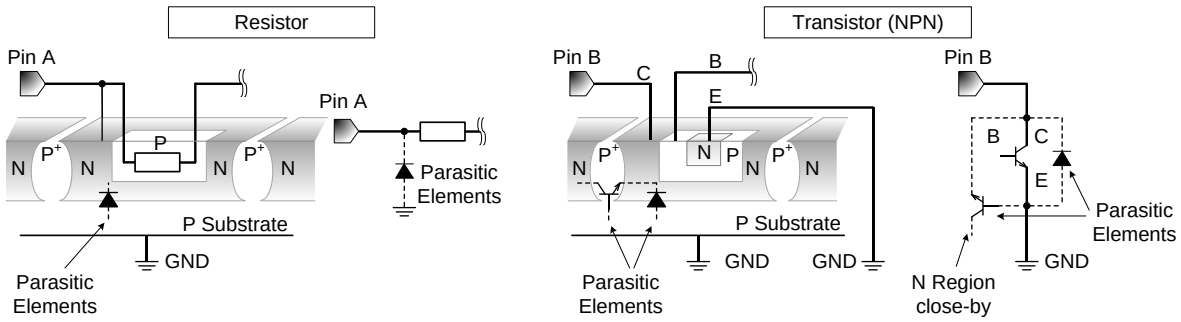


Figure 9. Example of monolithic IC structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others .

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

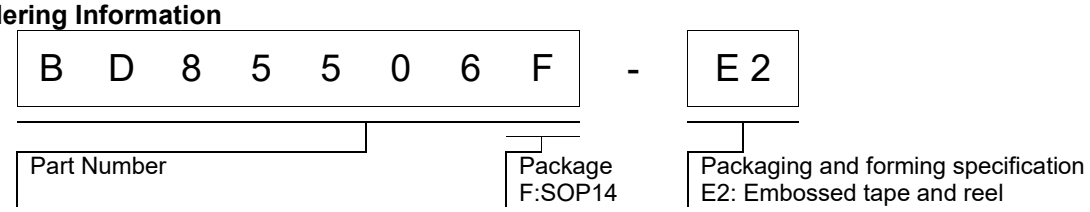
13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

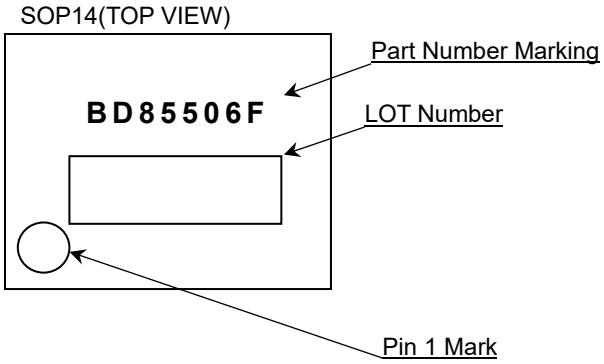
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Ordering Information



Marking Diagram

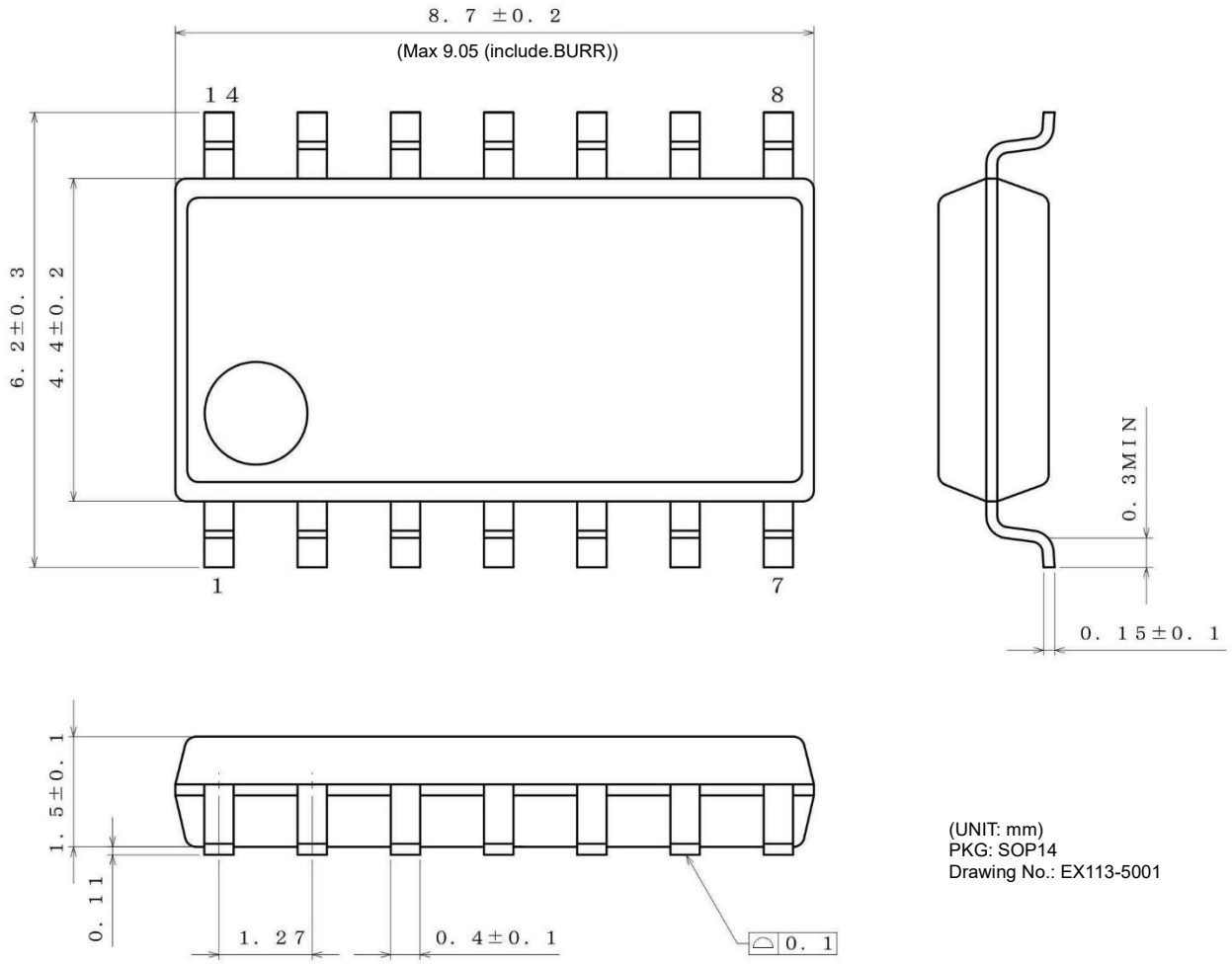


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Physical Dimension and Packing Information

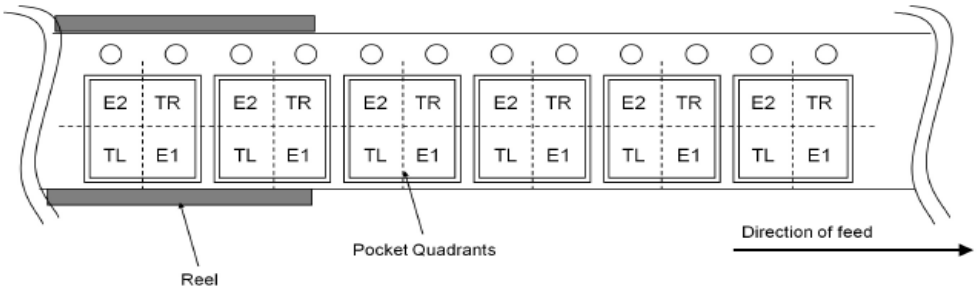
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(UNIT: mm)
PKG: SOP14
Drawing No.: EX113-5001

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Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



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Revision History

Date	Rev.	Changes
22.Aug.2018	001	New Release
28.Dec.2020	002	Updated packages and part numbers. P33-2,P33-3

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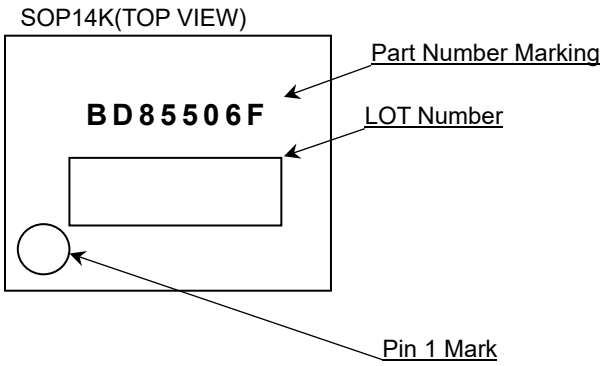
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Ordering Information

B D 8 5 5 0 6 F - Z E 2

- Part Number
- Package F:SOP14K
- Packaging and forming specification Production site Z: Added E2: Embossed tape and reel

Marking Diagram

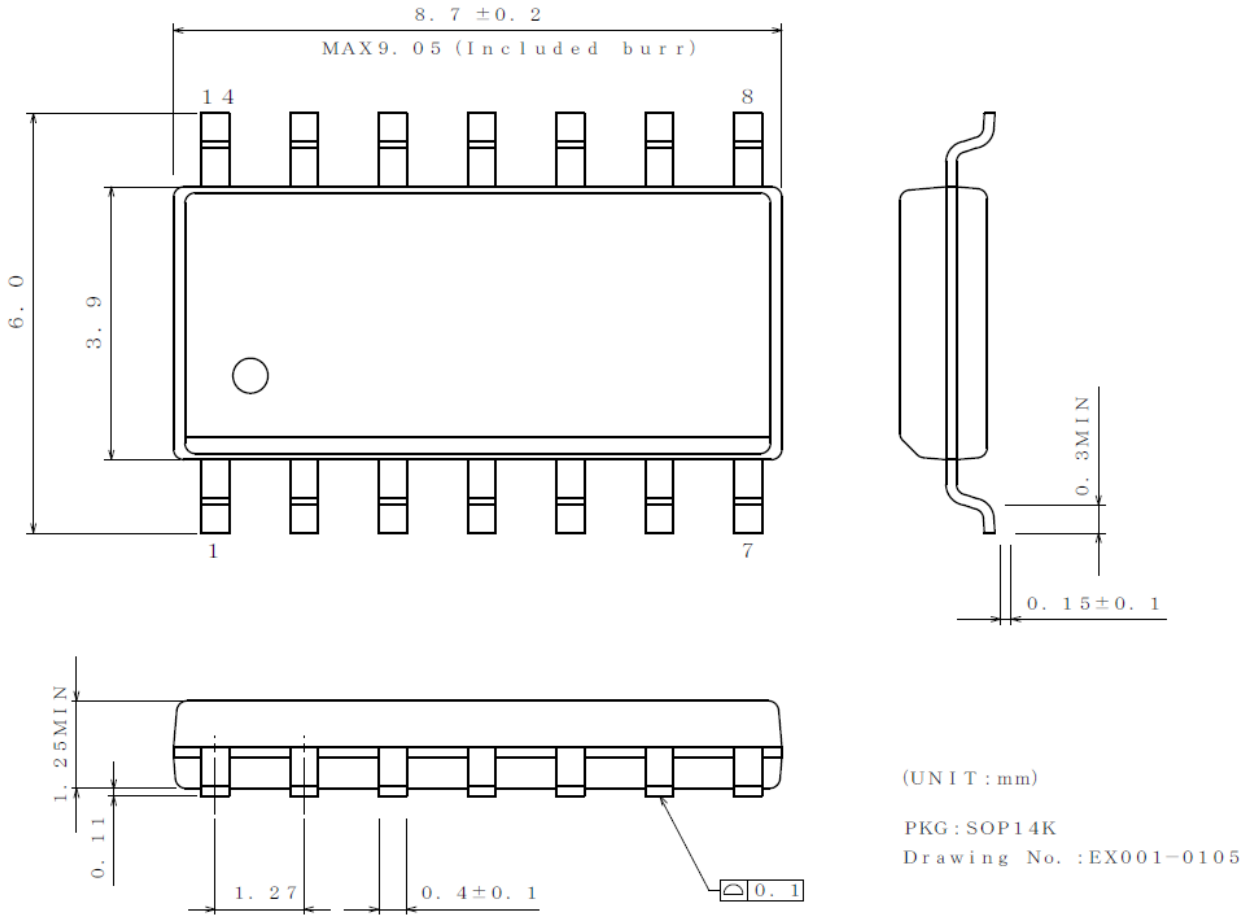


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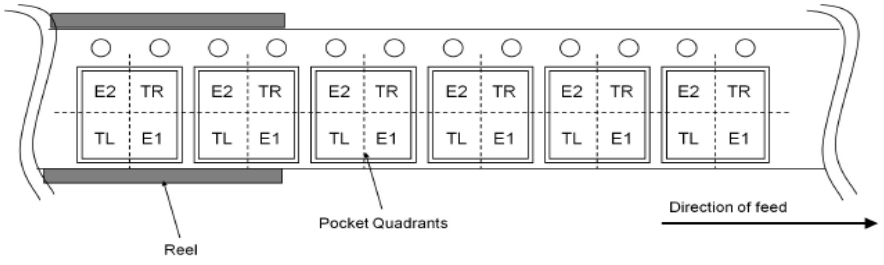
Physical Dimension and Packing Information

Package Name	SOP14K



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

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5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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