REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add new device types 02 and 03. Add case outline X for Leaded Chip Carrier package for device types 02 and 03 in figure 1. Update boilerplate paragraphs to current requirements of MIL-PRF-38535. - MAA	09-12-10	Thomas M. Hess

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A											
SHEET	15	16	17	18	19	20	21	22	23											
REV STATUS				REV			A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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DRAWING APPROVAL DATE
94-03-03

REVISION LEVEL
A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43218-3990
http://www.dscc.dla.mil

MICROCIRCUIT, DIGITAL, CMOS, LOW SKEW PLL CLOCK DRIVER, MONOLITHIC SILICON

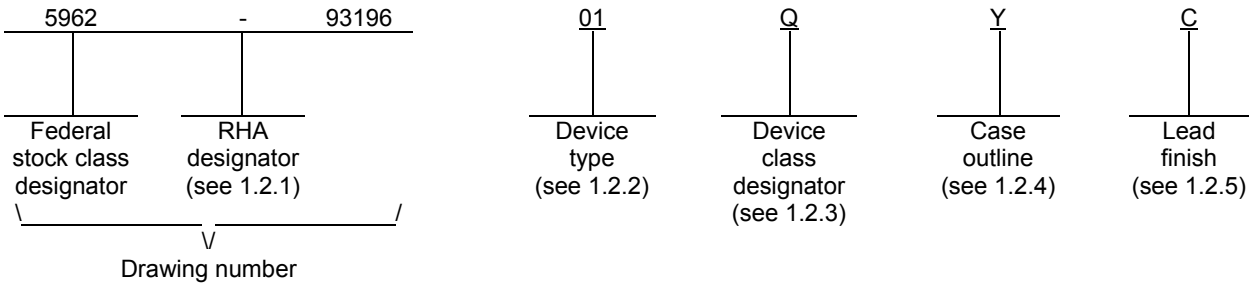
SIZE	CAGE CODE	
A	**67268**	**5962-93196**

SHEET 1 OF 23

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Maximum Clock frequency
01	88915	Low skew quad clock driver	55 MHz
02	TS88915T	Low skew PLL clock driver, TTL	70 MHz
03	TS88915T	Low skew PLL clock driver, TTL	100 MHz

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	see figure 1	28	Leaded Ceramic Chip Carrier
Y	see figure 1	28	Quad Flat package
Z	see figure 1	29	Pin grid array

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (reference to GND) V_{CC}	-0.5 V dc to +6.0 V dc
Input voltage range (reference to GND) V_{IN}	-0.5 V dc to V_{CC} + 0.5 V dc 2/
Output voltage range (reference to GND) V_{OUT}	-0.5 V dc to V_{CC} + 0.5 V dc
Output current (per pin) I_{OUT}	-±50 mA
Supply current V_{CC} or GND	-±100 mA
Maximum power dissipation (P_D) :	
For device type 01	300 mW
For device types 02 and 03	500 mW
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction-to-case (θ_{JC}):	
For device type 01, case Y	1.50 °C/W
For device type 01, case Z	6.74 °C/W
For device types 02 and 03 Case X and Z	7.0 °C/W

1.4 Recommended operating conditions.

Supply voltage range (reference to GND) $V_{CC:}$	
For device type 01	4.5 V dc to +5.5 V dc
For device types 02 and 03	4.75 V dc to +5.25 V dc
Input voltage range (reference to GND) V_{IN}	-0.0 V dc to V_{CC}
Output voltage range (reference to GND) V_{OUT}	-0.5 V dc to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Input rise or fall time rate, t_r, t_f	0 ns to 3.0 ns/v

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Input voltage must not be greater than the supply voltage by more than 2.5 V all times including power-on reset.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 398 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OH} = -36 mA	1, 3	01	3.86		V
			2		3.70		
		V_{CC} = 4.75 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OH} = -36 mA	1, 2, 3	02, 03	4.01		
		V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OH} = -12 mA (LOCK pin) 2/ 3/	1, 3	01	3.86		
			2		3.70		
		V_{CC} = 4.75 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OH} = -12 mA (LOCK pin)	1, 2, 3	02, 03	4.01		
		V_{CC} = 5.5 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OH} = -36 mA	1, 3	01	4.86		
			2		4.70		
		V_{CC} = 5.25 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OH} = -36 mA	1, 2, 3	02, 03	4.51		
		V_{CC} = 4.5 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OH} = -12 mA (LOCK pin) 2/ 3/	1, 3	01	4.86		
			2		4.70		
		V_{CC} = 5.25 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OH} = -12 mA (LOCK pin)	1, 2, 3	02, 03	4.51		
		V_{CC} = 5.5 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OH} = -88 mA	1, 2, 3	01	3.85		

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Low level output voltage	V_{OL}	For device type 01 at V_{CC} = 4.5 V, For device types 02,03 at V_{CC} = 4.75 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OL} = +36 mA	1, 3	All		0.44	V
			2			0.50	
		For device type 01 at V_{CC} = 4.5 V, For device types 02,03 at V_{CC} = 4.75 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OL}= +12 mA (LOCK pin) 2/	1, 3	All		0.44	
			2			0.50	
		For device type 01 at V_{CC} = 5.5 V, For device types 02,03 at V_{CC} = 5.25 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OL} = +36 mA	1, 3	All		0.44	
			2			0.50	
		For device type 01 at V_{CC} = 5.5 V, For device types 02,03 at V_{CC} = 5.25 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OL} = +12 mA (LOCK pin) 2/	1, 3	All		0.44	
			2			0.50	
		For device types 02,03 at V_{CC} = 4.75 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OL} = +15 mA	1, 2, 3	02, 03		0.50	
		For device types 02,03 at V_{CC} = 5.25 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OL} = +15 mA	1, 2, 3	02, 03		0.20	
		V_{CC} = 5.5 V, V_{IH} = 2.0 V, V_{IL} = 0.8 V I_{OL} = +88 mA	1, 2, 3	01		1.6	
Input high leakage current	I_{INH}	V_{CC} = 5.5 V, V_{IH} = 5.5 V, V_{IL} = 0.0 V	1, 3	01		±1.0	µA
			2			±2.0	
		V_{CC} = 5.25 V, V_{IN} = V_{CC} or GND, 5.5 V,	1, 2, 3	02, 03		±1.0	µA
Input low leakage current	I_{INL}	V_{CC} = 5.5 V, V_{IH} = 5.5 V, V_{IL} = 0.0 V	1, 3	01		±1.0	µA
			2			±2.0	
		V_{CC} = 5.25 V, V_{IN} = V_{CC} or GND, 5.5 V,	1, 2, 3	02, 03		±1.0	µA
Quiescent supply current	I_{CC}	V_{CC} = 5.5 V, I_{OUT} = 0.0 µA V_{IH} = 5.5 V, V_{IL} = GND, RC1 = 0 V	1, 2, 3	01		500	µA
		V_{CC} = 5.5 V, I_{OUT} = 0.0 µA V_{IH} = 5.5 V, V_{IL} = GND, RC1 = 2.4 V	1, 2, 3	01		3.0	mA
		V_{CC} = 5.5 V, I_{OUT} = 0.0 µA V_{IH} = 5.5 V, V_{IL} = GND, RC1 = 5.5 V	1, 2, 3	01		5.0	mA
		V_{CC} = V_{IH} = 5.25 V, V_{IL} = GND.	1, 2, 3	02, 03		1.0	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Additional quiescent supply current	I_{CCT}	V_{CC} = 5.5 V, I_{OUT} = 0.0 µA V_{IH} = 3.4 V (one input only) and all other inputs V_{IH} = 5.5 V V_{IL} = GND	1, 2, 3	01		1.6	mA
		V_{CC} = 5.5 V, I_{OUT} = 0.0 µA V_{IH} = 3.4 V (P/EN pin only) and all other inputs V_{IH} = 5.5 V V_{IL} = GND	1, 2, 3	01		3.0	mA
		$V_I = V_{CC} - 2.1\ V$, V_{CC} = 5.25 V 4/	1, 2, 3	02, 03		2.0	mA
		$V_{CC} = V_{IH}$ = 5.25 V, V_{IL} = GND.	1, 2, 3	02, 03		1.0	mA
Input capacitance	C_{IN}	V_{CC} = GND, T_A .= +25°C See 4.4.1c	4	01		6.5	pF
		V_{CC} = 5.0 V See 4.4.1c	4	02, 03	10 Typical		pF
Power dissipation capacitance	C_{PD}	V_{CC} = 5.0 V See 4.4.1c	4	02, 03	40 Typical		pF
Functional test		See 4.4.1b 4/	7, 8A, 8B	All	L	H	
Maximum operating clock frequency	f_{max1}	V_{IL} = 0.4 V, V_{IH} = 2.4 V V_{CC} = 4.5 V, C_L = 50 pF R_L = 100 Ω, Output Q*2 see figure 5 5/	9, 11	01	55		MHz
			10		50		
	f_{max2}	V_{IL} = 0.4 V, V_{IH} = 2.4 V V_{CC} = 4.5 V, C_L = 50 pF R_L = 100 Ω, Output Q0-Q4, $\overline{Q5}$ see figure 5 5/	9, 10, 11	01	27.5		MHz
	f_{max3}	V_{IL} = 0.4 V, V_{IH} = 2.4 V V_{CC} = 4.5 V, C_L = 50 pF R_L = 100 Ω, Output Q/2 see figure 5 5/	9, 10, 11	01	13.75		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Maximum operating clock frequency	f_{max4}	V_{CC} = 5.0 ± 5% V, Output 2X_Q see figure 5 6/	9, 10, 11	02	70		MHz
	f_{max5}	V_{CC} = 5.0 ± 5% V, Output Q0-Q4, $\overline{Q5}$ see figure 5 6/	9, 10, 11	02	35		MHz
	f_{max6}	V_{CC} = 5.0 ± 5% V, Output 2X_Q see figure 5 6/	9, 10, 11	03	100		MHz
	f_{max7}	V_{CC} = 5.0 ± 5% V, Output Q0-Q4, $\overline{Q5}$ see figure 5 6/	9, 10, 11	03	50		MHz
Propagation delay time SYNC to all Q's (test mode)	t_{PLH1}, t_{PHL1}	V_{IL} = 0.4 V, V_{IH} = 2.4 V V_{CC} = 4.5 V, C_L = 50 pF R_L = 100 Ω, Output Q*2 see figure 5 5/	9, 11	01	2.0	12.0	ns
			10		2.0	14.0	
Propagation delay time SYNC feedback (SYNC input to feedback delay measured at SYNC 0 to 1 and feedback pins)	t_{PD} 7/ 8/	V_{CC} = 5.0 ± 5% V, f_{max} = 70 MHz and 100 MHz R_L = 50 Ω terminated to $V_{CC}/2$	9, 10, 11	02, 03	1.25	3.25	ns
Propagation delay time $\overline{RST}$ to all Q's (test mode)	t_{PHL2}	V_{IL} = 0.4 V, V_{IH} = 2.4 V V_{CC} = 4.5 V, C_L = 50 pF R_L = 100 Ω, Output Q0-Q4, $\overline{Q5}$ see figure 5 5/	9, 11	01	1.5	6.5	ns
			10		1.5	8.0	
Propagation delay time SYC 0 or SYC1 to FDBK	t_{PLH2}	V_{IL} = 0.4 V, V_{IH} = 2.4 V V_{CC} = 4.5 V, C_L = 50 pF R_L = 100 Ω, see figure 5 5/	9, 10, 11	01	0.5	1.5	ns
Propagation delay time output enable time $\overline{OE}$ /$\overline{RST}$ to 2X_Q, Q0-Q4, $\overline{Q5}$ and Q/2	t_{PZL}	V_{CC} = 5.0 ± 5% V, f_{max} = 70 MHz and 100 MHz R_L = 50 Ω terminated to $V_{CC}/2$ Measured with the PLL_EN pin low.	9, 10, 11	02, 03	3.0	14.0	ns
Propagation delay time output disable time $\overline{OE}$ /$\overline{RST}$ to 2X_Q, Q0-Q4, $\overline{Q5}$ and Q/2	t_{PHZ}, t_{PLZ}	V_{CC} = 5.0 ± 5% V, f_{max} = 70 MHz and 100 MHz R_L = 50 Ω terminated to $V_{CC}/2$ Measured with the PLL_EN pin low.	9, 10, 11	02, 03	3.0	14.0	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Output rise and fall time	t_{TLH}, t_{THL}.	V_{IL} = 0.4 V, V_{IH} = 2.4 V V_{CC} = 4.5 V, C_L = 50 pF R_L = 100 Ω, see figure 5 5/	9, 10, 11	01	0.5	2.5	ns
	$t_{RISE/FALL}$	V_{CC} = 5.0 ± 5% V, R_L = 50 Ω terminated to $V_{CC}/2$ All output between 0.2 V_{CC} and 0.8 V_{CC} see figure 5 6/	9, 10, 11	02, 03	1.0	2.5	ns
Output to output skew rising edge only	t_{OSr1} 9/	V_{IL} = 0.4 V, V_{IH} = 2.4 V V_{CC} = 4.5 V, C_L = 50 pF R_L = 100 Ω, see figure 5 5/	9, 10, 11	01		3.0	ns
	t_{SKEWr} (RISING)	V_{CC} = 5.0 ± 5% V, Output Q0-Q4, Q/2 R_L = 50 Ω terminated to $V_{CC}/2$ see figure 5 6/	9, 10, 11	All		500	ps
Output to output skew falling edge only	t_{OSf1} 10/	V_{IL} = 0.4 V, V_{IH} = 2.4 V V_{CC} = 4.5 V, C_L = 50 pF R_L = 100 Ω, see figure 5 5/	9, 10, 11	01		3.0	ns
	t_{SKEWf} (Falling)	V_{CC} = 5.0 ± 5% V, Output 2X_Q, Q0-Q4, Q/2, $\overline{Q5}$ R_L = 50 Ω terminated to $V_{CC}/2$ see figure 5 6/	9, 10, 11	All		750	ps
Duty cycle skew	t_{DCS} 11/	V_{IL} = 0.4 V, V_{IH} = 2.4 V V_{CC} = 4.5 V, C_L = 50 pF R_L = 100 Ω, see figure 5	9, 10, 11	01		3.0	ns
RESET recovery time $\overline{RST}$ to SYNC test mode	t_{RR}		9, 11	01		9.0	ns
			10			12.0	
RESET $\overline{RST}$ pulse width	t_{PW}	V_{IL} = 0.4 V, V_{IH} = 2.4 V V_{CC} = 4.5 V, C_L = 50 pF R_L = 100 Ω, see figure 5 5/	9, 10, 11	01	5.0		ns
	t_{PW}	V_{CC} = 5.0 ± 5% V, R_L = 50 Ω terminated to $V_{CC}/2$ Output Q0-Q4, Q/2, $\overline{Q5}$ see figure 5 6/	9, 10, 11	02, 03	$0.5t_{cyc.}$ -0.5	$0.5t_{cyc.}$ +0.5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Time required to acquire phase-lock (LOCK) from SYNC inputs	t_{LOCK} 3/	$V_{IL} = 0.4\ V$, $V_{IH} = 2.4\ V$ $V_{CC} = 4.5\ V$, $C_L = 50\ pF$ $R_L = 100\ \Omega$, see figure 5 5/	9, 10, 11	01		10	ms
	t_{LOCK} 12/	$V_{CC} = 5.0 \pm 5\%\ V$, $R_L = 50\ \Omega$ terminated to $V_{CC}/2$ All output between $0.2\ V_{CC}$ and $0.8\ V_{CC}$ see figure 5 6/	9, 10, 11	02, 03	1.0	10	ms

1/ All testing to be performed using worst case test conditions unless otherwise specified.

2/ The LOCK pin may remain low, even though the device is phased-locked.

3/ This parameter is guaranteed, and not tested to the limits specified in table I.

4/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic pattern used for fault detection. Functional tests shall be performed in sequence as approved by the qualifying activity on qualify devices. H ≥0.5 V_{CC}, L < 0.5 V_{CC}; $V_{IH} = V_{IH}$ (min) +20 percent, -0 percent; V_{IL} (max) + 0 percent, -50 percent. Devices may be tested using any input voltage within this input voltage range but shall be guaranteed to V_{IH} (min) and V_{IL} (max).

5/ AC limits at V_{CC} = =5.5 V are guaranteed, if not tested to the limits specified in table I.

6/ Maximum operating frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50Ω terminated to $V_{cc}/2$.

7/ This specifications are not tested, they are guaranteed by statistical characterization.

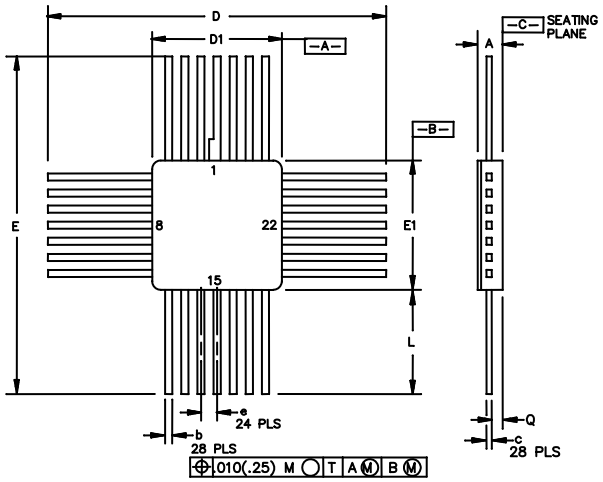
8/ The t_{PD} specification's min/max values may shift closer to zero of a larger pull up resistor is used.

9/ Calculated value (worst case) : t_{PLH1} (max) – t_{PLH1} (min) = t_{OSr1}.

10/ Calculated value (worst case) : t_{PHL1} (max) – t_{PHL1} (min) = t_{OSr1}.

11/ Calculated value (each output) : $t_{PLH1} – t_{PLH1} = t_{DCS}$.

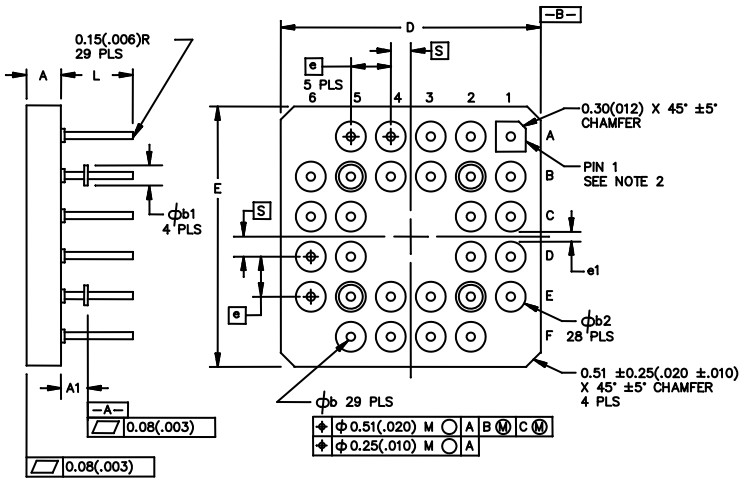
12/ With V_{CC} fully powered-on, and an output properly connected to the FEDBACK pin. t_{LOCK} maximum is with C1 = 0.1 µF, t_{LOCK} minimum is with C1 = 0.01 µF.



Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	1.52	2.03	0.060	0.080
B	0.36	0.48	0.014	0.019
C	0.10	0.18	0.004	0.007
D	23.88	25.65	0.940	1.010
D1	8.89	10.16	0.350	0.400
E	23.88	25.65	0.940	1.010
E1	8.89	10.16	0.350	0.400
e	1.27 BSC		0.050 BSC	
L	7.49	8.38	0.295	0.330
Q	0.89	1.09	0.035	0.043

Notes:
1. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. Dimension D1 and E1 allow for lid misalignment and glass meniscus.
3. Dimension Q shall be measured at the point of exist of the lead from the body.
4. Lead number 1 is identified by a tab located on the lead.
5. Dimension C includes solder lead finish.
6. Lead numbers are shown for reference only and do not appear on package.

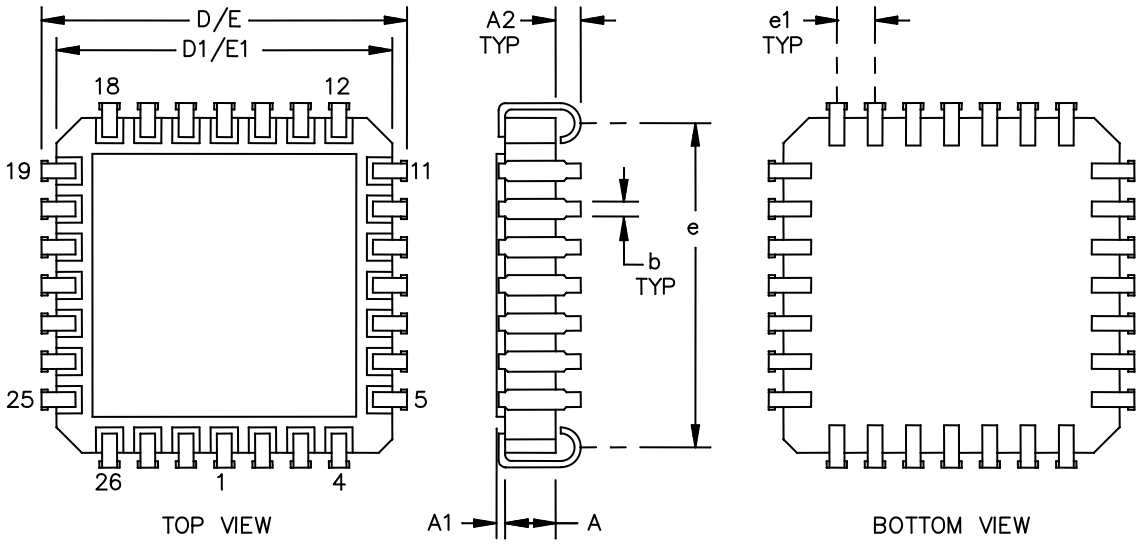
FIGURE 1. Case outline Y (device type 01).



Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	1.93	2.39	0.076	0.094
A1	1.14	1.40	0.045	0.055
Φb	0.43	0.48	0.017	0.019
Φb1	1.14	1.40	0.045	0.055
Φb2	1.52	1.78	0.060	0.070
D	15.09	15.39	0.594	0.606
E	15.09	15.39	0.594	0.606
e	2.54 BSC		0.100 BSC	
e1	0.64		0.025	
L	4.32	4.83	0.170	0.190
S	1.27 BSC		0.50 BSC	

Notes:
1. The US government preferred system of measurement is the metric SI system. However, this item was originally designed using inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence.
2. Pin 1 is identified by a 0.065 ± 0.005 square insulator.

FIGURE 1. Case outline Z (device type 01, 02 and 03) – continued.



Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	1.80	2.10	0.071	0.081
A1	1.37	1.67	0.054	0.066
b	0.43 typical		0.017 typical	
A2	0.89		0.035	
D/E	12.20	12.70	0.480	0.500
D1/E1	11.18	11.68	0.440	0.460
e	11.43	10.41	0.410	0.450
e1	1.27 typical		0.050 typical	

FIGURE 1. Case outline X (device types 02 and 03 Leaded Ceramic Chip Carrier) – continued.

Device type 01				Device type 02 and 03			
Case outlines Y		Case outline Z		Case outline X		Case outline Z	
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	GND	A1	NC	1	GND	A1	NC
2	$\overline{Q5}$	A2	V_{CC}	2	$\overline{Q5}$	A2	V_{CC}
3	V_{CC}	A3	GND	3	V_{CC}	A3	GND
4	$\overline{RST}$	A4	Q4	4	$\overline{OE}/\overline{RST}$	A4	Q4
5	FDBK	A5	Q*2	5	FEDBK	A5	Q*2
6	R/SL	B1	FDBK	6	REF_SEL	B1	FDBK
7	SYCO	B2	$\overline{RST}$	7	SYC0	B2	$\overline{RST}$
8	V_{CCA}	B3	$\overline{Q5}$	8	$V_{CC(AN)}$	B3	$\overline{Q5}$
9	RC1	B4	V_{CC}	9	RC1	B4	V_{CC}
10	GNDA	B5	Q/2	10	GND(AN)	B5	Q/2
11	SYC1	B6	GND	11	SYC1	B6	GND
12	F/SL	C1	SYC0	12	FREQ_SEL	C1	SYC0
13	GND	C2	R/SL	13	GND	C2	R/SL
14	Q0	C5	Q3	14	Q0	C5	Q3
15	VCC	C6	V_{CC}	15	V_{CC}	C6	V_{CC}
16	Q1	D1	V_{CCA}	16	Q1	D1	V_{CCA}
17	GND	D2	RC1	17	GND	D2	RC1
18	P/EN	D5	GND	18	PLL_EN	D5	GND
19	LOCK	D6	Q2	19	LOCK	D6	Q2
20	GND	E1	GNDA	20	GND	E1	GNDA
21	Q2	E2	SYC1	21	Q2	E2	SYC1
22	VCC	E3	GND	22	V_{CC}	E3	GND
23	Q3	E4	Q1	23	Q3	E4	Q1
24	GND	E5	P/EN	24	GND	E5	P/EN
25	Q/2	E6	LOCK	25	Q/2	E6	LOCK
26	Q*2	F2	F/SL	26	2X_Q	F2	F/SL
27	VCC	F3	Q0	27	V_{CC}	F3	Q0
28	Q4	F4	V_{CC}	28	Q4	F4	V_{CC}
		F5	GND			F5	GND

NC = No internal connection.

FIGURE 2. Terminal connections.

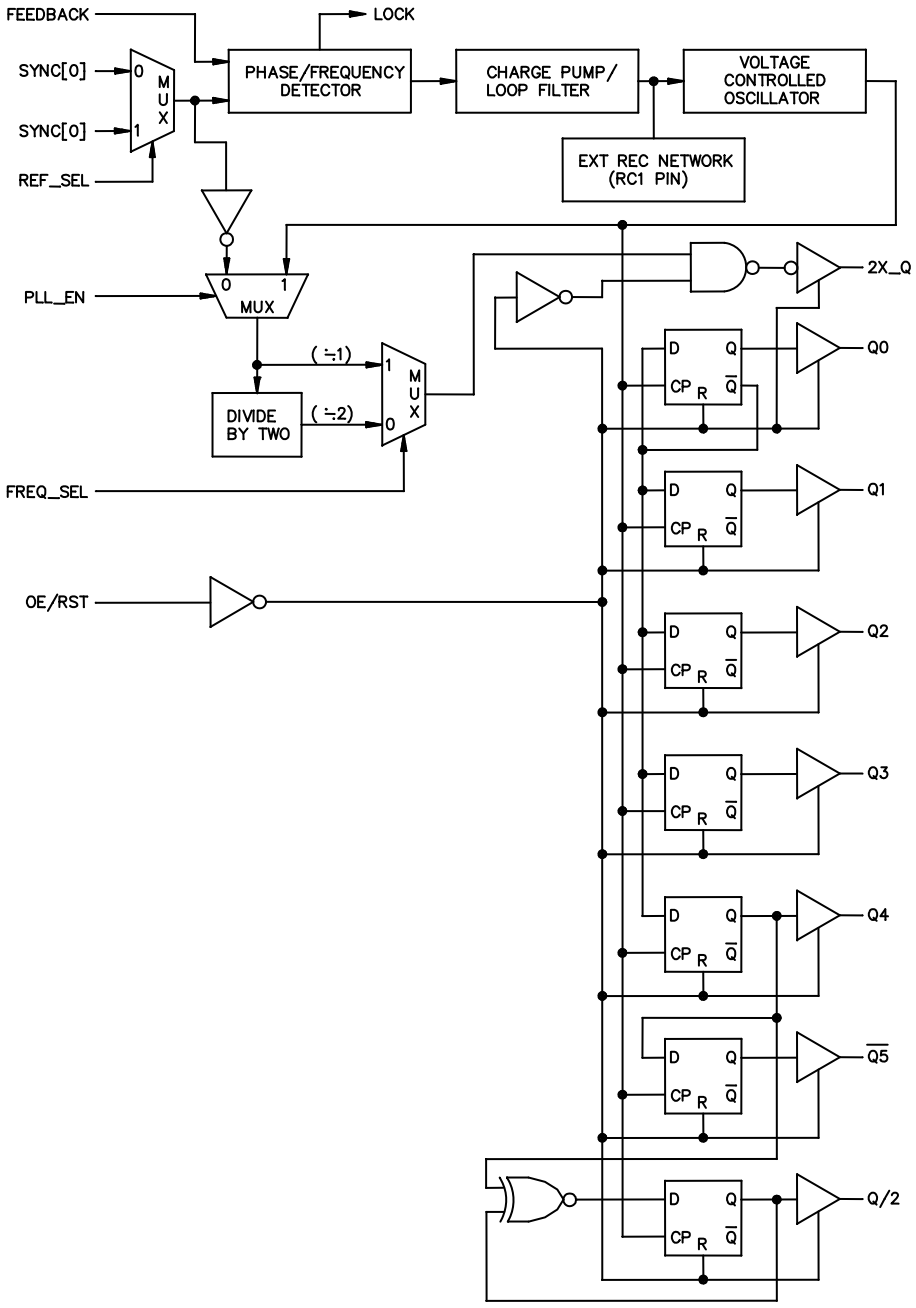
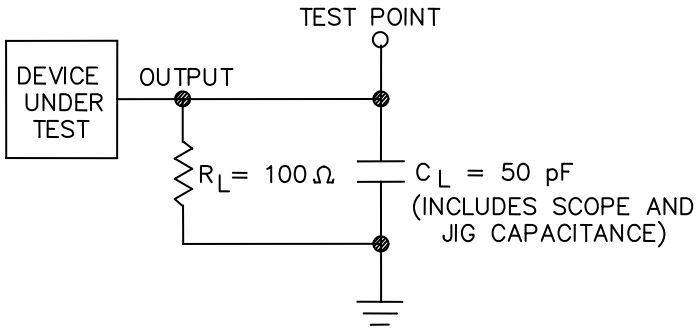


FIGURE 3. Logic diagram.



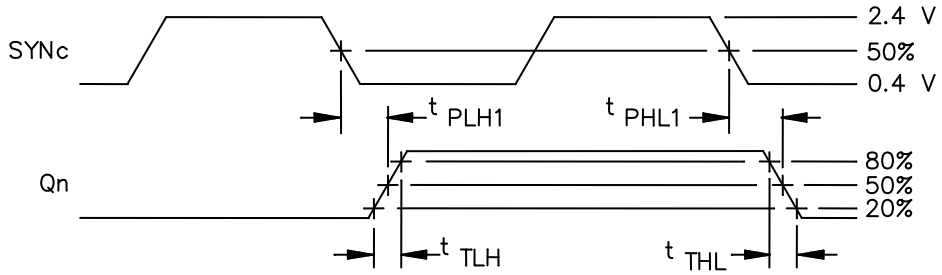


FIGURE 4. Test circuit and switching waveforms.

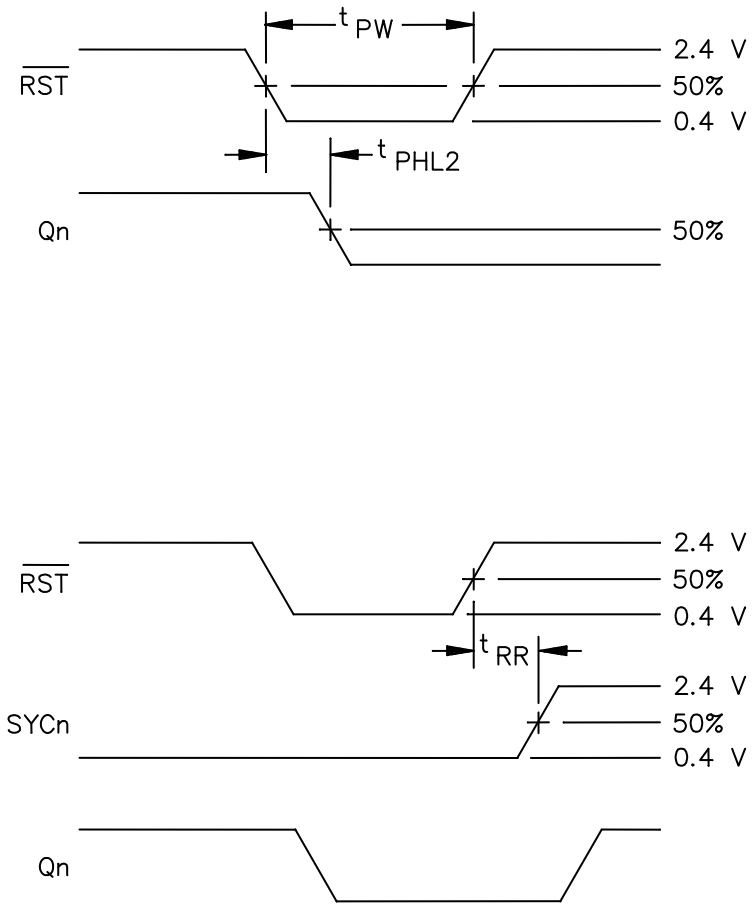
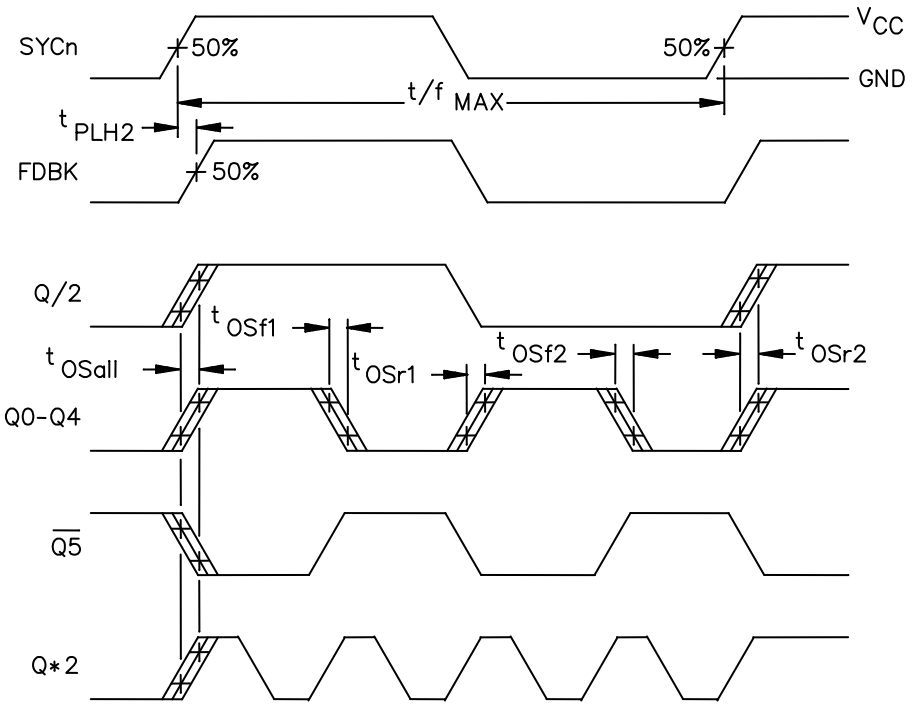


FIGURE 4. Test circuit and switching waveforms – Continued.



NOTE:

1. These waveform represent the 1:2 input to Q output frequency relationship.

FIGURE 4. Test circuit and switching waveforms – Continued.

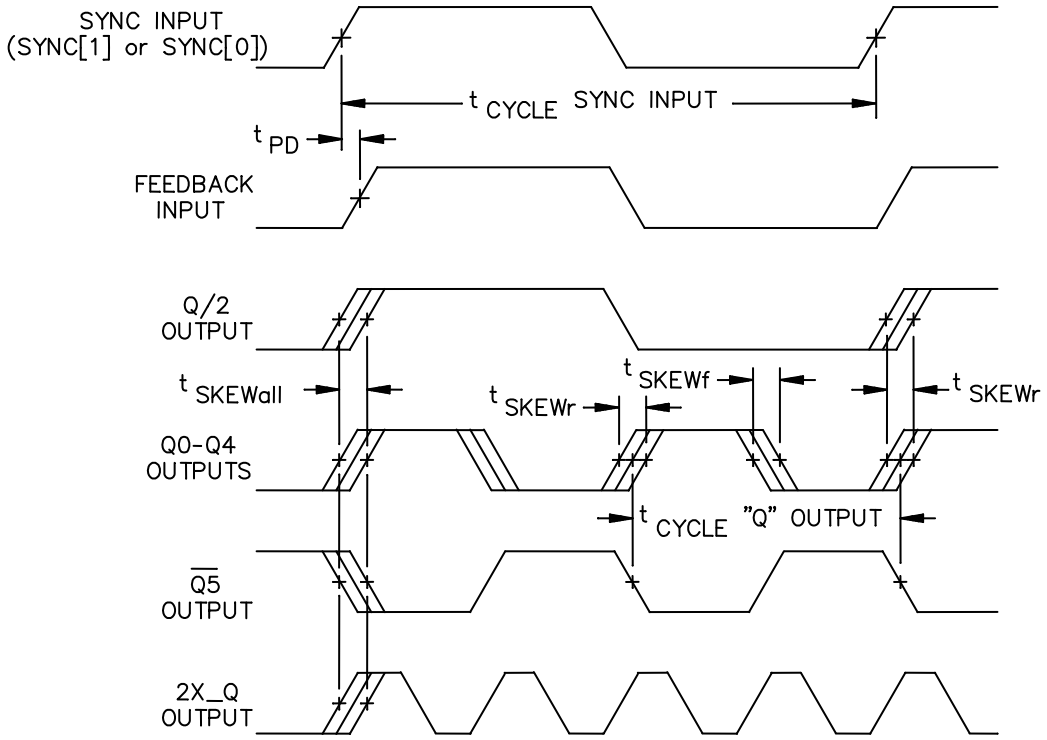


FIGURE 4. Test circuit and switching waveforms – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 2, 3	1, 2, 3	1, 2, 3
Final electrical parameters (see 4.2)	1, 2, 3, 7,8A, 8B, 9, 10, 11 1/	1, 2, 3, 7,8A, 8B, 9, 10, 11 1/	1, 2, 3, 7,8A, 8B, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7,8A, 8B, 9, 10, 11	11, 2, 3, 4, 7,8A, 8B, 9, 10, 11	1, 2, 3, 4, 7,8A, 8B, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3,	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	- - -		

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-12-10

Approved sources of supply for SMD 5962-93196 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/ .

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9319601QYC	3/	88915-55/BYAJC
5962-9319601QZC	3/	88915-55/BZAJC
5962-9319602QZC	F8385	TS88915TMRBQ70
5962-9319602QXC	F8385	TS88915TMWBQ70
5962-9319603QZC	F8385	TS88915TMRBQ100
5962-9319603QXC	F8385	TS88915TMWBQ100

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
F8385	E2V Semiconductors Avenue De Rochepleine BP 123 Saint Egreve CEDEX 38521, France

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.