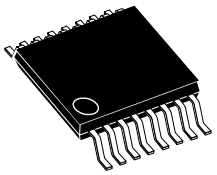
L6986I

Datasheet

38 V, 5 W synchronous iso-buck converter for isolated applications



HTSSOP16 (R_{TH}= 40 °C/W)

Maturity status link
L6986I

Features

- Designed for iso-buck topology
- 4 V to 38 V operating input voltage
- Primary output voltage regulation / no optocoupler required
- 1.9 A typical sink peak primary current capability
- Peak current mode architecture in forced PWM operation
- 300 ns blanking time
- 8 µA $I_{Q\text{-}SHTDWN}$
- Adjustable f_{SW} and synchronization
- Embedded primary output voltage supervisor
- Adjustable soft-start time
- Internal primary current limiting
- Overvoltage protection
- $R_{DS(on)\ HS}$ = 180 mΩ, $R_{DS(on)\ LS}$ = 150 mΩ
- Thermal shutdown

Applications

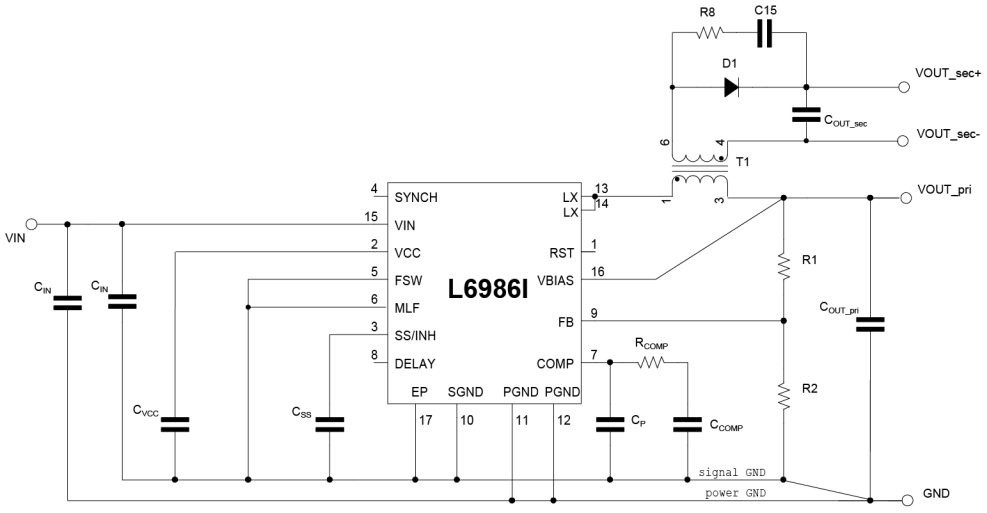
- Isolated power supply for SiC MOSFET and IGBT drivers
- Isolated power supply for isolated interfaces (RS232, I2C, SPI, etc.)
- EV chargers
- Motor drivers
- Automation
- UPS
- Solar converters
- Welding

Description

The L6986I is a device specifically designed for the isolated buck topology. Due to the P-Channel MOSFET as high-side power switch the device features 100% duty cycle operation. The primary output voltage can be accurately adjusted, whereas the isolated secondary output is derived by using a given transformer ratio. No optocoupler is required. The primary sink capability up to 1.9 A (even during soft-start) allows a proper energy transfer to the secondary side as well as enables a tracked soft-start of the secondary output. The control loop is based on a peak current mode architecture and the device operates in forced PWM. The 300 ns blanking time filters oscillations, generated by the transformer leakage inductance, making the solution more robust. Pulse by pulse current sensing on both power elements implements an effective constant current protection in the primary side. Due to the primary reverse current limit, the secondary output is protected against short circuit events. A primary output voltage supervisor, which notifies primary output voltage regulation through the RST open collector output, overvoltage protection, adjustable switching frequency, synchronization and a programmable soft-start are also available.

1 Application schematic

Figure 1. **Application schematic**



2 Pin connection

Figure 2. **Pin connection (top view)**

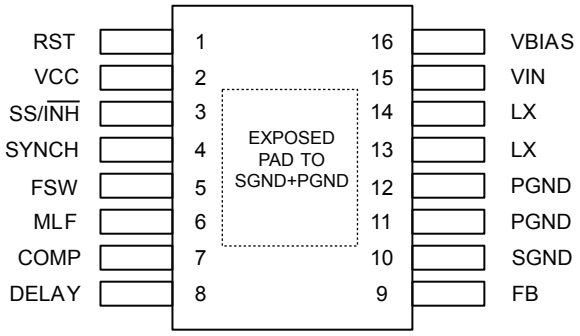


Table 1. **Pin description**

Number	Pin	Description
1	RST	The RST open collector output is driven low when the output voltage is out of regulation. The RST is released after an adjustable time DELAY once the primary output voltage is over the active delay threshold.
2	VCC	Connect a ceramic capacitor (≥ 470 nF) to filter internal voltage reference. This pin supplies the embedded analog circuitry.
3	SS / $\overline{\text{INH}}$	An open collector stage can disable the device clamping this pin to GND (INH mode). An internal current generator (4 µA typ.) charges the external capacitor to implement the soft-start.
4	SYNCH	The pin features master / slave synchronization. Leave this pin floating when it is not used.
5	FSW	A pull-up resistor (E24 series only) to VCC or pull-down to GND selects the switching frequency. Pin strapping is active only before the soft-start phase to minimize the IC consumption.
6	MLF	Connect this pin to ground either directly or through a pull-down resistor if the RST threshold should be adjusted (see Table 7).
7	COMP	Output of the error amplifier. The designed compensation network is connected at this pin.
8	DELAY	An external capacitor connected to this pin sets the time DELAY to assert the rising edge of the RST open collector after the output voltage is over the reset threshold. If this pin is left floating, RST is like a Power Good.
9	FB	Primary output voltage sensing
10	SGND	Signal GND
11	PGND	Power GND
12	PGND	Power GND
13	LX	Switching node
14	LX	Switching node
15	VIN	DC input voltage
16	VBIAS	Typically connected to the regulated primary output voltage, if it does not exceed 6 V. Otherwise connect it to GND.
-	Exposed pad	Exposed pad must be connected to SGND, PGND

2.1 Maximum ratings

Stressing the device above the rating listed in the table below may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
V_{IN}	See Table 1	-0.3	40	V
DELAY		-0.3	VCC + 0.3	V
PGND		SGND - 0.3	SGND + 0.3	V
SGND		-	-	V
V_{CC}		-0.3	(VIN + 0.3) or (max. 4)	V
SS /INH		-0.3	VIN + 0.3	V
MLF		-0.3	VCC + 0.3	V
COMP		-0.3	VCC + 0.3	V
VFB		-0.3	10	V
FSW		-0.3	VCC + 0.3	V
SYNCH		-0.3	VIN + 0.3	V
V_{BIAS}		-0.3	(VIN + 0.3) or (max. 6)	V
RST		-0.3	VIN + 0.3	V
LX		-0.3	VIN + 0.3	V
T_J	Operating temperature range	-40	150	°C
T_{STG}	Storage temperature range	-	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering 10 s.)	-	260	°C
I_{HS}, I_{LS}	High-side / low-side switch current	-	2	A

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction ambient (device soldered on the STMicroelectronics demonstration board)	40	°C/W
R_{thJC}	Thermal resistance junction to exposed pad for board design (not suggested to estimate T_J from power losses)	5	°C/W

Table 4. ESD protection

Symbol	Test conditions	Value	Unit
ESD	HBM	2	kV
	CDM	500	V
	CDM corner pins	750	V

3 Electrical characteristics

Table 5. Electrical characteristics (T_J = 25 °C, V_{IN} = 12 V unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max	Unit
V_{IN}	Operating input voltage range	-	4		38	V
V_{IN_H}	V_{CC} UVLO rising threshold		2.7		3.5	
V_{IN_L}	V_{CC} UVLO falling threshold		2.4		3.5	
I_{PK}	Peak current limit	Duty cycle < 20%	2.55			A
		Duty cycle = 100% closed loop operation	2.1			
I_{VY}	Valley current limit		2.7			
I_{VY_SNK}	Reverse current limit		1.285	1.9	2.61	
$R_{DS(on)HS}$	High-side R_{DSON}	I_{SW} = 1 A		0.18	0.36	Ω
$R_{DS(on)LS}$	Low-side R_{DSON}	I_{SW} = 1 A		0.15	0.30	
f_{SW}	Selected switching frequency	FSW pin strapping before SS	See Table 6			
I_{FSW}	FSW biasing current	SS ended		0	500	nA
I_{MLF}	MLF biasing current	SS ended		0	500	nA
D	Duty cycle (1)		0		100	%
$T_{ON\ MIN}$	Minimum on-time		281	330	383	ns
V_{CC} regulator						
V_{CC}	LDO output voltage	V_{BIAS} = GND (no switchover)	2.9	3.3	3.6	V
		V_{BIAS} = 5 V (switchover)	2.9	3.3	3.6	
SWO	V_{BIAS} threshold ($3\ V < V_{BIAS} < 5.5\ V$)	Switch internal supply from V_{IN} to V_{BIAS}	2.85		3.2	
		Switch internal supply from V_{BIAS} to V_{IN}	2.78		3.15	
Power consumption						
I_{SHTDWN}	Shutdown current from V_{IN}	VSS / INH = GND	4	8	15	µA
$I_{Q\ OPVIN}$	Quiescent current from V_{IN}	SWO V_{FB} = GND (NO SLEEP) V_{BIAS} = 3.3 V	0.5	1.5	5	mA
		NO SWO V_{FB} = GND (NO SLEEP) V_{BIAS} = GND	2	2.8	6	
$I_{Q\ OPVBIAS}$	Quiescent current from V_{BIAS}	SWO V_{FB} = GND (NO SLEEP) V_{BIAS} = 3.3 V	0.5	1.2	5	mA
Soft-start						
V_{INH}	V_{SS} threshold	SS rising	200	460	700	mV
$V_{INH\ HYST}$	V_{SS} hysteresis			75	140	
$I_{SS\ CH}$	C_{SS} charging current	$V_{SS} < V_{INH}$ or $t < T_{SS\ SETUP}$ or $V_{EA} + > V_{FB}$ (1)		1		µA
		$t > T_{SS\ SETUP}$ and $V_{EA} + < V_{FB}$ (1)		4		
$V_{SS\ START}$	Start of internal error amplifier ramp		0.995	1.1	1.150	V

Symbol	Parameter	Test condition	Min.	Typ.	Max	Unit
SS_{GAIN}	SS/INH to internal error amplifier gain			3		
Error amplifier						
V_{FB}	Voltage feedback		0.841	0.85	0.859	µA
I_{FB}	FB biasing current			50	500	nA
A_V	Error amplifier gain (1)			100		dB
I_{COMP}	EA output current capability		± 6	±12	±25	µA
Inner current loop						
g_{CS}	Current sense transconductance (VCOMP to inductor current gain) (1)	I_{pk} = 1 A		2.5		A/V
V_{PP*gCS}	Slope compensation (2)		0.45	0.75	1.1	A
Overvoltage protection						
V_{OVP}	Overvoltage trip (V_{OVP}/V_{REF})		1.15	1.2	1.25	
$V_{OVP\ HYST}$	Overvoltage hysteresis		0.5	2	5	%
Synchronization (fanout: 6 slave devices typ.)						
f_{SYNCH}	Synchronization frequency	FSW = V_{CC}	275		1000	kHz
		FSW = GND	475		2200	
$V_{SYN\ TH}$	SYNCH input threshold	SYNCH rising	0.70		1.2	V
I_{SYN}	SYNCH pull-down current	V_{SYN} = 1.2 V		0.7		mA
$V_{SYN\ OUT}$	High level output	5 mA sinking load	1.40			V
	Low level output	0.7 mA sourcing load			0.6	
Reset						
V_{THR}	Selected RST threshold	MLF pinstrapping before SS		2		%
$V_{THR\ HYST}$	RST hysteresis (1)				0.4	V
V_{RST}	RST open collector output	V_{IN} > V_{IN} HAND V_{FB} < V_{TH4} mA sinking load			0.8	
		2 < V_{IN} < V_{INH} 4 mA sinking load		2		%
Delay						
V_{THD}	RST open collector released as soon as V_{DELAY} > V_{THD}	V_{FB} > V_{THR}	1.19	1.234	1.258	V
$I_{D\ CH}$	C_{DELAY} charging current	V_{FB} > V_{THR}	1	2	3	µA
Thermal shutdown						
T_{SHDWN}	Thermal shutdown temperature (1)			165		°C
T_{HYS}	Thermal shutdown hysteresis (1)			30		

1. *Not tested in production.*
2. *Measured at f_{SW} = 250 kHz.*

Table 6. f_{SW} selection (T_J = 25 °C, V_{IN} = 12 V unless otherwise specified).

Symbol	R_{VCC} (E24 series)	R_{GND} (E24 series)	T_J	f_{SW} min.	f_{SW} typ.	f_{SW} max.	Unit
f_{SW}	0 Ω	NC	(1)	225	250	275	kHz
	1.8 kΩ	NC	(1) (2)	-	285	-	
	3.3 kΩ	NC		-	330	-	
	5.6 kΩ	NC		-	380	-	
	10 kΩ	NC		-	435	-	
	NC	0 Ω	(3)	450	500	550	
	18 kΩ	NC	(1)(3)	-	575	-	
	33 kΩ	NC		-	660	-	
	56 kΩ	NC		-	755	-	
	NC	1.8 kΩ		-	870	-	
	NC	3.3 kΩ	(3)	900	1000	1100	

1. *Synchronization as slave between 275 kHz and 1000 kHz.*
2. *Not tested in production.*
3. *Synchronization as slave between 475 kHz and 1000 kHz*

Figure 3. Circuit R_{VCC}, R_{GND}

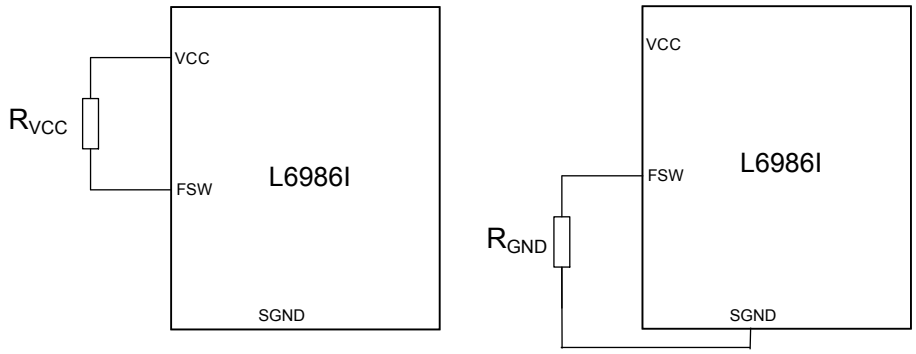


Table 7. RST threshold selection (T_J = 25 °C, V_{IN} = 12 V unless otherwise specified).

Symbol	R_{GND} (E241%)	V_{RST}/V_{OUT} (tgt. value)	V_{RST}min.	V_{RST}typ.	V_{RST}max.	Unit
V_{RST}	0 Ω (1)	93%	0.779	0.791	0.802	V
	8.2 kΩ ±1% (1)	80%	0.670	0.680	0.690	
	18 kΩ ±1% (1)	87%	0.728	0.740	0.751	
	39 kΩ ±1%	96%	0.804	0.816	0.828	

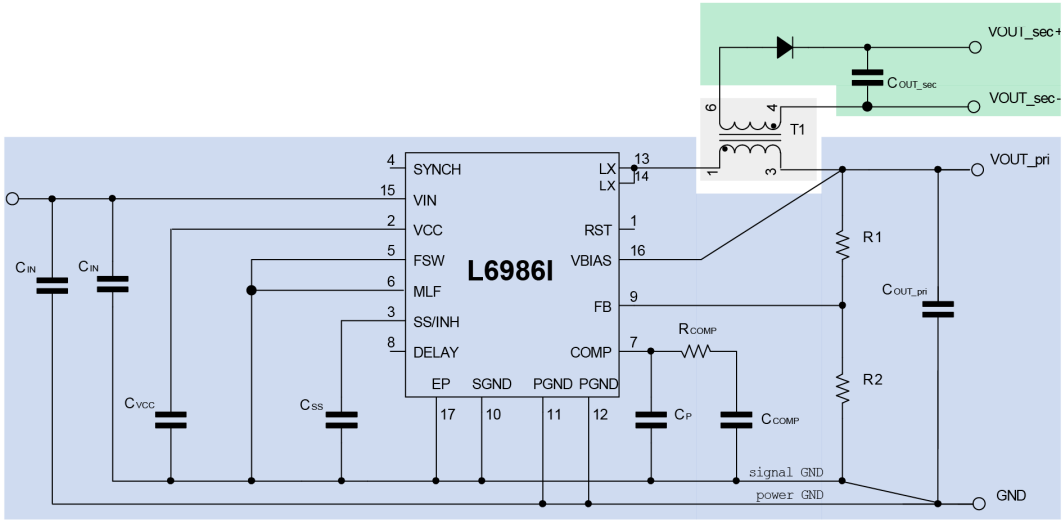
1. *please use the pre-defined resistor values.*
2. *do not exceed the indicated resistor value.*

4 Functional description

The iso-buck topology based on the L6986I consists of:

- Primary side, the regulation loop of the peak current mode architecture regulates the primary voltage (blue area in the picture below)
- A two-windings transformer (in grey)
- The secondary side, which generates the isolated output voltage (in green) given the selected transformer ratio

Figure 4. Iso-buck general schematic



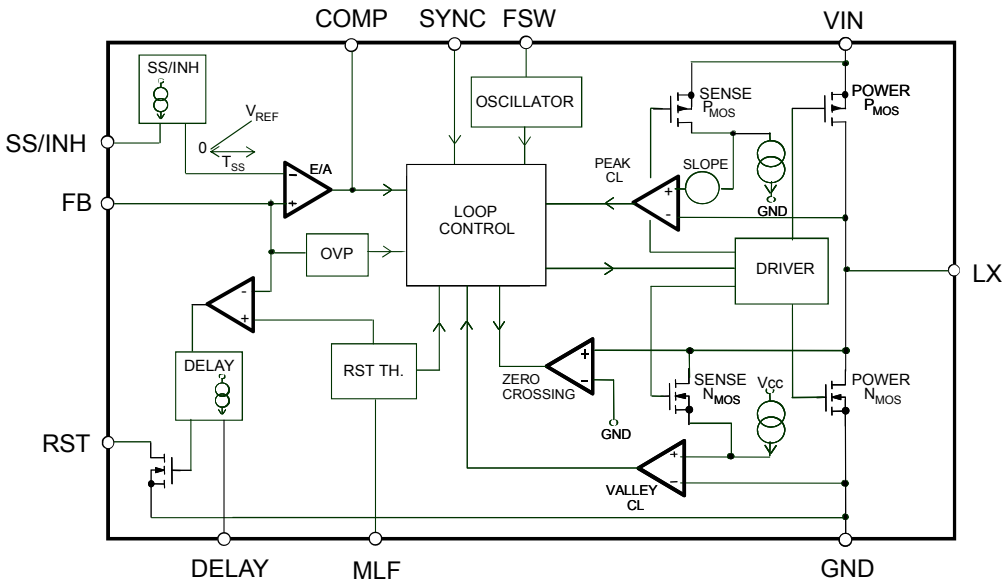
4.1 Primary side

The L6986I is based on a “peak current mode”, constant frequency control. The intersection between the error amplifier output and the sensed inductor current generates the PWM control signal to drive the power switch of the primary side, defining so the duty-cycle and regulating the primary output voltage.

The device operates in forced PWM control (MLF pin to GND), allowing negative currents to flow in the synchronous MOSFET, hence transferring energy to the secondary coil during the off-time.

The main internal blocks shown in the block diagram in figure below are:

Figure 5. **Internal block diagram**



- Embedded power elements. Thanks to the P-channel MOSFET as high-side switch the device features low- dropout operation
- A fully integrated sawtooth oscillator with adjustable frequency
- A transconductance error amplifier
- An internal feedback divider $G_{DIV\ INT}$
- The high-side current sense amplifier to sense the inductor current
- A “Pulse Width Modulator” (PWM) comparator and the driving circuitry of the embedded power elements
- The soft-start blocks to ramp the error amplifier reference voltage and so decreases the inrush current at power-up. The SS/$\overline{INH}$ pin inhibits the device when driven low
- The switchover capability of the internal regulator to supply a portion of the quiescent current when the V_{BIAS} pin is connected to an external output voltage
- The synchronization circuitry to manage master / slave operation and the synchronization to an external clock
- The current limitation circuit to implement the constant current protection, sensing pulse by pulse high-side / low-side switch current. In case of heavy short-circuit the current protection is fold back to decrease the stress of the external components
- A circuit to implement the thermal protection function
- The OVP circuitry to discharge the output capacitor in case of overvoltage event
- MLF normally connected to GND through a resistor to set the threshold of the RST comparator
- FSW pin strapping sets the switching frequency
- The RST open collector output

4.1.1 Power supply and voltage reference

The internal regulator block consists of a start-up circuit, the voltage pre-regulator that provides current to all the blocks and the bandgap voltage reference. The starter supplies the start-up current when the input voltage goes high and the device is enabled (SS/$\overline{INH}$ pin over the inhibits threshold).

The pre-regulator block supplies the bandgap cell and the rest of the circuitry with a regulated voltage that has a very low supply voltage noise sensitivity.

4.1.2 Switchover feature

The switchover scheme of the pre-regulator block is used to derive the main contribution of the supply current for the internal circuitry from an external voltage (3 V < V_{BIAS} < 5.5 V is typically connected to the primary regulated output voltage). This helps to decrease the equivalent quiescent current seen at V_{IN}.

4.1.3 Voltage monitor

An internal block continuously senses the V_{CC}, V_{BIAS} and V_{BG} (bandgap). If the monitored voltages are good, the regulator starts operating. There is also a hysteresis on the V_{CC} (UVLO).

4.1.4 Error amplifier

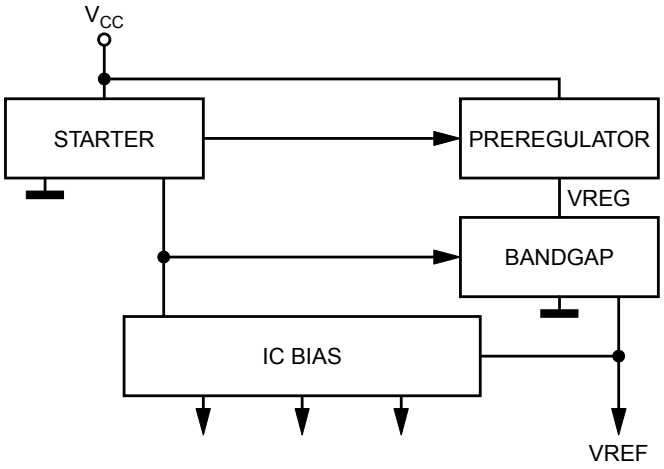
The voltage error amplifier is the core of the loop regulation of the primary output voltage. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (0.85 V), while the inverting input (FB) is connected to the external divider or directly to the output voltage.

Table 8. Uncompensated error amplifier characteristics

Description	Value
Transconductance	155 µS
Low frequency gain	100 dB

The error amplifier output is compared with the inductor current sense information to perform PWM control.

Figure 6. Internal circuit



4.2 Transformer

The transformer is the key component for the iso-buck, ensuring the desired isolation as well as allowing the energy transfer to the secondary side, hence generating the secondary isolated output voltage.

More details about the transformer selection are provided in the dedicated section (see Section 4.4.)

4.3 Secondary side

The secondary side includes an LC filter (secondary winding of the transformer and secondary output capacitor) and the rectifying element (Schottky diode).

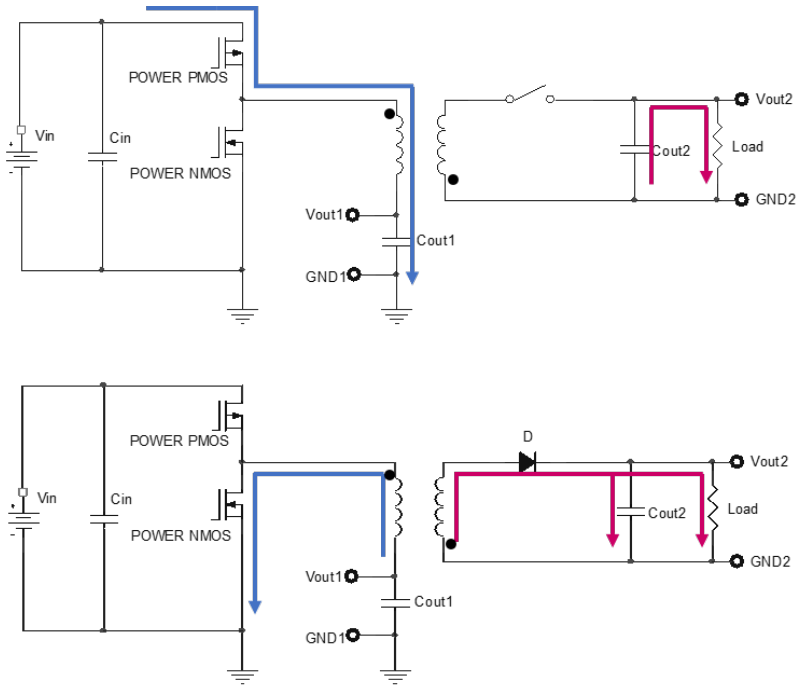
4.4 Iso-buck operation principle

The picture below describes the operation principle of the iso-buck converter.

When the high-side MOSFET is turned on, the current flows through the primary winding of the transformer and charges the primary output capacitor. Considering the dot convention of the transformer, the voltage at the anode of the Schottky diode is negative, hence the diode is reverse biased and no current flows in the secondary winding. The load connected to the secondary output is supplied by C_{OUT2}.

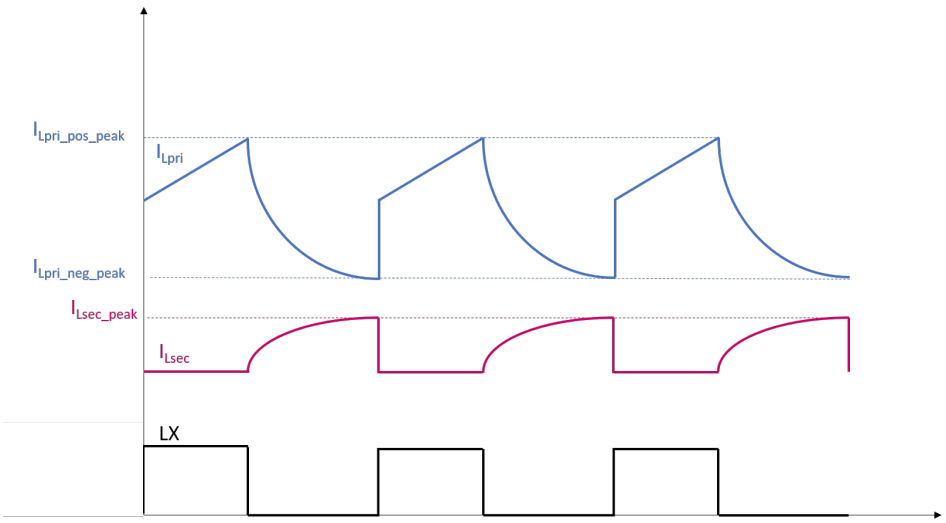
When the low-side MOSFET is turned on, the voltage applied at the transformer windings inverts its polarity. As consequence, the Schottky diode is now forward biased and allows the current to flow from the secondary winding to C_{OUT} and the load. Under this condition the energy transfer from primary to secondary side occurs.

Figure 7. Iso-buck basic operating principle



The waveforms in the figure below reproduce the trend of the current in the two windings in according to the switch node transitions.

Figure 8. Iso-buck primary and secondary current waveforms



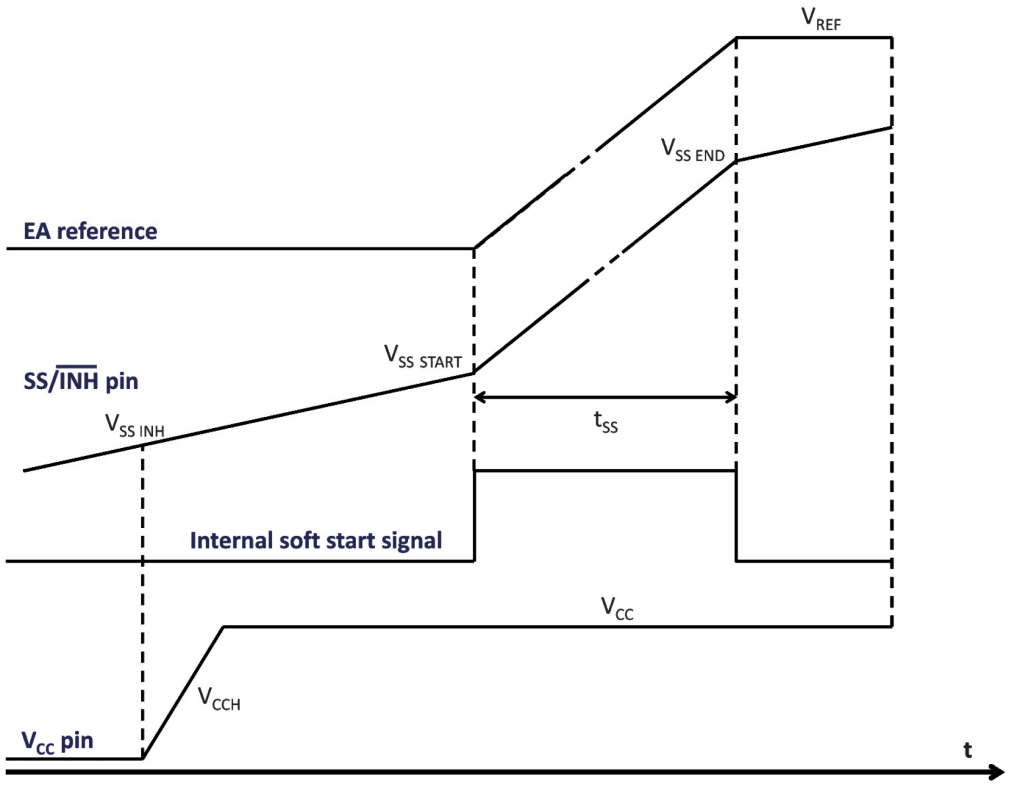
4.5 Soft-start and inhibit

The soft-start and inhibit features are multiplexed on the same pin. An internal current source charges the external soft-start capacitor to implement a voltage ramp on the SS/$\overline{INH}$ pin. The device is inhibited as long as the SS/$\overline{INH}$ pin voltage is lower than the V_{INH} threshold and the soft-start takes place when SS/$\overline{INH}$ pin crosses V_{SS} START. (See figure below).

The internal current generator sources 1 µA typ. current when the voltage of the V_{CC} pin crosses the UVLO threshold. The current increases to 4 µA typ. as soon as the SS/$\overline{INH}$ voltage is higher than the V_{INH} threshold. This feature helps to decrease the current consumption in inhibit mode. An external open collector can be used to set the inhibit operation clamping the SS/$\overline{INH}$ voltage below V_{INH} threshold.

The start-up feature minimizes the inrush current and decreases the stress of the power components during the power-up phase. The ramp implemented on the reference of the error amplifier has a gain three times higher (SS_{GAIN}) than the external ramp present at SS/$\overline{INH}$ pin.

Figure 9. Soft-start phase



The C_{SS} value is chosen accordingly with equation (1)

$$C_{SS} = SS_{GAIN} \cdot \frac{I_{SSCH} \cdot T_{SS}}{V_{FB}} = 3 \cdot \frac{4\mu A \cdot T_{SS}}{0.85V} \quad (1)$$

where T_{SS} is the soft-start time, $I_{SS\ CH}$ the charging current and V_{FB} the reference of the error amplifier.

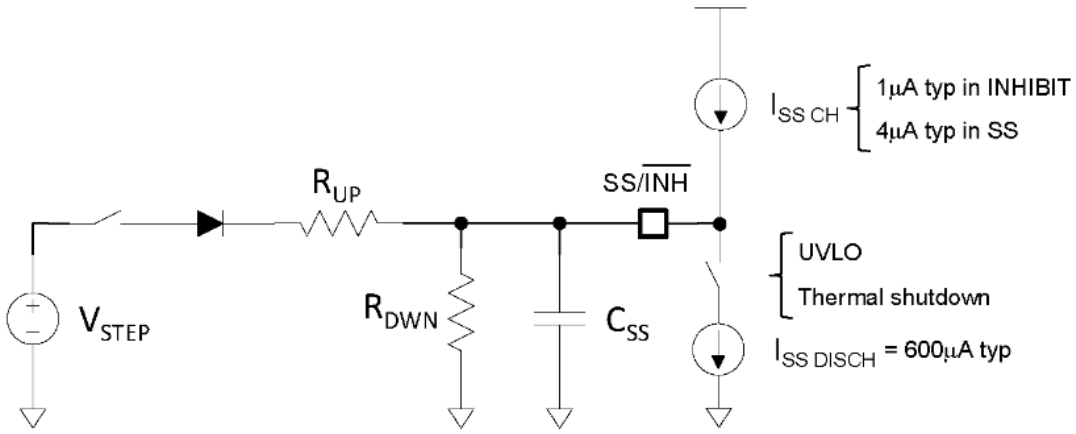
During normal operation a new soft-start cycle takes place in case of:

- Thermal shutdown event
- UVLO event
- The device is driven in INH mode

The soft-start capacitor is discharged with a 0.6 mA typ. current capability for 1 ms time max. For complete and proper capacitor discharge in case of fault conditions, a maximum C_{SS} = 67 nF value is suggested.

In case the soft-start should be externally driven by a voltage step, the circuitry in figure below can be used.

Figure 10. **Enable the device with external voltage step**

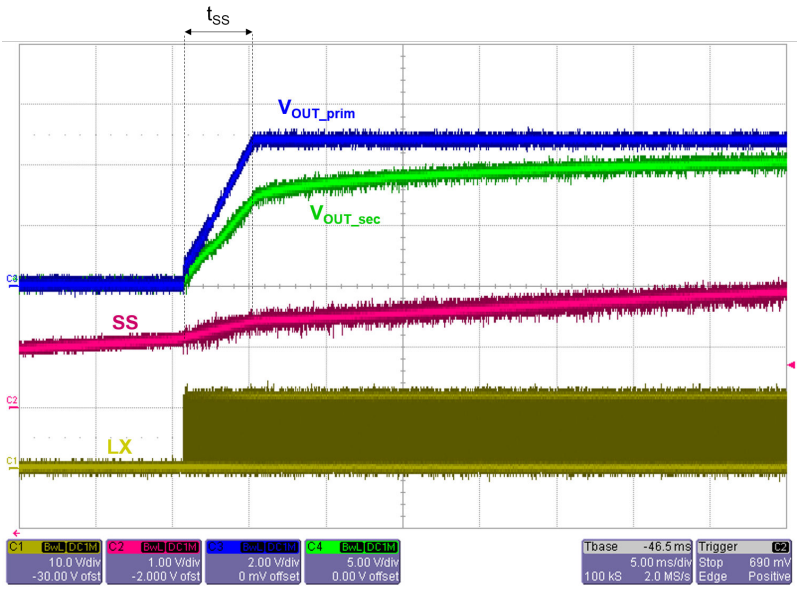


More details about the component selection can be found in Section 6.5: Design of the external components.

Secondary side soft-start

As soon as the soft-start begins at the primary circuit, the device already operates in forced PWM and the energy transfer to the secondary coil during the off-time can take place. Consequently, a tracked soft-start at the secondary side takes place too. Therefore, the secondary output voltage reaches its steady state value in tracking with the primary output voltage, as shown in figure below.

Figure 11. **Tracked soft-start at secondary side**



4.6 Minimum On-Time

The current sense in the high-side MOSFET is not active (masked) for a certain time at the beginning to the on-time (masking time, from which the parameter $T_{ON\ MIN}$ derives).

This current sense blanking time is implemented to prevent any primary side pulsed current at the high side turn-on (resonating with transformer drive leakage inductance and secondary side capacitance) overcomes the EA programmed switch current for the conversion and make to conversion unstable (depicted in Figure 12 and Figure 13. Simulation with appropriate masking time (330 ns)).

Figure 12. Simulation with insufficient masking time (< 100 ns)

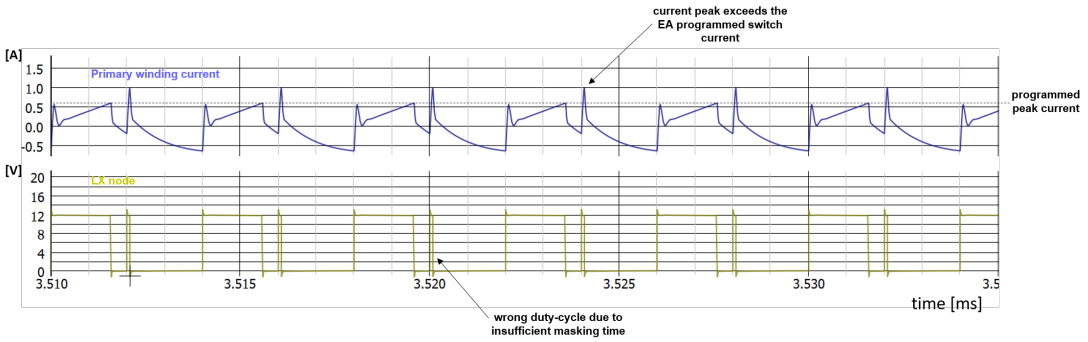
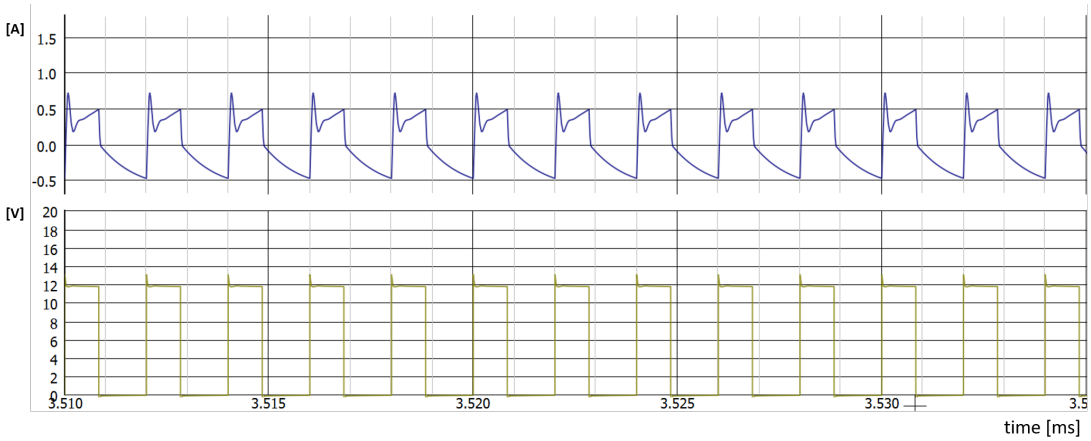
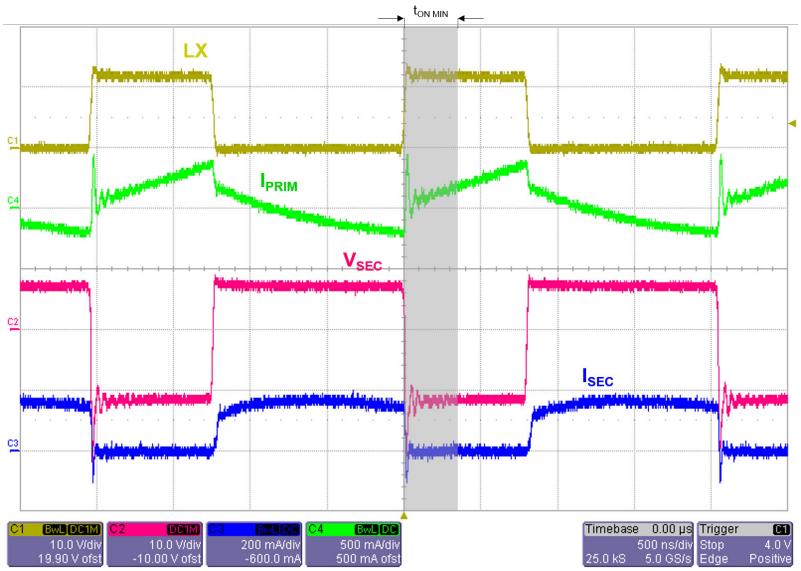


Figure 13. Simulation with appropriate masking time (330 ns)



Despite the masking time, an RC snubber circuit is normally recommended to dampen the oscillations. The figure below shows a typical application where the appropriate masking time is implemented as well as an RC snubber circuit.

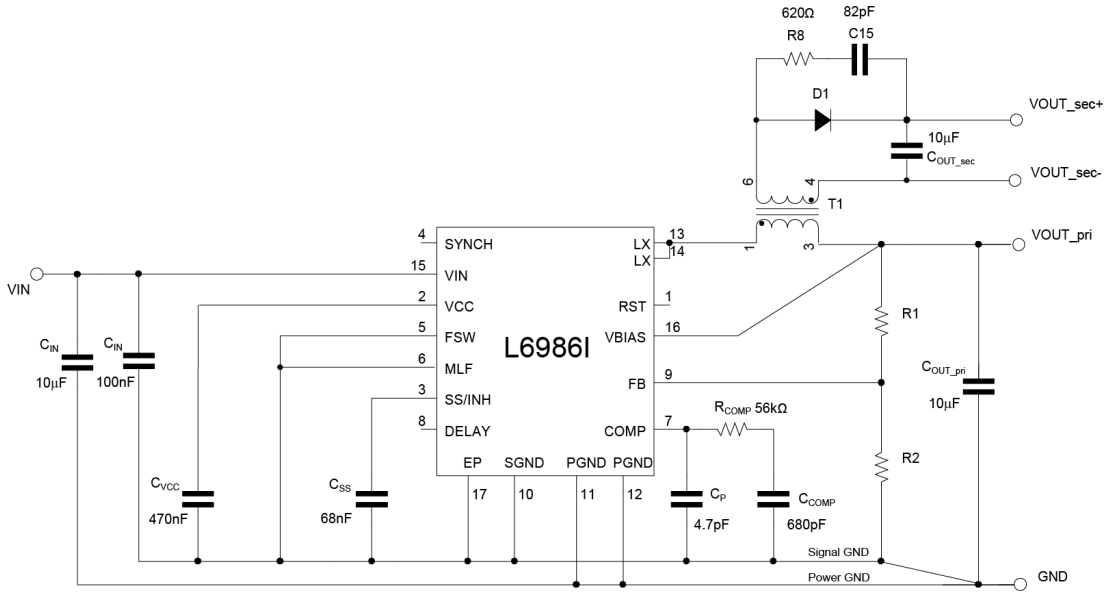
Figure 14. Remaining oscillations filtered by the masking time and RC snubber circuit V_{IN} = 12 V, N = 1.58, I_{OUTiso} = 100 mA



4.7 Output voltage line regulation

All results shown in this section come from measurements performed using the reference schematic depicted in figure below.

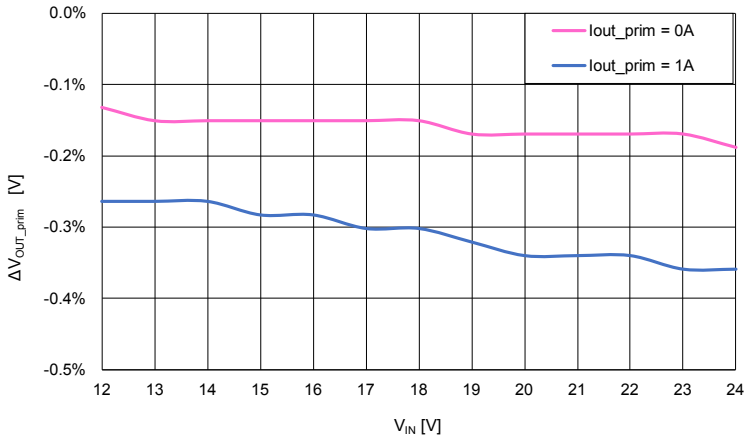
Figure 15. Schematic used for line and load regulation tests



Primary output line regulation

The regulator features an enhanced primary line regulation due to the peak current mode architecture. Figure 16 shows negligible output voltage variation (normalized to the value measured at V_{IN} = 12 V) over an input voltage range up to 24 V for L6986I with V_{OUT} prim = 5.3 V.

Figure 16. Primary line regulation

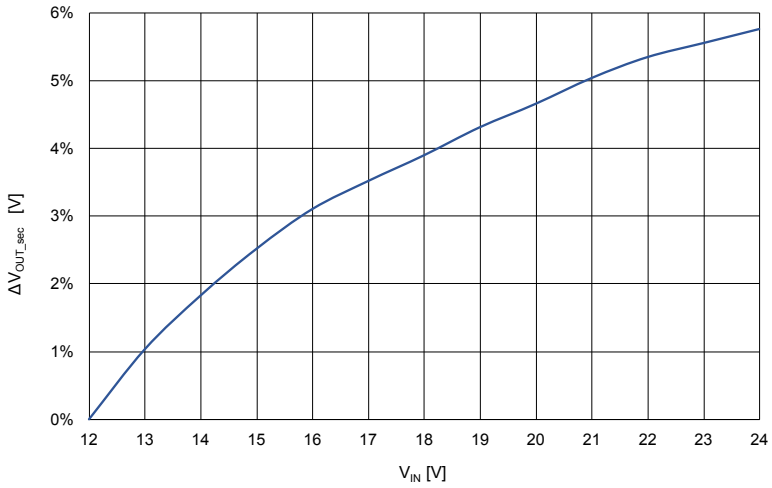


Secondary output line regulation

The secondary output line regulation is defined, similarly to the primary side, as the variation of secondary the output voltage due to the input voltage change at a specific current. The secondary output line regulation is mainly affected by the transformer and in particular by its leakage inductance.

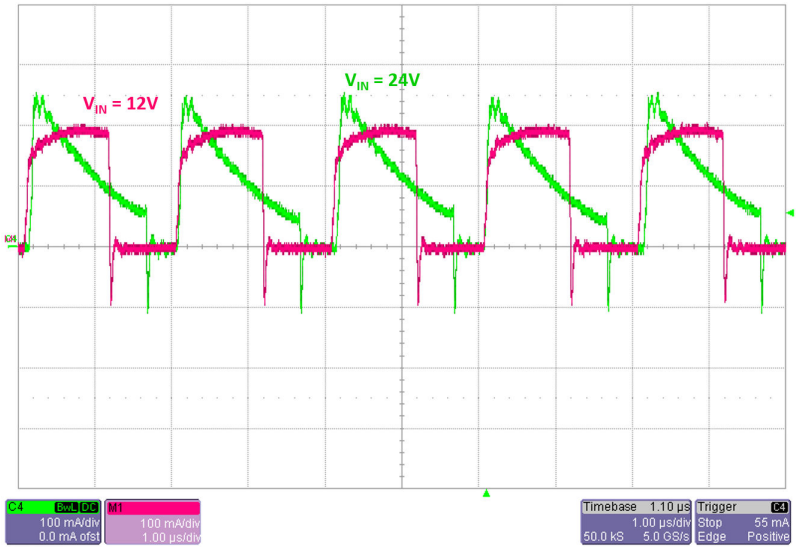
Keeping constant the leakage inductance (i.e. using the same transformer), an higher input voltage allows to slightly increase the isolated output voltage, as shown in figure below.

Figure 17. **Secondary output line regulation**



The input voltage value influences the peak current in the secondary winding (see figure below), hence determining the amount of energy delivered to the secondary output and in turn the isolated output voltage value.

Figure 18. **Secondary winding current at different input voltages**

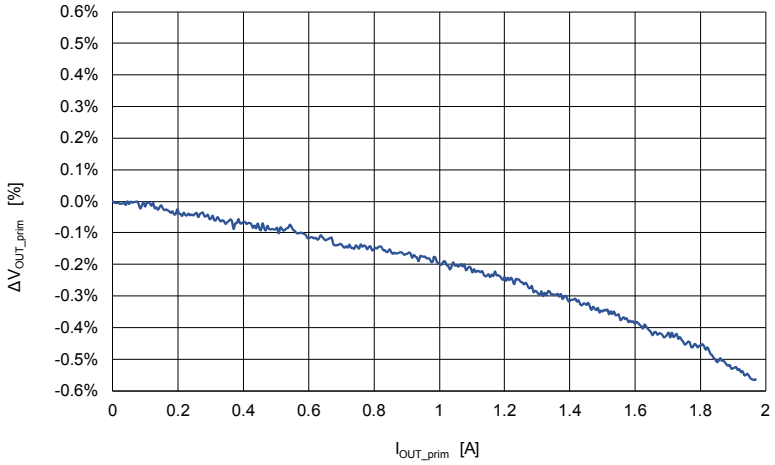


4.8 Output voltage load regulation

Primary output load regulation

Figure below shows negligible primary output voltage variation (normalized to the value measured at I_{OUT} = 0 A) over the entire output current range for the L6986I with V_{OUT} = 5.3 V.

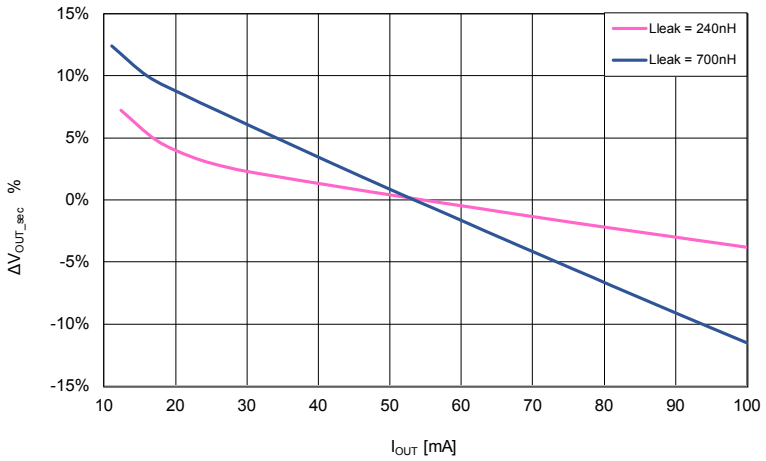
Figure 19. Load regulation of the not isolated output



Secondary output load regulation

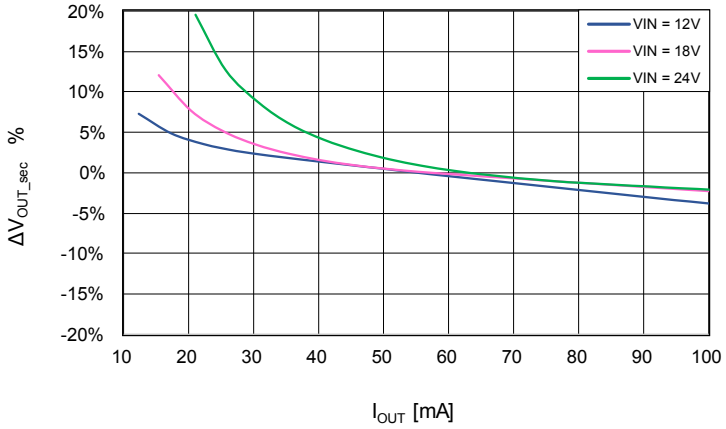
Since there is not a regulation loop involving the secondary output, its load regulation depends to some extent on the primary load regulation and is affected by the leakage inductance (see figure below) of the transformer, the voltage drops across to the Schottky diode (diode forward voltage) and the DCR of the secondary coil, as indicated by the equation (1) (where only the last two contribution are considered). Minimizing all the mentioned parameters leads to a better load regulation.

Figure 20. Effect of the transformer leakage inductance on the isolated output load regulation



The input voltage also plays a role in the isolated output regulation. The figure below further proves the slight dependency of the isolated output voltage on the input voltage.

Figure 21. **Input voltage effect on the load regulation of the isolated voltage**



4.9 Overcurrent protection

Protection against over current conditions and/or short circuit at the output is ensured at both primary and secondary side of the iso-buck converter.

Overcurrent protection at the primary side

The current protection circuitry features a constant current protection, so the device limits the maximum peak current (see Table 5) in overcurrent condition.

The L6986I device implements a pulse by pulse current sensing on both power elements (high-side and low-side switches), ensuring an effective current protection over the duty cycle range. The high-side current sensing is called “peak” the low-side sensing “valley”.

The internal noise generated during the switching activity makes the current sensing circuitry ineffective for a minimum conduction time of the power element. This time is called “masking time” because the information from the analog circuitry is masked by the logic to prevent an erroneous detection of the overcurrent event. Consequently, the peak current protection is disabled for a masking time after the high-side switch is turned on, the valley for a masking time after the low-side switch is turned on. In other words, the peak current protection can be ineffective at extremely low duty cycles, the valley current protection at extremely high duty cycles.

Summarizing, in case one of the two current sensing circuitry is ineffective because of the masking time, the device is protected sensing the current on the opposite switch. Thus, the combination of the “peak” and “valley” current limits assures the effectiveness of the overcurrent protection even in extreme duty cycle conditions.

The valley current threshold is designed higher than the peak to guarantee a proper operation. In case the current diverges because of the high-side masking time, the low-side power element is turned on until the switch current level drops below the valley current sense threshold. Under this condition the device can skip some cycle, leading to a switching frequency reduction. The Figure 22 shows an example of valley current limit intervention in a short circuit event (switching frequency set to 500 kHz, actual switching frequency 250 kHz).

Figure 22. **Valley current sense operation in short circuit**

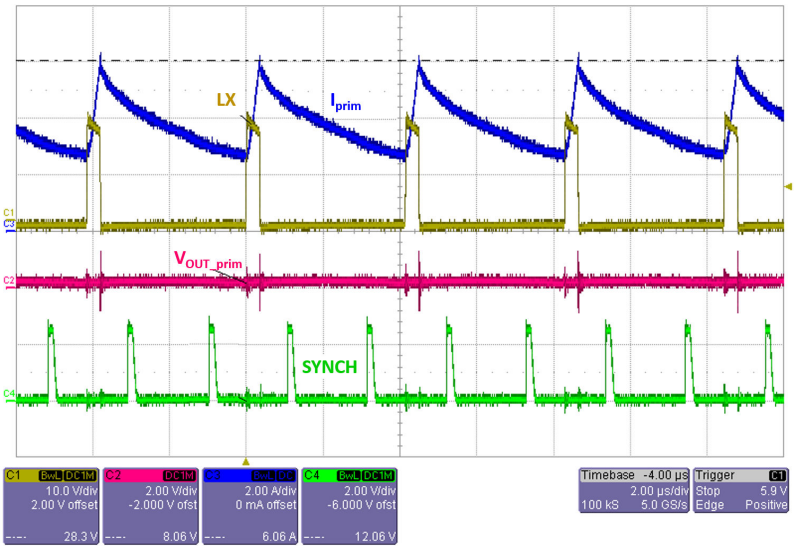


Figure 22 shows the switching frequency reduction during the valley current sense operation in case of extremely low duty cycle (V_{IN} = 12 V, f_{SW} = 2 MHz short-circuit condition).

In a worst case scenario of the overcurrent protection the switch current is limited to:

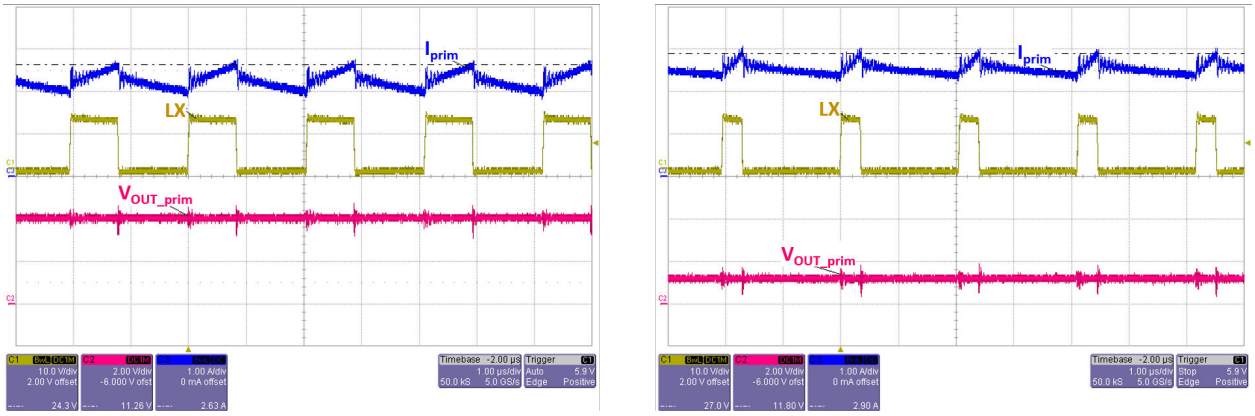
$$I_{MAX} = I_{VALLEYTH} + \frac{V_{IN} - V_{OUT}}{L} \cdot T_{MASKHS} \quad (2)$$

where I_{VALLEY_TH} is the current threshold of the valley sensing circuitry (see Table 1) and T_{MASK_HS} is the masking time of the high-side switch 330 ns typ.).

In most of the overcurrent conditions the conduction time of the high-side switch is higher than the masking time and so the peak current protection limits the switch current.

$$I_{MAX} = I_{PEAK\_TH} \quad (3)$$

Figure 23. **Peak current sense operation in overcurrent condition**



This figure shows the effect of the peak current protection. On the left the current (blue waveform) during the on time reaches the peak current protection threshold. From this point on, any increase of the output current causes the on-time to be reduced (picture on the right) so that the current provided to the output is limited. As a consequence, the output voltage drops, as the purple waveform depicts.

The DC current flowing in the load in overcurrent condition is:

$$I_{DCOC}(V_{OUT}) = I_{MAX} - \frac{V_{IN} - V_{OUT}}{2L} \cdot T_{ON} \quad (4)$$

Overcurrent protection at the secondary side

The increase of the secondary output current affects the current shape at primary side. In particular, the peak currents in the high side and low side MOSFETs rise (in absolute value in the low side, i.e. the current becomes more negative), in accordance with equations (5) and (6)).

$$I_{PEAK_{HS}} = I_{OUT\_pri} + N \cdot I_{OUT\_sec} + \frac{\Delta I_L}{2} \quad (5)$$

$$I_{PEAK_{LS}} = -N \cdot I_{OUT\_sec} \cdot \left(\frac{2D}{1-D}\right) - \frac{\Delta I_L}{2} + I_{OUT\_prim} \quad (6)$$

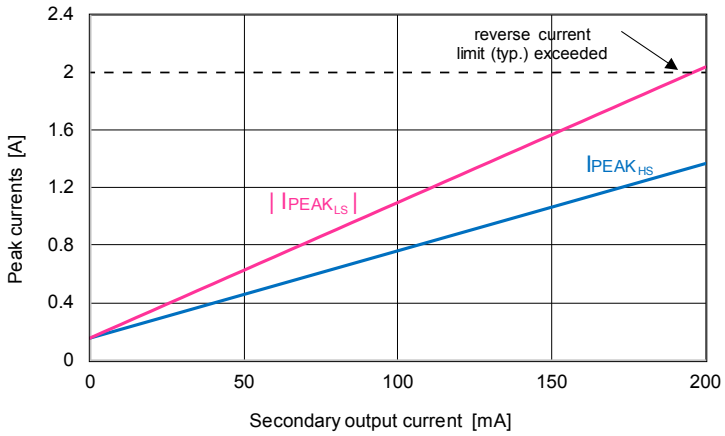
where I_{OUT_pri} and I_{OUT_sec} are respectively the primary and secondary output currents, N is the transformer turn ratio, D the duty cycle and ΔI_L the current ripple in the primary winding.

The Figure 24 depicts how these peak currents vary depending on the secondary output current, under the specified conditions.

Normally the negative current during the off-time is more critical and the secondary output is limited by relying on the reverse current limit (typ. 1.9 A), as shown in Figure 24.

A current drawn from the primary output helps to reduce the peak current in the low side MOSFET [as shown by the equation (25)], hence allowing a higher current from the secondary output.

Figure 24. Peak currents depending on the secondary output current (V_{IN} = 12 V, V_{OUT_pri} = 5.3, N = 6, f_{SW} = 500 kHz, no primary output current)



Reverse current limit

As mentioned in the previous section, the low side MOSFET is protected against negative currents. This feature limits the negative current in the MOSFETs especially during two events:

- Overvoltage at the primary output. Due to an overvoltage event the low side MOSFET is kept on to discharge the primary output.
- Overcurrent or short circuit event at the secondary output, as described in the previous section.

4.10 Overvoltage protection

The overvoltage protection monitors the VFB pin and enables the low-side MOSFET to discharge the output capacitor if the output voltage is 20% over the nominal value.

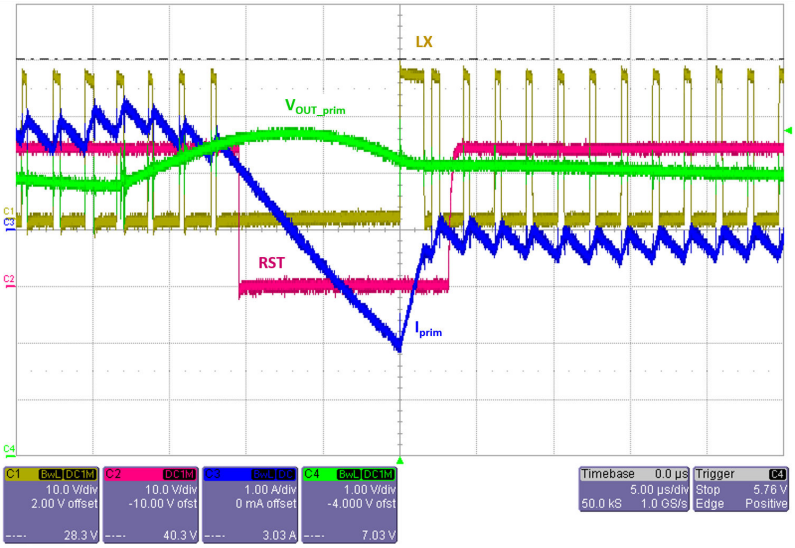
This is a second level protection and should never be triggered in normal operating conditions if the system is properly dimensioned. In other words, the selection of the external power components and the dynamic performance determined by the compensation network should guarantee an output voltage regulation within the overvoltage threshold even during the worst-case scenario in term of load transitions.

Figure 25 shows the overvoltage operation during a negative steep load transient and designed with a not optimized compensation network. This can be considered as an example for a system with dynamic performance not in line with the load request.

The L6986I device implements a 1.9 A typ. negative current limitation to limit the maximum reversed switch current during the overvoltage operation.

Moreover, the overvoltage protection also activates the internal pull-down on RST pin. Once OVP is deactivated, the L6986I releases the RST. The release of the RST pin can be delayed by connecting a capacitor to the DELAY pin (pin 9). For the selection of the capacitance value, equation (28) can be used.

Figure 25. Overvoltage operation



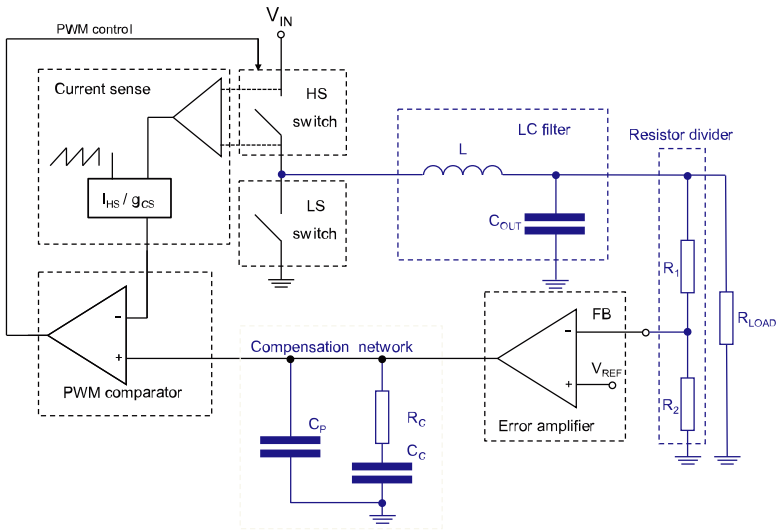
4.11 Thermal shutdown

The shutdown block disables the switching activity if the junction temperature is higher than a fixed internal threshold (165 °C typical). The thermal sensing element is close to the power elements, ensuring fast and accurate temperature detection. A hysteresis of approximately 30 °C prevents the device from turning ON and OFF continuously. When the thermal protection runs away a new soft-start cycle will take place.

5 Closing the loop

The iso-buck, compared to a standard buck, includes the transformer in place of the inductor and all the components connected to the secondary winding (at least the Schottky diode and the secondary output capacitor). Nevertheless, the regulation loop does not include the secondary side components. As a first approximation the control loop of an iso-buck can be assimilated to the one of a standard buck. Therefore, the block diagram in figure below can be still used (where the inductor symbol identifies the inductance of the primary winding) as well as all the equations and calculations in the next sections.

Figure 26. Block diagram of the loop



5.1 $G_{CO}(s)$control to output transfer function

The accurate control to output transfer function for a buck peak current mode converter can be written as:

$$G_{CO}(s) = R_{LOAD} \cdot g_{CS} \cdot \frac{1}{1+\frac{R_{LOAD} \cdot T_{SW}}{L} \cdot [m_C \cdot (1\text{-}D)\text{-}0.5]} \cdot \frac{1+\frac{s}{\omega_Z}}{1+\frac{s}{\omega_p}} \cdot F_H(s) \quad (7)$$

where R_{LOAD} represents the load resistance, g_{CS} the equivalent sensing transconductance of the current sense circuitry, w_p the single pole introduced by the power stage and w_z the zero given by the ESR of the output capacitor.

$F_H(s)$ accounts the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}} \quad (8)$$

$$\omega_p = \frac{1}{R_{LOAD} \cdot C_{OUT}} \cdot \frac{m_C \cdot (1\text{-}D)\text{-}0.5}{L \cdot C_{OUT} \cdot f_{SW}} \quad (9)$$

where:

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = V_{PP} \cdot g_{CS} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \end{cases} \quad (10)$$

Where I_{SLOPE} is equal to 1 [A].

S_n represents the on-time slope of the sensed inductor current, Se the on-time slope of the external ramp that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50%.

The sampling effect contribution $F_H(s)$ is:

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_p + \frac{s^2}{\omega_n^2}}} \quad (11)$$

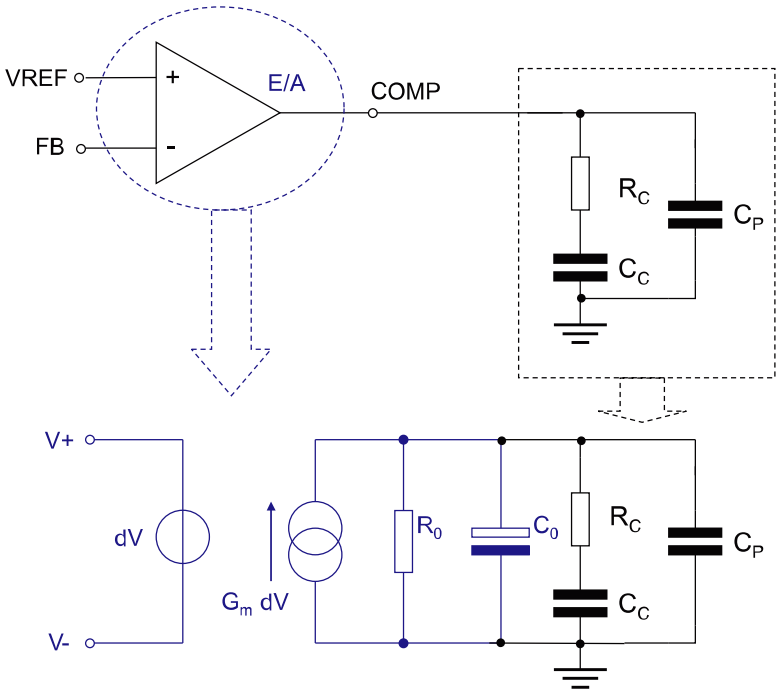
where

$$Q_P = \frac{1}{\pi \cdot [m_C \cdot (1 - D) - 0.5]} \quad (12)$$

5.2 Error amplifier compensation network

The typical compensation network required to stabilize the system is shown in figure below:

Figure 27. Transconductance embedded error amplifier



R_C and C_C introduce a pole and a zero in the open loop gain. C_P does not significantly affect system stability but it is useful to reduce the noise at the output of the error amplifier.

The transfer function of the error amplifier and its compensation network is:

$$A_0(s)=\frac{A_{V0}\cdot(1+s\cdot R_C\cdot C_C)}{s^2\cdot R_0\cdot(C_0+C_p)\cdot R_C\cdot C_C+s\cdot(R_0\cdot C_C+R_0\cdot(C_0+C_p)+R_C\cdot C_C)+1} \quad (13)$$

where $A_{V0}=G_m\cdot R_0$.

The poles of this transfer function are (if $C_C >> C_0 + C_P$)

$$f_{PHF}=\frac{1}{2\cdot\pi\cdot R_0\cdot C_C} \quad (14)$$

whereas the zero is defined as:

$$f_{PHF}=\frac{1}{2\cdot\pi\cdot R_0\cdot(C_0+C_p)} \quad (15)$$

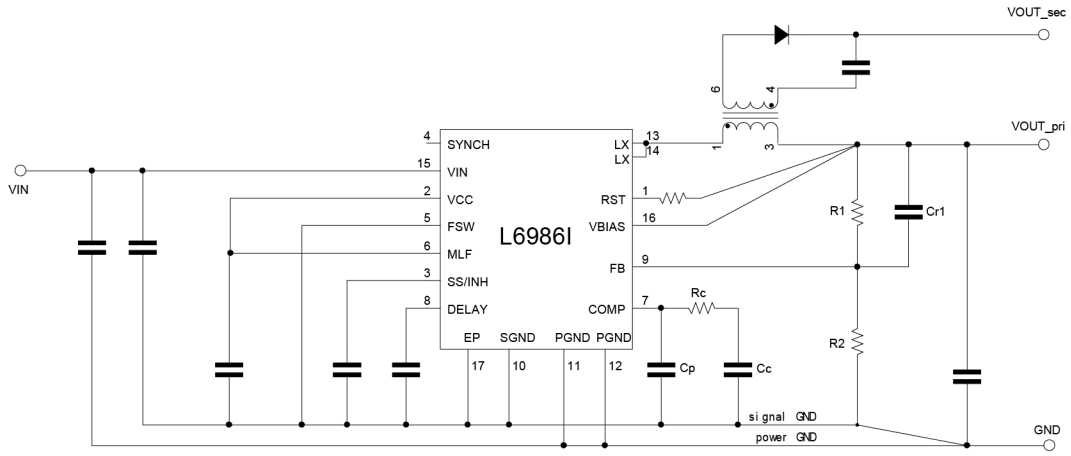
5.3 Voltage divider

The contribution of the internal voltage divider for fixed output voltage devices is:

$$G_{DIV}(s)=\frac{R_2}{R_1+R_2}=\frac{V_{FB}}{V_{OUT}} \quad (16)$$

A small signal capacitor in parallel to the upper resistor (see figure below) of the voltage divider implements a leading network ($f_{zero} < f_{pole}$), sometimes necessary to improve the system phase margin:

Figure 28. Leading network example



The Laplace transformer of the leading network is:

$$G_{DIV}(s)=\frac{R_2}{R_1+R_2}\cdot\frac{\left(1+\frac{s}{f_Z}\right)}{\left(1+\frac{s}{f_P}\right)} \quad (17)$$

where

$$f_Z=\frac{1}{2\cdot\pi\cdot R_1\cdot C_{R1}} \quad (18)$$

$$f_P=\frac{1}{2\cdot\pi\cdot\frac{R_1\cdot R_2}{R_1+R_2}\cdot C_{R1}}$$

$f_Z < f_P$

5.4 Total loop gain

In summary, the open loop gain can be expressed as:

$$G(s) = G_{DIV}(s) \cdot G_{C0}(s) \cdot A_0(s) \quad (19)$$

5.5 Compensation network design

The maximum bandwidth of the system can be designed up to $f_{SW}/6$ up to 150 kHz maximum to guarantee a valid small signal model

$$R_C = \frac{2 \cdot \pi \cdot BW \cdot C_{OUT} \cdot V_{OUT}}{0.85V \cdot g_{CS} \cdot g_{m\_typ}} \quad (20)$$

where:

$$f_{POLE} = \frac{\omega_P}{2 \cdot \pi} \quad (21)$$

ω_P is defined by eq. (9) , g_{CS} represents the current sense transconductance and $g_{m\ TYP}$ the error amplifier transconductance.

$$C_C = \frac{5}{2 \cdot \pi \cdot R_C \cdot BW} \quad (22)$$

Example 1:

V_{IN} = 12 V, V_{OUT_pri} = 5.3 V, R_{OUT_pri} = 5.6 Ω (corresponding to almost 1 A load).

Selecting the L6986I with V_{OUT_pri} = 5.3 V, f_{SW} = 500 kHz, L_{pri} = 18 µH, C_{OUT_pri} = 10 µF and ESR = 3 mΩ, R_C = 56 kΩ, C_C = 680 pF, C_P = 4.7 pF (please refer to Table 11), the gain and phase bode diagrams are plotted respectively in Figure 29 and Figure 30.

Figure 29. Bode plote (magnitude)

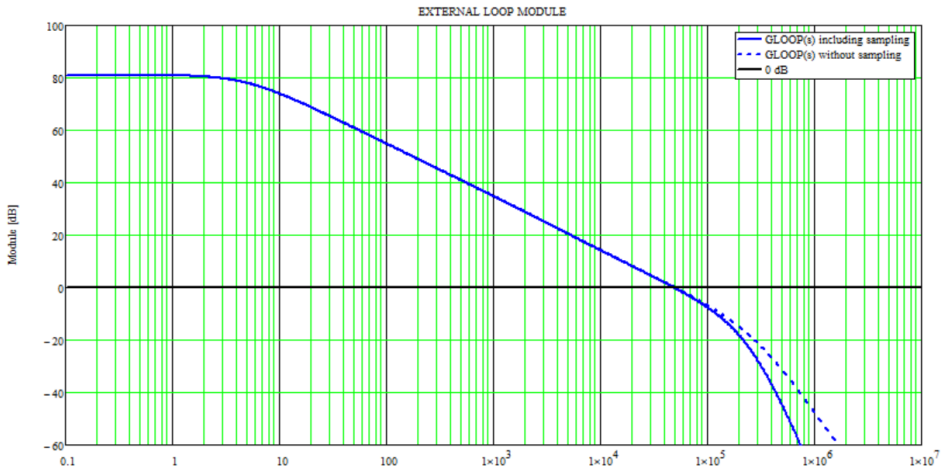
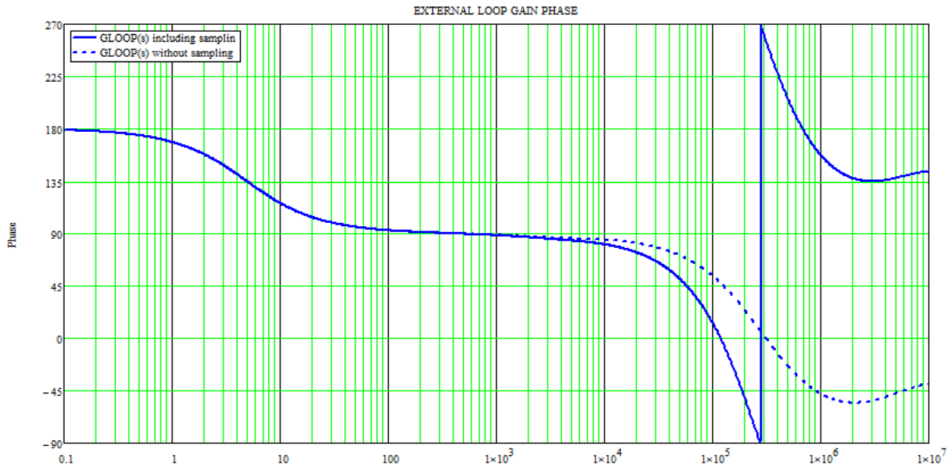


Figure 30. Bode plot (phase)



The blue solid trace represents the transfer function including the sampling effect term (see equation (11)), the dotted blue trace neglects the contribution.

Considering this example, bandwidth and phase margin are:

BW ≈ 50 kHz

Phase Margin → between 53° and 70°

6 Application notes

6.1 Output voltage adjustment

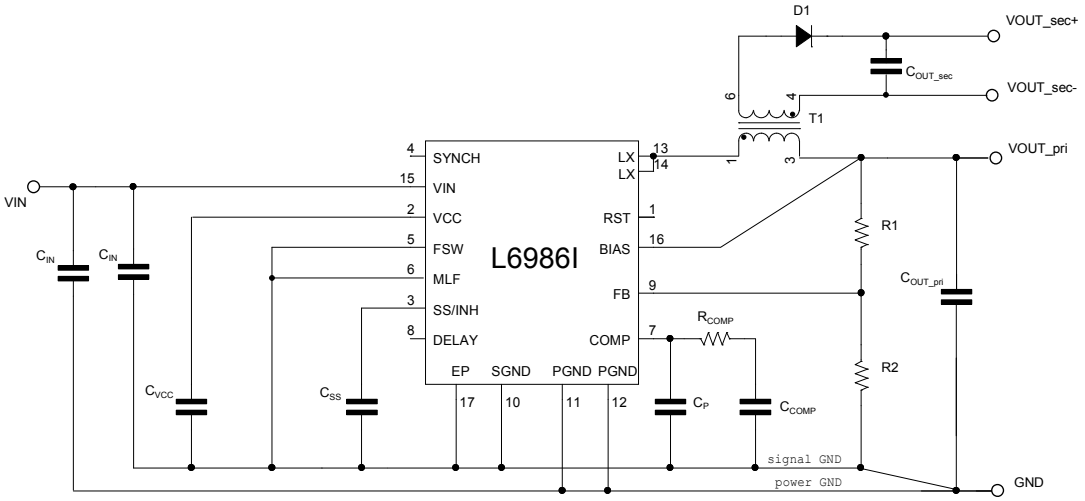
Primary output voltage

The error amplifier reference voltage is 0.85 V typical. The output voltage is adjusted accordingly to equation below:

$$V_{OUT\_pri} = 0.85 \cdot \left(1 + \frac{R_1}{R_2}\right) \quad (23)$$

where R_1 and R_2 are the resistors used in the output divider (see figure below).

Figure 31. L6986I application circuit



The integration of a P-channel MOSFET as high side switch theoretically allows duty cycle up to 100%. Nevertheless, in an iso-buck architecture some restrictions should be considered. A general recommendation is to keep the duty-cycle below 50-60%. A higher duty cycle would limit off time, limiting the time in which the energy transfer to the secondary side takes place.

Other restrictions in the duty cycle selection arise due to the minimum on time (see Switching frequency), generally summarized by the following equation:

$$D \geq D_{MIN} = T_{ON\ MIN} \cdot f_{SW} \quad (24)$$

Secondary output voltage

In the iso-buck converter, the secondary output voltage is not included in the regulation loop. Nevertheless, a good regulation of the secondary output voltage is achieved by relying on the primary output voltage regulation, the selection of a proper turn ratio of the transformer as well as considering the voltage drops due to the secondary winding resistance and the Schottky diode. That can be summarized by the following equation:

$$V_{OUT\_sec} = N \cdot \left[V_{OUT\_pri} + I_{OUT_{pri}} \cdot \left(R_{DS(on)LS} + R_{wind\_pri}\right)\right] - R_{wind\_sec} \cdot I_{OUT\_sec} - V_{FD1} \quad (25)$$

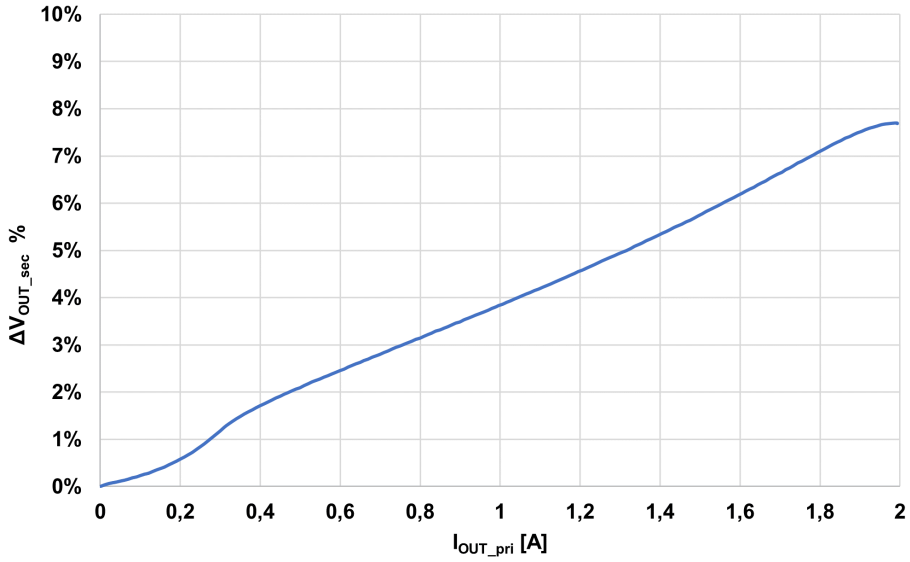
Where N is the turn ratio, Rwind_prim and Rwind_sec are the winding resistances of the primary and secondary side respectively and V_{FD1} is the forward voltage of the Schottky diode.

If no current is drawn from the primary output, the equation (25) can be simplified as follows:

$$V_{OUT\_sec} = N \cdot V_{OUT_{pri}} - R_{wind\_sec} \cdot I_{OUT\_sec} - V_{FD1} \quad (26)$$

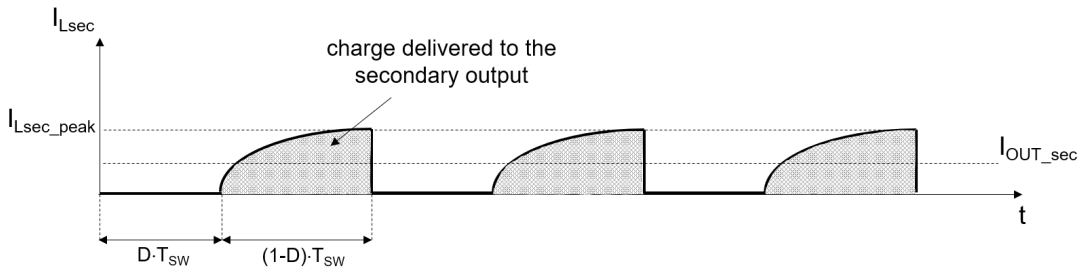
Equation (26) emphasizes how the selection of the transformer and, to some extent, the Schottky diode plays a crucial role in the accurate regulation of the secondary output voltage. The figure below shows instead the effect of the current drawn from the primary output on the isolated voltage, as described by the eq. (9).

Figure 32. **Isolated voltage variation due to the primary output current**



Another factor affecting the secondary output voltage regulation comes from the leakage inductance of the transformer. As described later on, the leakage inductance determines the peak current that can be reached in the secondary winding. This peak current defines the maximum current from the secondary isolated output by limiting the amount of charge delivered to the output. When the current demand from the secondary isolated output exceeds the maximum deliverable charge limited by the peak current, the isolated output voltage drops.

Figure 33. **Secondary output maximum current**



To some extent also the duty cycle can affect the secondary output voltage. Since the energy transfer from primary to secondary occurs only during the TOFF, a too high duty cycle could reduce the achievable peak current, hence limiting the deliverable current to the secondary output. Under this condition the secondary output could drop.

6.2 Switching frequency

A resistor connected to the FSW pin features the selection of the switching frequency. The pinstrapping is performed at power-up, before the soft-start takes place. The FSW pin is pinstrapped and then driven floating in order to minimize the quiescent current from VIN. Please refer to Table 6 to identify the pull-up / pull-down resistor value.

Setting f_{SW} = 250 kHz or f_{SW} = 500 kHz does not require any external resistor.

The selection of the switching frequency must take into account the minimum on time of the device ($T_{ON\ MIN}$, as indicated in the electrical characteristics table), as described by the following equation.

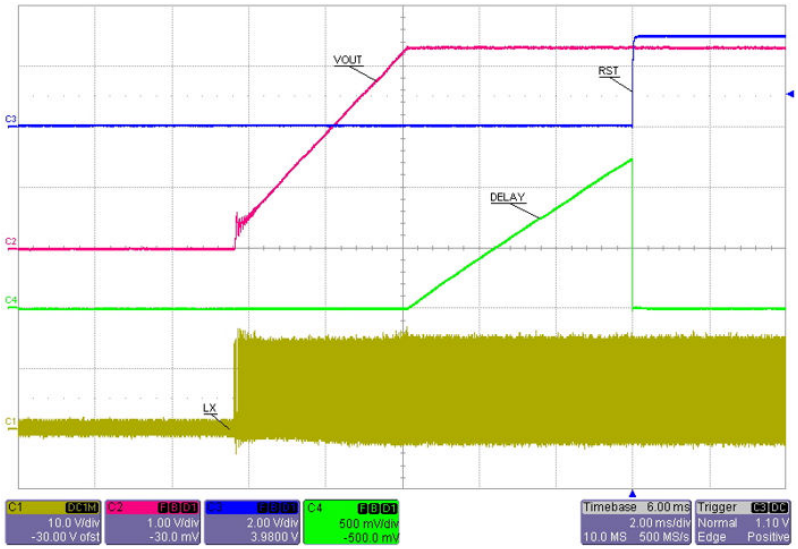
$$f_{SW\_max} \leq \frac{V_{OUT}}{T_{ON\ MIN} \cdot V_{IN} \cdot \eta} \quad (27)$$

The switching frequency affects the selection of the primary inductance as well as the transformer construction.

6.3 Voltage supervisor

The embedded voltage supervisor (composed of the RST and the DELAY pins) monitors the regulated output voltage and keeps the RST open collector output in low impedance as long as the V_{OUT} is out of regulation (i.e. lower than 93% of the target output voltage). In order to ensure a proper reset of digital devices with a valid power supply, the device can delay the RST assertion with a programmable time.

Figure 34. Voltage supervisor operation



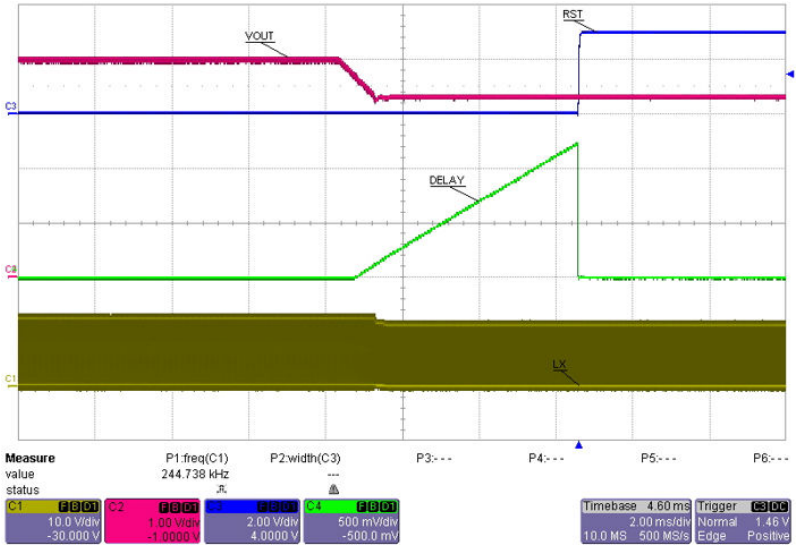
When the RST comparator detects the output voltage is in regulation, a 2 µA internal current source starts to charge an external capacitor to implement a voltage ramp on the DELAY pin. The RST open collector is then released as soon as V_{DELAY} = 1.234 V (see Figure 35). The C_{DELAY} is dimensioned as follows.

$$C_{DELAY} = \frac{I_{SSCH} \cdot T_{DELAY}}{V_{DELAY}} = \frac{2\mu A \cdot T_{DELAY}}{1.234V} \quad (28)$$

The maximum suggested capacitor value is 270 nF.

The L6986I also activates internal pull-down on RST pin in case overvoltage protection is triggered. As soon as the output voltage goes below OVP threshold (20% typ.), the 2 µA internal current source starts to charge an external capacitor to implement a voltage ramp on the DELAY pin. The RST open collector is then released as soon as V_{DELAY} = 1.234 V (see figure below).

Figure 35. Voltage supervisor operation during OVP



6.4 Synchronization

The synchronization feature helps the hardware designer to prevent beating frequency noise that is an issue when multiple switching regulators populate the same application board.

6.4.1 Embedded master - slave synchronization

The L6986I synchronization circuitry features the same switching frequency for a set of regulators simply connecting their SYNCH pin together, so preventing beating noise. The master device provides the synchronization signal to the others since the SYNCH pin is I/O able to deliver or recognize a frequency signal.

For proper synchronization of multiple regulators, all of them have to be configured with the same switching frequency (see Table 6), so the same resistor connected at the FSW pin.

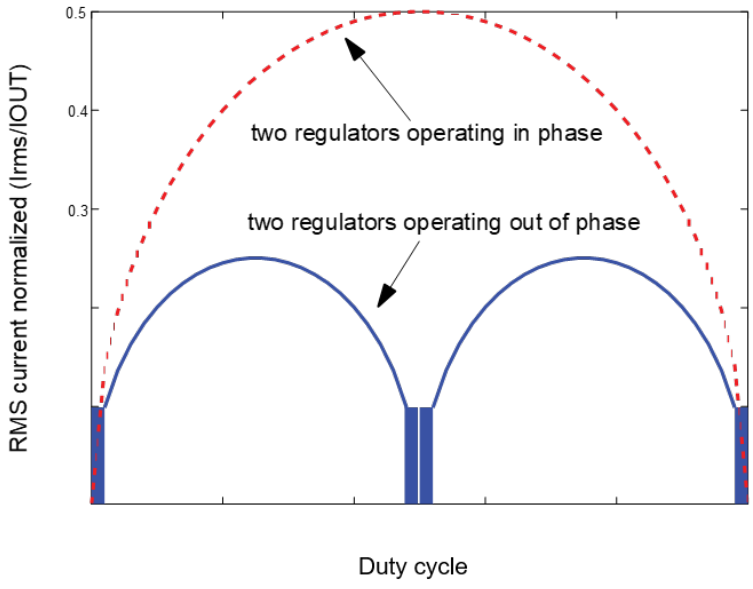
In order to minimize the RMS current flowing through the input filter, the L6986I device provides a phase shift of 180° between the master and the SLAVES. If more than two devices are synchronized, all slaves will have a common 180° phase shift with respect to the master.

Considering two synchronized L6986I which regulate the same output voltage (i.e.: operating with the same duty cycle), the input filter RMS current is optimized and is calculated as:

$$I_{RMS}\begin{cases}\frac{I_{OUT}}{2}\cdot\sqrt{2D\cdot(1-2D)} & if\ D<0.5\\ \frac{I_{OUT}}{2}\cdot\sqrt{(2D-1)\cdot(2-2D)} & if\ D>0.5\end{cases} \quad (29)$$

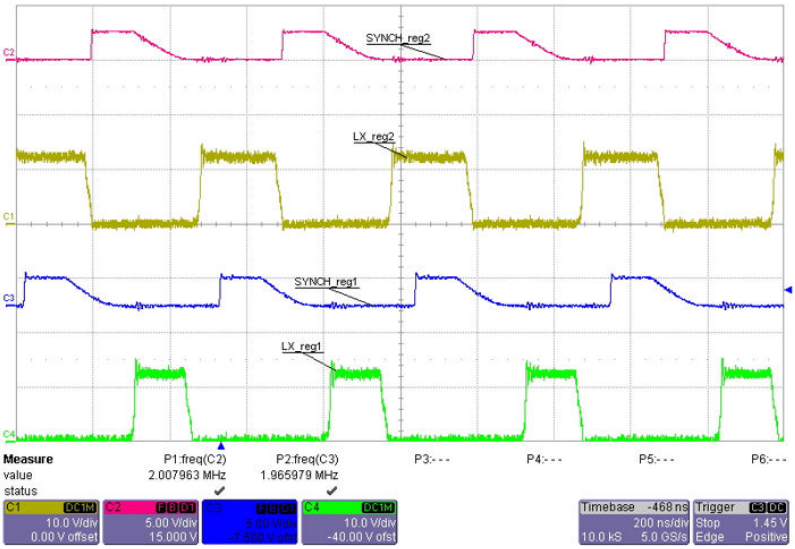
The graphical representation of the input RMS current of the input filter in the case of two devices with 0° phase shift (synchronized to an external signal) or 180° phase shift (synchronized connecting their SYNCH pins) regulating the same output voltage is provided in the figure below. To dimension the proper input capacitor please refer to the dedicate section.

Figure 36. Input RMS current



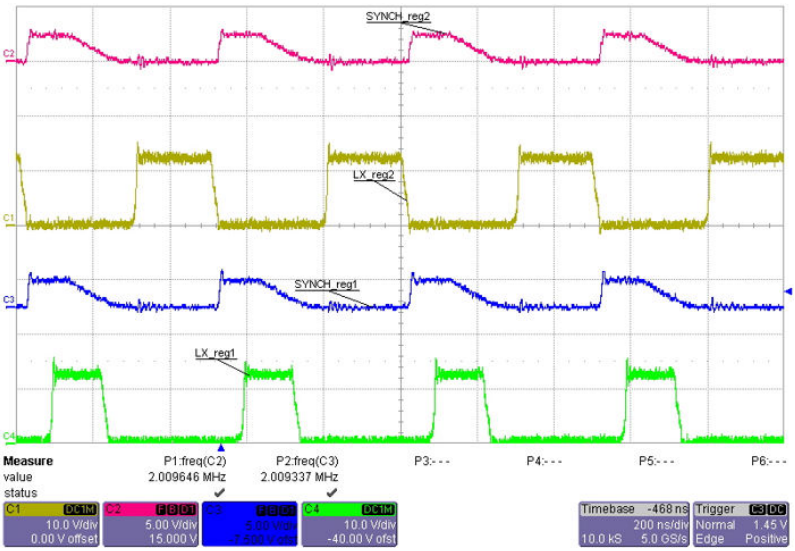
The figure below shows two not synchronized regulators with unconnected SYNCH pin.

Figure 37. **Two regulators not synchronized**



The figure below shows the same regulators working synchronized having the SYNCH pins connected. The MASTER regulator (LX_reg2 trace) delivers the synchronization signal to the SLAVE device (LX_reg1). The SLAVE regulator works in phase with the synchronization signal, which is out of phase with the MASTER switching operation.

Figure 38. **Two regulators not synchronized**



6.4.2 External synchronization signal

Multiple L6986I can be synchronized to an external frequency signal fed to the SYNCH pin. In this case the regulator set is phased to the reference and all the devices will work with 0° phase shift.

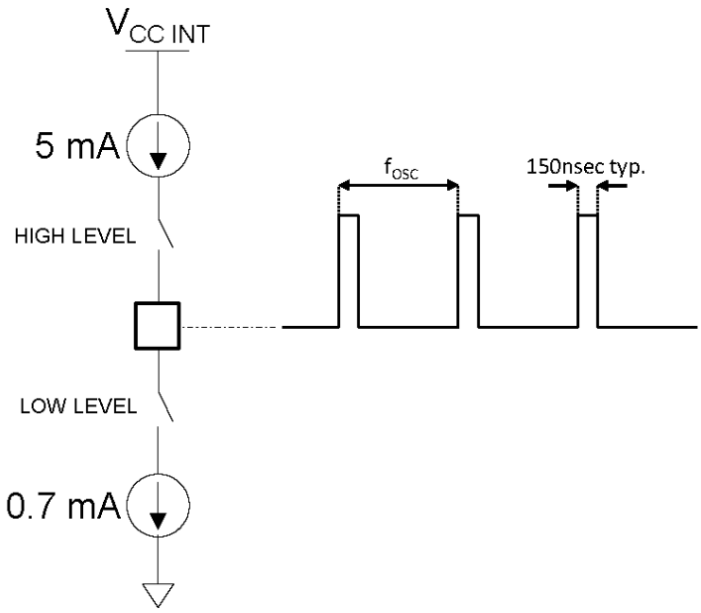
Considering that the minimum synchronization pulse width coincides with the $T_{ON\ MIN}$ (typ. 340 ns), it is recommended to synchronize with a frequency not higher than 1 MHz.

Since the internal slope compensation contribution that is required to prevent subharmonic oscillations in peak current mode architecture depends on the oscillator frequency, it is important to select the same oscillator frequency for all regulators (all of them operate as SLAVE) as close as possible to the frequency of the reference signal (please refer to Table 6). As a consequence, all the regulators have the same resistor value connected to the FSW pin, so the slope compensation is optimized accordingly with the frequency of the synchronization signal. The slope compensation contribution is latched at power-up and so fixed during the device operation.

The L6986I normally operates in the MASTER mode, driving the SYNCH line at the selected oscillator frequency as shown in Figure 39 and Figure 40.

In the SLAVE mode the L6986I sets the internal oscillator at 250 kHz typ. (see Table 6) and drives the line accordingly.

Figure 39. L6986I synchronization driving capability



In order to safely guarantee that each regulator recognizes itself in SLAVE mode when synchronized, the external master must drive the SYNCH pin with a clock signal frequency higher than the maximum oscillator spread of the selected line in Table 6 for at least 10 internal clock cycles.

Example 1: selecting R_{FSW} = 0 Ω to VCC

Table 9. Example of oscillator frequency selection

Symbol	R_{VCC} (E24 series	R_{GND} (E24 series)	f_{SW} min.	f_{SW} typ.	f_{SW} max.
f_{SW}	NC	0 Ω	225	250	275

the device enters in slave mode after 10 pulses at frequency higher than 275 kHz

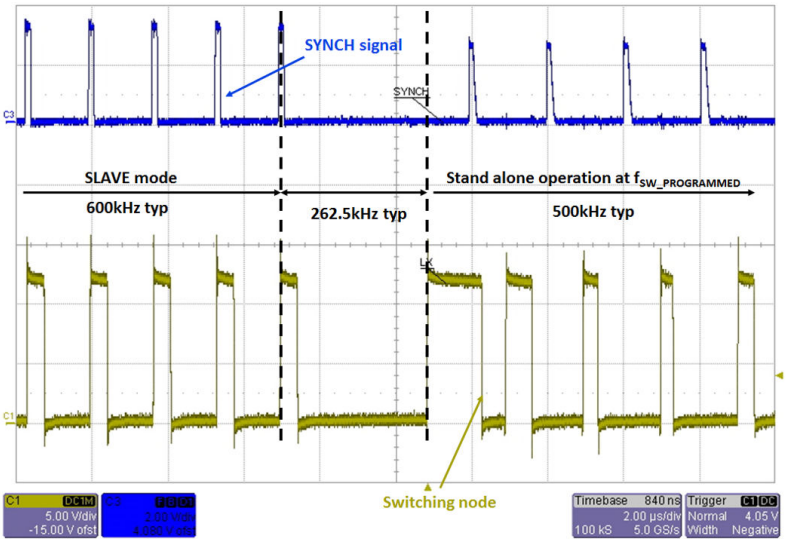
As anticipated above, in SLAVE mode the internal oscillator operates at 250 kHz typ. but the slope compensation is dimensioned accordingly with FSW resistors so it is important to limit the switching operation around a working point close to the selected oscillator frequency (FSW resistor).

As a consequence, to guarantee the full output current capability and to prevent the subharmonic oscillations, the master may limit the driving frequency range within ± 5% of the selected frequency.

A wider frequency range may generate subharmonic oscillation for duty > 50% or limit the peak current capability (see I_{PK} parameter in section 3) since the internal slope compensation signal may be saturated.

The device keeps operating in slave mode as far as the master is able to drive the SYNCH pin faster than 275 kHz, otherwise the L6986I goes back into MASTER mode at the programmed R_{FSW} oscillator frequency after successfully driving one pulse 250 kHz typ. (see Figure 40) in the SYNCH line.

Figure 40. **Slave-to-master mode transition**

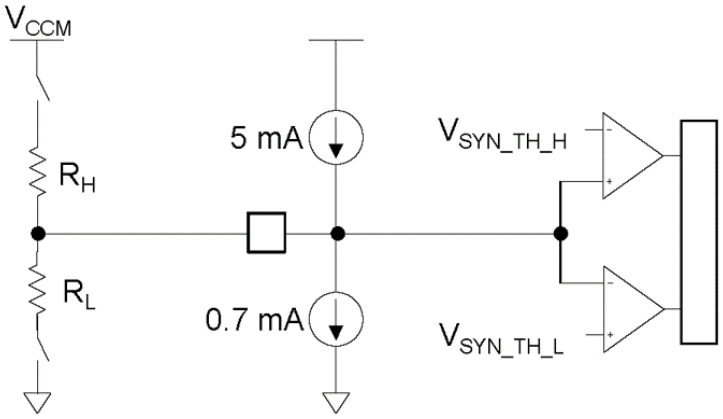


The external master can force a latched SLAVE mode driving the SYNCH pin low at power-up, before the soft-start begins the switching activity. So the oscillator frequency is 250 kHz typ. fixed until a new UVLO event is triggered regardless FSW resistor value, that otherwise counts to design the slope compensation. The same considerations above are also valid.

The master driving capability must be able to provide the proper signal levels at the SYNCH pin (see section 3):

- Low level < $V_{SYN\ THL}$ = 0.7 V sinking 5 mA
- High level > $V_{SYN\ THH}$ = 1.2 V sourcing 0.7 mA

Figure 41. **Master driving capability to synchronize the L6986I**



6.5 Design of the external components

6.5.1 Input capacitor selection

The input capacitor, just like in a standard buck, should limit the input voltage ripple. Key parameters of the input capacitor are, together with its value, the maximum operating voltage and the RMS current capability.

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity a pulsed current flows into the input capacitor and so its RMS current capability must be selected accordingly with the application conditions. Internal losses of the input filter depends on the ESR value so usually low ESR capacitors (like multilayer ceramic capacitors) have higher RMS current capability. On the other hand, given the RMS current value, lower ESR input filter has lower losses and so contributes to higher conversion efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

$$I_{RMS}=\left(I_{OUT\_pri}+\frac{I_{OUT\_sec}}{N}\right)\cdot\sqrt{\left(1-\frac{D}{\eta}\right)\cdot\frac{D}{\eta}} \quad (30)$$

In the ideal case of efficiency η = 1, the RMS current reaches its maximum value when D = 0.5.

In general, the maximum and minimum duty cycles can be calculated as:

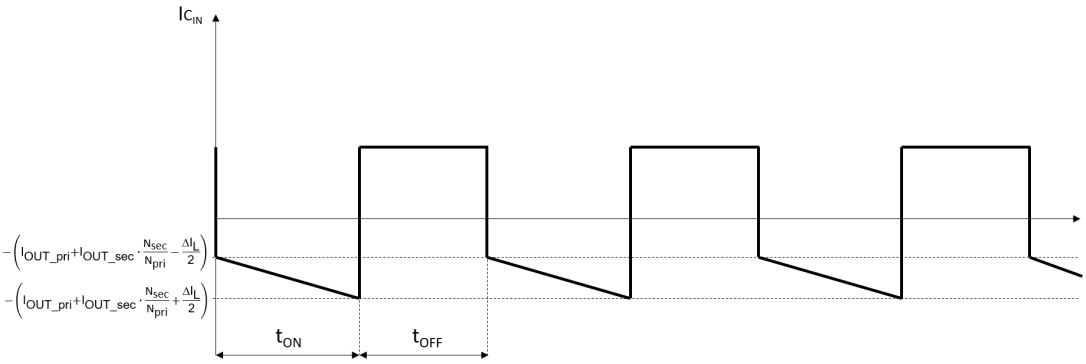
$$D_{MAX}=\frac{V_{OUT\_pri}+\Delta V_{LS}}{V_{INmin}+\Delta V_{LS}-\Delta V_{HS}} \quad (31)$$

$$D_{MIN}=\frac{V_{OUT\_pri}+\Delta V_{LS}}{V_{INmax}+\Delta V_{LS}-\Delta V_{HS}} \quad (32)$$

Where ΔV_{HS} and ΔV_{LS} are the voltage drop across the high side and low side MOSFETs respectively.

The AC component of the input current (see figure below) flows in the input capacitor, generating the input voltage ripple.

Figure 42. Input capacitor AC current



The peak to peak voltage across the input capacitor can be calculated as follows:

$$V_{PP}=\left(\frac{I_{OUT\_pri}+I_{OUT\_sec}\cdot\frac{N_{sec}}{N_{pri}}}{C_{IN}\cdot f_{SW}}\right)\cdot\frac{D}{\eta}\cdot\left(1-\frac{D}{\eta}\right)+ESR\cdot\left(I_{OUT\_pri}+I_{OUT\_sec}+\frac{\Delta I_L}{2}\right) \quad (33)$$

In case of negligible ESR (e.g. in case of MLCC capacitors) the equation (33) can be simplified. The value of the input capacitor can be so derived:

$$C_{IN}=\frac{I_{OUT\_pri}+I_{OUT\_sec}\cdot\frac{N_{sec}}{N_{pri}}}{V_{PP}\cdot f_{SW}}\cdot\frac{D}{\eta}\cdot\left(1-\frac{D}{\eta}\right) \quad (34)$$

Considering the ideal case of η = 1, the equation above reaches its maximum value when D = 0.5. Therefore, the minimum input capacitance value can be defined as follows:

$$C_{IN} \geq C_{INmin} = \frac{I_{OUT\_pri} + I_{OUT\_sec} \cdot \frac{N_{sec}}{N_{pri}}}{4 \cdot V_{PP} \cdot f_{SW}}. \quad (35)$$

Typically, C_{IN} is dimensioned to keep the maximum peak to peak voltage across the input filter in the order of 5% of V_{INmax}.

6.5.2 Transformer selection

The transformer has two essential tasks:

- Providing the isolation between primary and secondary side in accordance with the application requirements
- Generating the necessary secondary output voltage from the regulated primary voltage with the most suitable turn ratio

The transformer selection implies defining the following parameters:

- Isolation voltage
- Turn ratio
- Primary inductance
- Peak and RMS currents
- Windings resistance
- Leakage inductance
- Parasitic capacitances

Isolation voltage

The isolation of the transformer in terms of voltage capability (1.5 kV, 4 kV, and so on) and type (functional basic, reinforced, etc.) is mainly driven by the application. Both parameters normally affect the size of the transformer as well as other electrical characteristics (e.g. winding resistance, leakage inductance, etc.).

Turn Ratio

Naming N_{pri} and N_{sec} the number of turns of the primary and secondary windings respectively, the turn ratio is so defined:

$$N = \frac{N_{sec}}{N_{pri}} \tag{36}$$

Considering the equation (25), the turn ratio must be defined so that the voltage at the secondary output is the desired one over the whole secondary output current range:

$$N \geq \frac{V_{OUT\_sec} + R_{wind\_sec} \cdot I_{OUT\_sec} + V_{FD1}}{V_{OUT\_pri} + I_{OUT_{pri}} \cdot \left(R_{DS(on)LS} + R_{wind\_pri}\right)} \tag{37}$$

If no current is drawn from the primary output, the turn ratio should be only chosen to compensate the drops due to the secondary winding resistance and the Schottky diode.

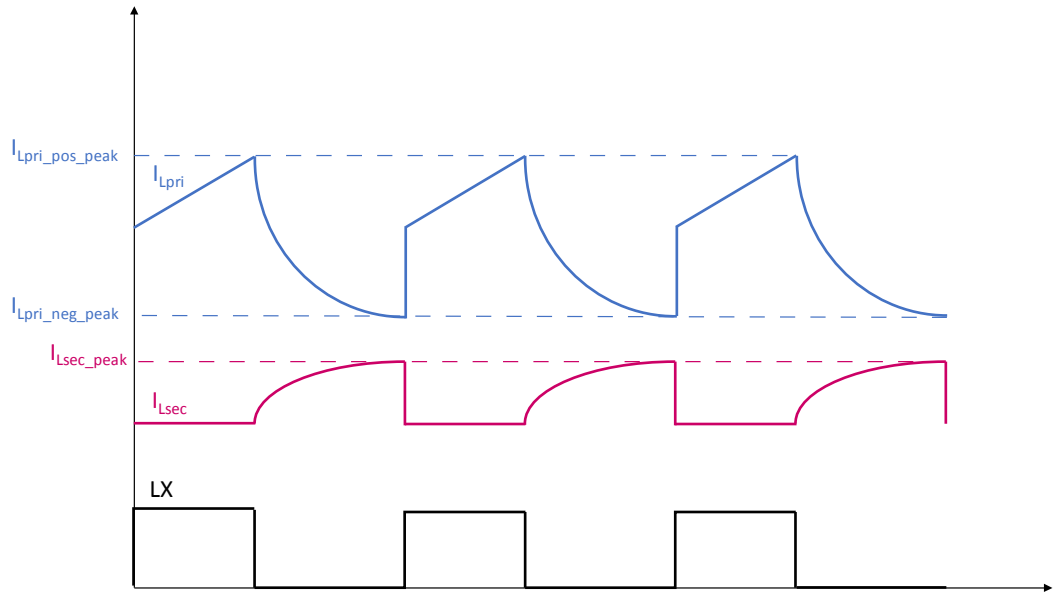
The effect of the leakage inductance on the secondary output voltage regulation (not included in the equation above) should be taken into account too. Figure 17 clearly shows how the secondary output voltage can drift due to the leakage inductance.

Primary inductance

The choice of the primary inductance does not differ so much from a standard buck. The magnetizing current, (see Figure 43) which combines the two winding currents, has the same shape of the buck inductor current and can be defined as:

$$I_{L\_mag} = I_{pri} + N \cdot I_{sec} \tag{38}$$

Figure 43. **Primary (blue) winding current, secondary (pink) winding current and magnetizing current (black)**



Therefore, setting the current ripple ΔI_L, the inductance is so defined:

$$L_{pri} = \frac{(V_{IN} - V_{OUT\_pri}) \cdot V_{OUT\_pri}}{V_{IN} \cdot f_{SW} \cdot \Delta I_L} \quad (39)$$

As example, assuming I_{OUT_prim} = 500 mA, I_{OUT_sec} = 100 mA, N= 5, the current ripple can be set around 30% of the total current $I_{OUT\_pri} + N \times I_{OUT\_sec}$ = 1 A, therefore 300 mA. If V_{IN} = 12 V, V_{OUT_pri} = 5 V and f_{SW} = 500 kHz, the inductor value should be 19.4 µH (→ 18 µH or 22 µH the closest standardized value).

Peak and RMS current

As any inductor, peak and RMS current for each winding must be calculated in order to define saturation and RMS currents that the transformer should fulfill.

For the primary winding, the equations below are valid:

$$I_{pri\_pos\_peak} = I_{OUT\_pri} + \frac{I_{OUT\_sec}}{N} + \frac{\Delta I_{pri}}{2} \quad (40)$$

$$I_{pri\_RMS} = \left(I_{OUT\_pri} + \frac{I_{OUT\_sec}}{N}\right) \cdot \sqrt{1 + \frac{1}{12} \cdot \left(\frac{\Delta I_{pri} \cdot N}{N \cdot I_{OUT\_pri} + I_{OUT\_sec}}\right)} \quad (41)$$

For the secondary winding the peak current can change depending on the leakage inductance. In the picture below secondary winding current waveforms with different leakage inductances are simulated. It is evident how the peak current can significantly vary. Considering the target leakage inductance value for an iso-buck (recommended up to 1% of the primary inductance), the waveform can be approximated with a sawtooth shape and the peak and RMS currents can be hence estimated as:

$$I_{sec\_pos\_peak} = \frac{2 \cdot I_{OUT\_sec}}{1 - D} \quad (42)$$

$$I_{sec\_RMS} = I_{sec\_pos\_peak} \cdot \sqrt{\frac{1 - D}{3}} \quad (43)$$

The equation (44) emphasizes what mentioned about the recommended duty cycle.

A duty cycle higher than 50-60% significantly increases the peak current in the secondary winding (see figure below). Furthermore, this affects the negative peak current at the primary side (see Figure 44).

Figure 44. Secondary winding positive peak current dependency on duty cycle (I_{OUT_sec} = 100 mA)

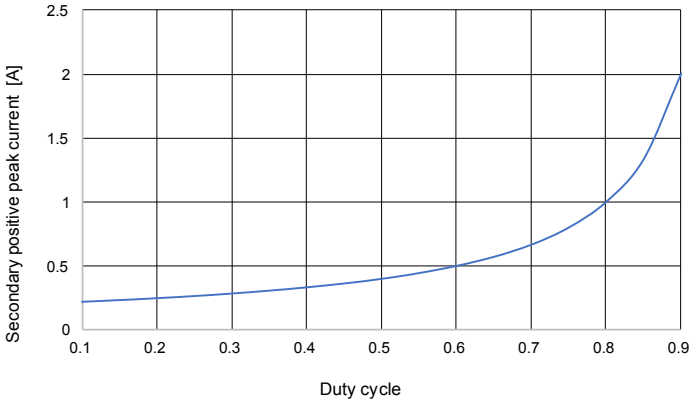
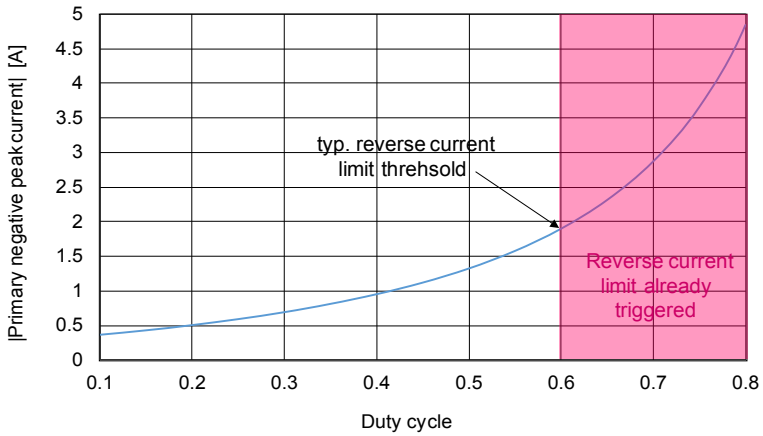


Figure 45. Primary negative peak current dependency on duty cycle (V_{OUT_pri} = 5 V, I_{OUT_pri} = 0, I_{OUT_sec} = 100 mA, N = 6, f_{SW} = 500 kHz, L = 19 µH)



Windings resistance

Winding resistances should be minimized as much as possible since they affect the secondary output load regulations. They also contribute to power losses, hence affecting the efficiency of the total solution.

Leakage inductance

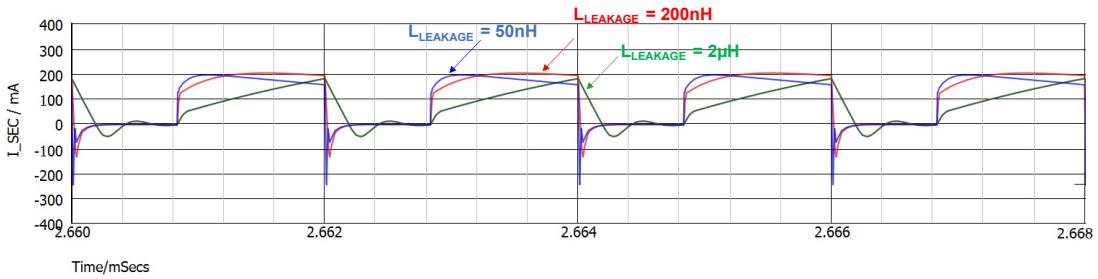
The leakage inductance of a transformer can be defined as an undesired inductive component due to the not perfect magnetic linking of the two windings. Leakage inductance is inherent to the transformer construction and can be only reduced but not eliminated.

As shown in the Figure 46 (resulting from a simulation), the leakage inductance affects the shape of the secondary winding current. In general, a very low leakage inductance implies that the current in the secondary winding can quickly ramp-up allowing the charge of the secondary output capacitor and supporting the load current demand.

A high leakage inductance slows down the secondary winding current rise, limiting the charge delivery to the output. Comparing solutions with different values of transformer leakage inductance shows that higher leakage inductance transformer are characterized by poorer load regulation performances.

In addition, higher leakage inductance means a reduction of the effective current slope in the primary winding, hence increasing the duty cycle. As consequence, the Schottky diode conduction time shorten, and higher peak and RMS current are present at the secondary winding. Higher peaks at light load negatively impact the load regulation.

Figure 46. Secondary winding current according to different leakage inductances (simulation)



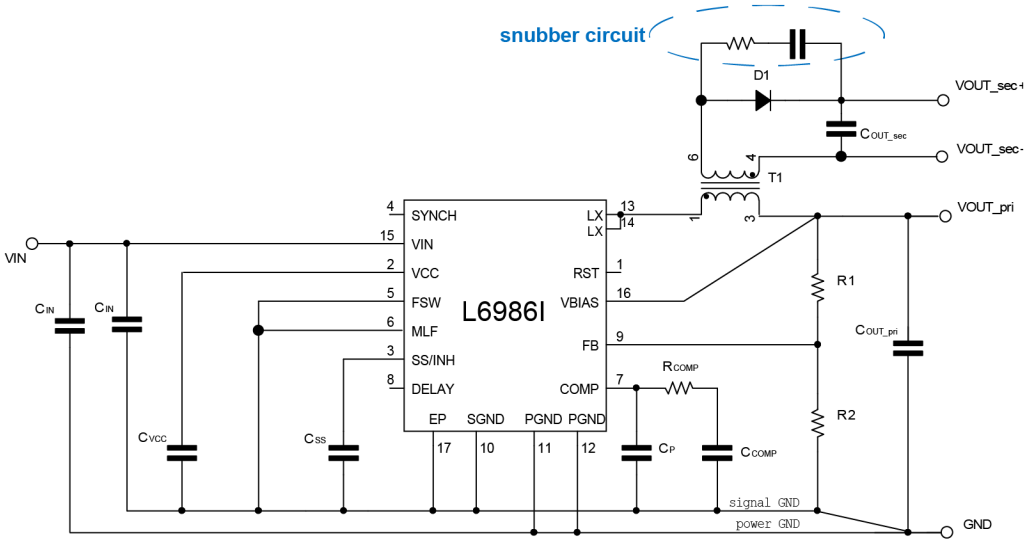
Another effect of the leakage inductance is the ringing observed when the transition from the off-phase to on-phase occurs. These oscillations are due to the LC circuit represented by the leakage inductance and the total parasitic capacitance observed by the primary winding. This capacitance consists of several contributions:

- Primary winding capacitance
- Secondary winding capacitance, reflected to the primary side
- Reverse capacitance of the Schottky diode, reflected to the primary side

The ringing at primary side could affect the regulation loop and falsely trigger the internal comparator, turning off the high side MOSFET although it should be kept on. This might result in undesired jitter at switch node.

A proper masking time ($T_{ON\ MIN}$) filters these oscillations, which otherwise can affect the loop on the primary side. Nevertheless, a snubber circuit to dump this ringing is always recommended, as shown in figure below.

Figure 47. Snubber circuit



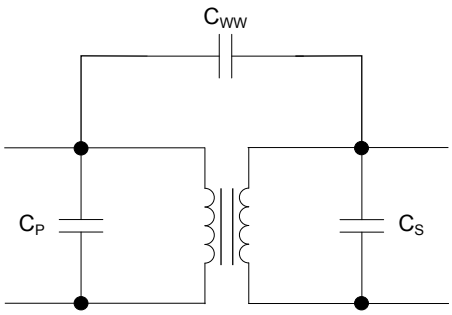
Capacitance

The parasitic capacitance of a real transformer mainly consists of the following contributions:

- Capacitance across each winding (C_P and C_S, in the picture below) due to the capacitve coupling between the coil and the core. As already mentioned, the winding capacitances are involved in the ringing observed during transition from off to on phase of the primary side

- Interwinding capacitance (C_{WW}), that is the capacitance between windings. The interwinding capacitance should be reduced in order to limit disturbance on the primary side due to possible steep voltage transitions present in the load connected to the secondary output

Figure 48. Transformer parasitic capacitances



6.5.3 Schottky diode

The selection of the Schottky diode should consider the following parameters:

- Maximum forward current, mainly defined by the secondary output current demand (see equation (43));
- Forward voltage drop, which affects the secondary output voltage regulation
- Maximum peak reverse voltage. During the on phase of the primary side, when in the secondary side no current flows, the diode is reverse biased and must withstand this voltage:

$$V_{D1\_rev} = N \cdot \left(V_{INmax} - V_{OUT\_pri}\right) + V_{OUT\_sec} \quad (44)$$

- Junction capacitance, which should be as low as possible in order to reduce the ringing described in the previous section

6.5.4 Output capacitors selection

Primary output capacitor

As in a standard buck converter, the primary output capacitor is involved in:

- Determining the output voltage ripple
- Supporting load transient
- The loop stability, by setting one pole and one zero in the transfer function

Considering the ouput voltage ripple requirement, the primary output capacitance should be selected according to the following equation:

$$C_{OUT\_pri} = \frac{\Delta I_{pri}}{8 \cdot f_{SW} \cdot \left(\Delta V_{OUT\_pri} - ESR \cdot \Delta I_{pri}\right)} \quad (45)$$

Normally MLCC capacitor are the best choice for the output capacitor, therefore the ESR contribution is negligible and the equation (46) can be simplified.

Secondary output capacitor

The secondary output capacitor supplies the secondary output load current during the t_{ON} (when diode D1 is reverse biased) and its value defines the secondary output voltage ripple (ΔV_{OUT}).

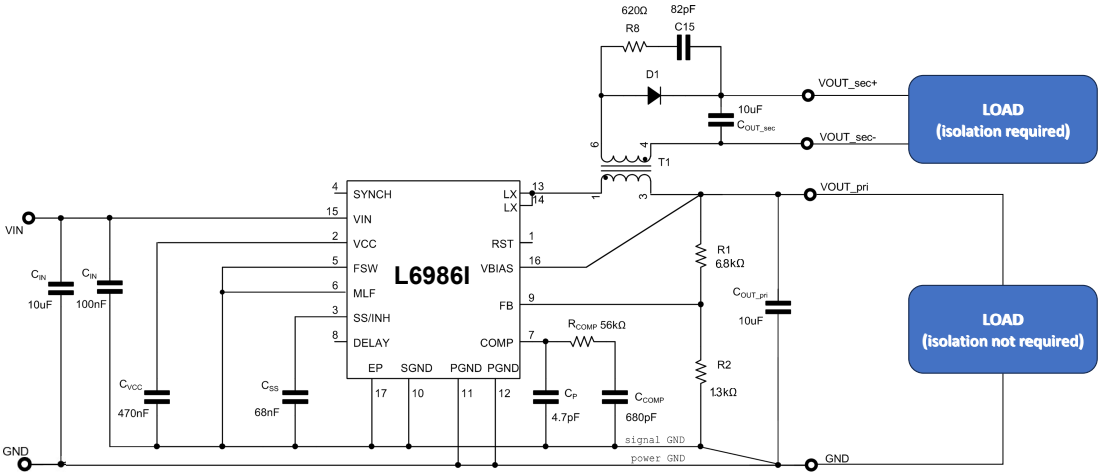
$$C_{OUT\_sec} = \frac{I_{OUT\_sec} \cdot D}{\Delta V_{OUT\_sec} \cdot f_{SW}} \quad (46)$$

7 Application example

The target of this section is to show a typical application example as well as to describe the expected performances.

The schematic below depicts a typical application (implemented by using the STEVAL_L6986IV1) where both an isolated voltage (single) and a not isolated voltage are required.

Figure 49. Typical schematic with load applied to both the isolated and not isolated outputs



This application generates 5 V at the primary output (not isolated) from an input voltage of 12 V with a switching frequency of 500 kHz. The secondary voltage (isolated) is generated by a transformer with a turn ratio 1:5.8. The voltage between VOUT_sec+ and VOUT_sec- changes with the current drawn from the load. A post-regulation might be used if the variation of the isolated voltage with the current is too wide (according to the application requirements) or in case the isolated voltage should split into two voltages (in many cases for gate driving, one positive and one negative voltage).

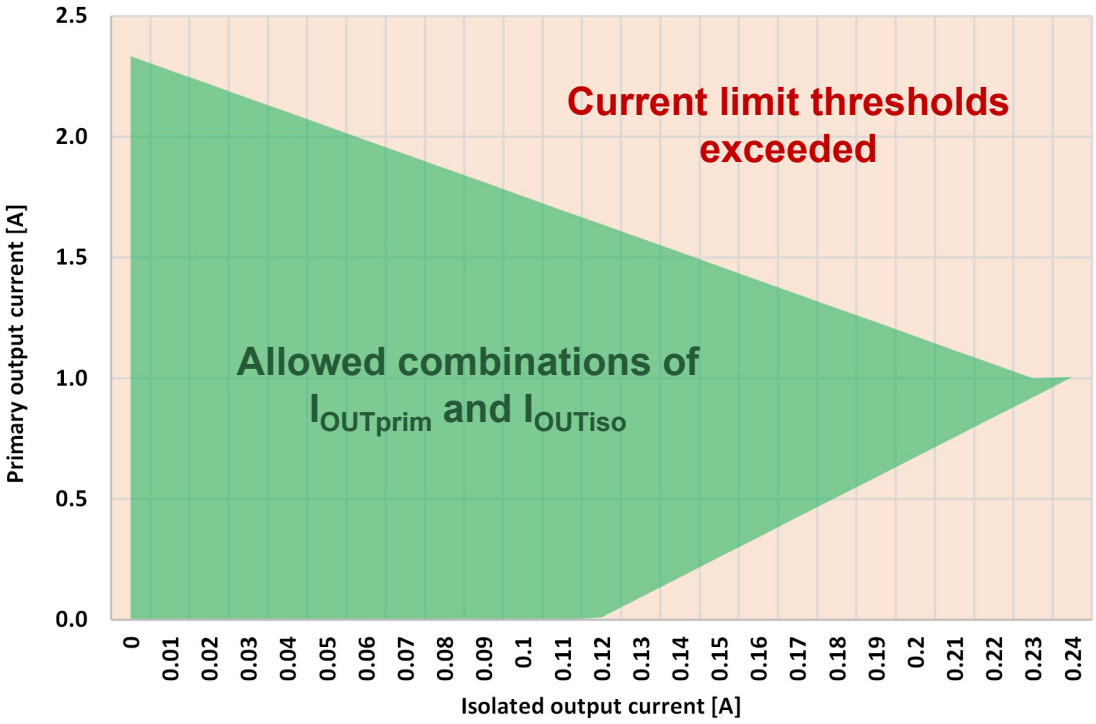
The maximum deliverable current in an iso-buck topology must take into account the equations (5) and (6). According to how much current is drawn from the isolated and not isolated outputs, I_{PEAKHS} or I_{PEAKLS} is the most stringent parameter.

Considering the schematic above and the components included, the graph below gives an idea about how much current, under these application conditions, can be drawn at the same time from the not isolated and isolated outputs, with different input voltages.

The green area represents all the combination of loads that can be applied at the same time to the primary (not isolated) and secondary (isolated) outputs. The area outside the green one represents combinations of load that would trigger either the peak current or reverse current protections.

The graph is a result of calculations and is based on the estimation of the peaks of the primary winding current, as described by the equations (5) and (6). Considerations about power dissipation and ambient temperature should be also taken into account.

Figure 50. **Maximum deliverable currents to the isolated and not isolated outputs**



8 Application board

The reference evaluation board schematic is shown in the figure below.

Figure 51. STEVAL-A6986IV1 evaluation board schematic

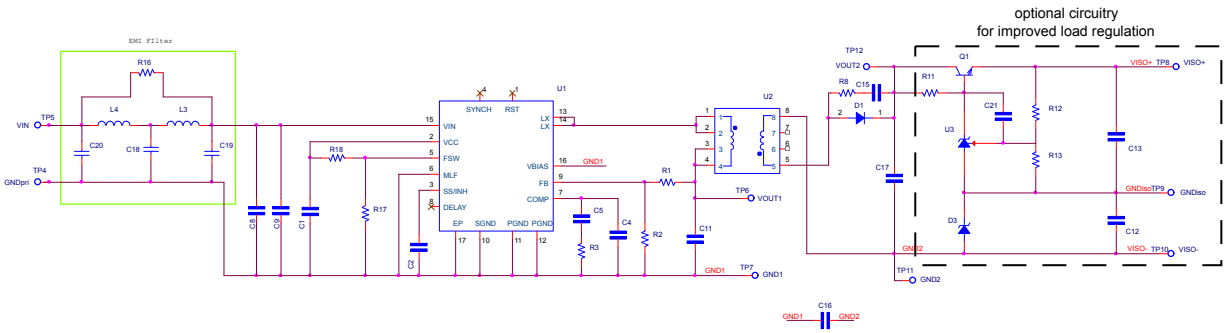


Figure 52. STEVAL-L6986IV1 evaluation board schematic

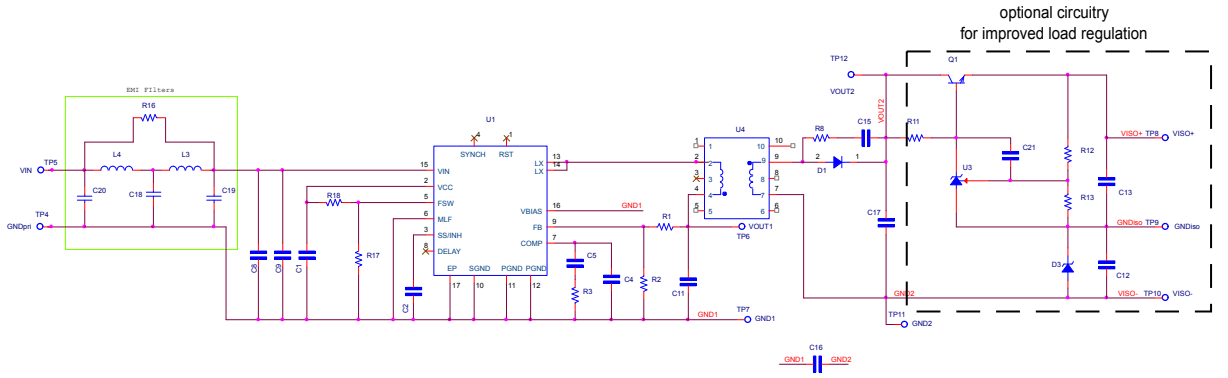
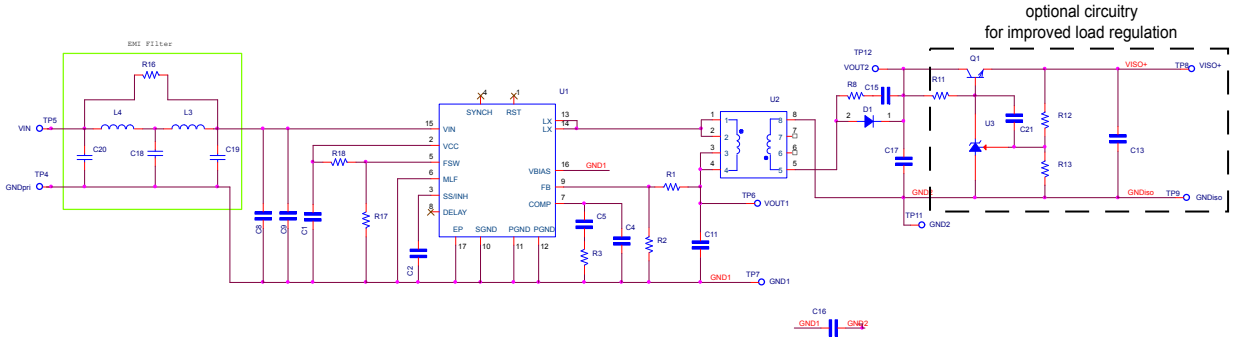


Figure 53. STEVAL-A6986IV2 evaluation board schematic



The additional input filter (C20, L4, C18, L3, C19) limits the conducted emission on the power supply. In case the filter is not necessary or should be by-passed for any test, a 0 Ω resistor can be placed at R16.

The evaluation board of the iso-buck is available with three different assemblies, mainly differentiated by the isolation of the transformer (3.3 kV / 1.5 kV) and the isolated output options (single or dual voltage), as summarized in the following table.

Table 10. Type of the evaluation boards

Assembly	Board name	Single/Dual isolated output(s)	Available isolated voltages
#1	STEVAL-A6986IV1	Dual	V_{ISO+} = 18 V, V_{ISO-} = -4.5 V
#2	STEVAL-L6986IV1	Dual	V_{ISO+} = 18 V, V_{ISO-} = -4.5 V
#3	STEVAL-A6986IV2	Single	V_{ISO+} = 5 V

Table 11. BOM of the evaluation boards

Reference		Part number	Description	Manufacturer
U1	#1, #3	A6986I		STM
	#2	L6986I		
C1			470 nF, 10 V, 0603	
C2			68 nF, 10 V, 0603	
C4			4.7 pF, 10 V, 0603	
C5			680 pF, 10 V, 0603	
C8, C11		CGA5L1X7R1H106K160AC	10 µF, 50 V, 1206	TDK
C9		CEU4J2X7R1H104K125AE	100 nF, 50 V, 0805	TDK
C12	#1, #2	CGA4J3X7R1H105K125AB	1 µF, 50 V, 0805	TDK
	#3		N/A	
C13		CGA4J3X7R1H105K125AB	1 µF, 50 V, 0805	TDK
C15	#1, #2		82 pF, 10 V, 0603	
	#3		68 pF, 10 V, 0603	
C16		not mounted		
C17		CNA6P1X7R1H106K250AE	10 µF, 50 V, 1210	TDK
C18		CGA5L3X5R1H475K	4.7 µF, 50 V, 1206	TDK
C19		CGA5L3X5R1H475K	4.7 µF, 50 V, 1206	TDK
C20		CGA5L3X5R1H475K	4.7 µF, 50 V, 1206	TDK
R1			6.8 kΩ, 1%	
R2			1.3 kΩ, 1%	
R3			56 kΩ, 1%	
R8	#1, #2		620 Ω, 1%	
	#3		180 Ω, 1%	
R11	#1, #2		430 Ω, 1%	
	#3		100 Ω, 1%	
R12	#1		36 kΩ, 1%	
	#2		22 kΩ, 1%	
	#3		10.7 kΩ, 1%	
R13	#1		5.6 kΩ, 1%	
	#2		4.3 kΩ, 1%	
	#3		11 kΩ, 1%	
R16			Not mounted	
R17			0 Ω	

Reference		Part number	Description	Manufacturer
R18			N.C.	
L3		XAL4030-472MEC	4.7 µH	Coilcraft
L4		MPZ2012S221A	Ferrite bead	TDK
D1		STPS1150AY	Schottky diode, 150 V, 1 A	STM
D3	#1, #2	BZT52B4V3-HE3-08	Zener Diode 4.3 V	Vishay Semiconductor
	#3	-	N/A	
Q1		2STR1215	NPN power transistor	STM
U2	#1	ZA9668-AE	Transformer, N = 5.8, 3.3 kV isolation	Coilcraft
	#2	2106.0007	Transformer, N = 5.6, 1.5 kV isolation	Magnetica
	#3	ZB1175-AE	Transformer, N = 1.53, 3.3 kV isolation	Coilcraft
U3		TL431AIL3T	Adjustable voltage reference	STM

8.1 Fine tuning of the evaluation boards

The evaluation boards can be customized to better match the user demands.

1. If a different dual isolated voltage is necessary (e.g. 15 V / - 6 V), the replacement of two components is enough to adapt the board: the Zener diode D3 (with a diode providing the most suitable Zener voltage) and the resistor divider (one of the two resistors) R12 - R13, in accordance with the equation:

$$V_{ISO+} = 2.49V \cdot \frac{R_{12} + R_{13}}{R_{13}} \quad (47)$$

   Obviously, the total voltage V_{ISO+} + $|V_{ISO-}|$ must be compatible with the available voltage at the secondarywinding of the transformer.

2. STEVAL-A6986IV1 and STEVAL-L6986IV1 can be also turned into a single isolated voltage board by soldering a 0 Ω resistor in place of the capacitor C12.

Any of the above-mentioned fine tunings could require an adjustment of the resistor R11.

Figure 54. **STEVAL-A6986IV1 (top layer)**

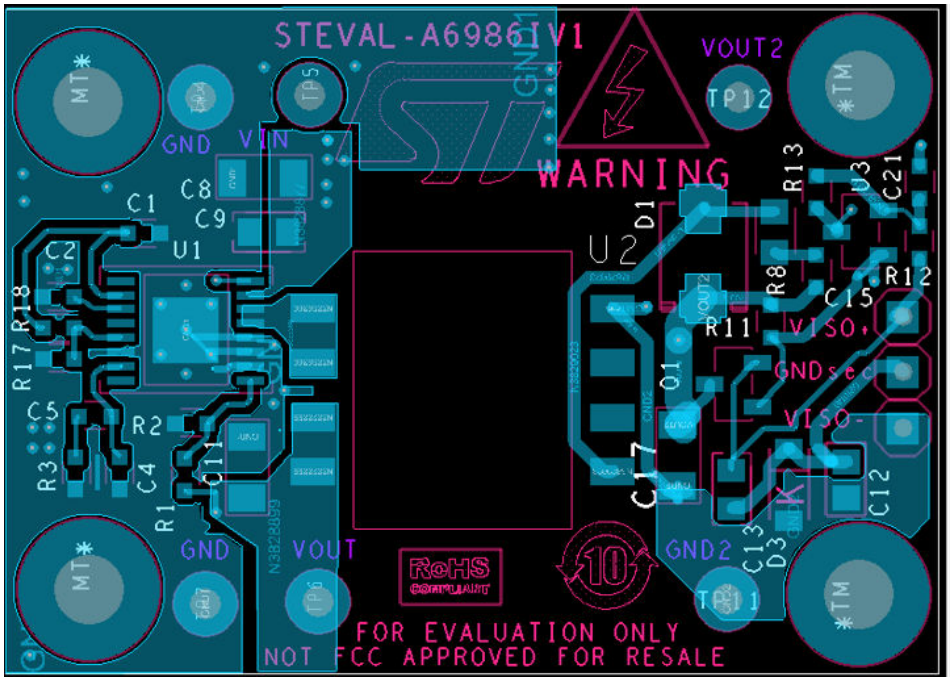


Figure 55. **STEVAL-A6986IV1 (bottom layer)**

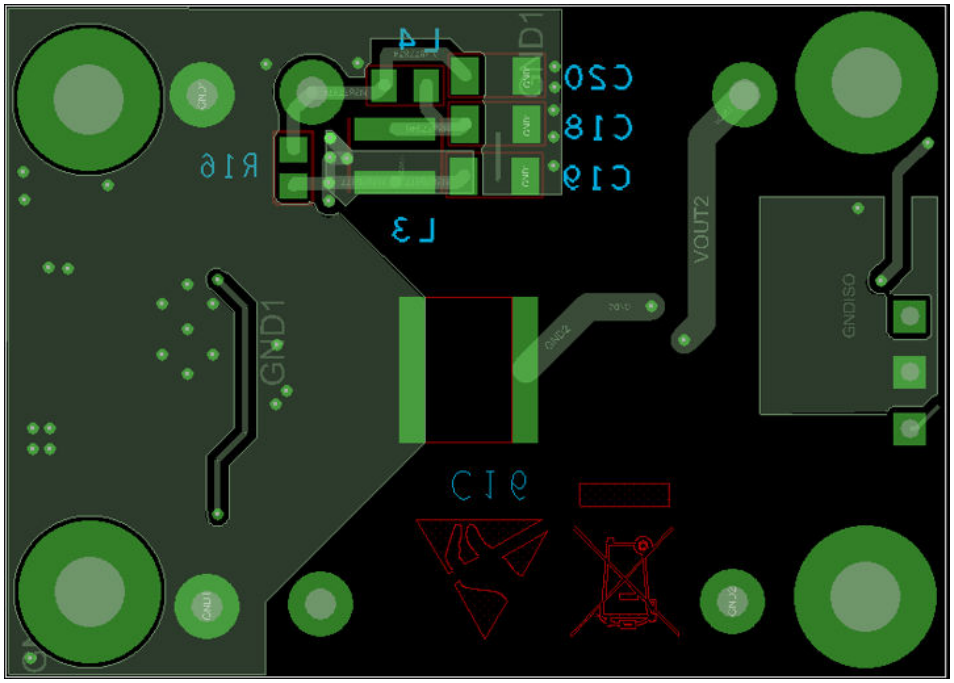


Figure 56. **STEVAL-L6986IV1 (top layer)**

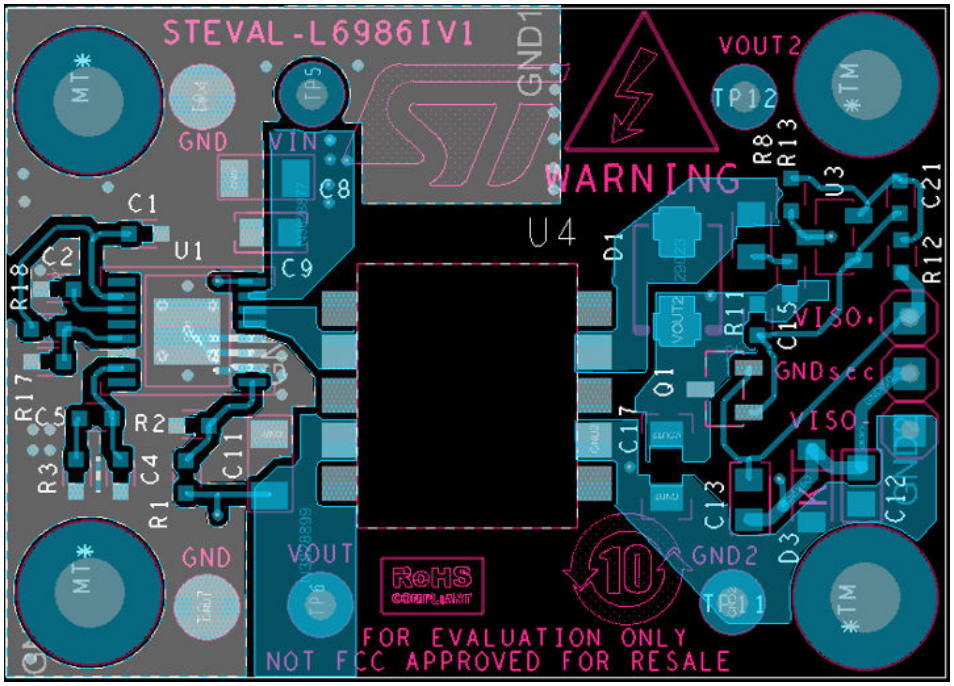


Figure 57. **STEVAL-L6986IV1 (bottom layer)**

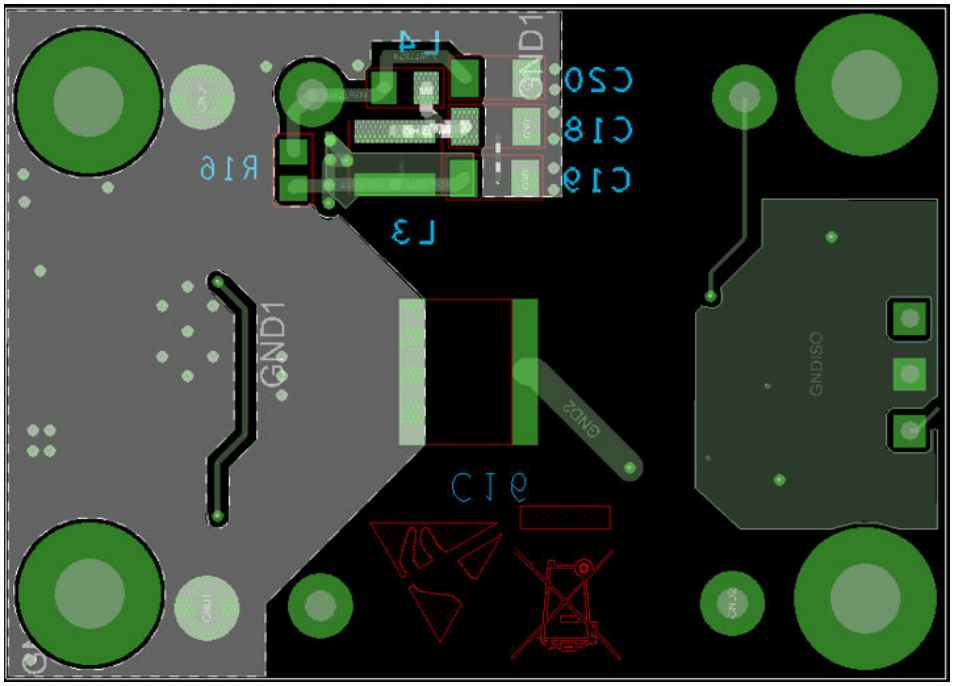


Figure 58. **STEVAL-A6986IV2 (top layer)**

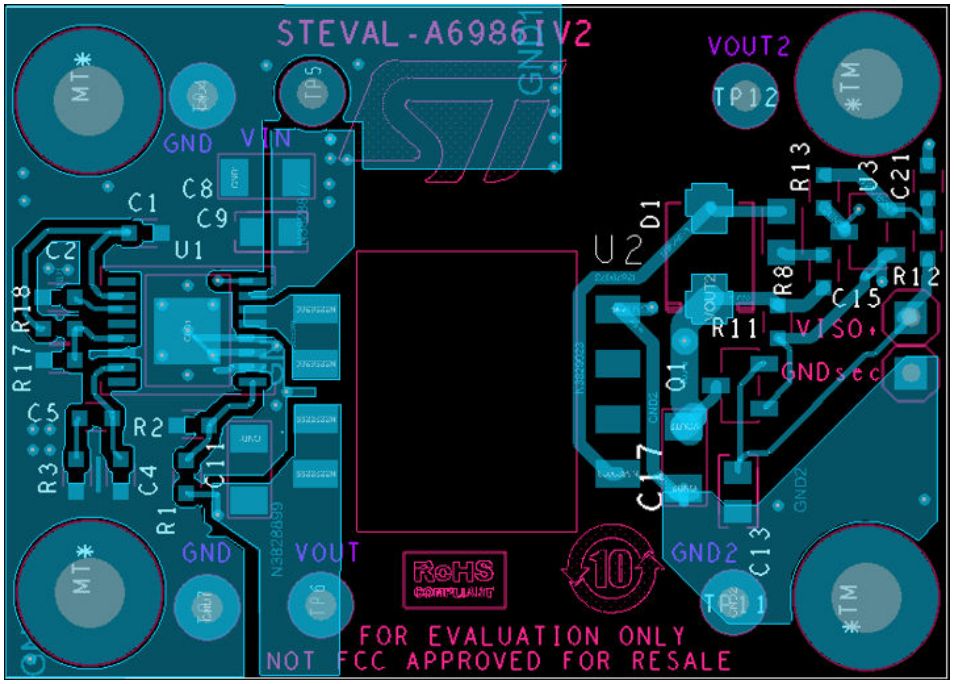
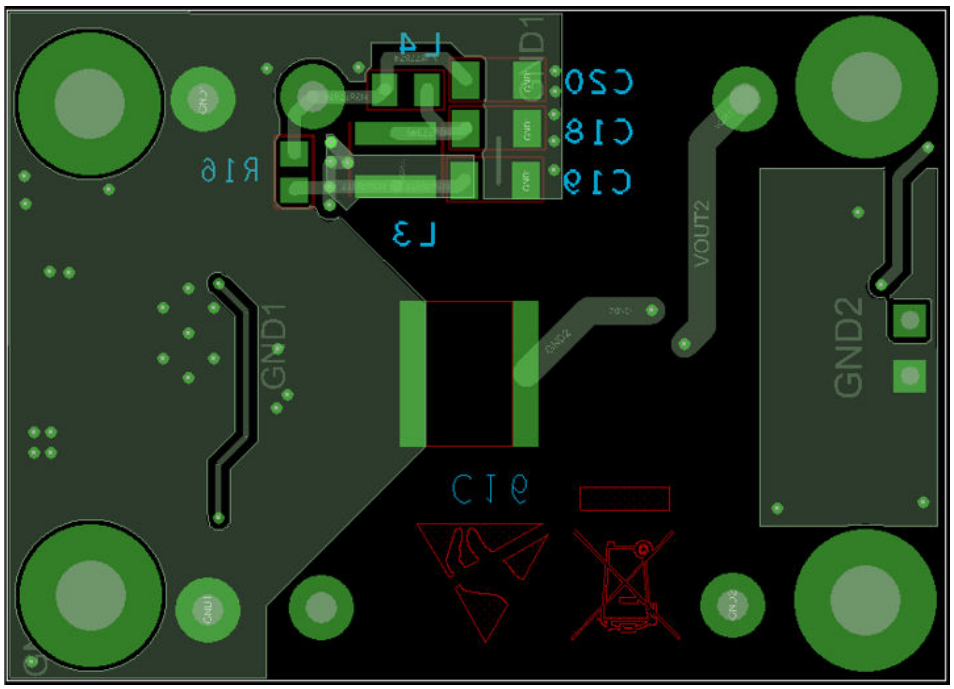


Figure 59. **STEVAL-A6986IV2 (bottom layer)**



8.2 Load regulation of the evaluation boards

Figure 60. STEVAL-A6986IV1, V_{IN} = 12 V, f_{SW} = 500 kHz (V_{ISO+})

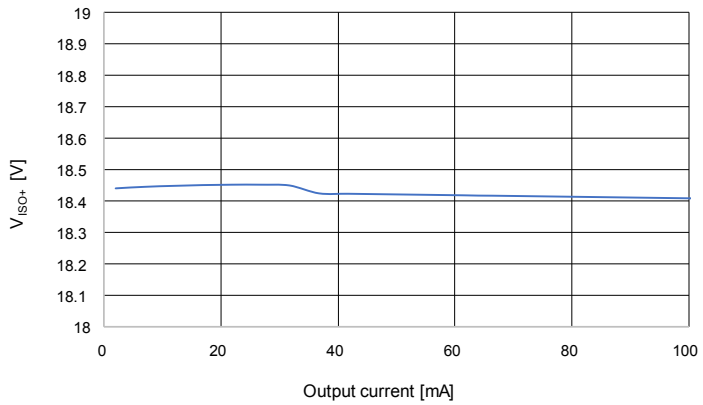


Figure 61. STEVAL-A6986IV1, V_{IN} = 12 V, f_{SW} = 500 kHz (V_{ISO-})

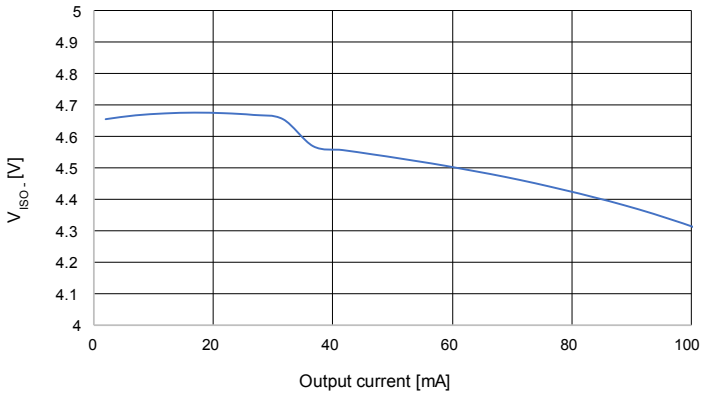


Figure 62. STEVAL-L6986IV1, V_{IN} = 12 V, f_{SW} = 500 kHz (V_{ISO+})

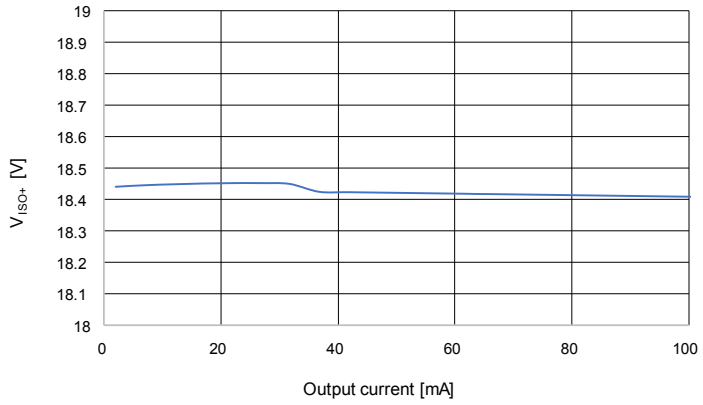


Figure 63. **STEVAL-L6986IV1, V_{IN} = 12 V, f_{SW} = 500 kHz (V_{ISO-})**

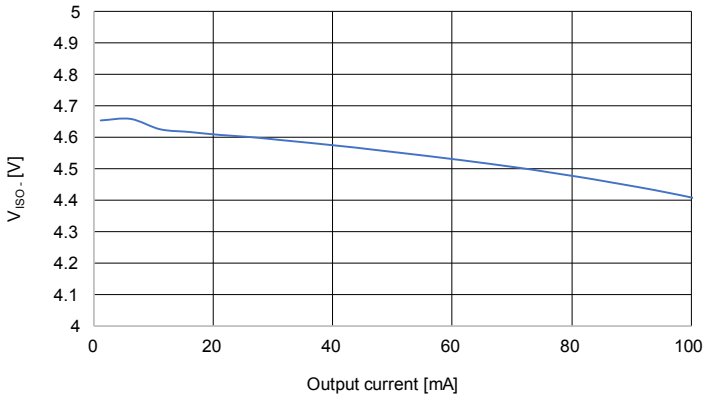
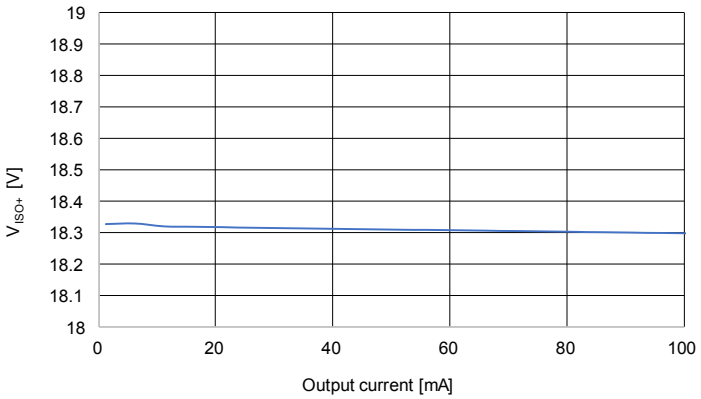


Figure 64. **STEVAL-A6986IV2, V_{IN} = 12 V, f_{SW} = 500 kHz (V_{ISO+})**



9 STEVAL-A6986IV3

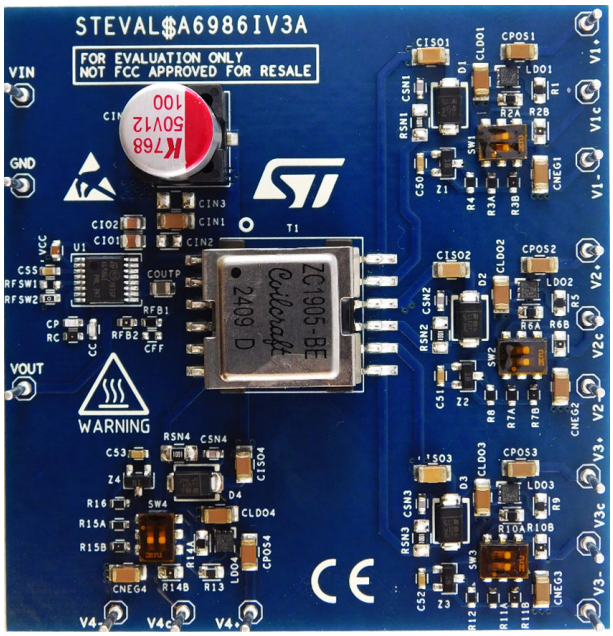
From a buck converter, with minor changes, an inverting buck-boost topology can be derived. The use of an inverting buck-boost in an isolated topology generates an isobuck-boost.

The advantages of implementing an isobuck-boost are extensively described in the application note AN5960.

Among them, the most relevant benefit consists of a better exploitation of the current capability of the device, with a remarkable increase in the deliverable power.

The STEVAL-A6986IV3 (see Figure 65) is based on the A6986I (it is however suitable for L6986I too) and implements an isobuck-boost topology

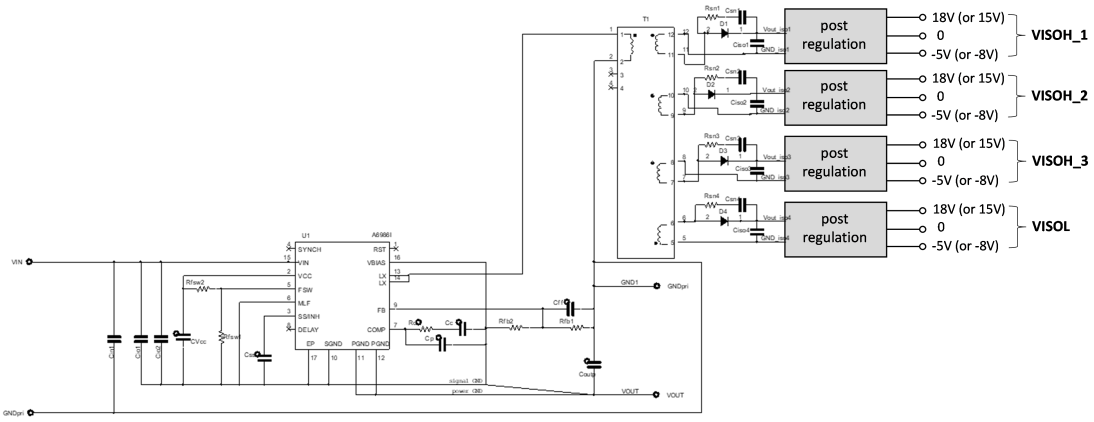
Figure 65. STEVAL-A6986IV3



The increased deliverable power allows for supporting a complete driving solution for a three-phase system, as depicted in Figure 66.

Each of the four outputs generates a dual voltage, which can be selected by a micro-switch: 18 V/-5 V or 15 V/-8 V. These voltages are extremely accurate. With minor changes (just replacing few resistors) it is also possible to regulate other commonly required voltages, for instance 6 V/-3 V or a single 12 V.

Figure 66. Principal scheme of STEVAL-A6986IV3



The BOM and other details about the STEVAL-A6986IV3 (settings, performances, etc.) can be found in the UM3340.

10 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 HTSSOP16 package information

Figure 67. HTSSOP16 package outline

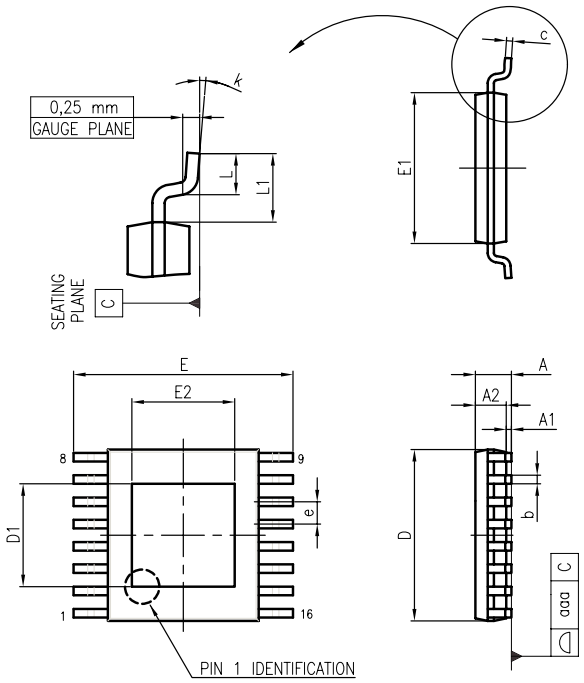


Table 12. **HTSSOP16 mechanical data**

Symbol	mm		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
D1	2.8	3	3.2
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.8	3	3.2
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
K	0.00		8.00
aaa			0.10

11 Ordering information

Table 13. **Ordering information**

Part number	Package	Packing
L6986I	HTSSOP16	Tube
L6986ITR		Tape and reel

Revision history

Table 14. **Document revision history**

Date	Version	Changes
26-Mar-2021	1	First release.
27-Set-2021	2	Updated Figure 13. Simulation with appropriate masking time (330 ns). Added R17 description in Table 11. BOM of the evaluation boards
14-Jan-2025	3	Update Section 7. Added Section 9.

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