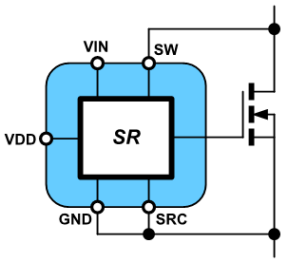
Flyback Sync Rect Controller IC

Features

High Frequency SR Controller

- Compatibility of continuous conduction mode (CCM), quasi-resonant (QR) and discontinuous conduction mode (DCM) at low side applications.
- Wide input voltage ranges up to 26.5V
- Optimized SR gate turn-off threshold control
- Proprietary CCM SR turn-off control algorithm
- Minimized SR turn-on/off propagation delay
- SR MOSFET gate passive clamp
- Low power saving mode
- Small footprint with SOT-23-6L package

SOT-23-6L Package



Simplified Schematic

Topologies / Applications

- USB PD quick chargers for smart phones, feature phones and tablet PCs
- Power adaptor for portable device
- Flyback power supply with fixed or variable output voltage

Description

NV9701 is a secondary-side synchronous rectifier (SR) controller for isolated flyback converters. By implementing proprietary turn-off control algorithm, NV9701 can reliably support discontinuous conduction mode (DCM), quasi-resonant (QR) and continuous conduction mode (CCM) operation, which will help to design robust flyback converters. Small footprint SOT-23-6L package enables designers to achieve simple, quick and reliable solutions. Navitas' controller IC technologies enable high frequencies, high efficiencies and low EMI to achieve unprecedented power densities at a very attractive cost structure.

Simplified Application Diagram

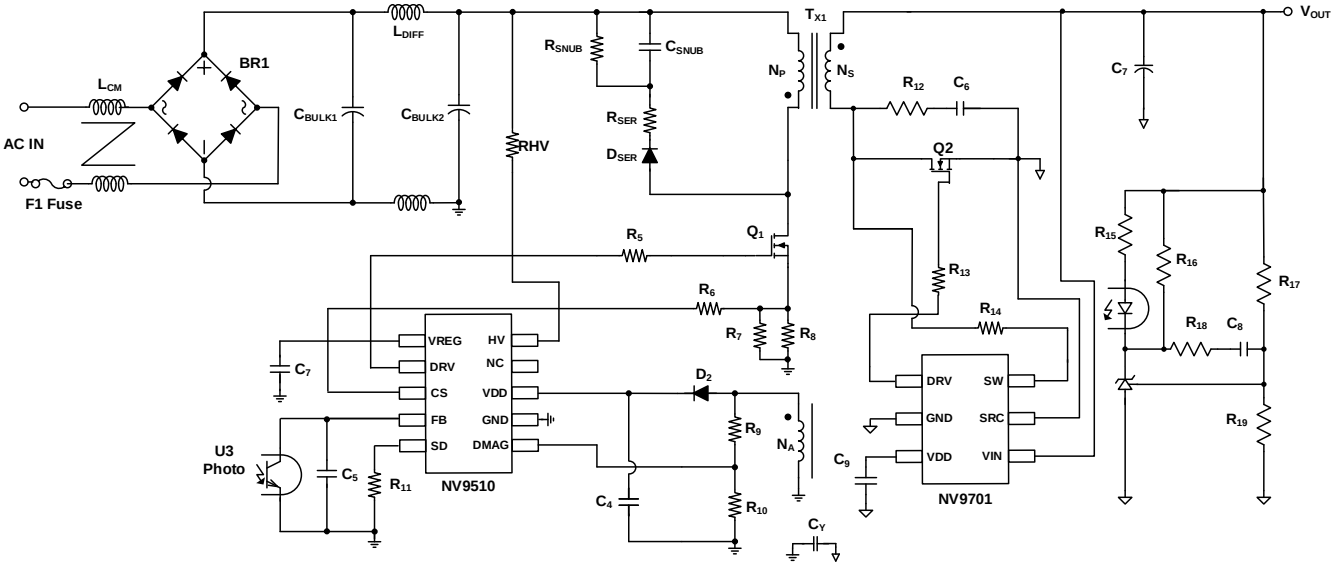
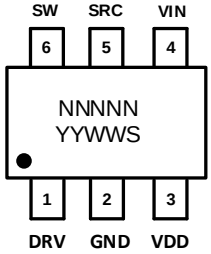


Figure 1. Low-Side SR Application Diagram

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
NV9701SC01	-40°C to +125°C	6-Lead, SOT23	3K/Tape & Reel

Pin Configuration and Marking Diagram



Symbol	Content
NNNNN	Lot Number
YY	Year Code
WW	Week Code
S	Supplier Code

Figure 2. NV9701 Pin Configuration & Marking Diagram (Top View)

Pin Function

Pin No.	Name	Description
1	DRV	Synchronous MOSFET gate drive output.
2	GND	Ground.
3	VDD	Internal regulator 5V output and gate driver power supply rail. Bypass with 1µF capacitor to GND.
4	VIN	Supports up to 26.5V operation, input of an integrated 5V LDO which generates the internal power supply for the low-voltage control circuitry.
5	SRC	Synchronous MOSFET source sense input.
6	SW	Synchronous MOSFET drain sense input.

Table 1. NV9701 Pin Definition

Internal Function Block Diagram

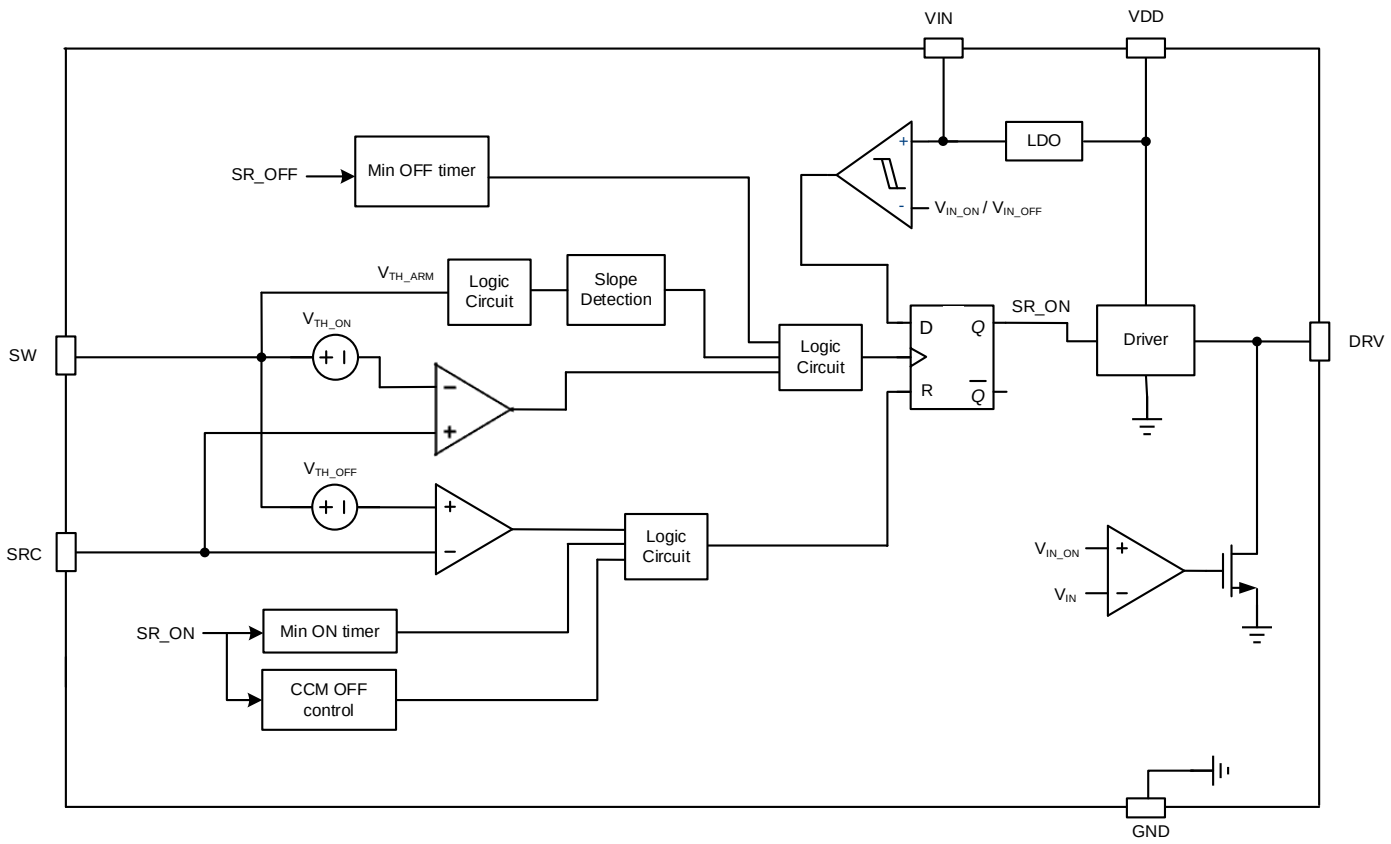


Figure 3. NV9701 Internal Function Block Diagram

Electrical Characteristics

Absolute Maximum Ratings(1)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
VIN	Power Supply Input Pin Voltage		-0.3	28	V
SW	SW Sense Input Pin Voltage		-1.0	120	V
VDD	Internal Regulator Output Pin Voltage		-0.3	6.0	V
DRV	Gate Drive Output Pin Voltage		-0.3	6.0	V
SRC	Source Sense Input Pin Voltage		-0.3	6.0	V
TJ	Operating Junction Temperature		-40	150	°C
TSTG	Storage Temperature Range		-60	150	°C
TL	Lead Soldering Temperature		-	260	°C
ESD	Electrostatic Discharge Capability	Human Body Mode, ANSI/ESDA/JEDEC JS-001-2017	-	2.0	kV
		Charge Device Mode, JED ANSI/ESDA/JEDEC JS-001-2018	-	2.0	kV

Notes (1):

- *Stress beyond those listed under absolute maximum ratings may cause permanent damage to the device.*
- *All voltage values are with respect to the GND pin*

Recommended Operating Conditions (2)

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance. Elevation does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
VIN	Power Supply Input Pin Voltage	3.0	-	24	V
SW	SW Sense Input Pin Voltage	-1.0	-	120	V
VDD	Internal Regulator Output Pin Voltage	-0.3	-	5.5	V
DRV	Gate Drive Output Pin Voltage	-0.3	-	5.5	V
SRC	Source Sense Input Pin Voltage	-0.3	-	5.5	V

Notes (2):

- *Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied, exposure to absolute maximum rated conditions of extended periods may affect device reliability. All voltage values are with respect to the normal operation ambient temperature range is from -40°C to +85°C unless otherwise noted.*

Electrical Specifications

V_{IN} (Typ.) = V_{DD} (Typ.) = 5V, T_A =-40°C to 85°C, and T_A (Typ.) =25°C, unless otherwise specified.

Parameter		Test Conditions	Min.	Type.	Max.	Unit
Power Supply						
V_{IN_ON}	Turn-on Input Voltage	Vin Rising	2.0	2.2	2.4	V
V_{IN_OFF}	Turn off Input Voltage	Vin Falling	1.8	2.0	2.2	V
I_{IN_GREEN}	Quiescent Current	No DRV Switching	-	200	260	µA
T_{GREEN}(3)	Time Threshold for Power Save		-	100	-	µs
$I_{IN\_OP\_20kHz\_5V}$	Operating Current at 5V	F_{SW} = 20kHz, V_{IN} = 5V	-	420	520	µA
$I_{IN\_OP\_100kHz\_5V}$	Operating Current at 5V	F_{SW} = 100kHz, V_{IN} = 5V	-	450	650	µA
$I_{IN\_OP\_100kHz\_20V}$ (3)	Operating Current at 20V	F_{SW} = 100kHz, V_{IN} = 20V	-	450	-	µA
V_{DD_ON}	VDD Turn-on Threshold	V_{DD} Rising	2.7	2.9	3.1	V
V_{DD_OFF}	VDD Turn-off Threshold	V_{DD} Falling	2.5	2.7	2.9	V
V_{DD_0A}	VDD Regulation Voltage W/O Load	V_{IN}=12V I_{VDD}=0A	4.8	5.0	5.2	V
V_{DD_10mA}	VDD Regulation Voltage with 10mA Load	V_{IN}=12V I_{VDD}=10mA	4.7	4.9	5.1	V
SW Pin Sensing						
V_{TH_ON}	Turn-on Threshold		-405	-250	-95	mV
T_{ON_DLY} (3)	Turn-on Delay Time		-	10	-	ns
V_{TH_OFF}	Turn-off Threshold		0.01	-	0.8	mV
T_{OFF_DLY} (3)	Turn-off Delay Time		-	10	-	ns
SR Gate Control						
T_{ON_MIN}	SR Minimum ON-Time		295	350	405	ns
$T_{ON\_MIN\_H}$	T_{ON_MIN} at Heavy Load		565	650	735	ns
T_{OFF_MIN} (3)	SR Minimum OFF-Time		-	1.2	-	µs
Output Driver						
V_{OL} (3)	Driver Output Low Voltage		-	-	0.25	V
V_{OH}	Driver Output High Voltage		4.85	5.0	VDD	V
t_R	DRV Rise Time	C_L=10nF, DRV=1→4V	9	20	31	ns
t_F	DRV Fall Time	C_L=10nF, DRV=4→1V	3	10	15	ns

Note (3):

- *Guaranteed by design*

Typical Performance Characteristics

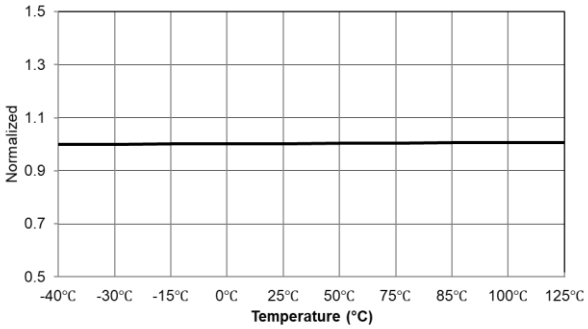


Figure 4 V_{IN_ON}

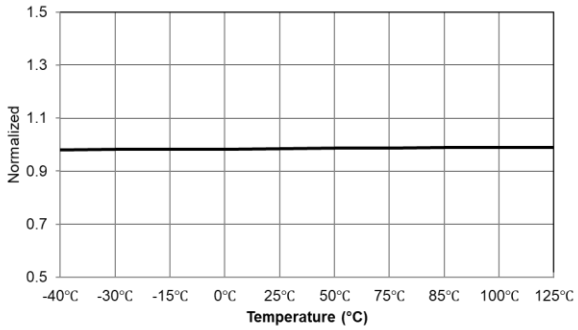


Figure 5 V_{IN_OFF}

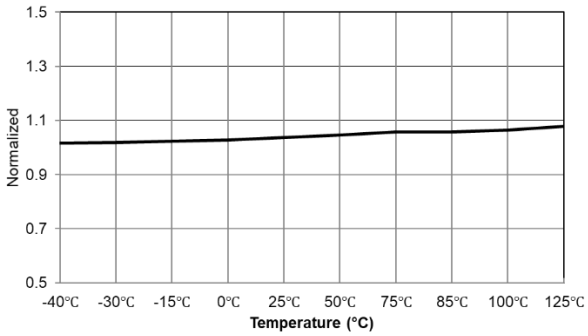


Figure 6 I_{IN_GREEN}

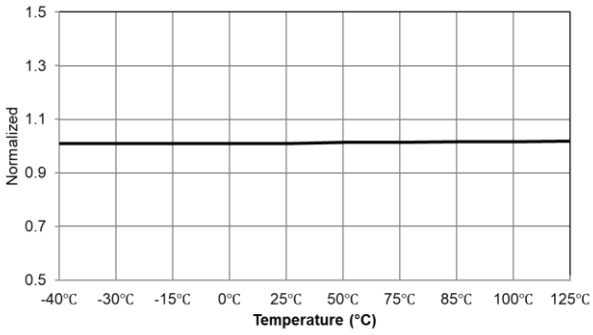


Figure 7 V_{DD_ON}

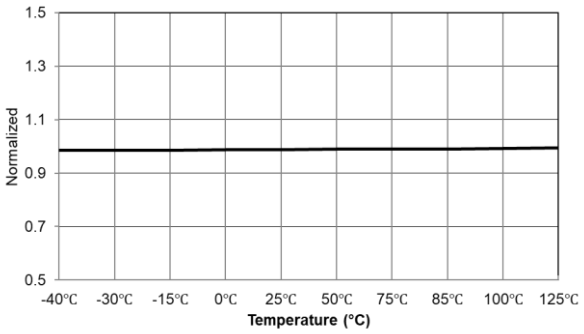


Figure 8 V_{DD_OFF}

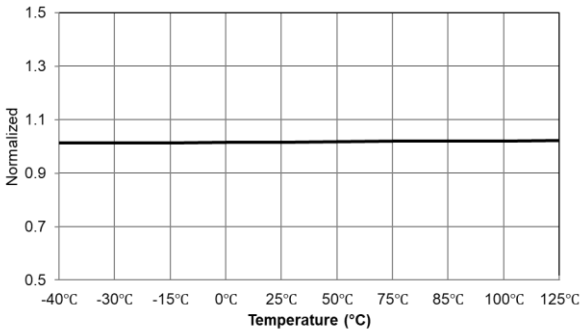


Figure 9 V_{DD_LDO}

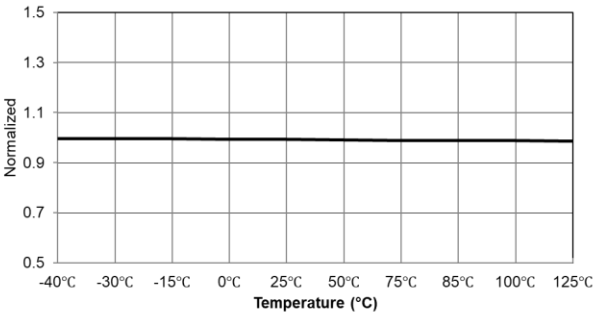


Figure 10 V_{LDO}

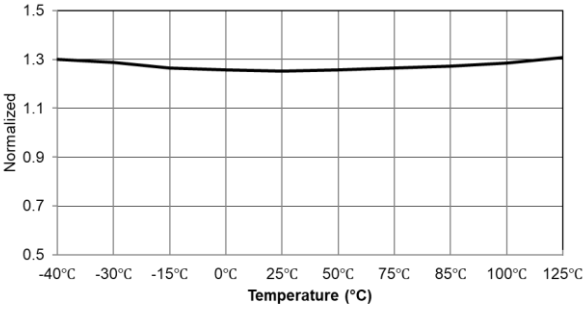


Figure 11 $I_{IN\_OP\_20kHz\_5V}$

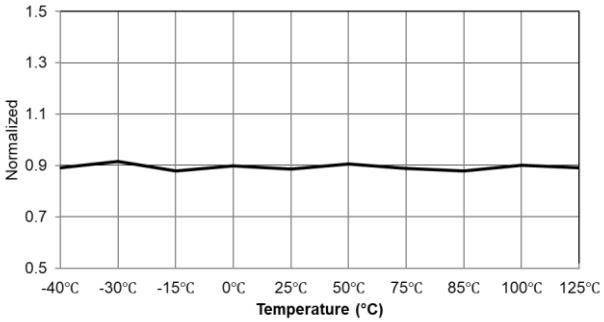


Figure 12 V_{TH_ON}

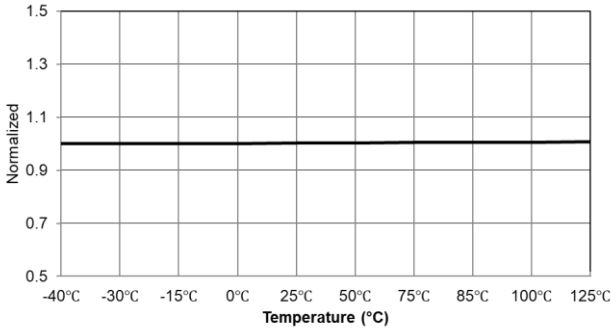


Figure 13 V_{TH_OFF}

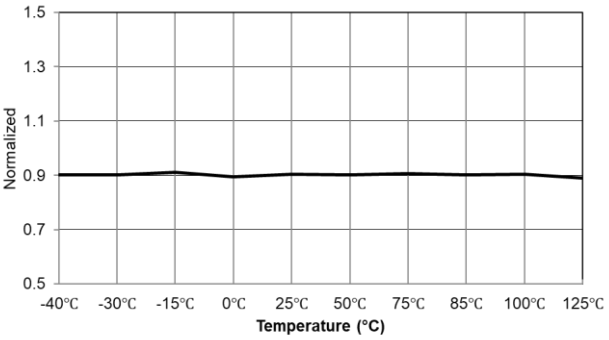


Figure 14 T_{ON_MIN}

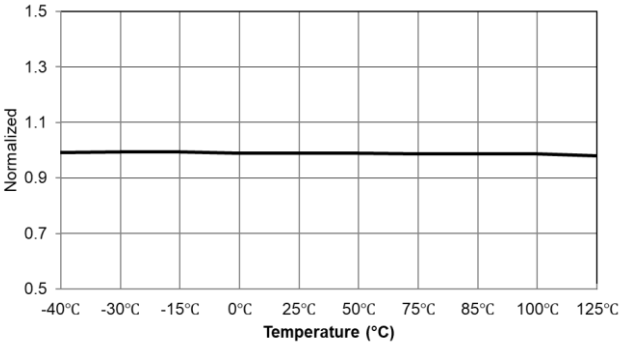


Figure 15 $T_{ON\_MIN\_H}$

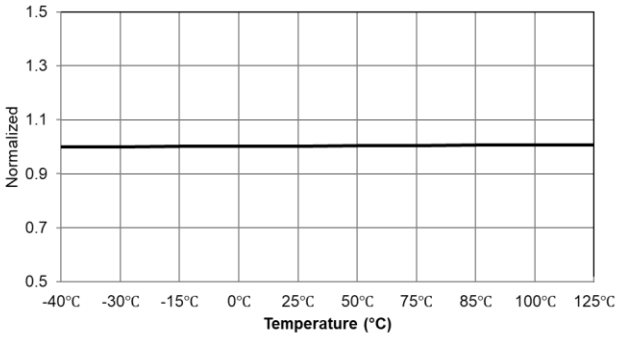


Figure 16 V_{OH}

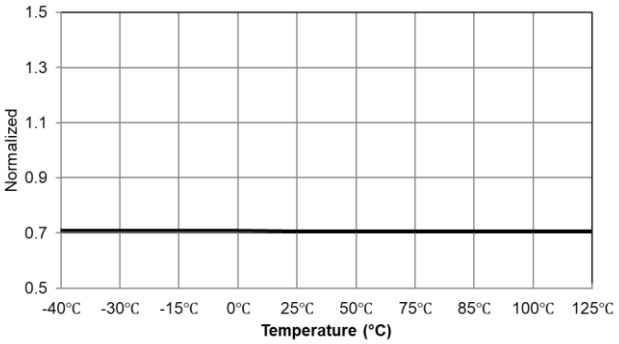


Figure 17 t_R

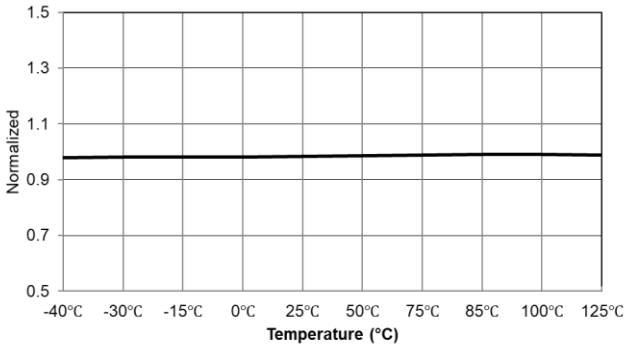


Figure 18 t_F

Typical Performance Characteristics *(Continued)*

Operating at 65W Flyback Application
VIN= 115VAC, VOUT= 5V, IOUT= 3A

CH1: VDS 20V/div, CH2: DRV 5V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 230VAC, VOUT= 5V, IOUT= 3A

CH1: VDS 20V/div, CH2: DRV 5V/div, CH3: VDD 5V/div

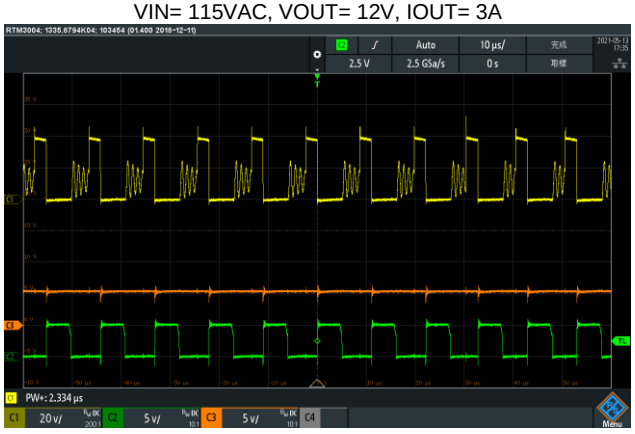
Operating at 65W Flyback Application
VIN= 115VAC, VOUT= 9V, IOUT= 3A

CH1: VDS 20V/div, CH2: DRV 5V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 230VAC, VOUT= 9V, IOUT= 3A

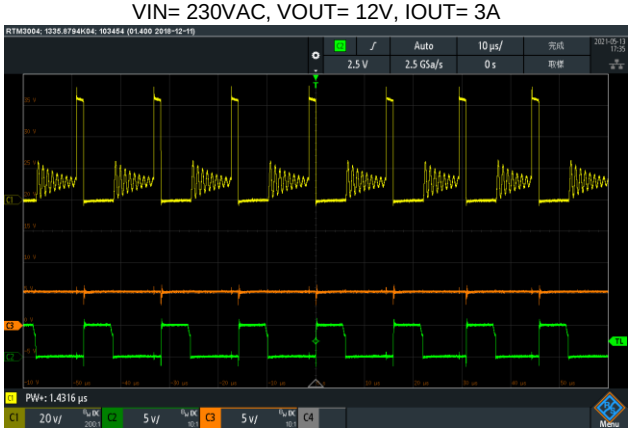
CH1: VDS 20V/div, CH2: DRV 5V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 115VAC, VOUT= 12V, IOUT= 3A



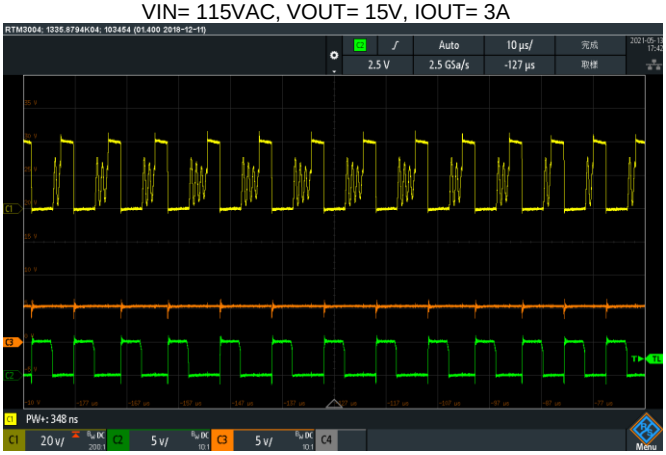
CH1: VDS 20V/div, CH2: DRV 5V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 230VAC, VOUT= 12V, IOUT= 3A



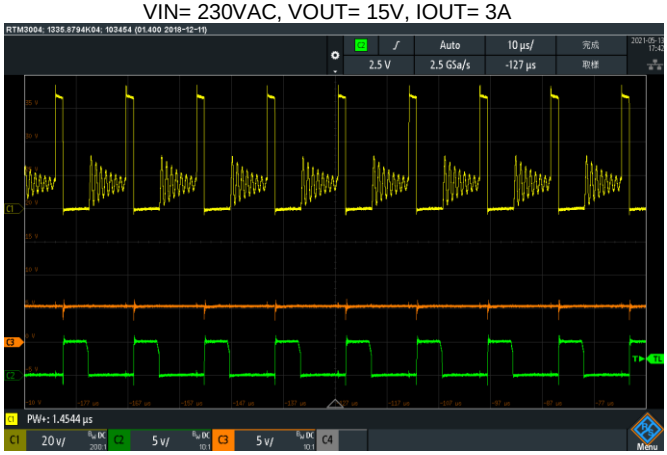
CH1: VDS 20V/div, CH2: DRV 5V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 115VAC, VOUT= 15V, IOUT= 3A



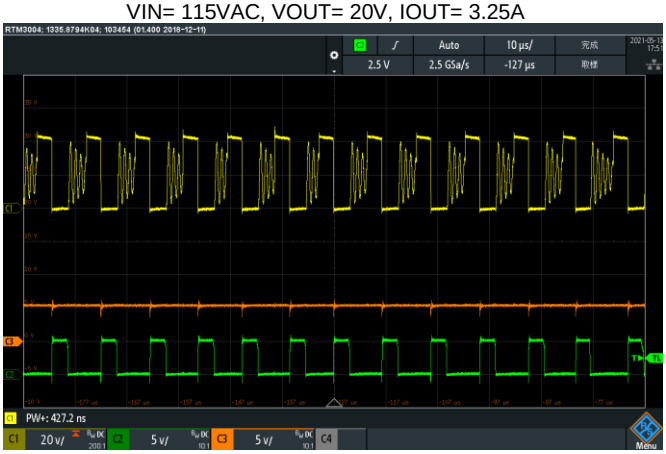
CH1: VDS 20V/div, CH2: DRV 5V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 230VAC, VOUT= 15V, IOUT= 3A



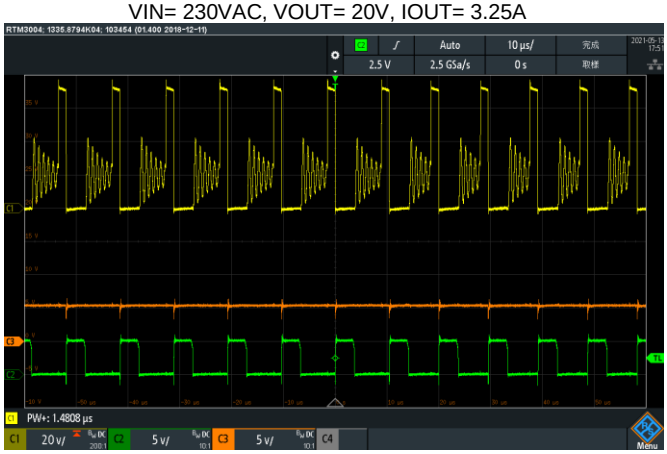
CH1: VDS 20V/div, CH2: DRV 5V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 115VAC, VOUT= 20V, IOUT= 3.25A



CH1: VDS 20V/div, CH2: DRV 5V/div, CH3: VDD 5V/div

Operating at 65W Flyback Application
VIN= 230VAC, VOUT= 20V, IOUT= 3.25A



CH1: VDS 20V/div, CH2: DRV 5V/div, CH3: VDD 5V/div

Detailed Function Description

Operation

NV9701 supports operation in discontinuous conduction mode (DCM), quasi-resonant (QR) and continuous conduction mode (CCM) flyback converters. The control circuitry controls the gate of synchronous rectification (SR) MOSFET on in forward mode and turn the gate off when the SR MOSFET current drops to certain value.

VDD Power Supply

VDD is the supply power for the NV9701, a bypass ceramic (typical 1μF) capacitor should be put closely from VDD to GND to guarantee the normal operation.

During startup, when V_{IN} rises above V_{IN_ON} (2.2V) and VDD rises to V_{DD_ON} (2.9V), NV9701 starts to operate according to its internal logic. When VDD falls below V_{DD_OFF} (2.7V) or V_{IN} falls below V_{IN_OFF} (2.0V), then NV9701 stops working right away.

SR Gate Turn-On Control

As shown in Figure 19, the turn-on of SR GATE is active when the SW sense voltage is lower than turn on threshold V_{TH_ON} (-250mV). To prevent the mis-trigger turn-on of SR MOSFET, a minimum off time T_{OFF_MIN} is used after SR MOSFET is turned off.

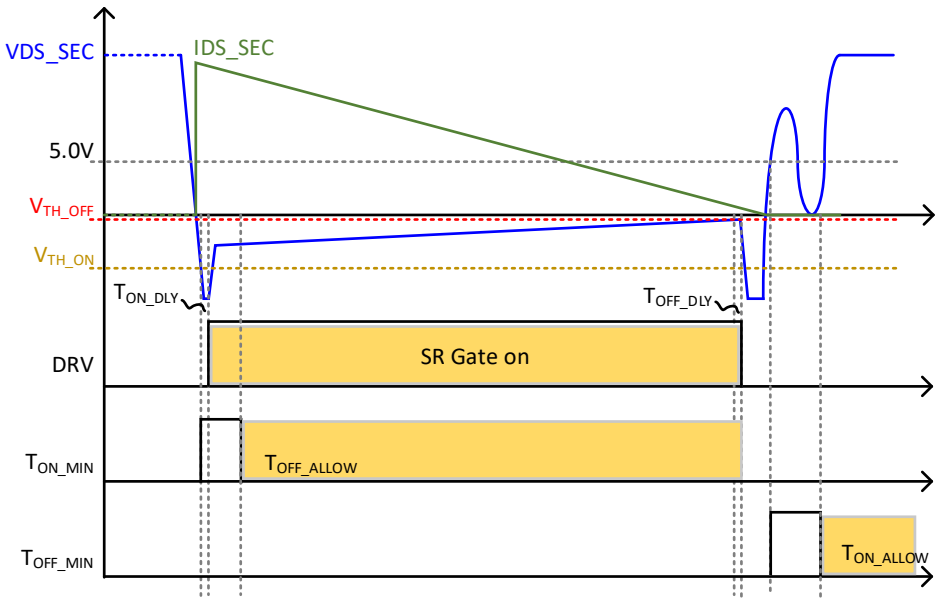


Figure 19. SR Turn-On Control Sequence

SR Gate Turn-Off Control

NV9701 will detect the SW voltage, when it is higher than V_{TH_OFF} (0mV), the GATE will be turned off.

PCB Layout Guidelines

Optimized PCB layout is key for stable operation. Please refer to following layout guidelines to design your platform.

Sensing Loop for VSW and VSRC

- Make the sensing path of SW, SRC as short to Drain and Source of SR MOSFET as possible.
- Make two independent routing trace to Drain and Source of SR MOSFET directly.
- Make NV9701 device out of the power loop to prevent interrupting from the switching noise.

SR Gate Driver Loop

- Make VDRV routing trace far away from the switching point (such as Drain and Source of SR MOSFET).
- Minimize the gate driver loop as short as possible to prevent the interference of noise.
- Do not make VDRV routing trace on the other side of VSW and VSRC.

Power Supply Loop

- Put a low ESR and low ESL decoupling ceramic capacitor from VDD to GND as close to NV9701 as possible for stable power supply. Below shows a layout example of a single layer with PowerPAK/SO-8 package SR MOSFET with SR MOSFET put in low side for reference.
- In the PCB layout, RSNUB and CSNUB are the RC snubber network for the SR MOSFET. The VDD decoupling capacitor (CVDD) is placed close to VDD GND. The sensing loop (SRC, SW to the Source and Drain of SR MOSFET) is minimized and keep away from the switching power loop.

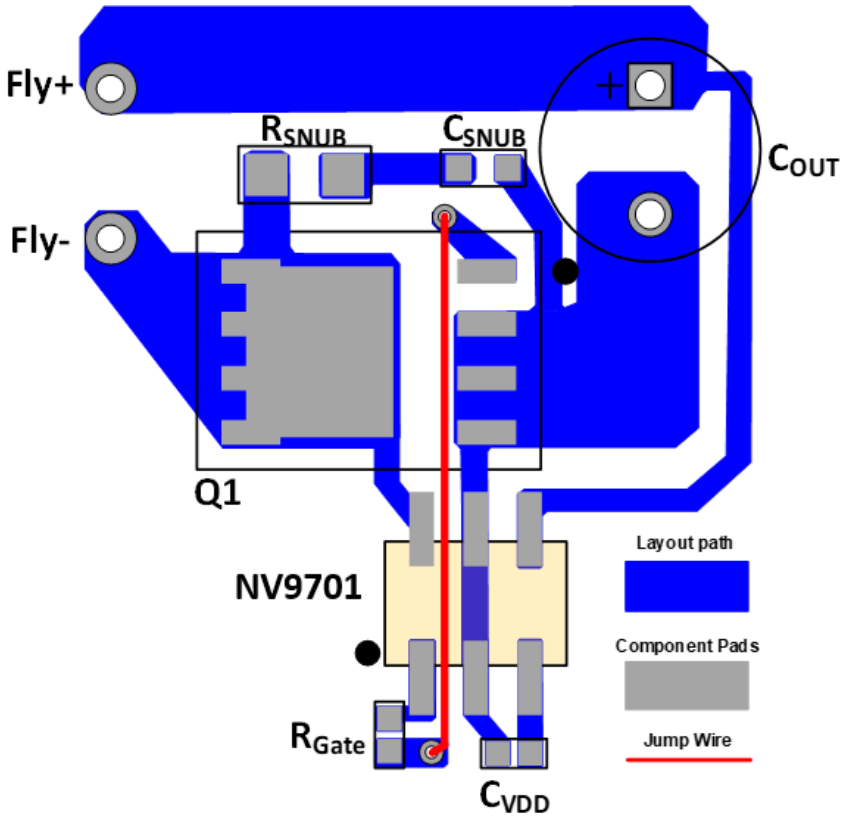
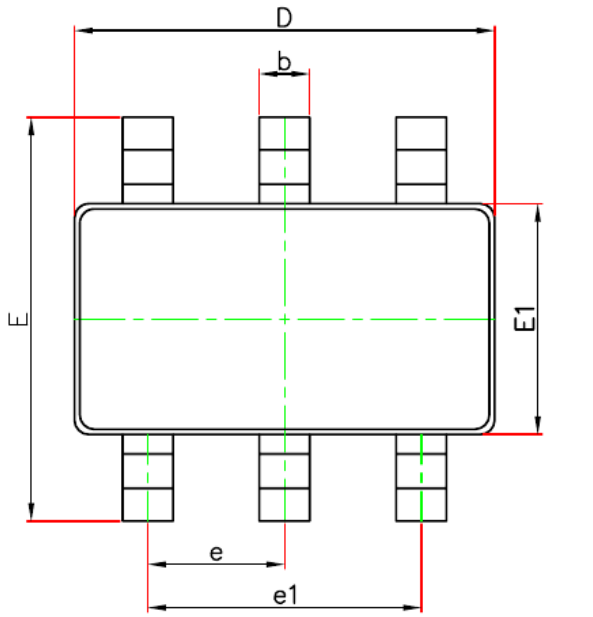
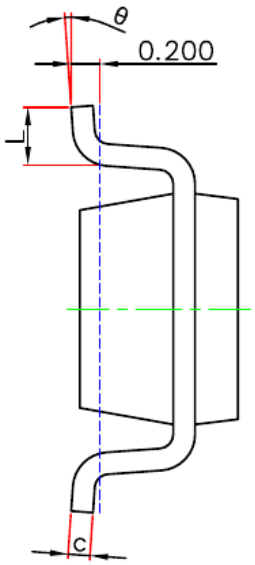


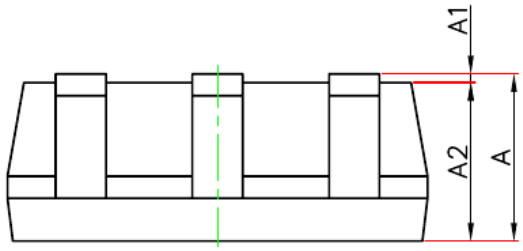
Figure 20. Layout with PowerPAK/SO-8 SR MOSFET

Package Dimensions

SOT-23-6L(12R) PACKAGE OUTLINE DIMENSIONS

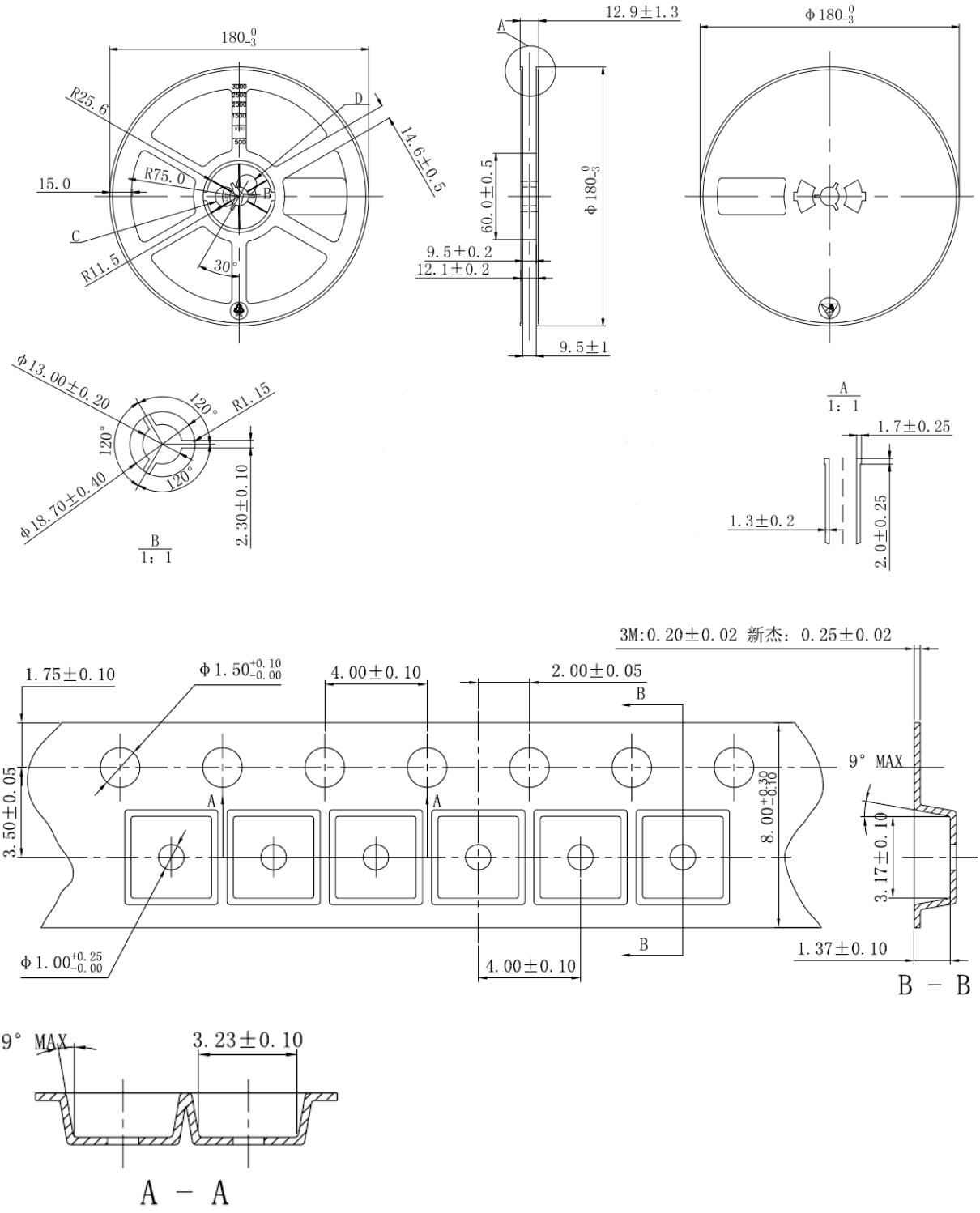






Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Tape and Reel Information



Revision History

Date	Status	Notes
May. 12, 2023	DATASHEET	First publication
Sep. 6, 2023		Update AMR data
Sep. 21, 2023		- Add Supplier Code in Pin Configuration and Marking Diagram - Revise T_{OFF_MIN} Specification (NO DESIGN CHANGE)
May. 27, 2024		- Remove high side application because it causes additional design effort to system cost and layout space. - Mark pin name on pin1~pin3 at Figure 2, page 2.

Additional Information

Contact info@navitassemi.com