DATA SHEET

GRF6402

RELEASE B DATA SHEET

31.75 dB RANGE / 0.25 dB STEP DSA
0.05 to 6 GHz

FEATURES

- 31.75 dB Range
- 0.25 dB Steps via 7-bit Control
- Serial Interface with Support for 8 Addresses
- Programmable *Rapid Fire* Attenuation Setting Which Circumvents Delays Associated with SPI Programming
- Defaults to Full Attenuation for Power-on Resets
- Glitchless Stepping (< 2 dB Over/Undershoot)
- 47 ns Settling Time for 0.25 dB Steps
- Bi-directional RF Use
- 3.3 V and 5 V Supply Voltages
- 50 Ω Single-ended Input and Output Impedances
- -40 to 115 °C Operating Temperature Range
- Compact 3 X 3 mm QFN-16 Package

Reference: 5 V / 2 GHz

- IL: 1.3 dB
- IP0.1dB: 30.5 dBm
- IIP3: 56.2 dBm
- INL Attenuation Error: 0.04 dB
- DNL Attenuation Error: 0.05 dB

APPLICATIONS

- 5G Wireless Infrastructure
- Cellular Repeaters/Boosters & DAS Systems
- Automotive Cellular and V2X Compensators
- Millimeter Wave IF Stages
- High-performance Gain Trim & AGC Loops
- TDD Applications Where a Common DSA Is Shared for Both TX and RX Modes of Operation

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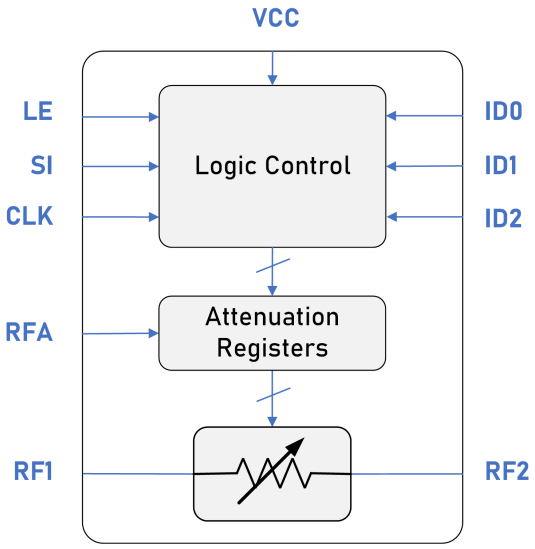
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DESCRIPTION

The GRF6402 is an SPI-controlled, bi-directional, 31.75 dB range digital step attenuator that provides precise stepping in 0.25 dB increments. The device's serial interface utilizes three externally defined address bits, allowing up to 8 unique devices to share a common SPI bus. In addition to supporting traditional serial programming, the GRF6402 also includes a special *Rapid Fire* selection pin which allows the device to be immediately switched into a pre-defined attenuation state.

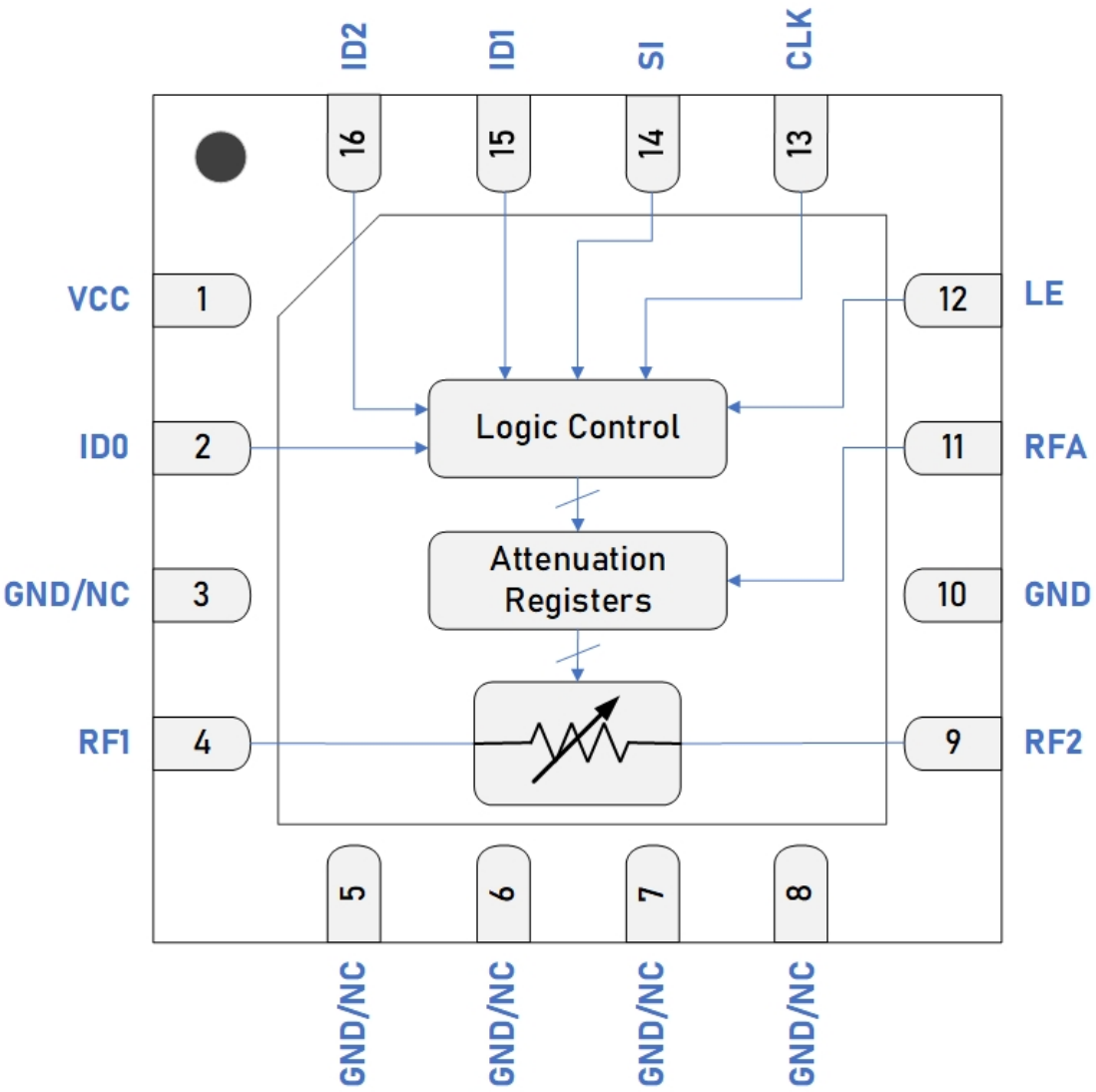
In terms of performance, the GRF6402 can cover the entire 50 MHz to 6 GHz range while still maintaining precise and monotonic gain stepping. Glitching has been minimized to < 2 dB for all steps. The device delivers up to 30.5 dBm of IP0.1 dB, 56.2 dBm of IIP3, and a low IL of less than 1.3 dB at 2 GHz.

BLOCK DIAGRAM



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Pin Out (Top View)

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Pin Assignments

Pin	Name	Description	Note
1	V_{CC}	V_{CC} Bias Voltage	Connect to V_{CC}. Use bypass capacitors as close to the pin as possible.
2	ID0	Chip ID Address Bit 0	External address bit 0. See the programming section for details. If left unconnected, an internal pull-down resistor will force the logic on this pin to LOW.
3, 5-8	GND/NC	Ground/No Connect	No internal connection to die. Although these pins are not connected to the die, they should be grounded with a via as close to the pin as possible.
10	GND	Ground	Internally grounded. This pin must be grounded with a via as close to the pin as possible.
4	RF1	RF Port 1	Internally matched to 50 Ω. An external DC blocking cap must be used if there is voltage present on the RF line. Since the device supports bi-directional operation, the RF1 port can serve as an input or output.
9	RF2	RF Port 2	Internally matched to 50 Ω. An external DC blocking cap must be used if there is voltage present on the RF line. Since the device supports bi-directional operation, the RF2 port can serve as an input or output.
11	RFA	*Rapid Fire* Attenuation Select	Logic control for engaging the "*Rapid Fire* Attenuation" feature. Logic HIGH sets the DSA to the pre-defined RFA attenuation state (which is typically set during the initial SPI programming phase). If a custom attenuation setting is not programmed in, then the RFA setting will default to the full attenuation state (31.75 dB). Logic LOW reverts to the previous attenuation state as defined during the last programming sequence. Refer to the programming section for details.
12	LE	Latch Enable	If left unconnected, logic will default to HIGH due to included weak pull-up on chip. A logic transition from **LOW** to **HIGH** updates the programming register. Serial data should be shifted in to the chip's buffer while LE is low, and latched into the register on LE's rising edge.

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Pin Assignments (Cont.)

Pin	Name	Description	Note
13	CLK	Clock	Serial clock input. If left unconnected, logic will default to a HIGH due to included weak pull-up on chip.
14	SI	Serial Input	Serial data input. If left unconnected, logic will default to a HIGH due to included weak pull-up on chip.
15	ID1	Chip ID Address Bit 1	External address bit 1. See the programming section for details. If left unconnected, an internal weak pull-up resistor will force the logic on this pin to HIGH.
16	ID2	Chip ID Address Bit 2	External address bit 2. See the programming section for details. If left unconnected, an internal weak pull-up resistor of 2000 kΩ will force the logic on this pin to HIGH.
PKG BASE	GND	Ground	Provides DC and RF ground for the amplifier, as well as a thermal heat sink. Recommend multiple 8 mil vias beneath the package for optimal RF and thermal performance. Refer to the evaluation board top layer graphic on the schematic page.

Note: CLK, SI, and LE are designed to include weak pull-ups which set the voltages to approximately 2.5 V. These pin voltages will be easily dominated by logic levels placed on the SPI bus by the SPI master.

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Absolute Ratings

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	V_{CC}	-0.3	6	V
SI, LE, CLK	V_{SPI}	-0.3	6	V
ID0, ID1, ID2, RFA	V_{LOGIC}	-0.3	6	V
Externally Applied DC Voltage to RF1 Pin	V_{RFIN}	-0.3	0.3	V
Externally Applied DC Voltage to RF2 Pin	V_{RFOUT}	-0.3	0.3	V
Short-term Exposure to RF Input Power (RF1 or RF2, Load VSWR = 1:1; Assumes Static State Only; All Attenuation States, V_{CC} = 5V, F_{TEST} ≥ 500 MHz, No Hot Switching, $T_{PKG\ BASE}$ = 25 °C)	$P_{IN\ MAX\ -\ ST}$		32	dBm
Long-term Exposure to RF Input Power (RF1 or RF2, Load VSWR = 1:1; Assumes Static State Only; Max Attenuation State (31.75 dB), V_{CC} = 5.5V, F_{TEST} = 50 MHz, No Hot Switching, $T_{PKG\ BASE}$ = 105 °C)	$P_{IN\ MAX\ -\ LT}$		26.5	dBm
Operating Temperature (Package Base)	$T_{PKG\ BASE}$	-40	115	°C
Maximum Junction Temperature	T_{J-MAX}		125	°C
Electrostatic Discharge				
Charged Device Model	CDM	750		V
Human Body Model	HBM	1		kV
Storage				
Storage Temperature	T_{STG}	-65	150	°C
Moisture Sensitivity Level	MSL		1	-

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Caution! ESD Sensitive Device.

Exceeding Absolute Maximum Rating conditions may cause permanent damage.

Note: For additional information, please refer to Manufacturing Note MN-001 - Packaging and Manufacturing Information.

All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging. For additional information, please refer to the Certificate of RoHS Compliance.

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Recommended Operating Conditions

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Power Supply Voltage	V_{CC}	3	5	5.5	V	
Operating Temperature Range	$T_{PKG\ BASE}$	-40		+115	°C	Measured on Package Heat Sink
RF Frequency Range **(note 1)**	F_{RF}	0.05		6	GHz	
RF Input Power @ $T_{PKG\ BASE}$ < 105 °C (Static States)	P_{IN-MAX}			26	dBm	Static attenuation state; all state changes occur in the absence of any RF power being applied to the device. $T_{PKG\ BASE}$ < 105 °C.
RF Input Power @ $T_{PKG\ BASE}$ < 105 °C. (Hot Switching)				20		Hot switching condition; state changes can occur at any time while RF power is applied to the device. $T_{PKG\ BASE}$ < 105 °C.
RF1 Port Impedance	Z_{RF1}		50		Ω	Single ended
RF2 Port Impedance	Z_{RF2}		50		Ω	Single ended

Note 1: Operation outside of this range is possible, but with degraded performance of some parameters.

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Nominal Operating Parameters - General

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Logic Input Low	V_{IL}	0		0.63	V	
Logic Input High	V_{IH}	1.17		V_{CC}	V	
Logic Current	I_{IL}, I_{IH}		12.5		µA	V_{CC}=5 V, $T_{PKG\ BASE}$=105 °C.
5 V Supply Current	I_{CC-5V}		260		µA	Static operation
3.3 V Supply Current	$I_{CC-3.3V}$		220		µA	Static operation
Serial Clock Speed	f_{CLK}			30	MHz	
LE to First Serial Clock Rising Edge	t_{LS}	10			ns	50% of LE falling edge to 50% of CLK rising edge.
Serial Data Hold Time	t_H	10			ns	50% of CLK rising edge to 50% of data falling edge.
Final Serial Clock Rising Edge to LE	t_{CLS}	10			ns	50% of CLK rising edge to 50% of LE rising edge.
DSA Settling Time	t_{ADJ}		47		ns	Any adjacent step (50% of LE to within 0.1 dB of the final value.)
	$t_{MAX-MIN}$		322		ns	Max to min attenuation (50% of LE to within 0.1 dB of the final value.)
	$t_{MIN-MAX}$		723		ns	Min to max attenuation (50% of LE to within 0.1 dB of the final value.)

Thermal Data

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Thermal Resistance (Infrared Scan)	Θ_{JC}		47.8		°C/W	On standard evaluation board. Max attenuation state.

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Nominal Operating Parameters - General

Thermal Data (Cont.)

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Junction Temperature @ $T_{PKG\ BASE}$ = +115 °C	$T_{J\ @\ 115°C}$		125		°C	V_{CC}=5.5 V, F_{TEST}=50 MHz, Max Attenuation (31.75 dB), P_{IN}=23 dBm, CW.
Junction Temperature @ $T_{PKG\ BASE}$ = +105 °C	$T_{J\ @\ 105°C}$		115		°C	V_{CC}=5.5 V, F_{TEST}=50 MHz, Max Attenuation (31.75 dB), P_{IN}=23 dBm, CW.

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Nominal Operating Parameters - RF

The following conditions apply unless noted otherwise: typical application schematic, V_{CC} = 5 V, 50 Ω system impedance, F_{TEST} = 2.0 GHz, $T_{PKG\ BASE}$ = 25 °C. Evaluation board losses are included within the specifications.

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Attenuation Range	G_{RANGE}		31.75		dB	
Attenuation Resolution	G_{STEP}		0.25		dB	
Over/Undershoot During Step Transition	$G_{OVER/UNDER}$		< 2		dB	Any step
Step Error Between Any Two Adjacent States	DNL		±0.02		dB	0.05 GHz ≤ F_{RF} ≤ 1 GHz
			±0.03			1 GHz ≤ F_{RF} ≤ 2 GHz
			±0.05			2 GHz ≤ F_{RF} ≤ 3 GHz
			±0.07			3 GHz ≤ F_{RF} ≤ 4 GHz
			±0.08			4 GHz ≤ F_{RF} ≤ 5 GHz
			±0.09			5 GHz ≤ F_{RF} ≤ 6 GHz
Absolute Attenuation Error at 0.5 GHz	$INL_{0.5GHz}$		0.07		dB	Atten=6 dB
			0.11			Atten=10 dB
			0.18			Atten=18 dB
			0.24			Atten=24 dB
			0.26			Atten=30 dB
Absolute Attenuation Error at 1 GHz	$INL_{1\ GHz}$		0.05		dB	Atten=6 dB
			0.09			Atten=10 dB
			0.13			Atten=18 dB
			0.17			Atten=24 dB
			0.15			Atten=30 dB
Absolute Attenuation Error at 2 GHz	$INL_{2\ GHz}$		0.03		dB	Atten=6 dB
			0.04			Atten=10 dB
			0.04			Atten=18 dB
			0.02			Atten=24 dB
			-0.03			Atten=30 dB

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Nominal Operating Parameters - RF

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Absolute Attenuation Error at 2.5 GHz	$INL_{2.5\ GHz}$		0.02		dB	Atten=6 dB
			0.01			Atten=10 dB
			-0.05			Atten=18 dB
			-0.12			Atten=24 dB
			-0.27			Atten=30 dB
Absolute Attenuation Error at 3.55 GHz	$INL_{3.55\ GHz}$		0.01		dB	Atten=6 dB
			-0.03			Atten=10 dB
			-0.19			Atten=18 dB
			-0.37			Atten=24 dB
			-0.66			Atten=30 dB
Absolute Attenuation Error at 4.7 GHz	$INL_{4.7\ GHz}$		0.03		dB	Atten=6 dB
			-0.06			Atten=10 dB
			-0.38			Atten=18 dB
			-0.72			Atten=24 dB
			-1.18			Atten=30 dB
Absolute Attenuation Error at 6 GHz	$INL_{6\ GHz}$		-0.08			Atten=6 dB
			-0.27			Atten=10 dB
			-0.84			Atten=18 dB
			-1.39			Atten=24 dB
			-2.13			Atten=30 dB
Relative Phase Between the MIN and MAX Attenuation States	Φ_{Δ}		7		°	F_{RF}=0.5 GHz
			12.5			F_{RF}=1 GHz
			25			F_{RF}=2 GHz
			31			F_{RF}=2.5 GHz
			42			F_{RF}=3.55 GHz
			54			F_{RF}=4.7 GHz
			68			F_{RF}=6 GHz

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Nominal Operating Parameters - RF

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Adjacent Step Phase Deviation at 0.5 GHz	$ASPD_{0.5\ GHz}$		0.13		°	Atten=6 dB
			0.09			Atten=10 dB
			0.11			Atten=18 dB
			0.33			Atten=24 dB
			0.4			Atten=30 dB
Adjacent Step Phase Deviation at 1 GHz	$ASPD_{1\ GHz}$		0.22		°	Atten=6 dB
			0.2			Atten=10 dB
			0.23			Atten=18 dB
			0.53			Atten=24 dB
			0.58			Atten=30 dB
Adjacent Step Phase Deviation at 2 GHz	$ASPD_{2\ GHz}$		0.42		°	Atten=6 dB
			0.45			Atten=10 dB
			0.54			Atten=18 dB
			1.04			Atten=24 dB
			0.89			Atten=30 dB
Adjacent Step Phase Deviation at 2.5 GHz	$ASPD_{2.5\ GHz}$		0.54		°	Atten=6 dB
			0.59			Atten=10 dB
			0.72			Atten=18 dB
			1.29			Atten=24 dB
			1.11			Atten=30 dB
Adjacent Step Phase Deviation at 3.55 GHz	$ASPD_{3.55\ GHz}$		0.84		°	Atten=6 dB
			0.92			Atten=10 dB
			1.1			Atten=18 dB
			1.89			Atten=24 dB
			1.45			Atten=30 dB

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Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Adjacent Step Phase Deviation at 4.7 GHz	$ASPD_{4.7\ GHz}$		1.18		°	Atten=6 dB
			1.31			Atten=10 dB
			1.55			Atten=18 dB
			2.47			Atten=24 dB
			1.89			Atten=30 dB
Adjacent Step Phase Deviation at 6 GHz	$ASPD_{6\ GHz}$		1.55		°	Atten=6 dB
			1.69			Atten=10 dB
			2.04			Atten=18 dB
			3.11			Atten=24 dB
			2.52			Atten=30 dB
Insertion Loss	S21, S12		1.1		dB	F_{RF}=0.5 GHz
			1.15			F_{RF}=1 GHz
			1.3			F_{RF}=2 GHz
			1.35			F_{RF}=2.5 GHz
			1.6			F_{RF}=3.55 GHz
			1.95			F_{RF}=4.7 GHz
			2.55			F_{RF}=6 GHz
Gain Flatness Over any 200 MHz Band	$S21_{FLAT}$		0.06		dB	0.05 GHz ≤ F_{RF} ≤ 2 GHz
			0.06			2 GHz ≤ F_{RF} ≤ 3 GHz
			0.06			3 GHz ≤ F_{RF} ≤ 4 GHz
			0.06			4 GHz ≤ F_{RF} ≤ 5 GHz
			0.06			5 GHz ≤ F_{RF} ≤ 6 GHz
Gain Variation Over Temp	$S21_{TEMP}$		+0.35/-0.25		dB	$T_{PKG\ BASE}$=-40 to 115 °C, Referenced to $T_{PKG\ BASE}$=25 °C

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Nominal Operating Parameters - RF

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
RF Port 1 Return Loss Over all Attenuation Settings	S11		> 24		dB	0.05 GHz ≤ F_{RF} ≤ 2 GHz
			> 25			2 GHz ≤ F_{RF} ≤ 3 GHz
			> 21			3 GHz ≤ F_{RF} ≤ 4 GHz
			> 17			4 GHz ≤ F_{RF} ≤ 5 GHz
			> 15			5 GHz ≤ F_{RF} ≤ 6 GHz
RF Port 2 Return Loss Over All Attenuation Settings	S22		> 22			0.05 GHz ≤ F_{RF} ≤ 2 GHz
			> 22			2 GHz ≤ F_{RF} ≤ 3 GHz
			> 20			3 GHz ≤ F_{RF} ≤ 4 GHz
			> 17			4 GHz ≤ F_{RF} ≤ 5 GHz
			> 15			5 GHz ≤ F_{RF} ≤ 6 GHz
Input 3rd Order Intercept ATTN = 0 dB, Over Frequency **(Note 2)**	IIP3		56.6		dBm	F_{RF}=0.5 GHz
			58			F_{RF}=1 GHz
			56.2			F_{RF}=2 GHz
			59.6			F_{RF}=2.5 GHz
			58.8			F_{RF}=3.55 GHz
			60.1			F_{RF}=4.7 GHz
			62.1			F_{RF}=6 GHz
Input 3rd Order Intercept F_{RF} = 2 GHz, Over Attenuation **(Note 3)**	IIP3		59		dBm	ATTN=0 dB
			56.5			ATTN=15.75 dB
			54			ATTN=31.75 dB
Input 0.1 dB Compression ATTN = 0 dB, Over Frequency	$IP_{0.1dB}$		29.6		dBm	F_{RF}=0.5 GHz
			30.4			F_{RF}=1 GHz
			30.5			F_{RF}=2 GHz
			31.1			F_{RF}=2.5 GHz
			31.3			F_{RF}=3.55 GHz
			31.1			F_{RF}=4.7 GHz
			31.7			F_{RF}=6 GHz

Note 2: 18 dBm P_{OUT} per tone at 2 MHz spacing.
Note 3: 19 dBm P_{IN} per tone at 50 MHz spacing.

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Nominal Operating Parameters - RF

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Input 0.1 dB Compression F_{RF} = 2 GHz, Over Attenuation	$IP_{0.1dB}$		30.2		dBm	ATTN=0 dB
			30.3			ATTN=12 dB
			30.5			ATTN=18 dB
Maximum Non-RF Driven Spurious Over Rated Frequency Range of 50 MHz to 6 GHz **(Note 4)**	$SPUR_{MAX}$		-114		dBm	F_{RF}=50 MHz to 65 MHz
			-120			F_{RF}=65 MHz to 115 MHz
			-125			F_{RF}=115 MHz to 6 GHz

Note 4: Spurious due to on-chip negative voltage generator. Typical fundamental frequency is approximately 10 MHz. Measured at either RF port when externally terminated into 50 Ω.

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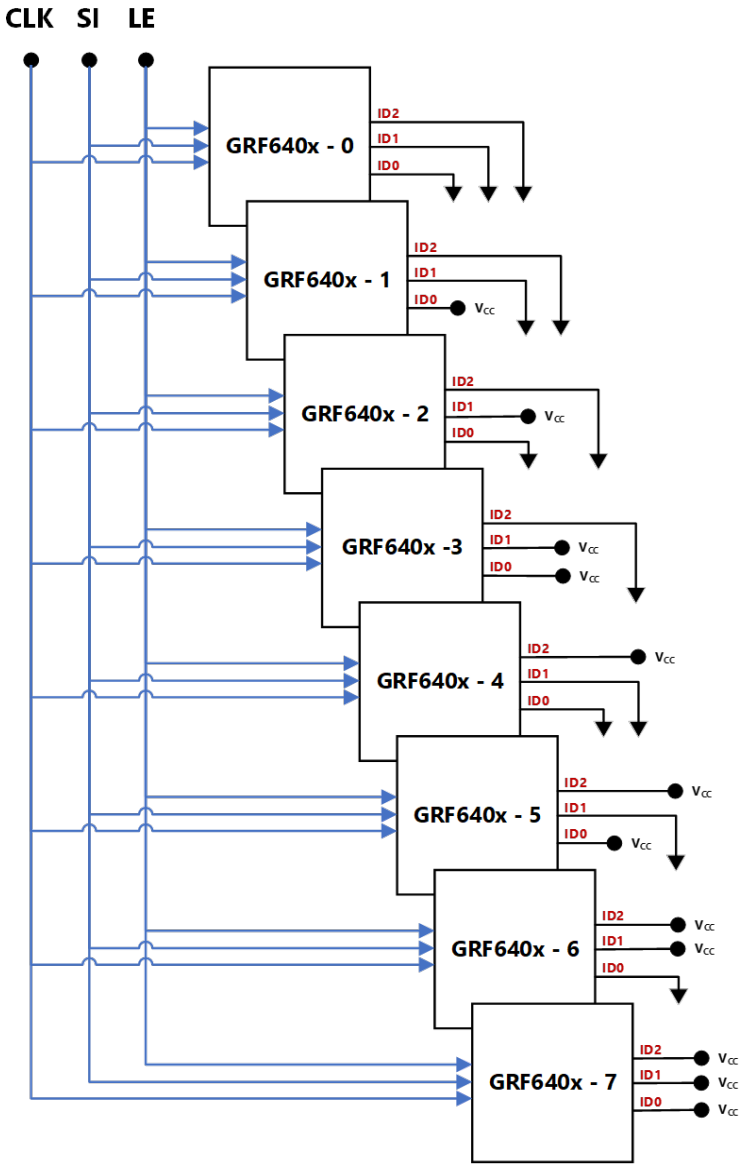
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Functional Description

The GRF6402 employs a number of programming options to control the device's digital step attenuator. The primary programming mode utilizes an enhanced 3-wire SPI (serial-parallel interface) which incorporates multi-device addressing. In addition to supporting traditional serial programming, the GRF6402 also includes a special "*Rapid Fire*" selection pin which allows the device to be immediately switched into a pre-defined attenuation state. The following sections provide specific details on each programming mode. The CLK, SI, and LE pins are designed to include weak pull-ups which set the voltages to approximately 2.5 V. These pin voltages will be easily dominated by logic levels placed on the SPI bus by the SPI master.

Multi-IC Addressing Scheme

The GRF6402 can share a common serial interface line with up to eight similar devices. A unique address is assigned to each component by applying logic to pins ID0 (pin 2), ID1 (pin 15), and ID2 (pin 16). The figure below illustrates such a multi-IC addressing scheme using hardwired logic settings.



Static Chip Address

ID2	ID1	ID0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Multi-IC Addressing Using Hardwired Logic

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As shown, each GRF6402 device shares a common LE control line. The logic present on pins ID0, ID1, and ID2 will be compared with the relevant sub-addressing bits that are delivered as part of the standard 16-bit serial payload. (Refer to the payload figure below for details.) If the addressing in the payload matches the logic on ID0, ID1, and ID2, then the device recognizes the programming within the payload as being relevant and the SPI commands are executed accordingly. If the addresses do not match then the device simply ignores the programming command.

Note that utilizing the multi-IC addressing scheme is completely optional. ***If the application only calls for using a single dedicated LE control line, then it is recommended to simply assign a default address of 000 to the device by connecting ID0, ID1, and ID2 to ground.*** The pins can also be floated (i.e. left in a "no connect" or "NC" state); if pins ID0, ID1, and ID2 are floating, the chip address will default to **110** or decimal **6**.

A summary of the chip identifier mapping is provided in the table below:

Static Address Truth Table

ID2 (PIN 16)	ID1 (Pin 15)	ID0 (Pin 2)	Static Identifier
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
NC[5]	NC[5]	NC[5]	6
1	1	1	7

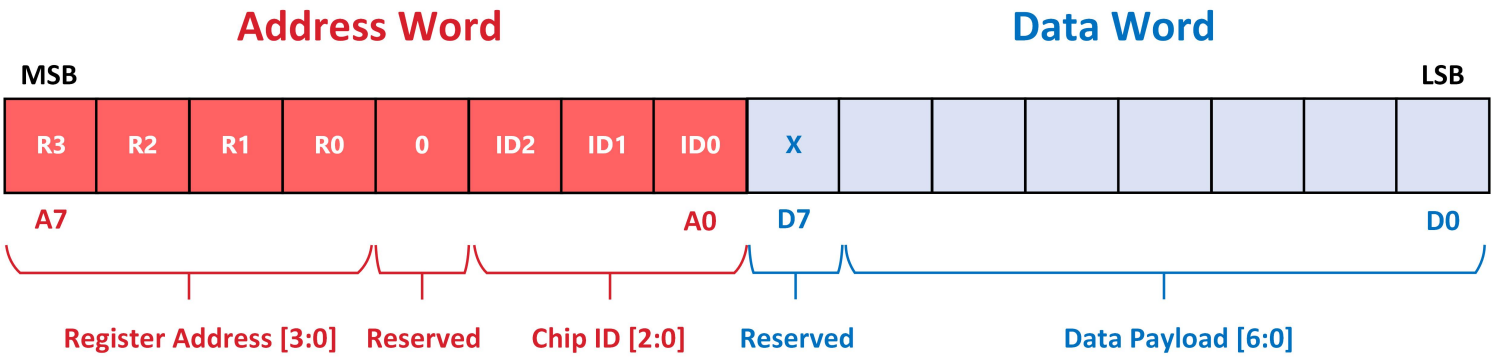
Note 5: If left unconnected, ID2 (Pin 16) and ID1 (Pin 15) will default to a logic HIGH state due to internal pull-ups to 1.8 V. Conversely, ID0 (Pin 2) will default to a logic LOW state due to an internal pull-down to GND. When all three address pins are left unconnected, the resulting address will be 110 (static identifier "6").

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Serial Programming

The GRF6402 utilizes a 16-bit payload to perform its various addressing and programming functions. Information is shifted in with the least significant bit (LSB) first. Refer to the figure below for an overview of the relevant bit assignments:

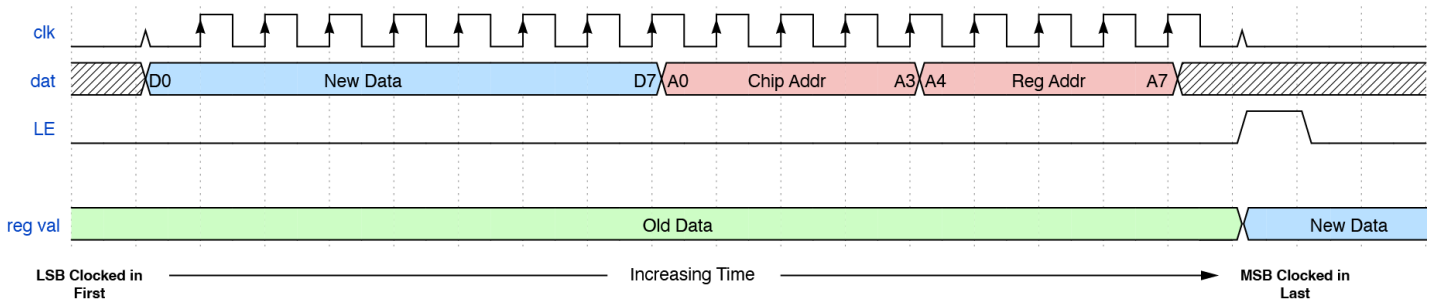


SPI Transaction Payload Diagram

The payload consists of two separate 8-bit words. The data word is clocked in first. ***Bit D7 is reserved; program in a "0" or a "1" for each SPI transaction.*** Bits D6-D0 make up the 7-bit data payload. Note that the data payload will vary depending upon the register being targeted with the write command; *separate 16-bit SPI transactions are therefore required for programming each of the device's three registers.*

The address word is clocked in next. Note that this word includes two separate bit fields. Bits A2-A0 are used to identify the targeted device for each write command, and bits A7-A4 identify the desired register address. ***Bit A3 is reserved, and it must be programmed with a "0" during each SPI transaction.***

The figure below depicts the timing associated with each programming sequence. The GRF6402 is designed to be operated as a MODE 0 SPI device, with the CLK idle state defined as a logic LOW, and with data sampled on the RISING EDGE of the CLK as depicted below.



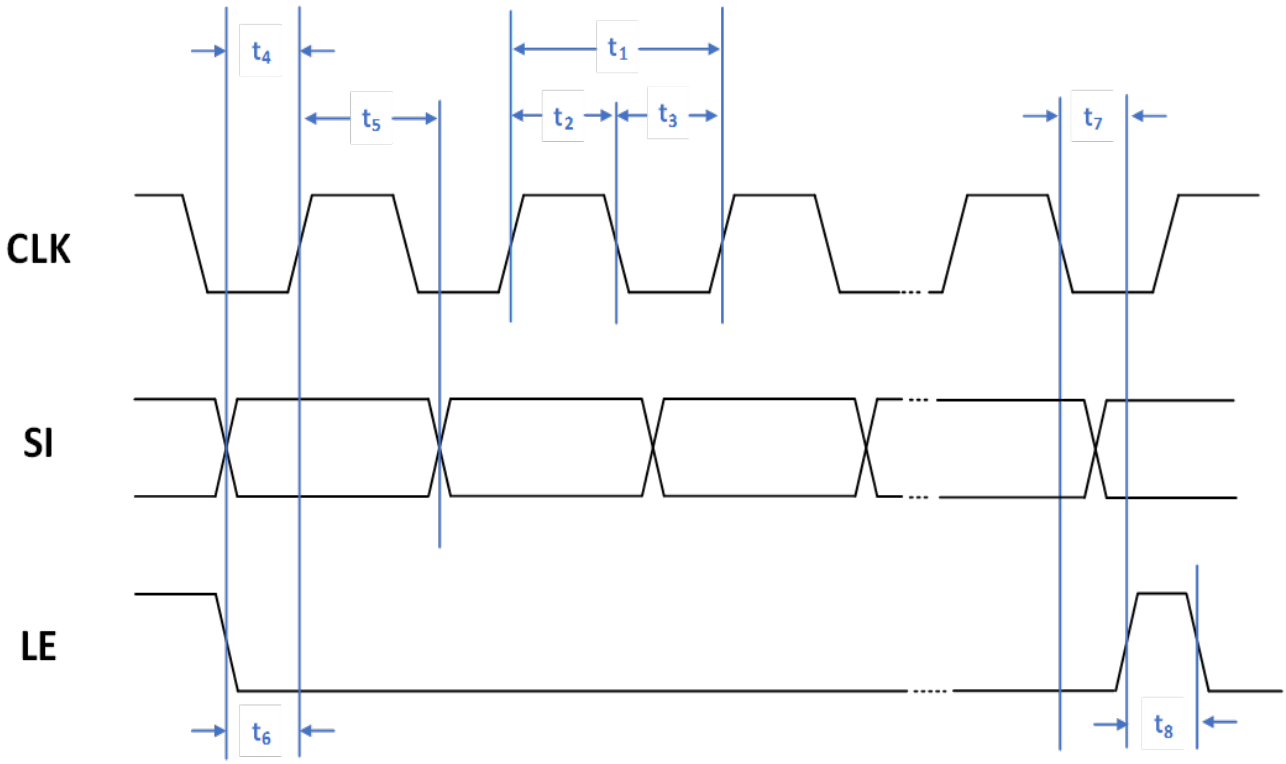
16-Bit SPI Programming Sequence

The sequence begins with the latch enable (LE) line set to logic LOW. After clocking in all 16 bits of the SPI payload, an LE line transition to HIGH will trigger a comparison between bits A3-A0 (the chip ID) with the logic seen on pins ID2, ID1, and ID0. If the two addresses match, then the device will proceed with latching bits D7-D0 into the addressed register. ***This latching process occurs on LE's rising edge.*** If the chip ID bit field does not match the logic on pins ID2, ID1, and ID0, then the transaction is ignored.

Note that if the LE line is left in a HIGH state, then data will be immediately passed on from the buffer to the targeted register provided there is still a match between bits A3-A0 (the chip ID) and the logic present on pins ID2, ID1 and ID0. Conversely, if the LE line is left in a LOW state, then any data being clocked into the chip's buffer will be ignored (i.e. remain unlatched) until the LE line is brought back to HIGH. When writing to the GRF6402, it is therefore recommended that the 16-bit transaction be shifted in while the LE line is held LOW.

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SPI Timing Intervals



SPI Timing Diagram

This drawing is only intended to convey the relative timing relationships between the CLK, SI, and LE signals.

The 16-Bit SPI Programming Sequence drawing should be followed as the reference for programming the DSA.

SPI Timing Specifications

Parameter	Symbol	Specification			Unit	Condition
		Min.	Typ.	Max.		
Serial Clock (CLK) Speed	f_{CLK}			30	MHz	
CLK Period	t_1	33.3			ns	
CLK High Duration Time	t_2	16.7			ns	
CLK Low Duration Time	t_3	16.7			ns	
SI to CLK Setup Time	t_4	10			ns	
SI Hold Time	t_5	10			ns	
LE Low Setup Time	t_6	10			ns	
LE High Setup Time	t_7	10			ns	
LE High Time	t_8	10			ns	

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Register Mapping

The GRF6402 includes 3 separate 8-bit registers which help to facilitate the device's various programming functions. The first, **ATTEN**, is used to set the device's attenuation state when operated in its normal serial mode. Upon all power-on resets (PORs), the register defaults to [01111111], meaning that the attenuator will be set to its maximum attenuation state.

The **CONFIG** register is used to activate the RFA feature. Upon PORs, all bits within the register will default to 0s, thus placing the RFA feature in a disabled state. If the user decides to employ the RFA option, then the [1] bit field must be set to 1 with a separate SPI transaction.

The third register, **RFAREG**, is tied to the GRF6402's *Rapid Fire* Attenuation feature. As with the ATTEN register, the RFAREG will default to its maximum attenuation state for all POR conditions. Subsequent SPI programming transactions allow the user to set this register to any customized state between 0 and 31.75 dB. The bit assignments within this particular register get passed along to the attenuator core whenever the RFA feature is enabled **and** the external RFA pin (pin 11) goes HIGH.

The remaining registers are unused, and they should NOT be written to with any SPI transactions.

Detailed Register Map

Register Address	Name	Width	Description	Bit Fields	POR Value
0x0	ATTEN	8 bits	Attenuator state when in serial mode.	**[6:0]:** DSA Attenuation Word [1111111] = Max Atten [1000000] = Half Max Atten [0000000] = Min Atten **[7]:** *Unused; set to either 0 or 1*	[01111111]
0x1	CONFIG	8 bits	Stores configuration settings	**[0]:** *Rapid Fire Pointer Flag* **0** = RFA attenuation is set from RFAREG **[1]:** *Rapid Fire Feature On/Off Selection* **0** = RFA Disabled **1** = RFA Enabled **[7:2]:** *Unused; set to either 0 or 1*	[00000000]
0x2	RFAREG	8 bits	Stored value for Rapid-Fire mode attenuation	**[6:0]:** RFA (Rapid Fire Attenuation) Word [111111] = Max Atten [100000] = Half Max Atten [000000] = Min Atten **[7]:** *Unused; set to either 0 or 1*	[01111111]
0x3-0xF	Unused	8 bits	Do not write to these registers		[00000000]

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Register Truth Tables

The following truth tables pertain to the attenuator words as used within the ATTEN and RFAREG registers.

7-bit SPI Word Bit Assignments

Data Bit	Attenuation Control
D7	Not Used
D6	16 dB Attenuator Control
D5	8 dB Attenuator Control
D4	4 dB Attenuator Control
D3	2 dB Attenuator Control
D2	1 dB Attenuator Control
D1	0.5 dB Attenuator Control
D0	0.25 dB Attenuator Control

Serial Control Word Abbreviated Truth Table

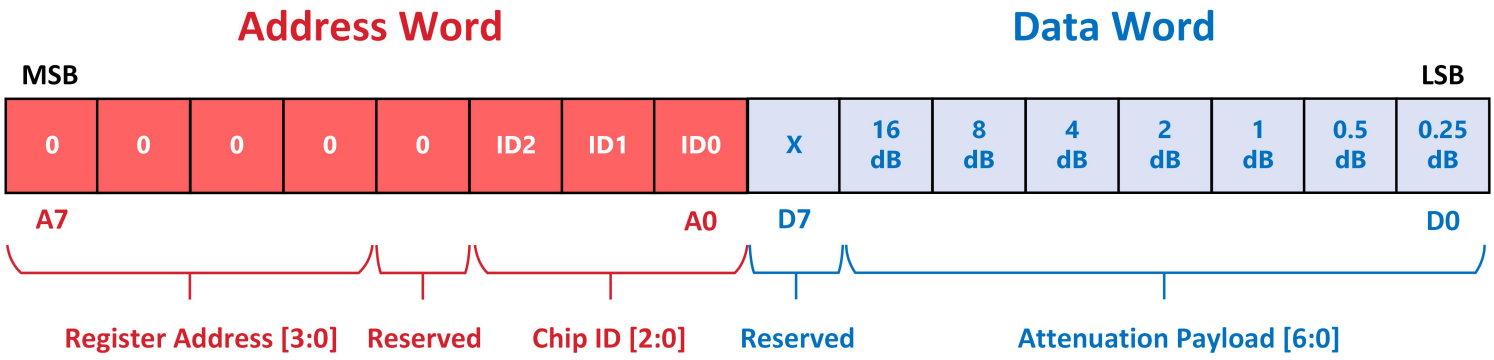
Attenuation	D7	D6	D5	D4	D3	D2	D1	D0
0 dB	X	0	0	0	0	0	0	0
0.25 dB	X	0	0	0	0	0	0	1
0.5 dB	X	0	0	0	0	0	1	0
1 dB	X	0	0	0	0	1	0	0
2 dB	X	0	0	0	1	0	0	0
4 dB	X	0	0	1	0	0	0	0
8 dB	X	0	1	0	0	0	0	0
16 dB	X	1	0	0	0	0	0	0
31.75 dB	X	1	1	1	1	1	1	1

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Basic DSA Serial Programming

Upon power-on / reset (POR), the GRF6402 will default to an attenuation setting of 31.75 dB. A simple SPI command can then be executed to change this attenuation setting by writing directly to the device's ATTEN register (0x0). Be sure to include the relevant Chip ID addressing bits, as well as the placeholder bits noted in the diagram below for bits A3 and D7. Apply the relevant attenuation bits within the data word per the truth tables provided above.

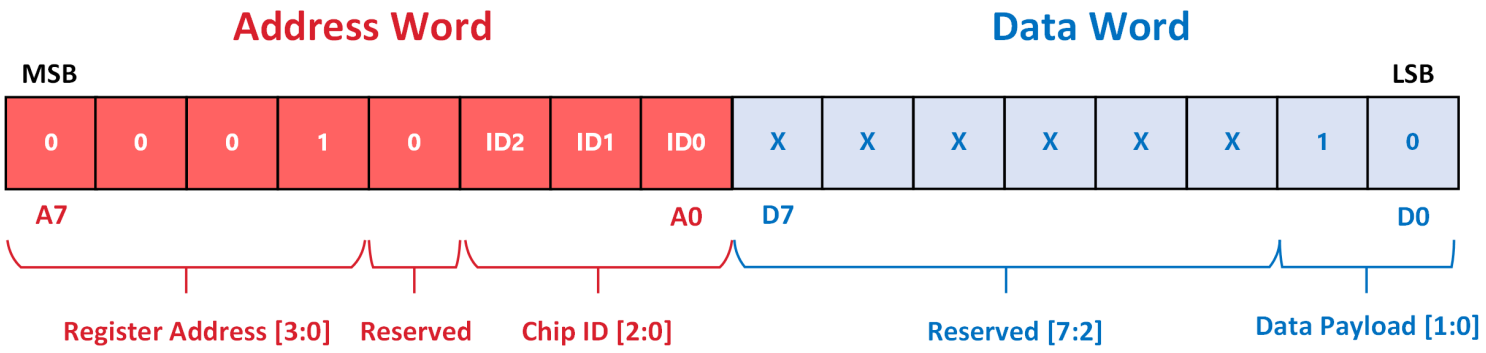


SPI Payload for Basic DSA Programming

Rapid Fire™ Attenuation (RFA) Feature

The RFA feature enables the user to quickly switch the attenuator into a pre-defined state, thus circumventing the delays commonly associated with serial programming. A single control line allows the user to rapidly toggle between two attenuation states. In essence, the RFA feature provides a hybrid control mechanism that combines the speed of parallel programming with the convenience of a single control line. This form of control is useful for a multitude of applications where fast switching is critical for protecting downstream stages from overexposure to excessively large RF signals. This ability to quickly shift into a secondary state also allows a single device to be used in TDD applications where different attenuation levels are needed for RX and TX applications.

To use the GRF6402's RFA feature, a one-time SPI command must first be sent to the device to activate the feature set. (Note that any subsequent PORs will also require the user to re-activate the RFA feature; PORs force the CONFIG register to revert to its default setting, and the RFA is deactivated as part of this default).



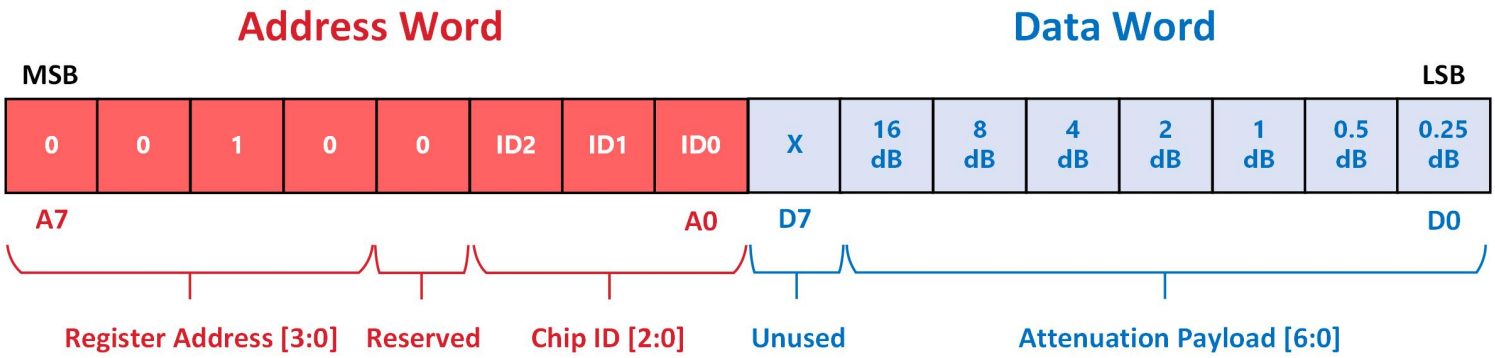
SPI Payload for Activating the RFA Feature

Be sure to include the relevant Chip ID addressing bits, as well as the placeholder bits noted in the diagram for bit A3 and D7. D1 is set to "1" to activate the RFA feature. **Note that D0 must also be set to "0" as part of this activation process.** Setting D0 to "0" instructs the device to pull the attenuation setting directly from the RFAREG whenever the RFA pin is pulled HIGH.

To deactivate the RFA feature, simply perform an identical SPI transaction, but set D1 to "0" instead.

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To customize the amount of attenuation being "fired in," an additional SPI command must also be sent to change the RFA level from its default of 31.75 dB. Simply perform a separate SPI transaction to write a new, customized attenuation level to the RFAREG register:



SPI Payload for Customizing the RFA's Attenuation Setting

As mentioned earlier, be sure to include the relevant Chip ID addressing bits, as well as the placeholder bits noted in the diagram for bits A3 and D7. Apply the relevant attenuation bits within the data word per the truth tables provided above.

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Using the GRF640X DSA Control GUI

Requirements

Windows PC with the following:

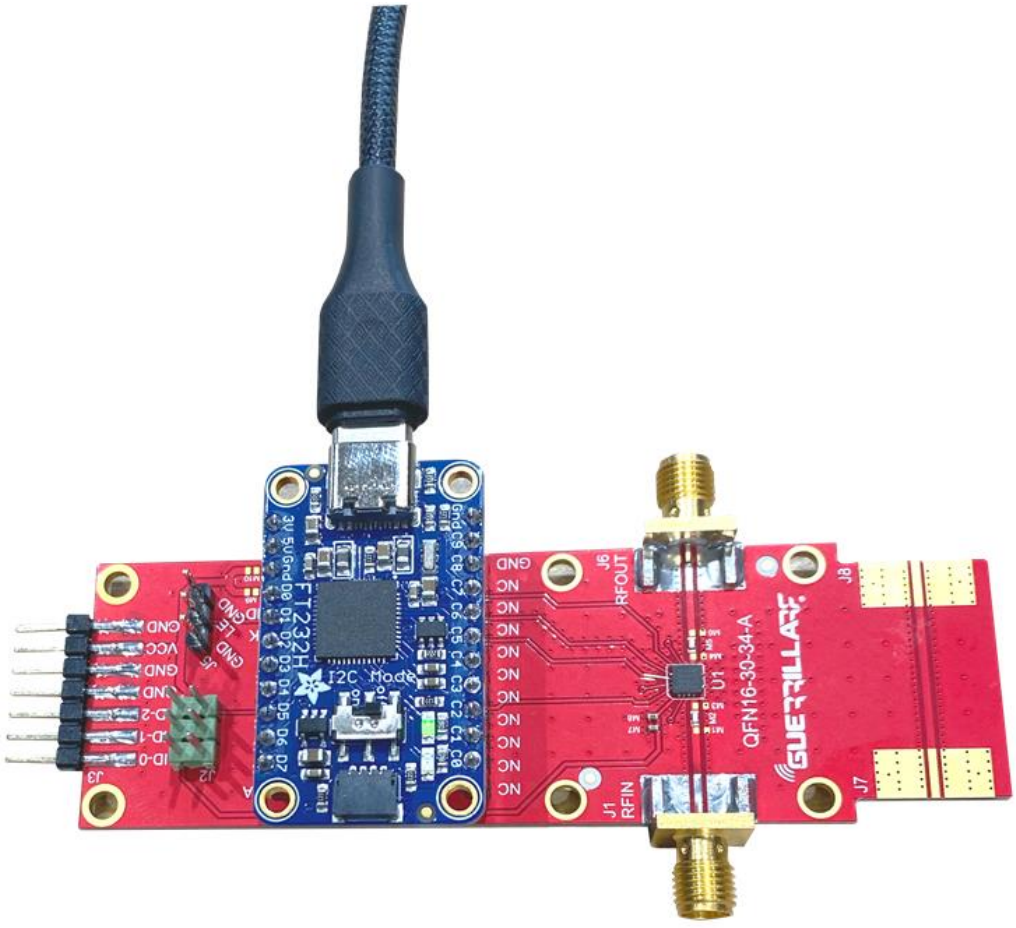
- Windows 10 (or newer) operating system. (Note: the GUI will not run on Mac OS or Linux machines.)
- USB-C capability (either native or via a USB-A to USB-C adapter)

GRF Control GUI

- Executable GUI Application File (.exe)
- GUI can be downloaded directly from the GRF6402 product page. Click here to access the page within Guerrilla RF's website.

Overview

The GRF6402 evaluation board is designed to work in conjunction with the *Adafruit FT232H USB-C to GPIO, SPI, and I2C Controller*. This separate breakout board attaches directly to the GRF6402's QFN16-30-34-A evaluation board as shown below. After downloading the GRF DSA control software, any USB-C equipped PC running Windows 10 (or newer) can be used to activate the control panel GUI. Please note that more in-depth programming details can be found in the "Detailed Register Map" section of this datasheet.



The evaluation board is connected to an Adafruit breakout board that uses a USB-C port.

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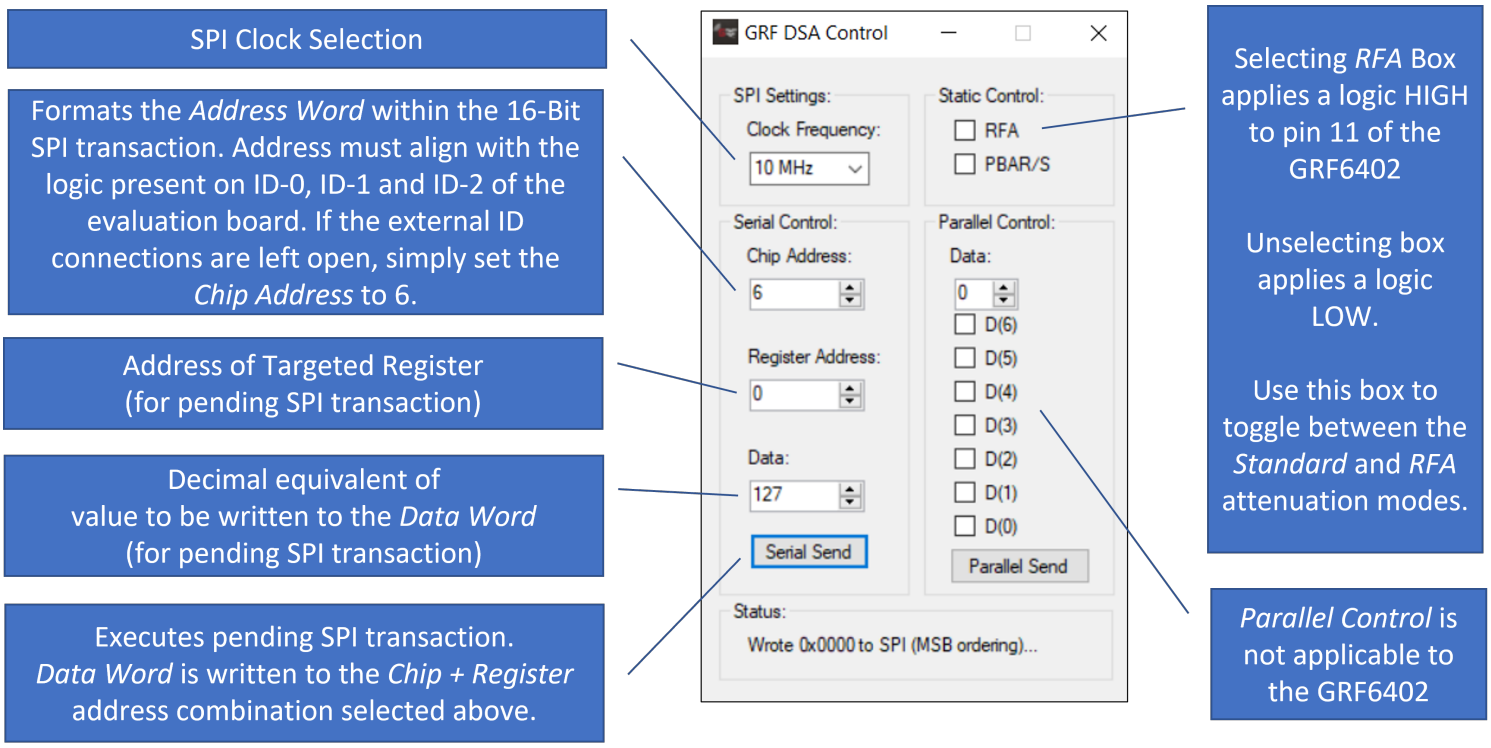
Getting Started

After downloading the GUI control application onto your PC, simply follow the steps below to initiate communication between your PC and the GRF6402 evaluation board.

1. Connect the Adafruit controller to your computer via any USB-C connection. The appropriate drivers for the controller should load automatically for PCs running Windows 10 or 11.
2. To activate the "GRF6402 GRF DSA Control" GUI, launch the executable called "grf_dsa_gui.exe."

Note: Since the GUI is an executable file, your PC's security software may prevent you from simply downloading and running the application without some form of override or intervention. Review the instructions associated with your preferred security software to allow the executable to launch.

Once launched, the GUI application will reveal the control panel shown below.



The DSA Control Panel

Selectable Control Options

SPI SETTINGS

Clock Frequency

- Use the pull-down menu to select from a set of pre-determined frequencies ranging from 1 MHz to 30 MHz.

SERIAL CONTROL

Chip Address

- This entry automatically formats the three address bits (A0-A2) used within the 16-bit SPI transaction.
- Select from *one of the 8* possible addresses supported by the GRF6402.
- The selected address must align with the logic being assigned to the ID-0, ID-1 and ID-2 control pins on the evaluation board's J3 header.
- If external logic is not provided via the J3 header, then the GRF6402 will have a default address of "**6**." [As noted in the datasheet's "Static Address Truth Table," internal pull-ups/pull-downs on the device's three address pins (A0-A3) will force the address logic on these pins to state 110 (i.e. address 6) when the pins are left unconnected.]

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Register Address

- This entry selects the targeted register to be written to with the pending SPI transaction.
- Select from one of 3 possible addresses.
  - Address 0: ATTEN register
  - Address 1: CONFIG register
  - Address 2: RFAREG register

Data

- Use this entry to program bits D0-D7 (the data word) for the pending SPI transaction.
- Select from one of 128 possible word combinations.
  - 0 = x0000000
  - 127 = x1111111

Serial Send

- Click on the "Serial Send" button when ready to execute the SPI transaction.
- All data present within the "Chip Address," "Register Address" and "Data" fields will be formatted and sent to the GRF6402 via a 16-bit word.

STATIC CONTROL

- Use the "Static Control" boxes to select the logic on the RFA (applicable for the GRF6402) and PBAR/S (applicable for the GRF6403) pins.
- Note: *Rapid Fire* feature must be first enabled within the CONFIG register in order for the RFA functionality to respond to these commands.
- RFA Logic Assignments *(**GRF6402 Only**)*
  - RFA box checked: Logic HIGH assigned to pin 11 [RFA attenuation (from Register 2) Switched In]
  - RFA box unchecked: Logic LOW assigned to pin 11 [Primary Attenuation (from Register 0) Switched In]
- PBAR/S Logic Assignments *(**GRF6403 Only**)*
  - This static control box is only applicable to the GRF6403; selecting/unselecting the box has no impact on the GRF6402
  - PBARS/S box checked: Logic HIGH assigned to pin 3 on the GRF6403
  - PBARS/S box unchecked: Logic LOW assigned to pin 3 on the GRF6403

PARALLEL CONTROL (Applicable to the *GRF6403 Only*)

Data

- Use this entry to program in the external logic for bits D0-D6 (pins 1, 24, 23, 22, 21, 20 and 19) on the GRF6403
- Select from one of 128 possible word combinations.
  - 0 = x0000000
  - 127 = x1111111

Parallel Send

- Click on the "Parallel Send" button when ready to apply the parallel logic to pins 1, 24, 23, 22, 21, 20 and 19 on the GRF6403

Changing the Attenuation Level within the ATTEN Register

1. To make any changes via the GUI, be sure that the "Chip Address" matches up with the logic being applied to the ID-0, ID-1 and ID-2 connections on the evaluation board. If these connections have been left "Open," then be sure to set the chip address to "6."

2. Set the "Register Address" to "0" to select the "ATTEN" register.

3. Select the desired attenuation step within the data field. Since the GRF640x series are 7-bit devices, there are 128 discrete 0.25 dB steps. Selecting a "0" in the data field places the DSA in its MINIMUM attenuation state. Conversely, selecting 127 will activate all of the attenuation cells, resulting in a MAXIMUM attenuation state of 31.75 dB. Use the following equation to select the desired attenuation state:

   ATTEN State (decimal) = [ATTEN State (dB)] / 0.25

4. The "Static Control" and "Parallel Control" fields can be ignored when simply programming the primary ATTEN DSA register.

5. Click on the "Serial Send" button to execute the SPI transaction. Assuming the RFA bit is set to "0" (i.e. the RFA static control box is left unchecked), the DSA will load in the new attenuation value as soon as the SPI transaction is completed.

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Utilizing the *Rapid Fire™* Feature Via the GUI

The control panel can be used to switch between the two attenuation states (standard and *Rapid Fire*) by simply using the RFA checkbox in the "Static Control" field. However, in order to use the RFA feature, the *Rapid Fire* option must first be activated within the CONFIG register.

Enabling the *Rapid Fire* Feature on the GRF6402

1. Make sure that the "Chip Address" entry is set to the proper address per the instructions above.
2. Set the "Register Address" to 1 to select the CONFIG register.
3. Set the "Data" field to 2.
4. Hit the "Serial Send" button. Doing so will write a "10" to data bits D0-D1 within the CONFIG register.

Setting the *Rapid Fire* Attenuation State

Upon PORs (Power on Resets), the RFAREG (*Rapid Fire* register) will automatically be set to represent a full attenuation state of 31.75 dB. To override this default attenuation state, simply reprogram the values in RFAREG with the followings steps:

1. Make sure that the "Chip Address" entry is set to the proper address per the instructions above.
2. Set the "Register Address" to 2 to select the RFAREG register.
3. Select the desired attenuation step within the data field. As with the ATTEN register, there are 128 discrete 0.25 dB steps that can be chosen. Selecting a "0" in the data field places the DSA in its MINIMUM attenuation state. Conversely, selecting 127 will activate all of the attenuation cells, resulting in a MAXIMUM attenuation state of 31.75 dB. Use the following equation to select the desired attenuation state:

   RFA ATTEN state (decimal) = [RFA ATTEN State (dB)] / 0.25

4. Hit the "Serial Send" button.

Toggling Between the Standard and *Rapid Fire* Attenuation States

Once the *Rapid Fire* feature has been enabled within the CONFIG register, simply apply a checkmark to the RFA box within the Static Control Field.

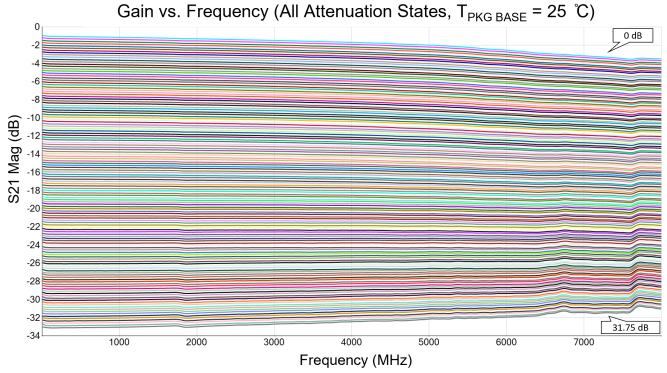
- RFA box checked: Logic HIGH assigned to pin 11 [RFA Attenuation (from Register 2) Switched In]
- RFA box unchecked: Logic LOW assigned to pin 11 [Primary Attenuation (from Register 0) Switched In]

Please note that more in-depth programming details can be found in the "Detailed Register Map" section of this datasheet.

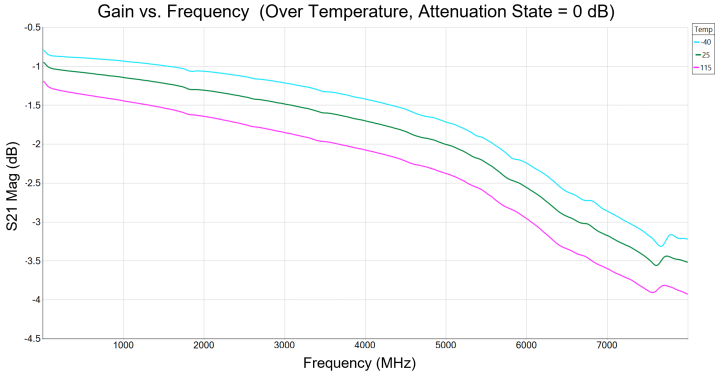
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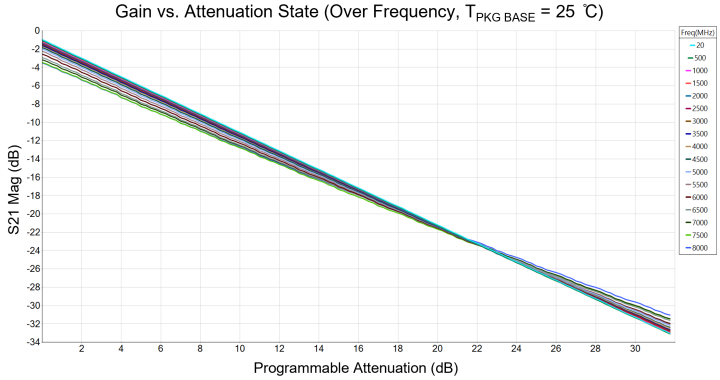
Gain vs. Frequency (All Attenuation States, $T_{PKG\ BASE}$ = 25 ℃)



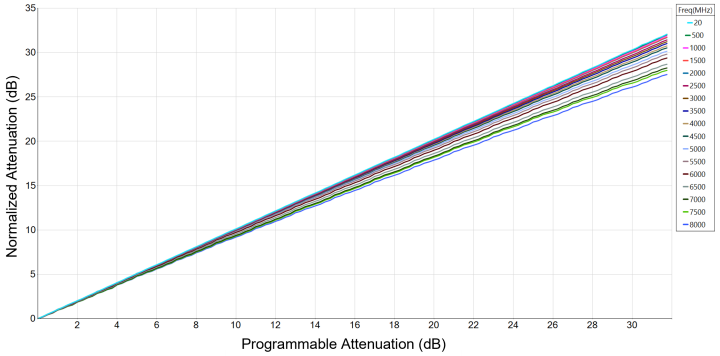
Gain vs. Frequency (Over Temperature, Attenuation State = 0 dB)



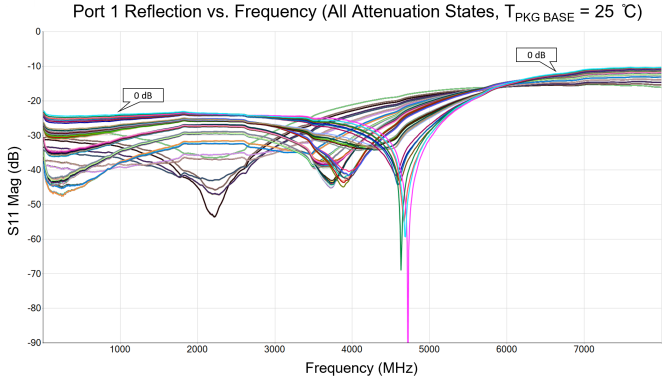
Gain vs. Attenuation State (Over Frequency, $T_{PKG\ BASE}$ = 25 ℃)



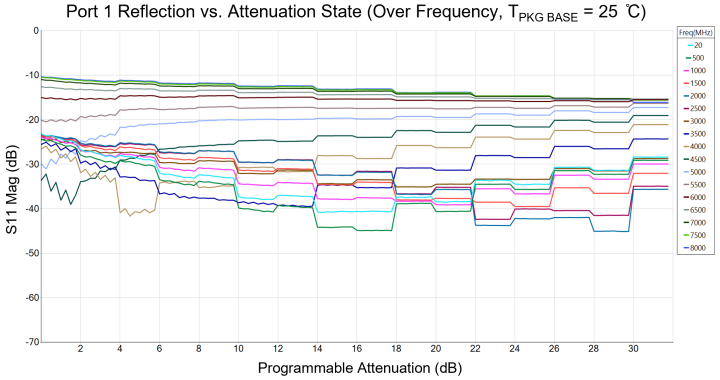
Normalized Attenuation vs. Attenuation State (Over Frequency, $T_{PKG\ BASE}$ = 25 ℃)



Port 1 Reflection vs. Frequency (All Attenuation States, $T_{PKG\ BASE}$ = 25 ℃)



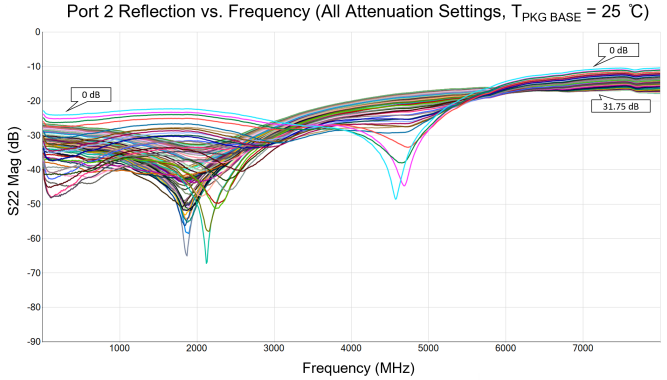
Port 1 Reflection vs. Attenuation State (Over Frequency, $T_{PKG\ BASE}$ = 25 ℃)



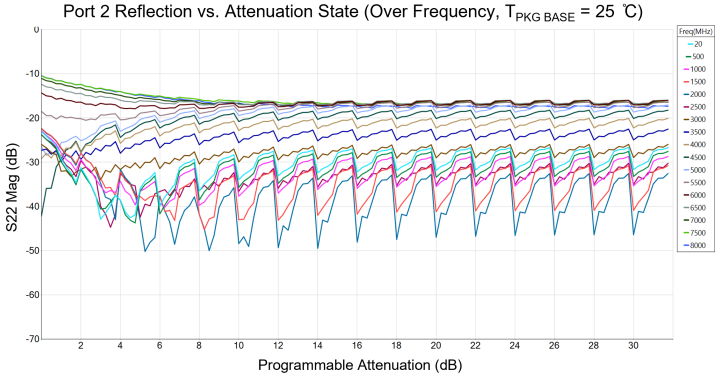
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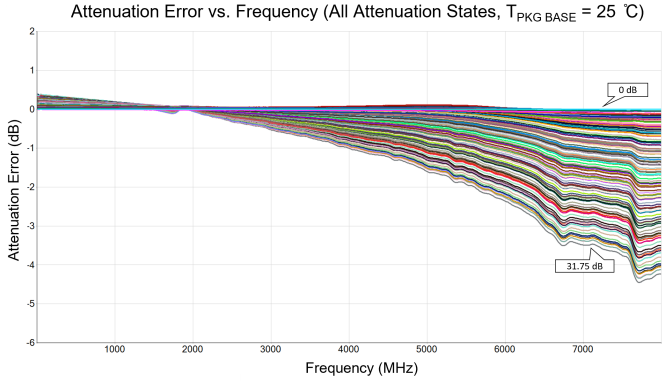
Port 2 Reflection vs. Frequency (All Attenuation Settings, $T_{PKG\ BASE}$ = 25 ℃)



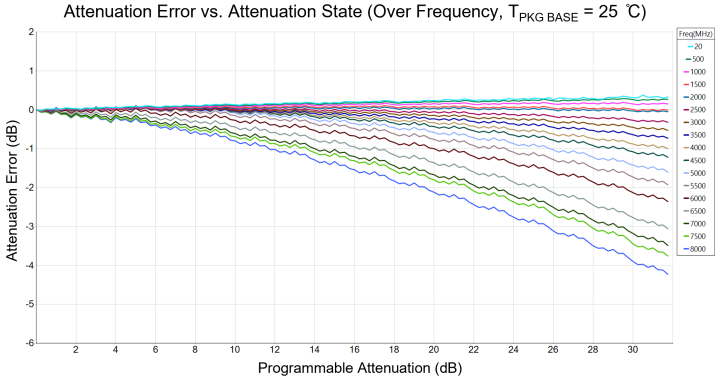
Port 2 Reflection vs. Attenuation State (Over Frequency, $T_{PKG\ BASE}$ = 25 ℃)



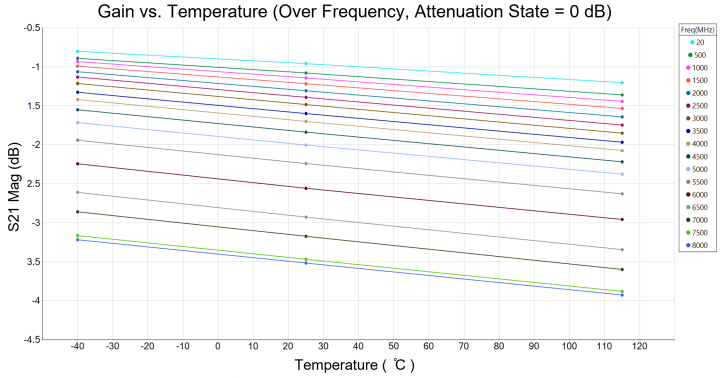
Attenuation Error vs. Frequency (All Attenuation States, $T_{PKG\ BASE}$ = 25 ℃)



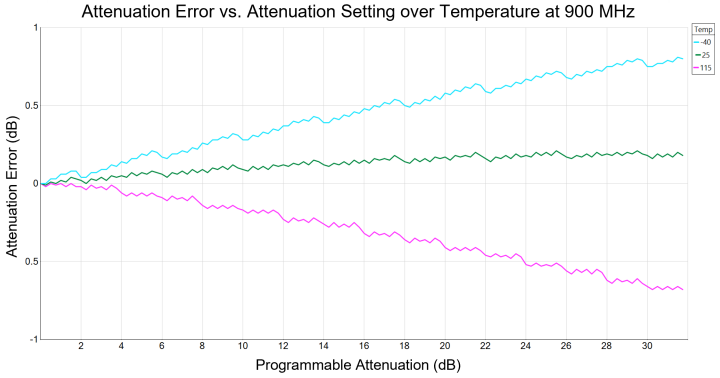
Attenuation Error vs. Attenuation State (Over Frequency, $T_{PKG\ BASE}$ = 25 ℃)



Gain vs. Temperature (Over Frequency, Attenuation State = 0 dB)

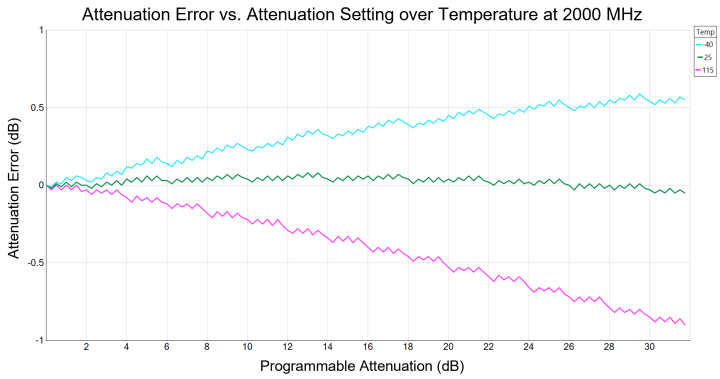


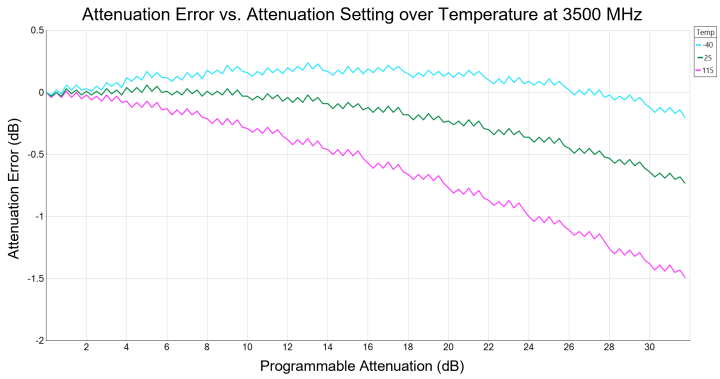
Attenuation Error vs. Attenuation Setting over Temperature at 900 MHz

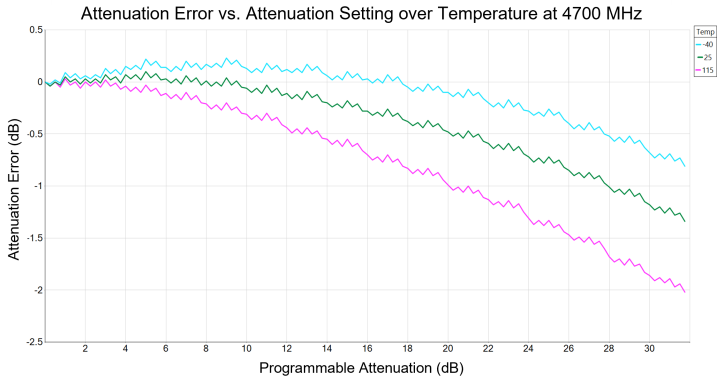


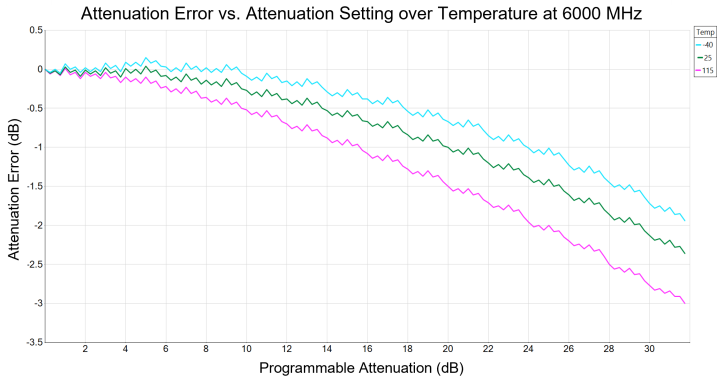
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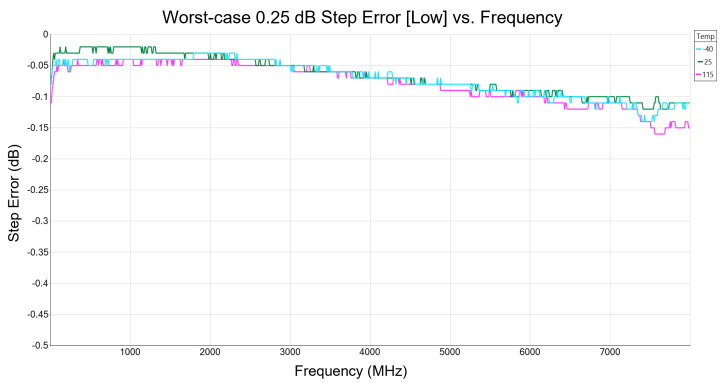
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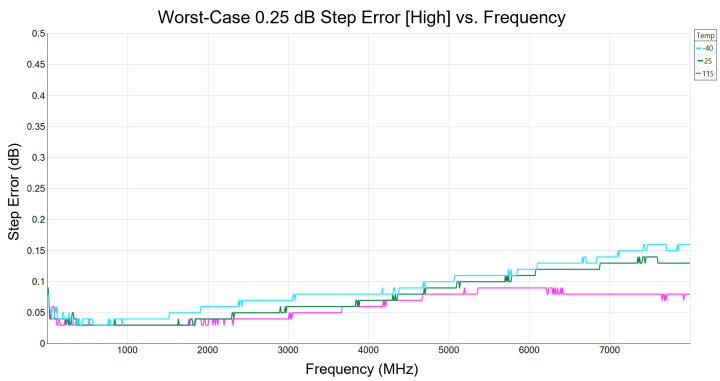








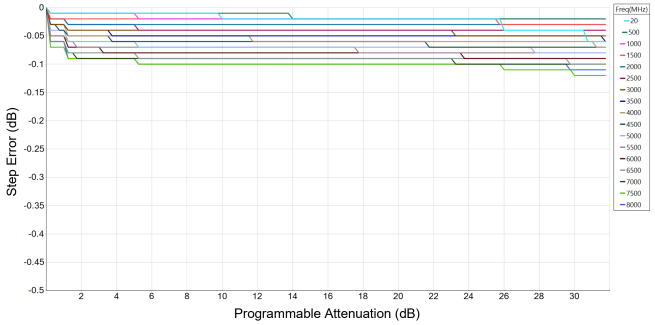




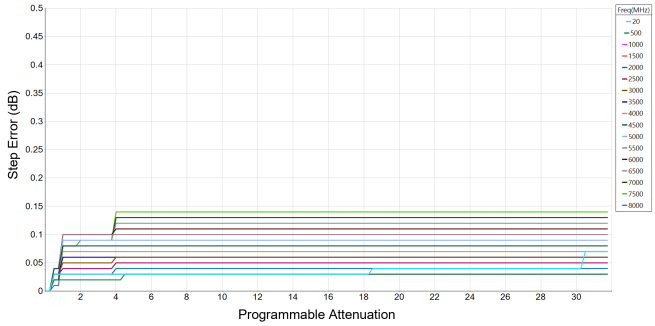
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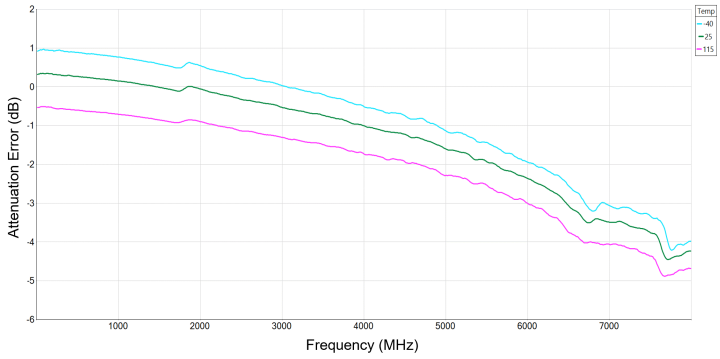
Worst-case 0.25 dB Step Error [Low] vs. Attenuation State (Over Frequency, $T_{PKG\ BASE}$ = 25 ℃)



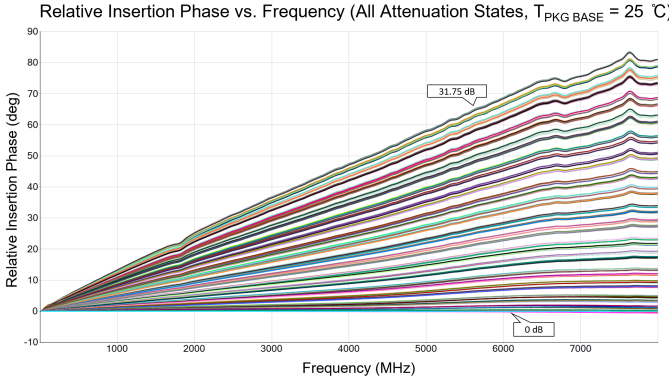
Worst-Case 0.25 dB Step Error [High] vs. Attenuation State (Over Frequency, $T_{PKG\ BASE}$ = 25 ℃)



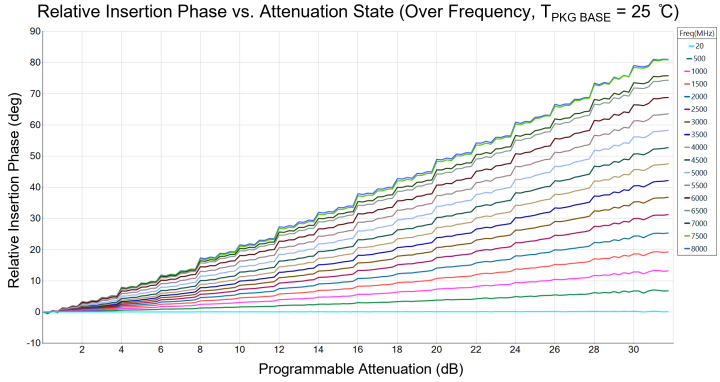
Worst-case Absolute Error vs. Frequency (Over Temperature)



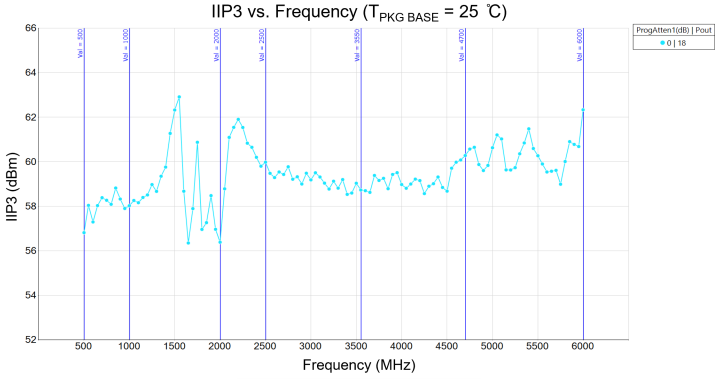
Relative Insertion Phase vs. Frequency (All Attenuation States, $T_{PKG\ BASE}$ = 25 ℃)



Relative Insertion Phase vs. Attenuation State (Over Frequency, $T_{PKG\ BASE}$ = 25 ℃)



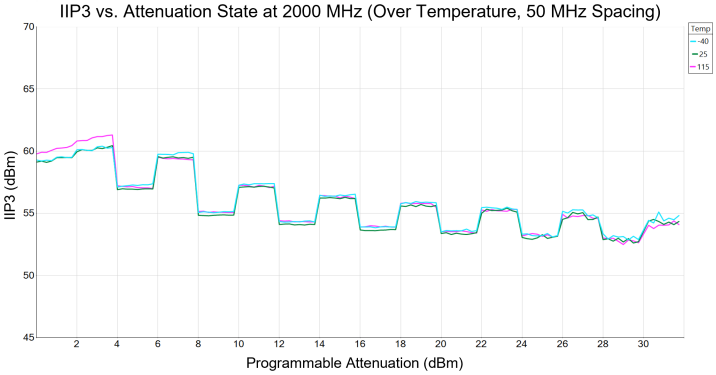
IIP3 vs. Frequency ($T_{PKG\ BASE}$ = 25 ℃)



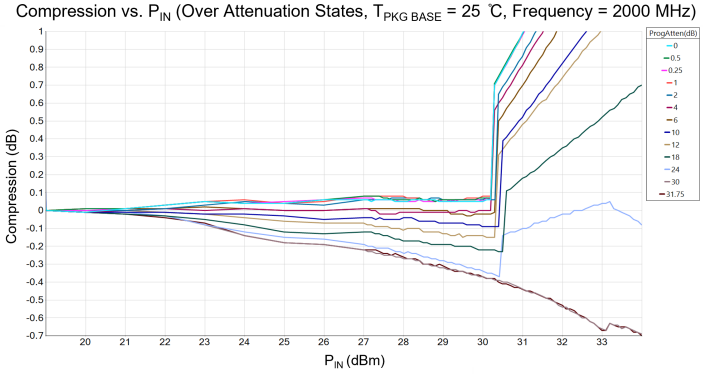
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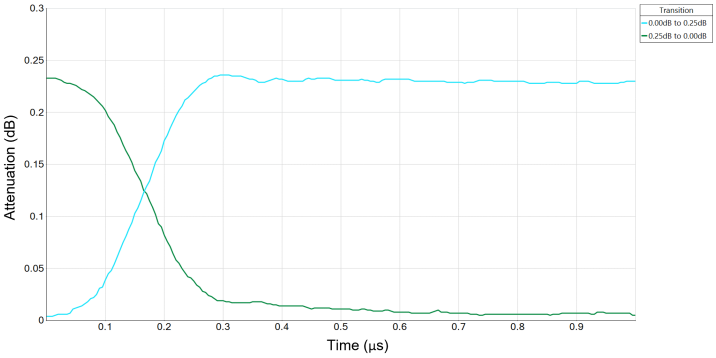
IIP3 vs. Attenuation State at 2000 MHz (Over Temperature, 50 MHz Spacing)



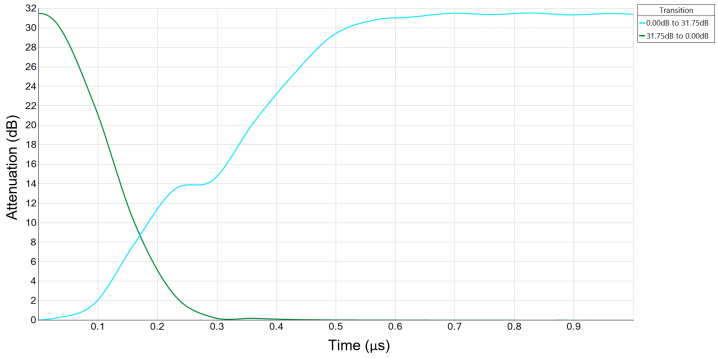
Compression vs. P_{IN} (Over Attenuation States, $T_{PKG\ BASE}$ = 25 ℃, Frequency = 2000 MHz)



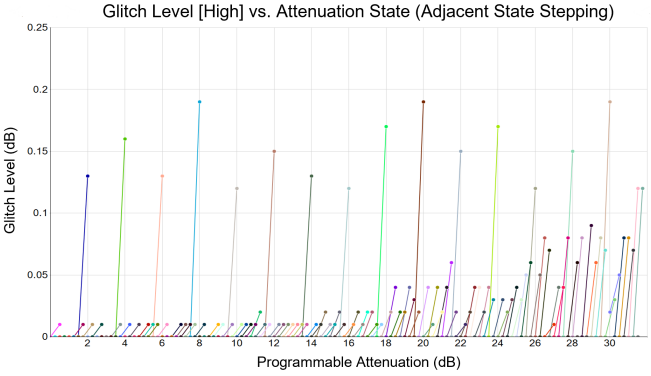
Typical Switching Time – 0.25 dB Steps



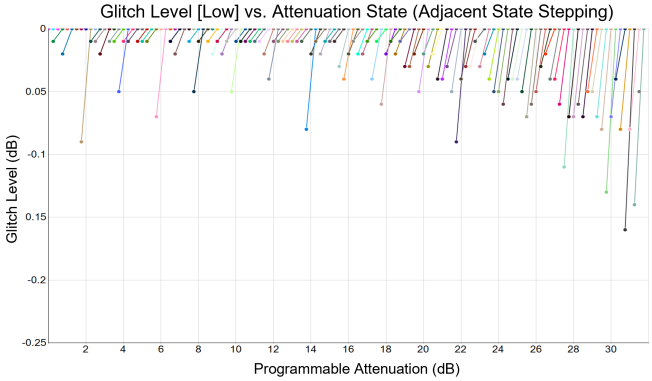
Typical Switching Time – Full Range Steps



Glitch Level [High] vs. Attenuation State (Adjacent State Stepping)



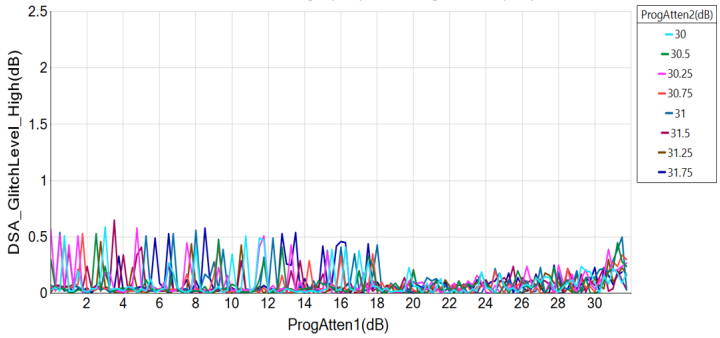
Glitch Level [Low] vs. Attenuation State (Adjacent State Stepping)



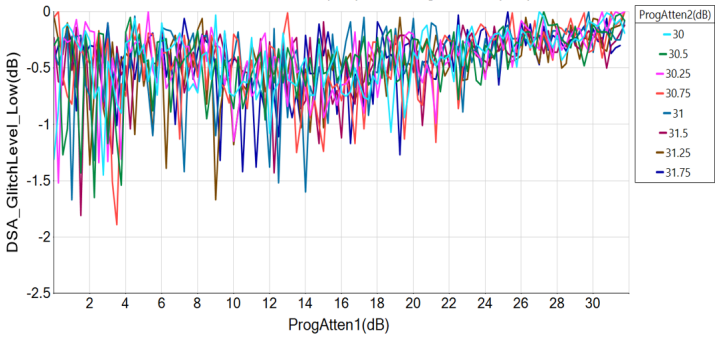
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GRF6402 DSA_GlitchLevel_High(dB) vs ProgAtten1(dB) at Pin = 15 dBm

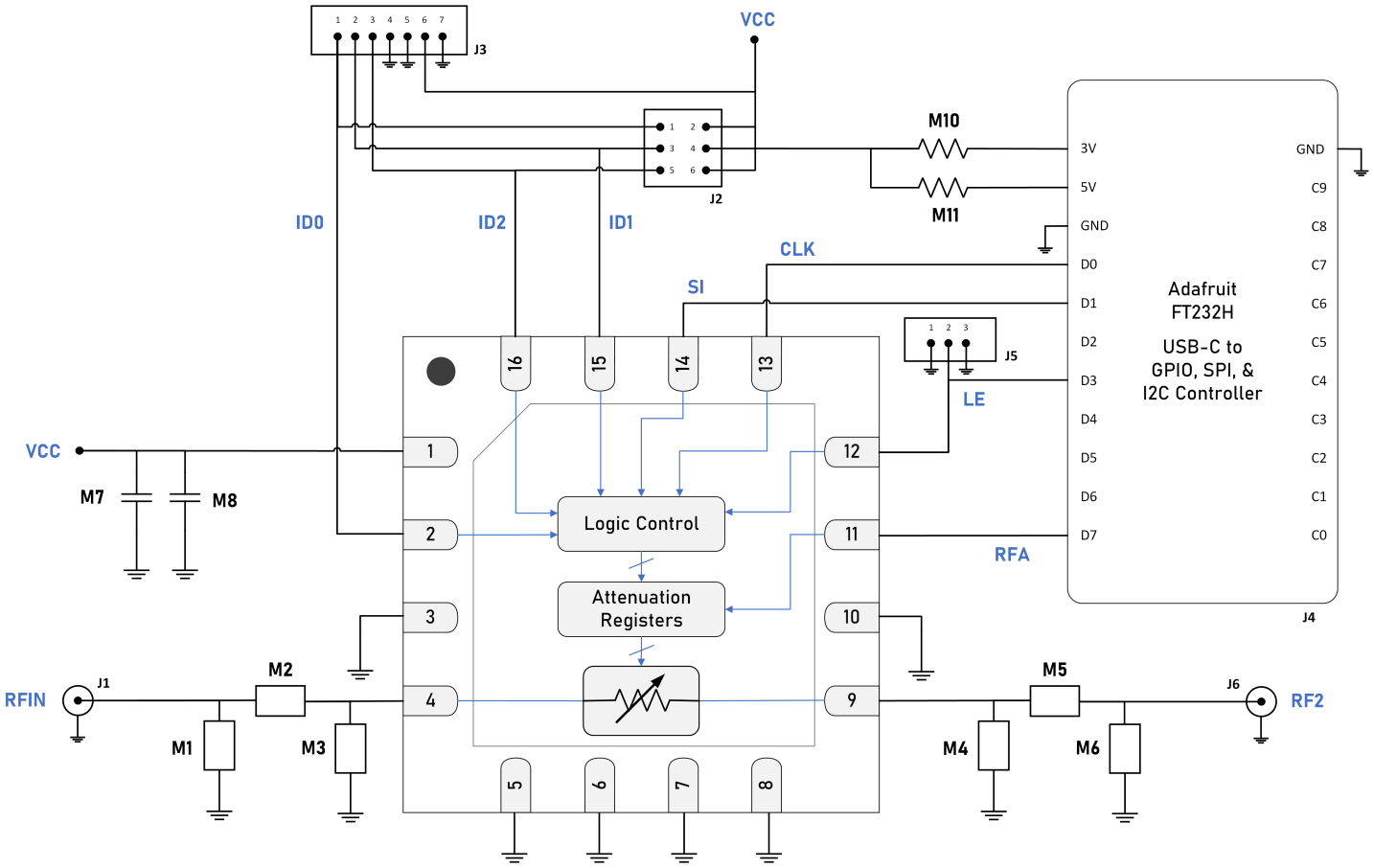


GRF6402 DSA_GlitchLevel_Low(dB) vs ProgAtten1(dB) at Pin = 15 dBm



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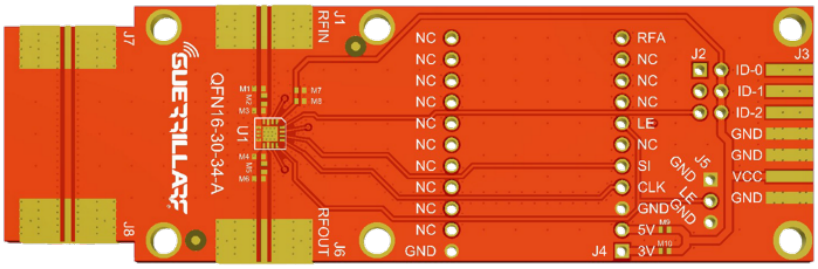
NOTE: ***Do not apply DC voltage to pins 4 (RF1) and 9 (RF2).*** DC blocking capacitors must be used if there is voltage present on the RF lines from the preceding or following stages. As a matter of good practice, it is recommended that DC blocks be used as a precaution.

The DSA will not generate DC voltages on either pins 1 and 9; as such, the blocking capacitors can be omitted in cases where it can be guaranteed that no DC will couple onto the RF lines from the preceding or following RF stages. Any DC voltage applied to the RF1 and RF2 pins may lead to electrical overstress, so be cautious when contemplating the removal of these components.

GRF6402 Application Schematic

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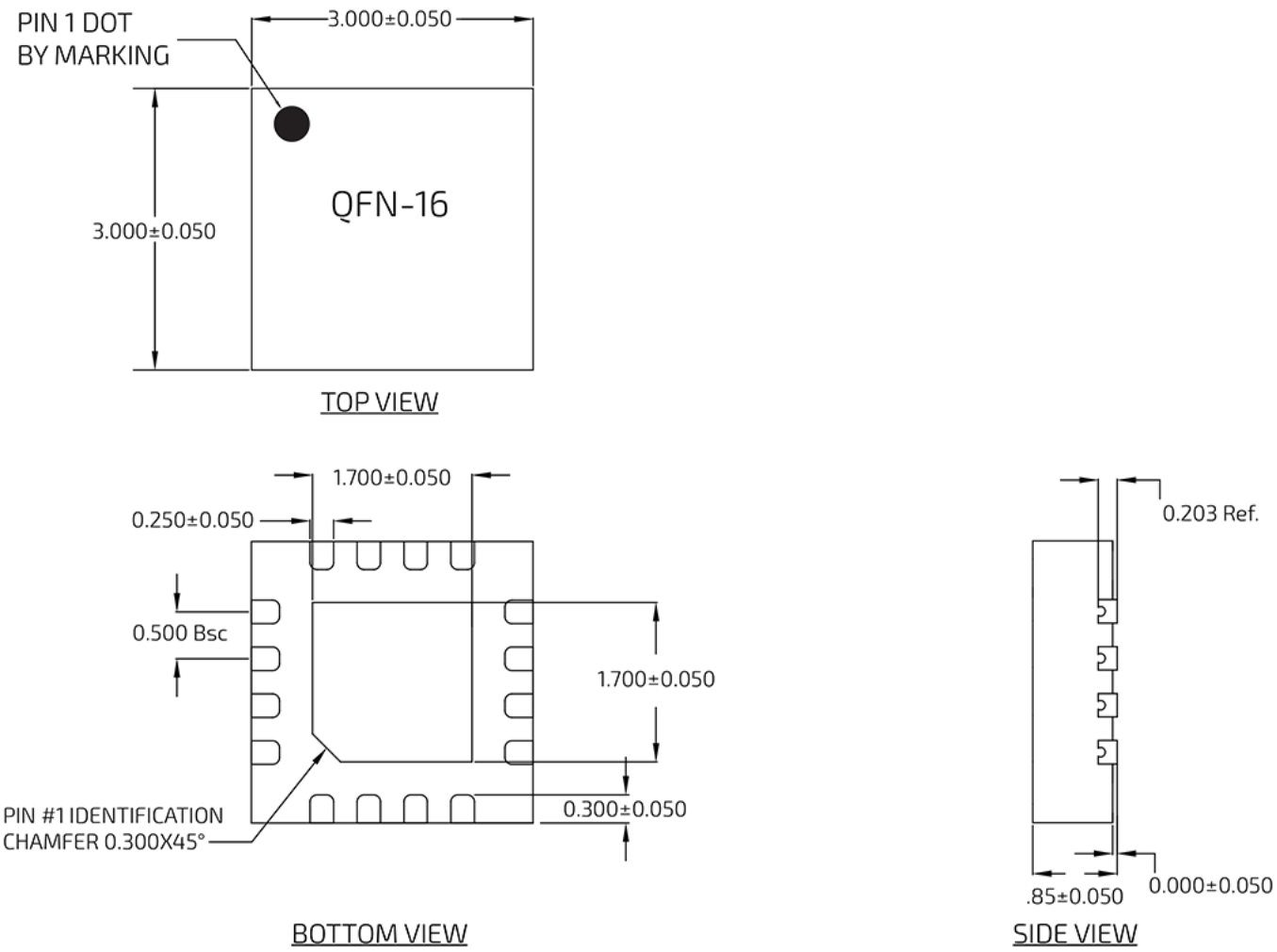
GRF6402 Evaluation Board Assembly Diagram

GRF6402 Evaluation Board Assembly Diagram Reference

Component	Type	Manufacturer	Family	Value	Package Size	Substitution
M1				DNP		Ok
M2	Resistor	Murata	--	0 Ω	0402	Ok
M3				DNP		Ok
M4				DNP		Ok
M5	Resistor	Murata	--	0 Ω	0402	Ok
M6				DNP		Ok
M7	Capacitor	Murata	GJM	10 nF	0402	Ok
M8	Capacitor	Murata	GJM	1 µF	0402	Ok
Control Board	FT232H USB-C to GPIO, SPI and I2C Controller	Adafruit	2264 **Note 2**			
Evaluation Board	QFN16-30-34-A					

Note 1: Standard evaluation board bias: V_{CC} = 5.0 V
Note 2: For additional product details, go to https://www.adafruit.com/product/2264

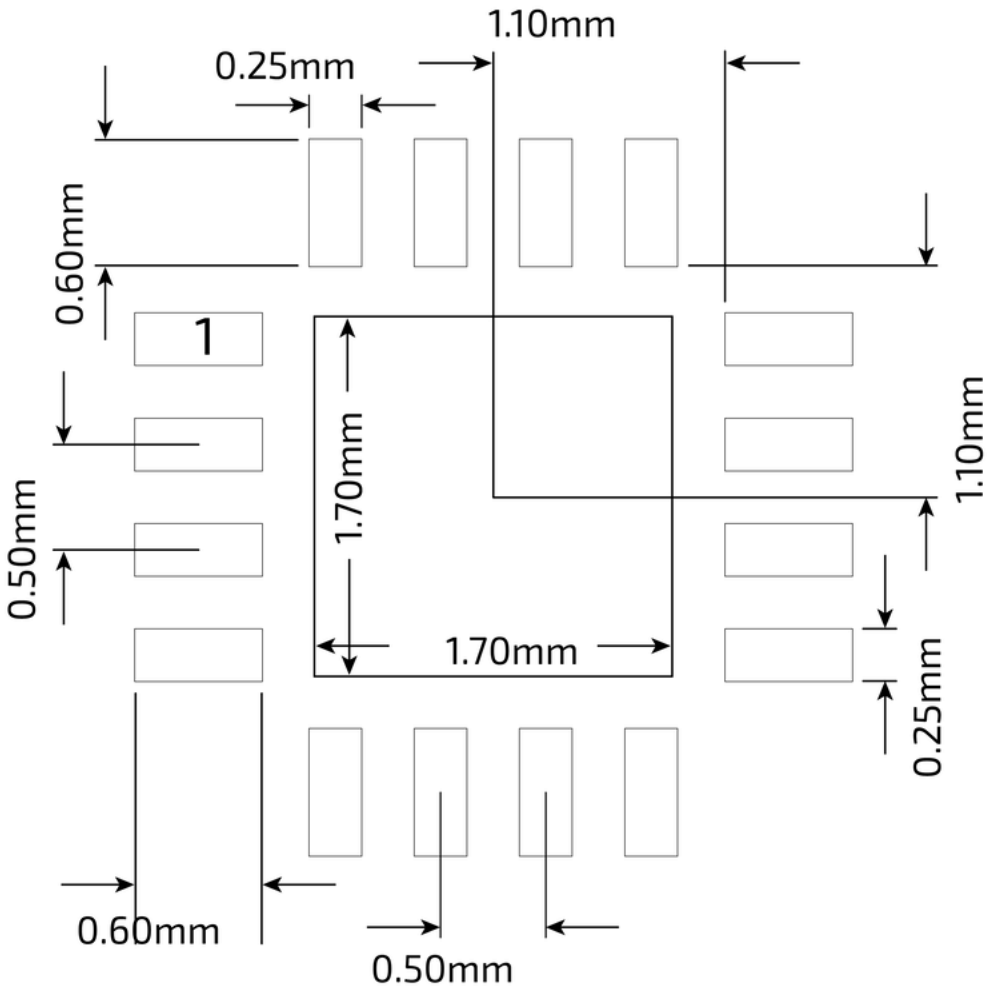
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QFN 16 3x3mm Package Dimensions

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QFN 16 3x3mm Suggested PCB Footprint (Top View)

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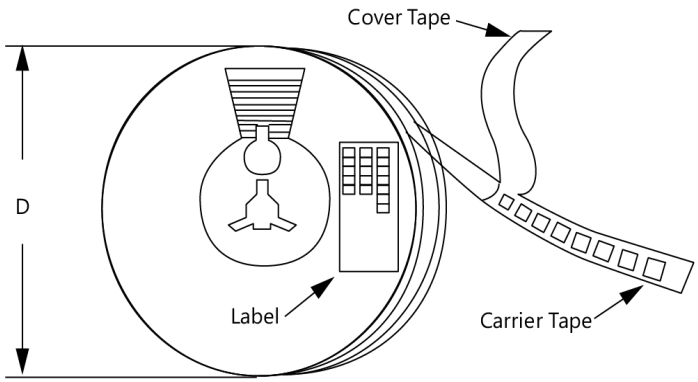
Package Marking Diagram



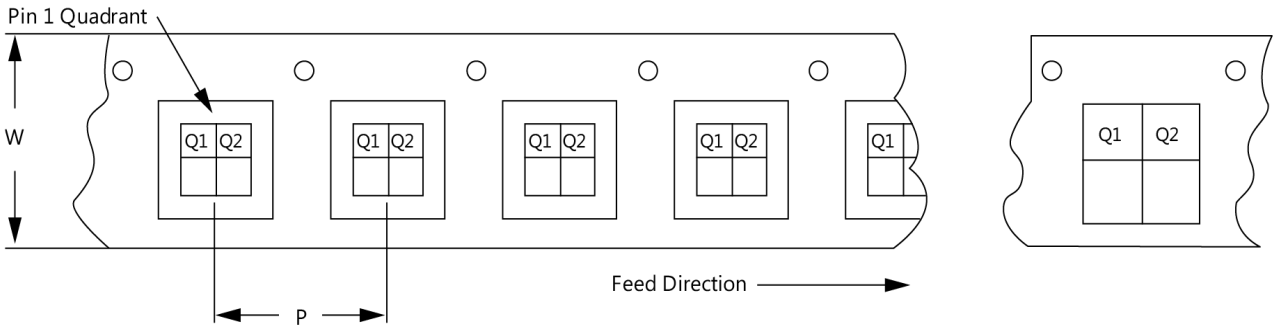
Line 1: “YY” = Year. “WW” = WORK WEEK the Device was assembled.
Line 2: “GRF” = Guerrilla RF
Line 3: “XXXX” = Device Part Number.

Tape and Reel Information

Guerrilla RF's tape and reel specification complies with Electronics Industries Association (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag, and the outside surface of the box. For the latest reel specifications and package information (including units/reel), please visit Package Manufacturing Information | Guerrilla RF (guerrilla-rf.com).



Tape and Reel Packaging with Reel Diameter Noted (D)



Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information

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Revision History

Revision Date	Description of Change
June 30, 2023	Release Ø Datasheet – Initial Publication
January 19, 2024	Release A Datasheet. Increased CDM ESD limit from 500 V to 750 V. Updated applications schematic to include Adafruit FT232H USB-C to GPIO, SPI and I2C Controller. Revised programming section to properly define the *Rapid Fire* Pointer Flag within the CONFIG register. With this corrected setting, a '0' assigned to bit [0] in the CONFIG register pulls the *Rapid Fire* attenuation value directly from the RFAREG register.
January 29, 2024	Release B Datasheet. Updated timing diagram to clarify that bits are latched into registers after the LE line is toggled high and then low. Added verbiage to LE pin description stating that if left unconnected, logic will default to HIGH due to included pull-up on chip.
December 5, 2024	Added new Glitch-Level High & Low plots.
August 29, 2025	Added verbiage clarifying Mode 0 SPI operation and default states for all I/O pins when left in an unconnected state.
January 28, 2026	Corrected language surrounding the serial data latching procedure. Updated the *SPI Programming Sequence* section, adding details on how the static logic on the LE line affects the latching of serial data into the device's targeted registers. Clarified that the latching process occurs on the rising edge of the LE command as the logic transitions from LOW to HIGH (as opposed to the falling edge of a LOW - HIGH - LOW LE command toggle). Updates similarly made to the LE pin description.

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Data Sheet Classifications

Data Sheet Status	Notes
Advance	S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices.
Preliminary	All data based on evaluation board measurements taken within the Guerrilla RF Applications Lab. Any MIN/MAX limits represented within the data sheet are based solely on *estimated* part-to-part variations and process spreads. All parametric values are subject to change pending the collection of additional data.
Release Ø	All data based on measurements taken with *production-released* material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory.
Release A-Z	All data based on measurements taken with production-released material *derived from multiple lots which have been fabricated over an extended period of time*. MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads.

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