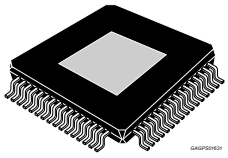
life.augmented

FDA801B

4 x 50 W 110 dB dynamic range class-D digital input automotive power amplifier with load value recognition

Datasheet - production data



LQFP64 (exposed pad up)

Features

- AEC-Q100 revision H qualified
- Integrated 110 dB D/A conversion
- I^2S and TDM digital input (3.3/1.8 V)
- Input sampling frequency: 44.1 kHz, 48 kHz, 96 kHz, 192 kHz
- Class-D channels with 93% efficiency
- EMI control for AM compatibility
- EMI compliance evaluated following normative IEC61967-4 and IEC62132-4
- Low radiation function (LRF)
- Idle tones free DAC
- Output low-pass filter included in the feedback allowing lower cost filter components and maximizing damping factor
- High output power capability
  - 28 W/4 Ω 10% THD, V_d = 14.4 V
  - Max. output power: 4 x 50 W/4 Ω @ 15.2 V, 1 kHz
- Full I^2C bus driving (3.3/1.8 V):
  - Channels independent tristate
  - Channel independent and intrinsically pop-free play/mute
  - I^2C bus diagnostics, including both AC and DC impedance test with programmable thresholds
  - AC diagnostic possible with both internally generated signal (20 kHz) and externally generated signals
- Integrated fault protection
- Input and output offset detector
- Clipping detector
- ESD protection
- 6 V operation (“Start - Stop” engines compatibility)
- 2 and 1 Ω load driving capability

Description

FDA801B is a new BCD technology quad bridge class D amplifier, specially intended for automotive applications.

Thanks to the technology used, it is possible to integrate a high performance D/A converter together with powerful MOSFET outputs in class-D configuration, to get outstanding efficiency compared with the standard class AB.

The integrated D/A converter allows to reach outstanding performances (115 dB S/N ratio with 110 dB of dynamic range). The feedback loop is including the output L-C low-pass filter, allowing superior frequency response linearity and lower distortion independently from the inductor and capacitor quality.

FDA801B is fully configurable through I^2C bus interface and integrates a full diagnostics array specially intended for automotive applications. Thanks to the solutions implemented to contain EMI emissions, the device is intended to be used in the standard single DIN car-radio box together with the tuner.

Moreover FDA801B is able to work with power supply as low as 6 V, thus supporting the most recent low voltage ('start-stop') car-makers specification.

Table 1. Device summary

Order code	Package	Packing
FDA801B-VYY	LQFP64 (exp. pad up)	Tray
FDA801B-VYT	LQFP64 (exp. pad up)	Tape & Reel

This is information on a product in full production. www.st.com

Contents

List of tables

List of figures

1 Block diagram and pins description

Figure 1. Block diagram

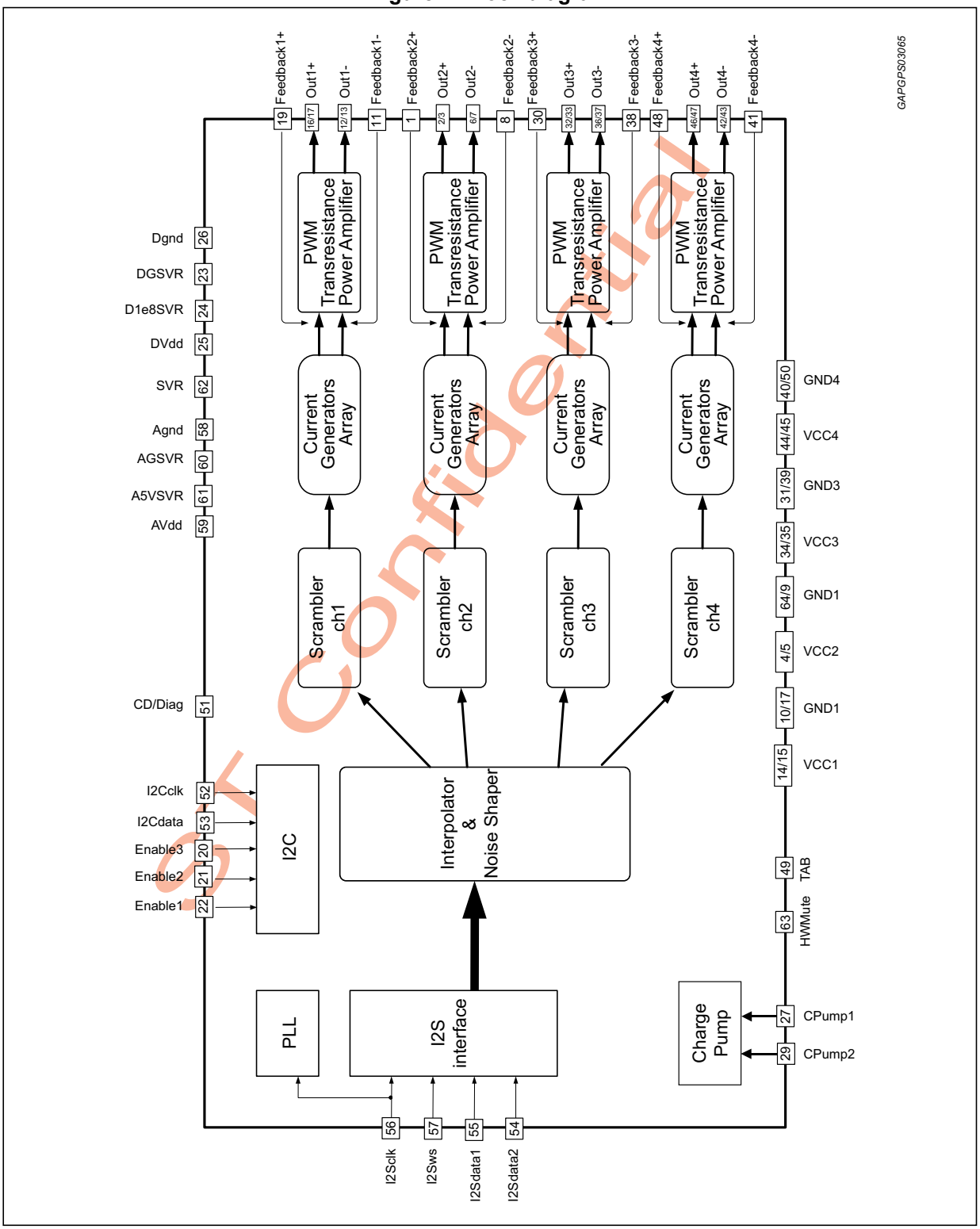


Figure 2. Pins connection diagram (top view)

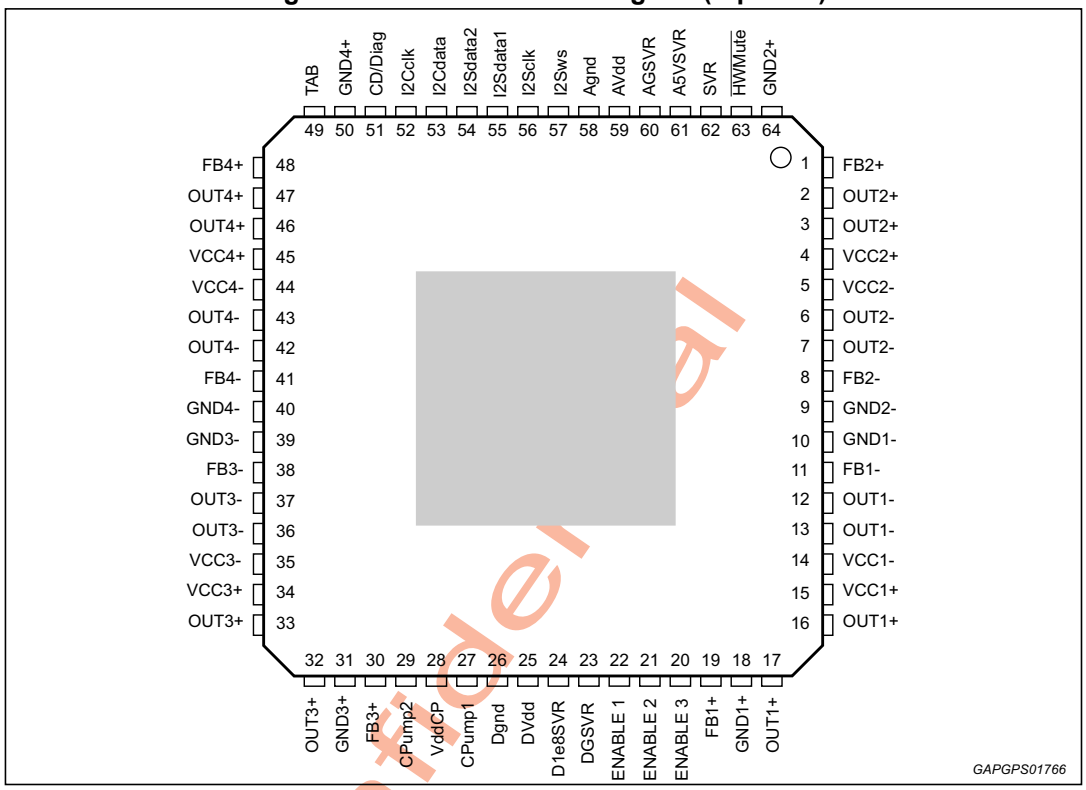


Table 2. Pins list description

N#	Pin	Function
1	FB2+	Channel 2, half bridge plus, Feedback
2	OUT2+	Channel 2, half bridge plus, Output
3	OUT2+	Channel 2, half bridge plus, Output
4	VCC2+	Channel 2, half bridge plus, Power Supply
5	VCC2-	Channel 2, half bridge minus, Power Supply
6	OUT2-	Channel 2, half bridge minus, Output
7	OUT2-	Channel 2, half bridge minus, Output
8	FB2-	Channel 2, half bridge minus, Feedback
9	GND2-	Channel 2, half bridge minus, Power Ground
10	GND1-	Channel 1, half bridge minus, Power Ground
11	FB1-	Channel 1, half bridge minus, Feedback
12	OUT1-	Channel 1, half bridge minus, Output
13	OUT1-	Channel 1, half bridge minus, Output
14	VCC1-	Channel 1, half bridge minus, Power Supply
15	VCC1+	Channel 1, half bridge plus, Power Supply
16	OUT1+	Channel 1, half bridge plus, Output

Table 2. Pins list description (continued)

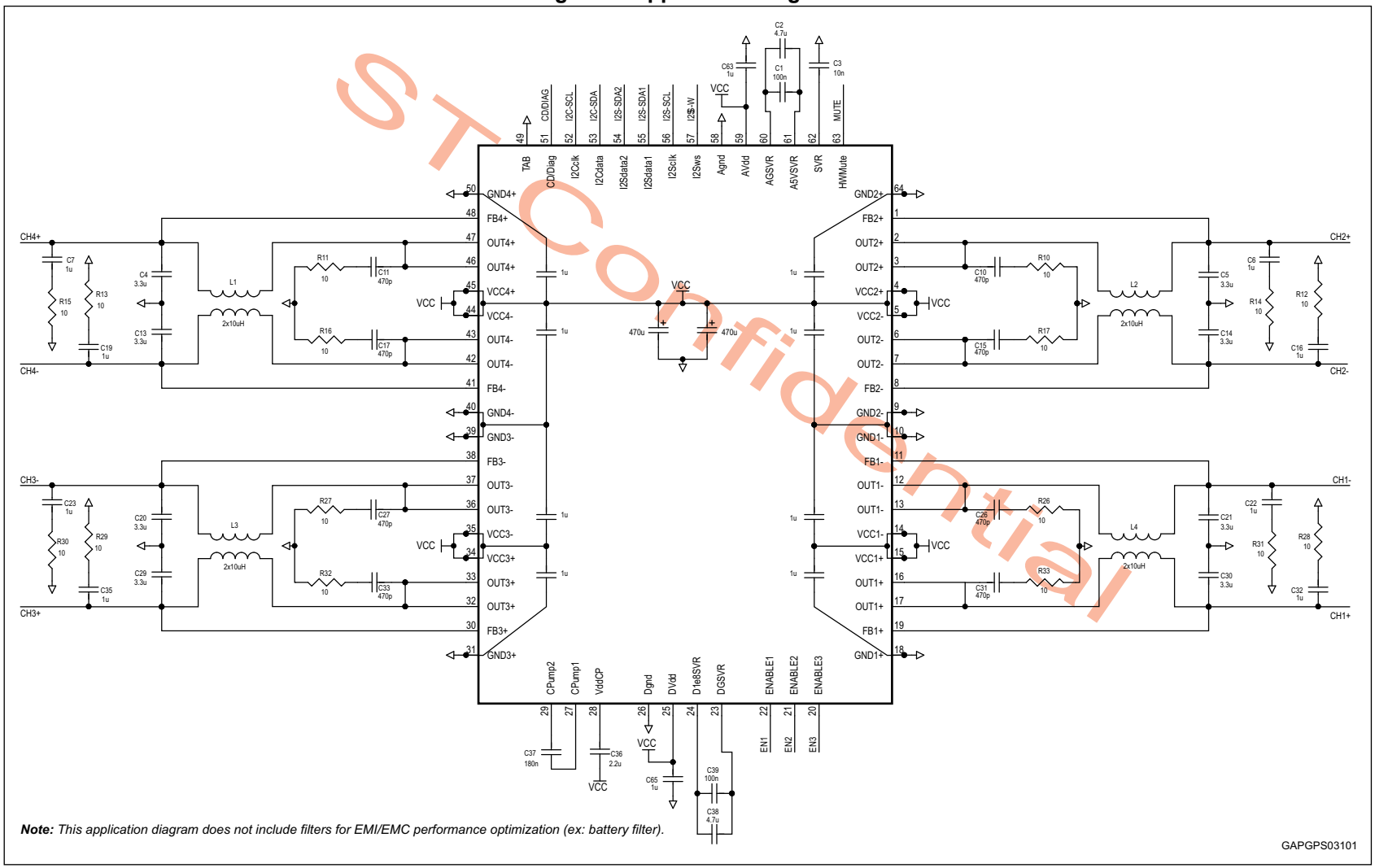
N#	Pin	Function
17	OUT1+	Channel 1, half bridge plus, Output
18	GND1+	Channel 1, half bridge plus, Power Ground
19	FB1+	Channel 1, half bridge plus, Feedback
20	ENABLE 3	Enable 3
21	ENABLE 2	Enable 2
22	ENABLE 1	Enable 1
23	DGSVR	Negative digital supply V(SVR)-0.9V (Internally generated)
24	D1e8SVR	Positive digital supply V(SVR)+0.9V (Internally generated)
25	DVdd	Digital supply
26	Dgnd	Digital ground
27	CPump1	Charge Pump pin1 (auxiliary pin)
28	VddCP	Charge Pump output voltage, Output
29	CPump2	Charge Pump pin2 (auxiliary pin)
30	FB3+	Channel 3, half bridge plus, Feedback
31	GND3+	Channel 3, half bridge plus, Power Ground
32	OUT3+	Channel 3, half bridge plus, Output
33	OUT3+	Channel 3, half bridge plus, Output
34	VCC3+	Channel 3, half bridge plus, Power Supply
35	VCC3-	Channel 3, half bridge minus, Power Supply
36	OUT3-	Channel 3, half bridge minus, Output
37	OUT3-	Channel 3, half bridge minus, Output
38	FB3-	Channel 3, half bridge minus, Feedback
39	GND3-	Channel 3, half bridge minus, Power Ground
40	GND4-	Channel 4, half bridge minus, Power Ground
41	FB4-	Channel 4, half bridge minus, Feedback
42	OUT4-	Channel 4, half bridge minus, Output
43	OUT4-	Channel 4, half bridge minus, Output
44	VCC4-	Channel 4, half bridge minus, Power Supply
45	VCC4+	Channel 4, half bridge plus, Power Supply
46	OUT4+	Channel 4, half bridge plus, Output
47	OUT4+	Channel 4, half bridge plus, Output
48	FB4+	Channel 4, half bridge plus, Feedback
49	TAB	Device slug connection
50	GND4+	Channel 4, half bridge plus, Power Ground

Table 2. Pins list description (continued)

N#	Pin	Function
51	CD/Diag	Clipping detector and diagnostic output pin: – Overcurrent protection intervention – Thermal warning – Offset detection
52	I2Cclk	I2C Clock
53	I2Cdata	I2C Data
54	I2Sdata2	I2S/TDM Data input 2
55	I2Sdata1	I2S/TDM Data input 1
56	I2Sclk	I2S/TDM Clock input
57	I2Sws	I2S/TDM Sinc input
58	Agnd	Analog ground
59	AVdd	Analog supply
60	AGSVR	Negative Analog Supply V(SVR)-2.5V (Internally generated)
61	A5VSVR	Positive Analog Supply V(SVR)+2.5V (Internally generated)
62	SVR	Supply Voltage Ripple Rejection Capacitor
63	$\overline{\text{HWMute}}$	Hardware mute pin
64	GND2+	Channel 2, half bridge plus, Power Ground

2 Application diagram

Figure 3. Application diagram



Note: *This application diagram does not include filters for EMI/EMC performance optimization (ex: battery filter).*

3 Electrical specifications

3.1 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	-0.3 to 28	V
V_{CC}	Transient supply voltage for t = 100 ms	-0.3 to 50	V
Gnd_{max}	Ground pin voltage difference	-0.3 to 0.3	V
V_{i2c}	I^2C bus pins voltage	-0.3 to 5.5	V
V_{i2s}	I^2S bus pins voltage	-0.3 to 5.5	V
Enable, V_{hwm}	Enable and HWMute pins voltage	-0.3 to 5.5	V
V_{CD}	CD/DIAG pin	-0.3 to 5.5	V
I_O	Output current (repetitive f > 10 Hz)	internally limited	A
T_{amb}	Ambient operating temperature	-40 to 105	°C
T_{stg}, T_j	Storage and junction temperature	-55 to 150	°C
ESDHBM	ESD protection HBM(1)	2000	V
ESDCDM	ESD protection CDM(1)	500	V

1. Conforming to ESD standard.

3.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Typ	Max	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction-to-case	1.15	1.6	°C/W

3.3 Electrical characteristics

V_{cc} = 14.4V; R_L = 4Ω; f = 1kHz; T_{amb} = 25°C; I^2C defaults, unless otherwise specified.
LC filter: L = 10 µH, C = 3.3 µF. PWM in In-phase modulation.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
General characteristics						
V_S	Supply voltage range	-	6	-	25	V
		R_L = 2 Ω	6	-	18	V
I_{VCC}	Quiescent current	Device in standby	-	-	2	µA
		Device on(1)	-	136	-	mA
		ECO-mode	-	95	115	mA

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{OS}	Offset voltage	Mute & Play	-10	-	10	mV
-	Overcurrent protection(2)	IB12-D7/6 = 00	9.5	11	12.5	A
		IB12-D7/6 = 01	6.7	8	9.3	A
		IB12-D7/6 = 10	4.4	5.5	5.6	A
		IB12-D7/6 = 11	3.5	4.5	5.5	A
-	Overvoltage shutdown	-	28	29	30	V
V_{lowM}(3)	V_{CC} low supply mute threshold (Min I^2C setting - default)	Attenuation <0.5 dB, digital mute disabled	-	-	5.7	V
		Attenuation ≥60 dB, digital mute disabled	5.1	-	-	V
	V_{CC} low supply mute threshold (Max I^2C setting)	Attenuation <0.5 dB, digital mute disabled	-	-	7.7	V
		Attenuation ≥60 dB, digital mute disabled	6.8	-	-	V
	V_{CC} low supply mute threshold in diagnostic	Attenuation <0.5 dB	-	-	7.8	V
		Attenuation ≥60 dB	5.1	-	-	V
V_{uvVcc}	Vcc supply UVLO threshold	Min I^2C setting IB1-d4 = "0", (default)	-	5.1	5.4	V
		Max I^2C setting IB1-d4 = "1"	-	6.9	7.4	V
V_{uvhyst}(4)	Vcc supply UVLO hysteresis	-	-	0.4	-	V
Tph	Thermal protection junction temperature	Attenuation = 60 dB	163	173	186	°C
Tpl		Attenuation = 0.5 dB	150	160	173	°C
Tw1	Thermal warning junction Temperature	-	-	Tpl-5	-	°C
Tw2		-	-	Tpl-20	-	°C
Tw3		-	-	Tpl-30	-	°C
Tw4		-	-	Tpl-45	-	°C
Audio performances						
P_O	Output power (5)	Max power; V_{cc} = 25 V	125	135	-	W
		Max power; V_{cc} = 15.2 V	45	50	-	W
		THD = 10%	28	30	-	W
		THD = 1%	22	25	-	W
		R_L = 2 Ω; THD 10%	50	55	-	W
		R_L = 2 Ω; THD 1%	40	45	-	W
		R_L = 2 Ω; max power	72	80	-	W
G_{V1}	Voltage gain 1	at Amplitude = -10 dBFs	7.6	8.3	9	Vp
G_{V2}	Voltage gain 2		5.5	6	6.5	Vp
G_{V3}	Voltage gain 3		3.2	3.5	3.8	Vp
G_{V4}	Voltage gain 4		2.35	2.55	2.75	Vp
DGv	Voltage gain match (6)	Gv = Gv1 or Gv = Gv2	-1	-	+1	dB

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
PSRR	Power supply rejection ratio	f = 1 kHz; Vr = 1 Vpk; See *Figure 19* for behavior vs. frequency.	75	85	-	dB
THD	Total harmonic distortion	P_O = 1 W, f = 1 kHz	-	-	0.03	%
		V_s = 25 V, R_L = 4 Ω, P_O = 1 W, f = 1 kHz	-	-	0.05	%
C_T (2)	Cross talk	f = 1 kHz	-	100	-	dB
E_{out1}	Output noise	A-wtd and brick wall 20 kHz filter used, no output signal; $G_V = G_{V1}$ $G_V = G_{V4}$	- -	30 27	45 42	µV
E_{out2}	Output noise	ITU-R 468 and brickwall filter, no output signal	-	70	110	µV
DR	Dynamic range	A-wtd and brickwall 20 kHz filter	-	110	-	dB A-wtd
SNR	Signal to noise ratio	A-wtd and brickwall 20 kHz filter	111	115	-	dB A-wtd
ΔV_{OITU} (7)	Peak of absolute value of output voltage (ITU-R ARM filtered)	Standby to Eco-mode and Eco to Standby transition	-5	-	+5	mV
		Eco mode to play and play to Eco mode transition	-7.5	-	+7.5	mV
Control pins characteristics						
V_{enl}	Enable pins low voltage	-	-	-	0.9	V
V_{enh}	Enable pins high voltage	-	2.4	-	-	V
Mute						
V_{Mth} (3)	Mute pin voltage threshold	Attenuation <0.5 dB, and digital mute disabled	2.6	-	-	V
		Attenuation ≥60 dB, and digital mute disabled	-	-	1.6	
I_M	Mute pin source current	-	4.5	6	7.5	µA
V_{Mcl}	Mute pin internal clamp voltage	-	4.3	5	5.5	V
I_{feed}	Peak current flowing in the feedback pins	Standby condition, all feedbacks forced to V_{cc}, output floating	-	140	200	µA
I^2C bus interface						
f_{SCL}	Clock frequency	-	-	-	400	kHz
V_{IL}	I2C pins low voltage	-	-	-	0.8	V
V_{IH}	I2C pins high voltage	-	1.3	-	-	V
V_{OLMAX}	Maximum I^2C data pin low voltage when current I_{sink} is sinked	I_{sink} = 3 mA	-	-	0.4	V

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{LIMAX}	Maximum input leakage current	V = 3.6V	-	-	1	µA
I^2S bus interface						
V_{IL-I2S}	I2S pins low voltage	-	-	-	0.8	V
V_{IH-I2S}	I2S pins high voltage	-	1.3	-	-	V
Clipping and offset detector						
CD_{THD}	Clip detection THD (8)	THD @ 100 Hz with average Vclipdet = 2 V	5	7	9	%
CD_{SAT}	Clip detection saturation voltage	CD on; I_{CD} = 1 mA	-	150	300	mV
CD_{LK}	Clip detection leakage current	CD pin at 3.6 V	-	-	15	µA
V_{offin}	Input DC offset detection threshold	Threshold at which an offset present at inputs is detected; Output DC offset disabled	-	-18	-	dBfs
V_{offout}	Output DC offset detection threshold	Input DC offset disabled	1.5	2.2	2.9	V
Diagnostic						
I_{Pgnd}	No short to GND detection (below this output current limit, the output is considered in normal conditions)	-	-	-	4	mA
	Short to GND detection (above this output current limit, the output is considered shorted to GND)	-	35	-	-	mA
I_{Pps}	No Short to Supply detection (below this output current limit, the output is considered in normal conditions)	-	-	-	-4	mA
	Short to Supply detection (over this output current limit, the output is considered in short circuit to V_S)	-	-35	-	-	mA

1. Value measured using output coil with following characteristics: core saturation current higher than 10 A, Rs at 400 kHz = 145 mΩ
2. Measured at bench during product validation.
3. See *Chapter 6: Muting function architecture* for more details.
4. Hysteresis on V_{CC} raising edge.
5. Parameter not directly measured at ATE (values expressed are based on correlation with R_{dson} measurement).
6. The parameter specifies the difference in gain between the two channels that show the highest and lowest gain (in one IC).
7. Mute to play and play to mute transitions are guaranteed by design (intrinsically immune from any pop).
8. Tested at ATE with f = 1 kHz, V_{cc} = 8 V, guaranteed by correlation factor.

3.4 Typical curves of the main electrical parameters

Figure 4. Efficiency and power dissipation (V_S = 14.4 V, R_L = 4 x 4 Ω, f = 1 kHz sine wave)

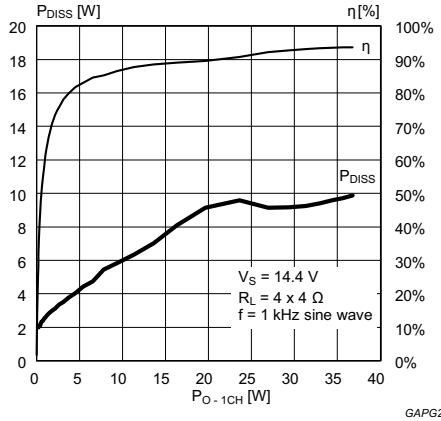


Figure 5. Efficiency and power dissipation (V_S = 14.4 V, R_L = 4 x 4 Ω, pink noise wave)

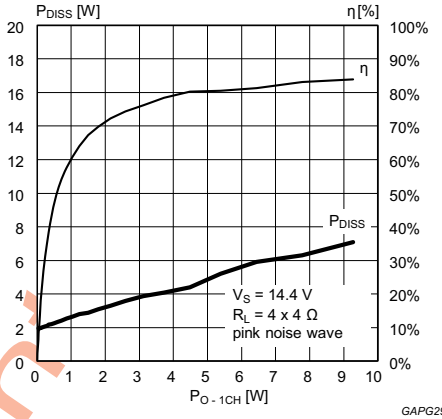


Figure 6. Efficiency and power dissipation (V_S = 25 V, R_L = 4 x 4 Ω, f = 1 kHz sine wave)

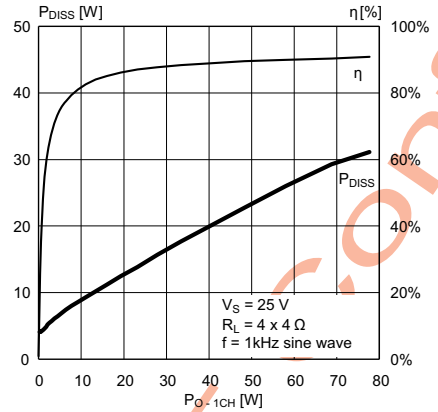


Figure 7. Efficiency and power dissipation (V_S = 25 V, R_L = 4 x 4 Ω, pink noise wave)

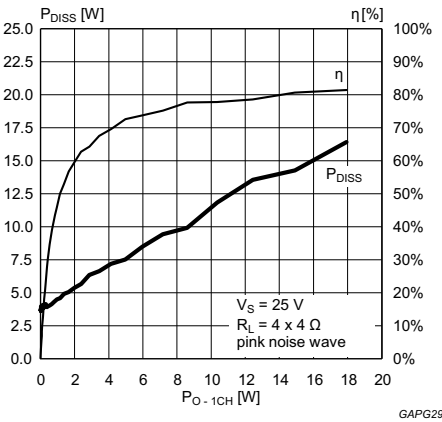


Figure 8. Efficiency and power dissipation (V_S = 25 V, R_L = 2 x 2 Ω, f = 1 kHz sine wave)

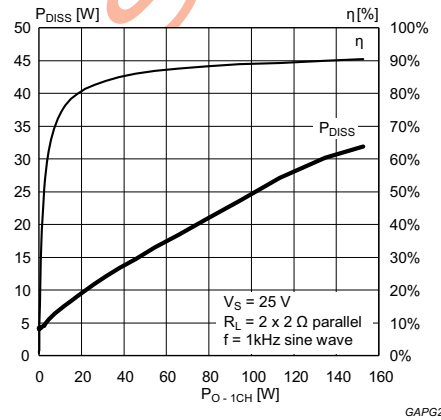


Figure 9. Efficiency. and power dissipation (V_S = 25 V, R_L = 2 x 2 Ω, pink noise wave)

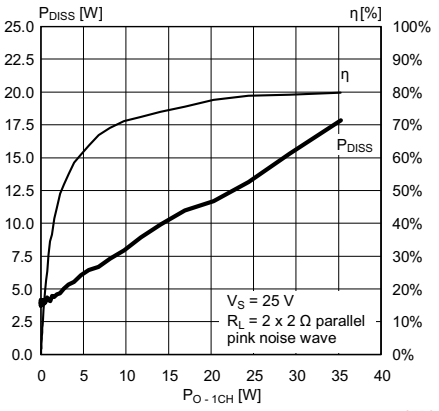


Figure 10. Efficiency and power dissipation (V_S = 18 V, R_L = 4 x 2 Ω, f = 1 kHz sine wave)

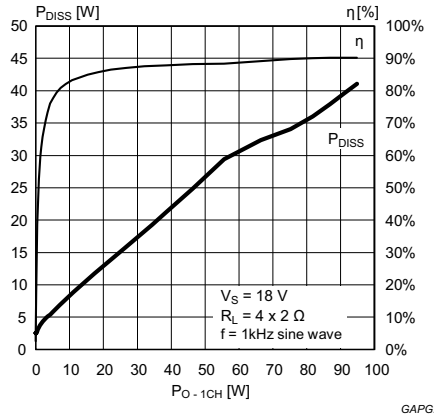


Figure 11. Efficiency and power dissipation (V_S = 18 V, R_L = 4 x 2 Ω, pink noise wave)

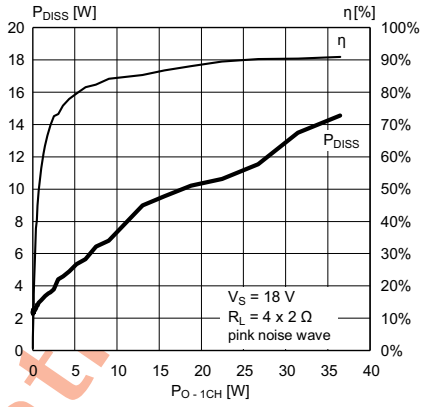


Figure 12. Output power vs. supply voltage (R_L = 4 Ω, sine wave)

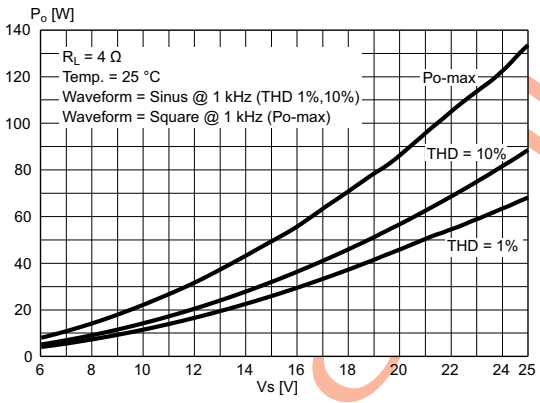


Figure 13. Output power vs. supply voltage (R_L = 2 Ω single mode, sine wave)

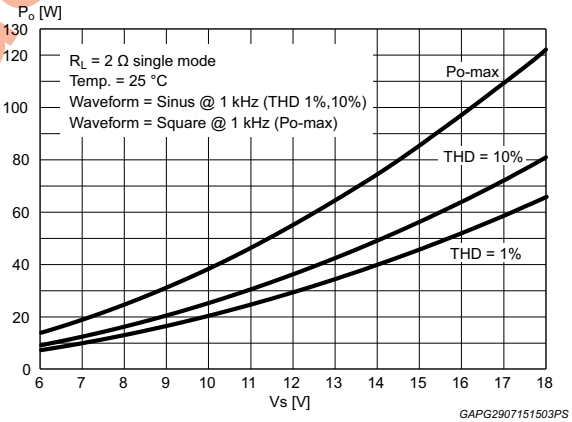


Figure 14. Output power vs. supply voltage (R_L = 2 Ω parallel mode, sine wave)

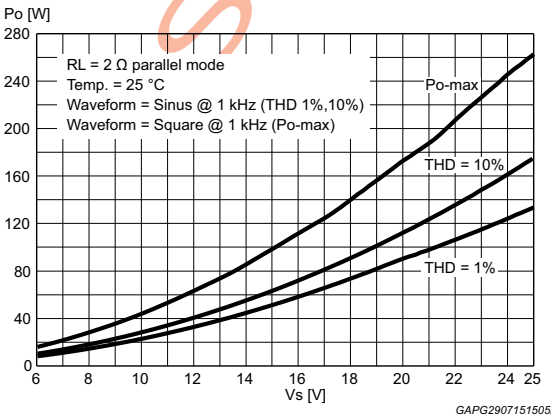


Figure 15. THD vs output power (V_S = 14.4 V, R_L = 4 Ω)

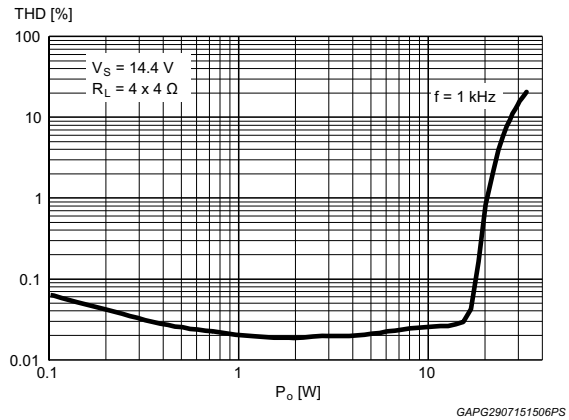


Figure 16. THD vs output power (V_S = 14.4 V, R_L = 2 Ω single mode)

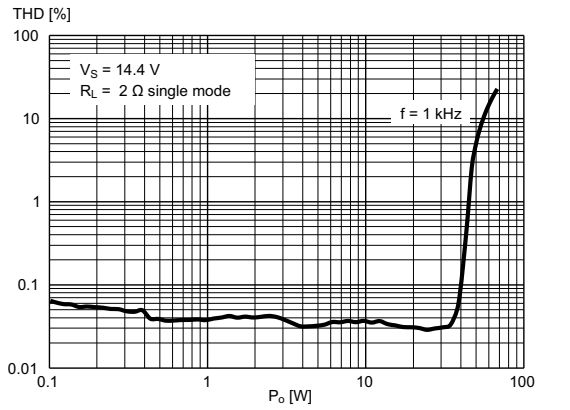


Figure 17. THD vs output power (V_S = 14.4 V, R_L = 2 Ω parallel mode)

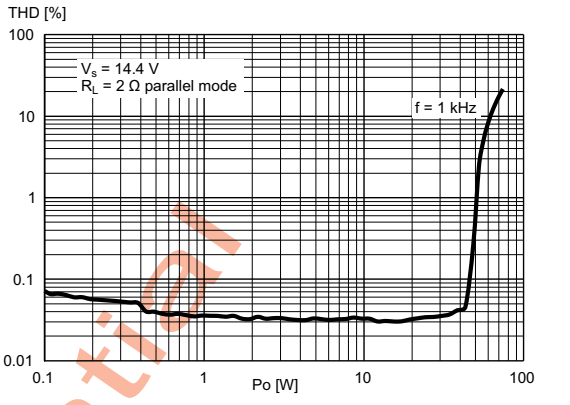


Figure 18. Crosstalk vs frequency

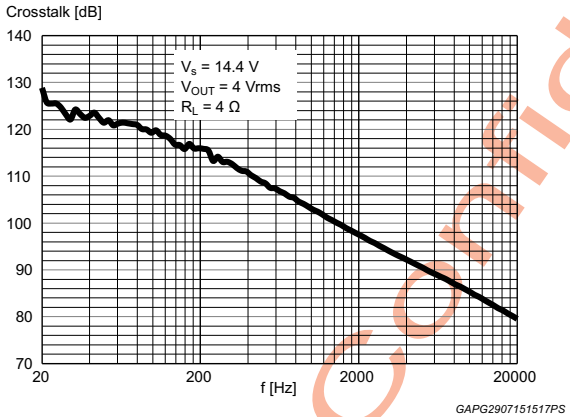


Figure 19. PSRR vs. frequency

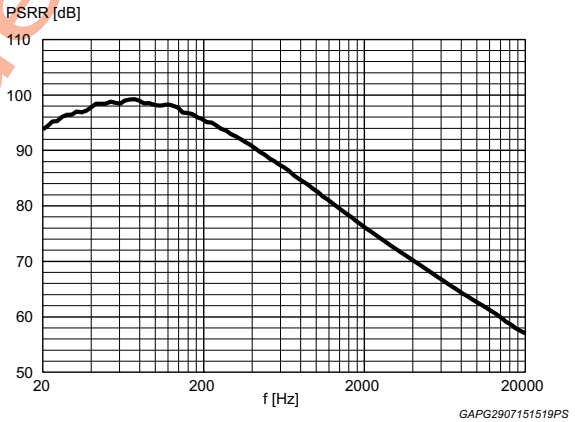


Figure 20. THD vs. frequency (V_S = 14.4 V, R_L = 4 Ω, P_o = 1 W)

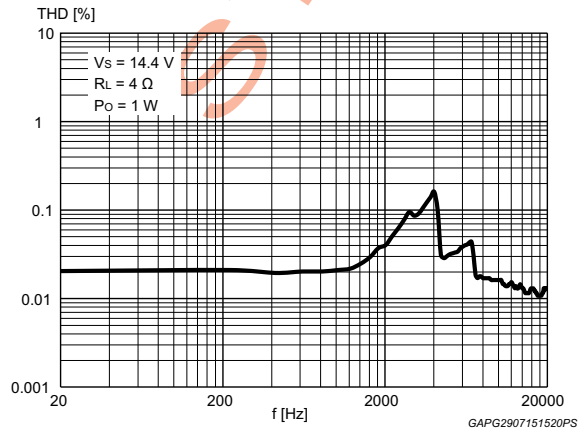


Figure 21. THD vs. frequency (V_S = 14.4 V, R_L = 2 Ω single mode, P_o = 2 W)

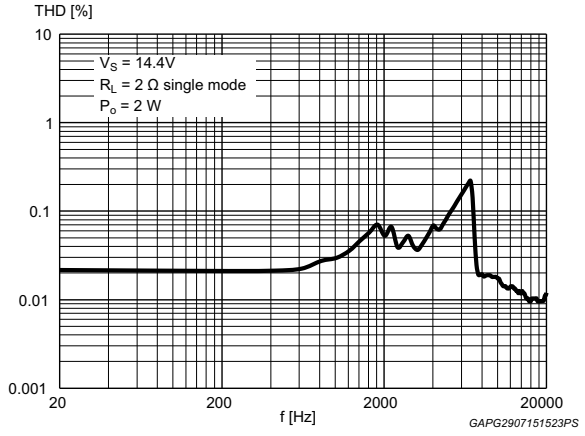


Figure 22. Frequency response (R_L = 4 x 4 Ω, P_o = 1 W, sine wave @ 1 kHz)

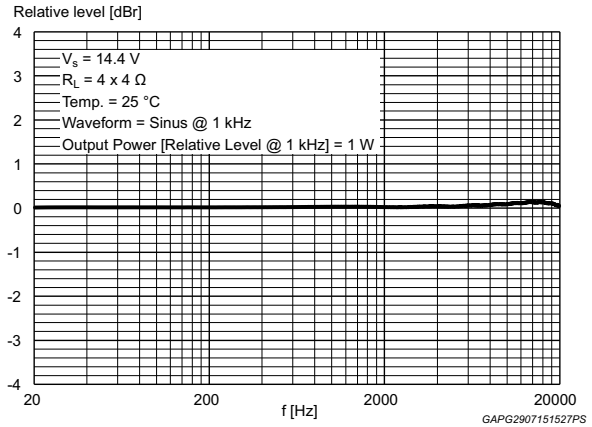


Figure 23. Frequency response (R_L = 4 x 2 Ω, P_o = 1 W, sine wave @ 1 kHz)

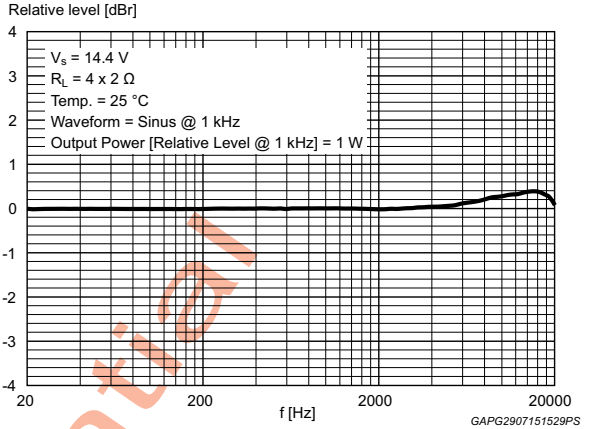


Figure 24. 'LC filter compensation effect on frequency response (4 Ω load and open load)

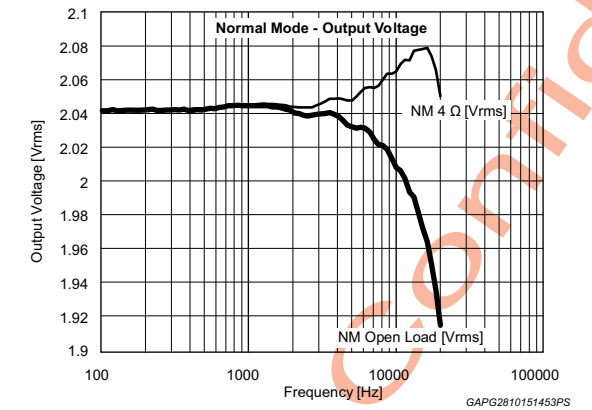


Figure 25. Dynamic range

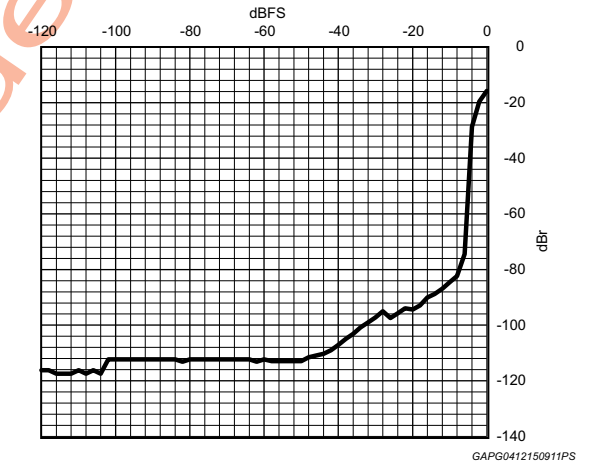
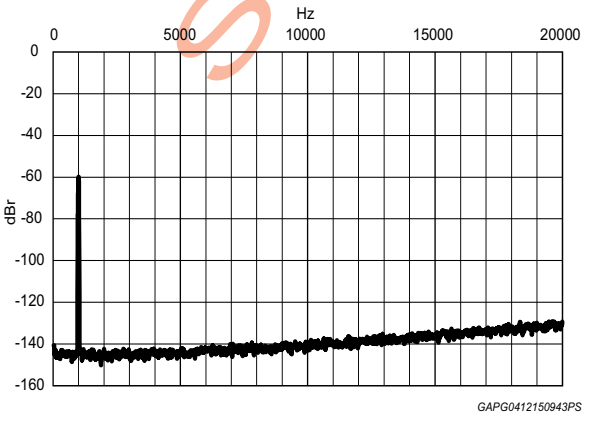


Figure 26. FFT - Output spectrum (-60 dBFS input signal)



4 General introduction

FDA801B is a fully digital single chip class D amplifier with high immunity to the demodulation filter effects. The high integration level and the on-board signal processing allow excellent audio performance to be achieved.

Thanks to the digital input and to the feedback strategy in the power stage that make the amplifier immune from the output filter components non-linearity, the number and size of the external components are minimized.

A number of features is included to reduce EMI and the fully digital approach provides a strong GSM immunity.

FDA801B includes: digital I^2C and I^2S interfaces, internal 24 bits DAC conversion, digital signal processing for interpolation and noise shaping, innovative self-diagnostic functions and automatic detection of wrong load connections or variation of the load, internal PLL for a clock generation. Moreover FDA801B provides a breakthrough innovative digital impedance-meter which is able to communicate via I^2C the output load value.

4.1 New feedback topology

FDA801B adopts an innovative feedback topology, where the LC filter is included in the feedback loop making the amplifier highly insensitive to the characteristics of such a demodulation circuit. This solution optimizes the system performance in terms of THD and frequency response in any load conditions.

Regardless of the big phase shifting introduced by the output filter the device shows an adequate phase margin for any load condition. The system stability has been tested taking into account:

- PWM switching variation (from 300 to 440 kHz)
- Silicon temperature variation (from -40 to 150 °C)
- Load variation (both inductive and capacitive considered)
- LC demodulator filter variation and tolerance
- Voltage supply variation (from 6 to 25 V)

The system has been designed to guarantee a phase margin > 45 deg for any working condition.

The new feedback topology assures a strong control of voltage and current across the load making the diagnostic load detection reliable. Moreover this topology allows to reach exceptionally good values of output damping factor, as demonstrated by the frequency responses with/without load shown in the *Figure 24*.

4.2 LC filter design

The audio performance of a Class D amplifier is heavily influenced by the characteristics of the output LC filter. The choice of its components is quite critical because a lot of constraints have to be fulfilled at the same time: size, cost, not EMI filtering, efficiency. In particular, both the inductor and the capacitor exhibit a non linear behavior: the value of the inductance is a function of the instantaneous current in it and similarly the value of the capacitor is a function of the voltage across it.

In the classical approach, where the feedback loop is closed right at the output of the power stage, the LC filter is placed outside the loop and these nonlinearities cause the Total Harmonic Distortion (THD) to increase. The only way to avoid this phenomenon would be to use components which are highly linear, but this means they are also bigger and/or more expensive.

Furthermore, when the LC filter is outside the loop, its frequency response heavily depends on the impedance of the loudspeaker; this is one of the most critical aspects of Class-D amplifiers. In standard class D this can be mitigated, but not solved, by means of additional snubber networks, increasing cost, volume and power dissipation. FDA801B, instead, provides a very flat frequency response over audio-band which cannot be achieved by standard class D without feedback after LC filter.

Since the demodulator group is now in the feedback path, some constraints regarding the inductor and capacitor choice are still present but of course less stringent than in the case of a typical switching application.

4.3 Load possibilities

FDA801B supports several load possibilities and configurations. The default configuration is suitable for a 4-channel application (front/rear - left/right). By means of I^2C bus bit IB1-d7, d6 it is possible to choose a 2-channel solution with parallel outputs (left/right) or a 2.1 configuration for sub-woofer application.

Possible channel configurations:

- 4 x 4 ohm (up to 25 V)
- 4 x 2 ohm (up to 18 V)
- 2 x 1 ohm (through channels connected in parallel; limited to 18 V)
- 2 x 4 ohm + 1 x 2 ohm (through parallelized channels).

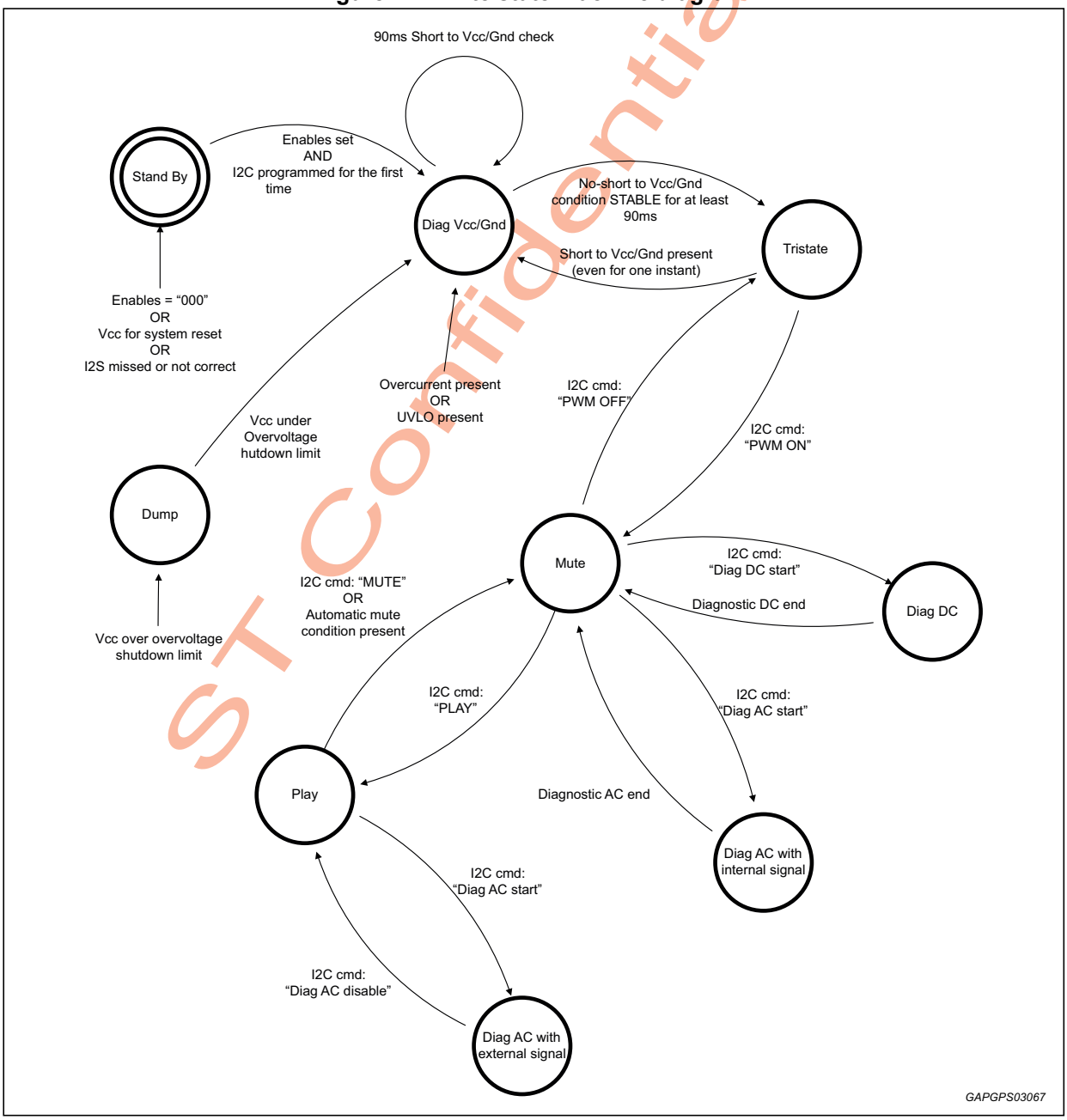
5 Operation states

FDA801B has a finite state machine which manages amplifier functionality, reacting to user and system inputs.

5.1 Finite state machine

FDA801B finite state machine is represented by the following diagram.

Figure 27. Finite state machine diagram



5.2 Standby state

ENABLE1, ENABLE2, ENABLE3 pins have a double function: set of I^{2}C addresses and start-up of the system.

If ENABLE1/2/3 are all low, ("000"), then the FDA801B system is off, the outputs remain biased to ground and the current consumption is limited to I_{sb}. In this case the FSM is in “Standby” state.

5.2.1 Out of stand-by and address selection

Through combinations of Enable1/2/3 it is possible to select 4 different I^{2}C addresses (see *Table 6*).

Table 6. Operation mode (under definition)

Operation	Enable 1	Enable 2	Enable 3
Standby mode	0	0	0
I^{2}C mode address 1 (1101100)	0	1	0
I^{2}C mode address 2 (1101101)	1	1	0
I^{2}C mode address 3 (1101110)	0	0	1
I^{2}C mode address 4 (1101111)	0	1	1
Reserved (test mode)	1	0	0
Reserved (test mode)	1	0	1
Reserved (test mode)	1	1	1

In this way, 4 devices can be easily used in the same application with a single I^{2}C bus.

The internal I^{2}C registers are pre-settled in "default condition", waiting for the I^{2}C next instruction.

FDA801B can work only in I^{2}C slave mode.

5.3 Diagnostic Vcc-Gnd state

As it can be seen in *Figure 5*, after exiting from Stand-By state the device passes through Diagnostic Vcc/Gnd state.

In this state the amplifier checks the presence of the following faults:

- Shorts to ground or to Vcc
- Under-voltage (UVLO)
- Over-voltage.

FDA801B will move to the next state (Eco-mode) only if there isn't any of these faults for at least 90ms, thus avoiding any danger for the amplifier and the user system.

Meanwhile, if a stable fault is present, it will be communicated to the user via I2C after 90ms, in order to provide always only stable information about the system. In this case the device will not move to Eco-mode, waiting for the fault cause removal.

While the amplifier is in Diagnostic Vcc-Gnd state it can receive all the I2C commands, but it will actuate the PWM turn-on only when it enters in the next state: ECO-mode. This procedure guarantees that wrong or unwanted I2C communication can lead the amplifier to dangerous situation if a short to Vcc or Gnd is present.

Three conditions will move the amplifier in Diagnostic Vcc-Gnd state from any other functional state:

- Over current protection trigger
- UVLO
- Over voltage (through DUMP condition)

5.4 ECO-mode state

In ECO-mode state the amplifier is fully operative from a communication point of view and can receive and actuate all the commands given by the user.

In ECO-mode the output switching is disabled, permitting a low quiescent current and power dissipation. The device is also able to move from ECO-mode state to MUTE state, turning on the output switching, in about 1ms without experiencing POP-noise. This permits a very fast transition from ECO-mode to PLAY.

5.5 MUTE-PLAY states

The amplifier can move from ECO-mode state to MUTE state selecting "PWM-ON" via I^2C. This operation turns-on the output PWM.

From MUTE state FDA801B can move to PLAY state via "PLAY" I^2C command and returns to MUTE state from PLAY state acting on the same bit.

Transition time between mute and play states could be selected via I^2C.

Some external conditions could lead the amplifier in mute state automatically:

- Low battery mute
- High battery mute
- Thermal mute
- Hardware pin mute

Once the mute condition is no more present the FDA801B will return automatically in PLAY state, following I^2C register program set. Of course the user can decide to change the amplifier programming in the meanwhile, avoiding thus the automatic return in PLAY.

5.6 Diagnostic states

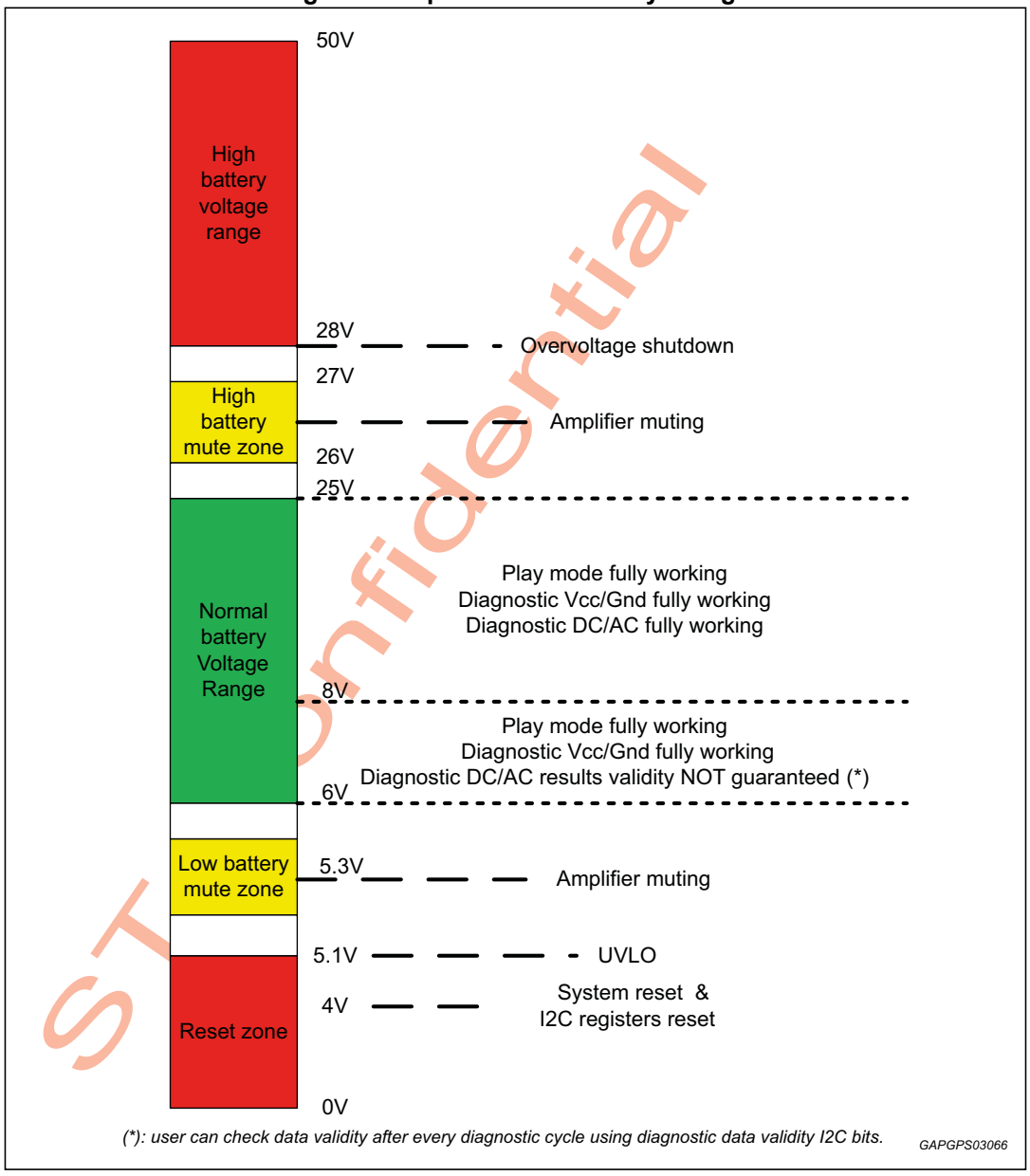
From MUTE state the user can choose among DC or AC diagnostic procedures with internal generated signal.

When the device is in PLAY the user can also activate the AC diagnostic with external signal. In this way the FDA801B will process the input signal received in order to perform a reliable AC diagnostic.

5.7 Operation compatibility vs battery

The FDA801B operation compatibility versus the battery value is reported in the figure below.

Figure 28. Operation vs. battery charge



6 Muting function architecture

FDA801B uses a mixed signal approach for muting function.

A mute command signal is a system parameter that triggers the mute function. The mute command signals are:

- “High voltage mute”: active when Vcc enters in a voltage window above the max voltage; the window is specified in the electrical parameters table.
- “Low Battery mute”: active when Vcc enters in a voltage window belove the max voltage; the window is specified in the electrical parameters table.
- “Hardware mute”: active when HWMute pin enters in the voltage window specified in the electrical parameters table.
- Thermal mute”: active when temperature enters in the temperature window above the max temperature; the window is specified in the electrical parameters table.
- I2Sws watchdog mute: active when I2Sws is missed for 3 ms. This function can be disable using I^2C bit IB13-d2.
- “I^2C Mute”: active user select mute/play I2C bits

The mute is achieved by the combination of two separated actuators, “Analog-mute” and “Digital-mute”.

6.1 Command dependence

Analog and digital mute actuators activation could be different based on the mute command signal. This is described in the following table:

Table 7. Command dependence

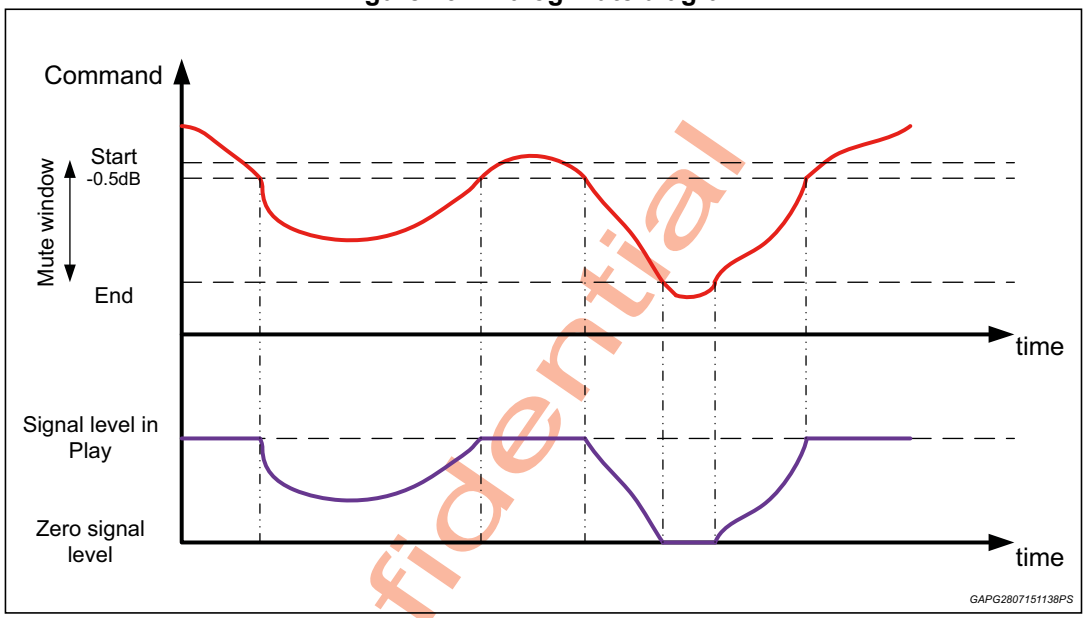
Command signal	When?	Mute	Unmute
Low Battery mute	When Vcc enters inside the low battery mute window	Mixed mute. Analog & Digital, at the same time (1)	Digital (1)
High Voltage mute	When Vcc enters inside the high voltage mute window	Analog (2)	Digital (1)
Thermal Mute	When temperature enters inside thermal mute window	Analog	Analog
Hardware Mute	When hardware pin voltage enters inside its mute window	Mixed mute. Analog & Digital, at the same time(1)	Digital (1)
I2Sws missing	When I^2C bit "watchdog on I2Sws" is selected (IB13-d2)	Digital	Digital
I2C Mute	When I^2C mute bits are selected	Digital	Digital

1. User can decide to disable Digital-Mute/Unmute using bit IB13-d6; in this case in all the conditions, (except I^2C Mute), the Mute/Unmute will be purely Analog.
2. Fast attenuation with threshold transition <15 µs.

6.2 Analog-Mute

Analog-Mute senses when the mute command signal transits across the muting-window and attenuates the output signal proportionally to the input level inside the muting-window.

Figure 29. Analog-Mute diagram



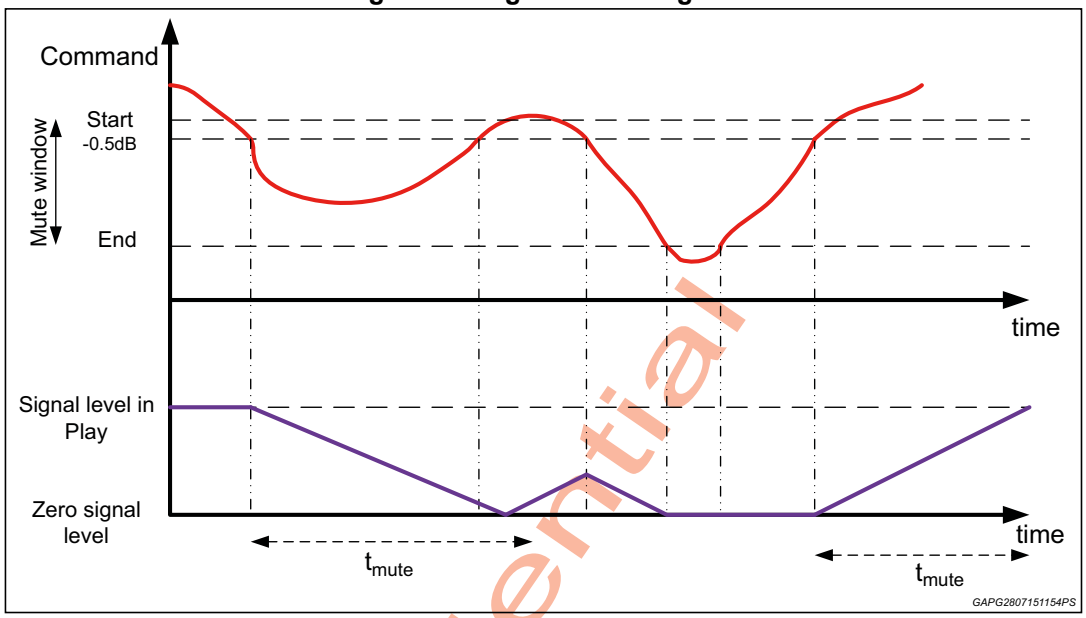
6.3 Digital-Mute

Digital-Mute acts on the digitally elaborated output signal attenuating it gradually to zero with digital steps in a pre-defined time frame (t_{mute}). The muting time, (t_{mute}), can be selected by I^2C (IB3-d7,d6). There are two different actions performed by the digital-mute function:

Mute: it starts when Analog-Mute attenuation becomes higher than 0.5 dB. It ends after t_{mute}.

UnMute: it starts when Analog-Mute attenuation becomes lower than 0.5 dB. It ends after t_{mute}, regardless of Analog-mute attenuation. In case Analog-Mute attenuation gets higher than 0.5 dB during the unmute ramp the system will start the mute from the signal level reached.

Figure 30. Digital-Mute diagram



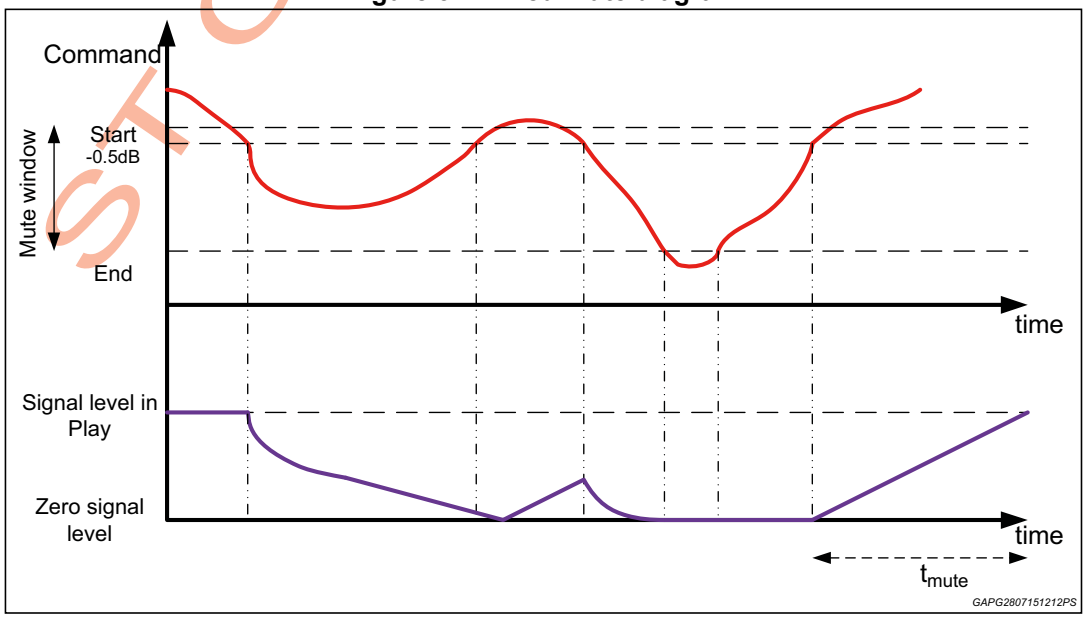
Note: in case of I^2C mute the Digital-mute actuation does not follow Analog-mute level but only the I^2C command.

6.4 Mixed mute advantages

The mixed mute approach, analog-mute and digital-mute at the same time, is the superposition of the two mute actuators.

Here below the example of the previous pages with mixed mute:

Figure 31. Mixed mute diagram



There are several advantages in terms of robustness in a multitude of different situations in which Analog-Mute or only Digital-Mute standalone is not robust. The effects are more visible when the mute command signal variation is faster than Digital-Mute time.

Here below 2 examples:

Figure 32. Analog-Mute / Digital-Mute standalone no robust (example 1)

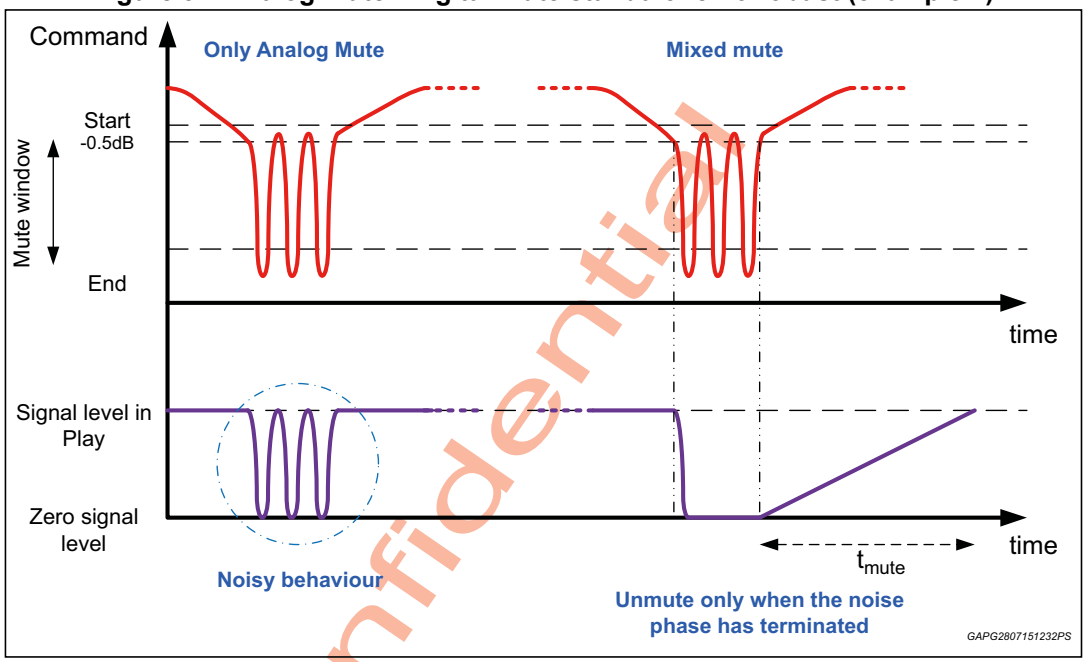
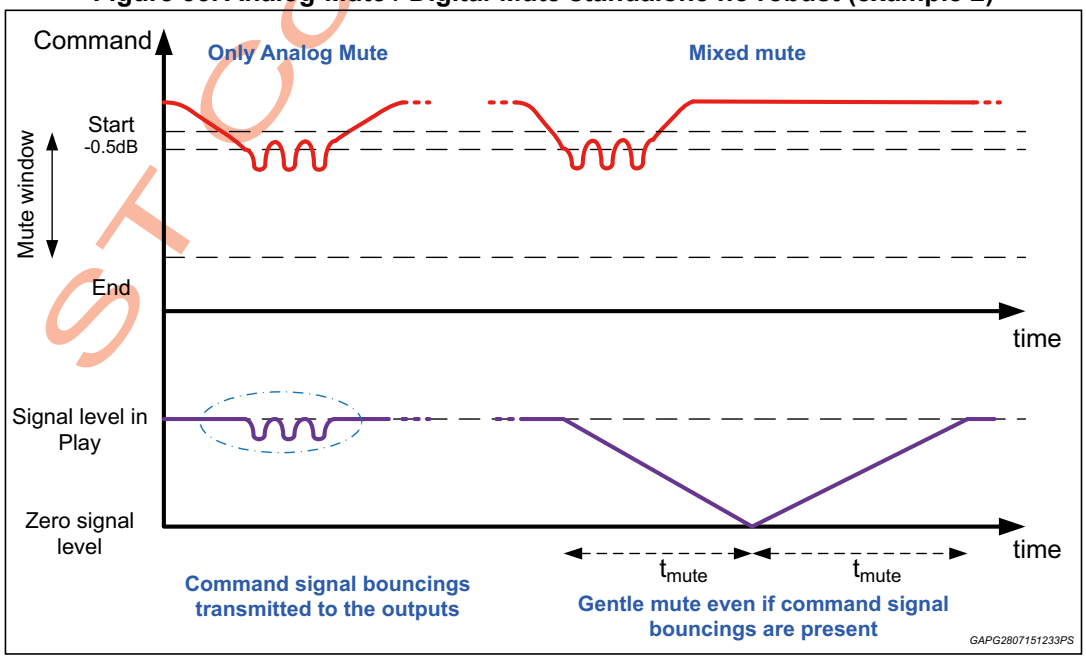


Figure 33. Analog-Mute / Digital-Mute standalone no robust (example 2)



In any moment the user can disable the Digital-mute, acting on I^2C bit Dx-dy, obtaining the standard Analog-mute function.

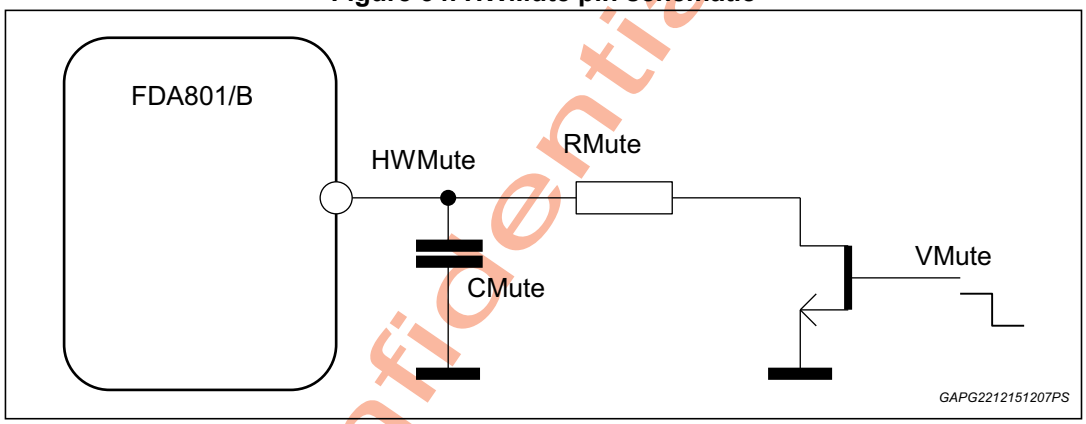
6.5 Hardware mute pin

The pin “HWMute" (pin 63) acts as mute for all the channels. The device is muted when this pin is low, while it is in play when this pin is high (low/high threshold in electrical characteristics table).

Inside the device, connected to this pin a pull-up current generator puts the device in play if left floating. A 5 V internal clamp limits the Mute pin voltage. If not used, this pin should remain floating.

To drive the Mute pin to get a hardware mute an external pull-down open drain ,5 V tolerant is needed. (See *Figure 34*), RMute must be < 100 kΩ

Figure 34. HWMute pin schematic



7 Diagnostics functional description

The FDA amplifiers family provides diagnostic function for detecting several possible faults conditions.

Any warning information will be stored in the I^2C interface and kept until the first I^2C bus reading operation. Here reported the FDA801B's diagnostic features:

- Short to VCC/GND faults
- Load detection, both DC and AC diagnostic
- Under/over voltage events
- Chip over temperature
- Digital input offset
- Output offset
- Output clipping

7.1 Load detection & short to Vcc/Gnd detection

A new concept of load diagnostic is provided by FDA family, specially designed for automotive applications. Advanced digital algorithms provide extremely reliable results.

The FDA family diagnostic is performed in three phases and can be classified in:

- Short to Vcc/Gnd diagnostic
- DC load diagnostic
- AC load diagnostic

7.1.1 DC and AC diagnostic

In FDA801B every channel could run its own DC or AC diagnostic independently from the other channels.

This flexibility gives to the µP the possibility to analyze one single channel meanwhile the other channels are playing.

If diagnostic start commands are sent to all 4 channels in a single I^2C instruction the 4 diagnostics will be performed simultaneously.

If the diagnostic start commands are sent to all 4 channels in different instants the 4 diagnostics will be performed sequentially.

Diagnostic enable

DC and AC diagnostic can be run independently by means of two I^2C bits for each channel: "Start Diag DC" and "Start Diag AC".

Once AC or DC diagnostic I^2C bits are set to "1" the amplifier channel performs the selected diagnostic.

At the end of the diagnostic cycle the "Start Diag DC" or "Start Diag AC" instruction bits are set back to "0" by the device itself.

Diagnostics can be launched only if the channel is in "MUTE" state.

Diagnostic sequencing and some special cases

If both "Start Diag DC" and "Start Diag AC" instruction bits are set to "1" the amplifier channel will perform first DC diagnostic and then AC diagnostic.

If "Start Diag DC" or "Start Diag AC" bits are set to "1" while the channel is not in "MUTE" state, (for example: "PLAY" state or "Eco-mode" state), the channel will perform the selected diagnostic as soon as it enters in "MUTE" state.

The DC diagnostics could be launched at the same time on all 4 channels or separately.

The AC diagnostics could be launched at the same time on all 4 channels or separately.

However the user should avoid these two special cases:

a) DC diagnostic on channel "X" and AC diagnostic on channel "Y" at the same time, (with X different from Y).

b) AC diagnostic with INTERNAL signal on channel "X" and AC diagnostic with EXTERNAL signal on channel "Y" at the same time (with X different from Y).

If the amplifier channel is in "Eco-mode" and I2C instructions for PWM ON + DIAG DC + DIAG AC + PLAY are given at the same time the channel will perform the following sequence automatically:

1. turn on power stage
2. perform DC diagnostic
3. perform AC diagnostic
4. enter PLAY mode

Diagnostic start conditions

Diagnostic signal is generated and test is performed only if:

1. Channel is in MUTE state.
2. DC or AC (or both) test enable bits are set from '0' to '1'.
3. The channel has power stage ON
4. The PWM modulation is "In phase"
5. Device is NOT kept in mute by means of the dedicated hardware pin

Relation with phase modulation

Diagnostic is performed only with PWM "In phase" modulation.

"Out of phase" modulation, if desired, must be selected after the AC-DC load diagnostic execution in order to avoid pop noise.

If amplifier is in "PLAY" state and user wants to launch the diagnostic the amplifier should be set in "MUTE" with PWM "In Phase" modulation by means of I^2C bits.

Relation with short circuit protection activation

After a short circuit protection intervention amplifier is set automatically in a protected status during which "Short to Vcc/Gnd" diagnostic is performed.

At the end of "Short to Vcc/Gnd" diagnostic, if no shorts to Vcc/Gnd are present on the outputs, amplifier will run DC and/or AC diagnostic only if the corresponding "Start Diag DC" and/or "Start Diag AC" bit are set to "1". Otherwise the amplifier will go back to play without performing diagnostic cycles.

After the diagnostic completion "Start Diag DC" and/or "Start Diag AC" bits are set back to "0" by the amplifier.

7.1.2 Short to Vcc/GND diagnostic

The short to Vcc/GND diagnostic performs the detection of:

- "Hard" and "soft" short to Vcc
- "Hard" and "soft" short to Gnd

Timing

Short to Vcc/Gnd diagnostic cycle duration is 90ms.

If a short to Vcc/Gnd is not stable during diagnostic cycle the channel will remain in "short to Vcc/Gnd diagnostic" state until a fault or non-fault condition is stable for at least 90ms.

This special function avoids wrong communication in case of disturbs caused by mechanical stress applied to the speaker (e.g. car door closing).

Short to Vcc/Gnd diagnostic automatic start

Short to Vcc/Gnd diagnostic starts automatically after stand by and every time an overcurrent event occurs at the amplifier channel outputs.

Results communication and I2C control

After 90 ms of diagnostic with stable fault/non-fault conditions there are two different situations:

a) Fault is present: the channel will communicate the short presence by means of I2C data bytes, (2 bits for each channel). The amplifier channel will remain in short to Vcc/Gnd diagnostic until the short is removed.

b) Fault is not present: "Short to Vcc/Gnd" diagnostic ends and the channel can actuate I2C commands. After short to Vcc/Gnd diagnostic ends without faults present, if I2C commands are already set the amplifier will execute them immediately.

7.1.3 DC diagnostic

The load presence test is usually affected by noise, due for example to supply voltage variations or mechanical stress induced on the speaker (e.g. car door closing). FDA amplifiers family provides a highly reliable and noise immune load diagnostic algorithm, with self-generated stimuli.

There are two different DC diagnostic modes: SPEAKER MODE, LINE DRIVER MODE.

SPEAKER mode

Load range:

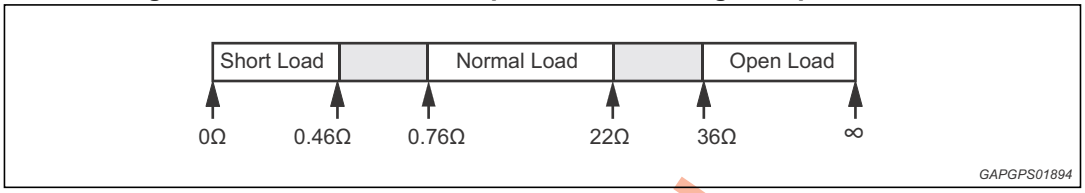
the load range can be configured based on some I^2C bits (IB3[2,1] - IB12[7,6] - IB11[6]). For an extensive description of the feature, please refer to the FDA801B device family Diagnostic user manual.

In the following example it is shown the case when IB3[2,1]=00; IB12[7,6]=11, IB11[6]=0.

From 0.76 Ω to 22 Ω the load value is considered as normal load.

When the detected value is above 30 Ω amplifier outputs are considered open, while values below 0.5 mΩ are considered as a short across the outputs (see *Figure 35*).

Figure 35. DC load detection precision and range in speaker mode



Timing: DC diagnostic pulse has maximum time duration of 250 ms.

Results communication: For loads above 36 Ω or below 0.46 Ω an "open load" or "short load" message respectively will be displayed via I^2C.

LINE DRIVER mode

Load range in LINE DRIVER mode:

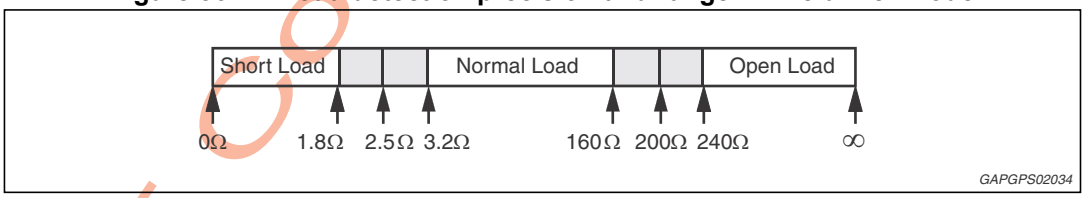
the load range can be configured based on some I^2C bits (IIB12[7,6] - IB11[6]). For an extensive description of the feature, please refer to the FDA801B device family diagnostic user manual.

In the following example it is shown the case when IB12[7,6]=00, IB11[6]=1.

From 3.2 Ω to 160 Ω the load value is considered as normal load.

When the detected value is above 240 Ω amplifier outputs are considered open, while values below 1.8 Ω are considered as a short across the outputs (see figure below).

Figure 36. DC load detection precision and range in line driver mode



Timing: DC diagnostic pulse has maximum time duration of 250 ms.

Results communication: For loads above 240 Ω or below 1.8 Ω an "open load" or "short load" message respectively will be displayed via I^2C.

7.1.4 AC diagnostic

AC diagnostic checks the accidental disconnection of tweeters in a 2-way speaker and, more in general, the presence of capacitive (AC) coupled loads.

FDA801B provides an accurate AC diagnostic insensible to LC filter value thanks to a patented algorithm that is based on the measurement of both magnitude and phase of the load connected: this makes AC diagnostic able to correctly detect even very small AC load impedance variations in module after tweeter disconnection.

As a basic description, the AC diagnostic use a sinusoidal stimulus to verify if the tweeter is present measuring the impedance connected to the outputs and giving a result according to a threshold.

The basic threshold is 25 Ω ± 20%.

The tweeter is considered present if the load impedance is below 25 Ω ± 20% (while, if higher than this threshold the tweeter is considered not connected).

AC diagnostic can be performed both with internally generated signal and with externally generated signal.

However, the result of the AC diagnostic test (AC load impedance and consequently the threshold for connected/disconnected tweeter) is influenced by the following register settings:

- Normal/parallel operation (IB1[7-6])
- Sampling and PWM frequencies (IB0[3-2])
- Low-side full/half – Differential or single ended bridge (IB3[5-3])
- Diagnostic current-voltage phase delay offset compensation (IB9-12 [5-0])
- LC filter setup (IB14[3:1])
- D/A conversion level control (IB3[2:1])
- Overcurrent setting (IB11[6] and IB12[7-6])
- Low/high current sensing (IB13[7]).

Moreover the AC diagnostic test performed using an externally generated signal is dependent also from the configuration of the Voltage gain Gv (IB5-8[6-5]) register. In case of AC diagnostic test using the internally generated signal, voltage gains Gv (IB5-8[6-5]) are internally controlled during the test, so the result is independent from Gv setting.

For an extensive description of the feature, please refer to the FDA801 device family Diagnostic user guide.

Internally generated signal

FDA801B AC diagnostic creates an optimized signal for load analysis. The signal is a high frequency amplitude-modulated sine wave.

During the AC diagnostic with internal signal the positive output is automatically fixed at half Vcc in order to enhance diagnostic precision.

This function is commonly referred as ‘CMC in single ended mode’, (CMC = common mode control).

The user can switch from the automatic ‘CMC in single ended mode’ setup to ‘CMC in differential mode’ acting on IB3-d5, d3: IB3-d5 = ‘1’, IB3-d3 = ‘1’. This selection is suggested in case of external LC filter with coupled inductors.

Please note that IB3-d5,d3 selection over-writes standard CMC controls. Therefore it is highly suggested to use this selection only if it is needed and only during diagnostic.

In detail, the IB3 D[5:3] configuration selection table is:

Table 8. IB3 D[5:3] configuration

IB3[5]	IB3[4]	IB3[3]	Function
0	x	x	Automatic control
1	0	0	Full power - diff. driving
1	0	1	Full power - single ended driving
1	1	0	Half power - diff. driving
1	1	1	Half power - single ended driving

where automatic control means:

- during play and AC external signal test: Full power and differential driving
- during DC test: half power and differential driving
- during AC internal signal test: Half power and single ended driving

To be noted that switching from differential to single ended driving (and viceversa) may result in a click noise if the output voltage is not zero. When half power is selected, overcurrent threshold is halved.

The internal generated signal has a frequency that varies according to PWM switching frequency selected (IB0-d2,d3).

Table 9. Frequency according to PWM switching frequency

Parameter	Value						Unit
Fs	48	48	48	44.1	44.1	44.1	kHz
Fpwm	336	384	432	308.7	352.8	396.9	kHz
Fsignal	21	24	27	19.29	22.05	24.81	kHz

Timing: AC diagnostic pulse has maximum time duration of 30 ms band.

7.2 Diagnostic time-line diagrams

Figure 37. Case 1: DC diagnostic before turn on

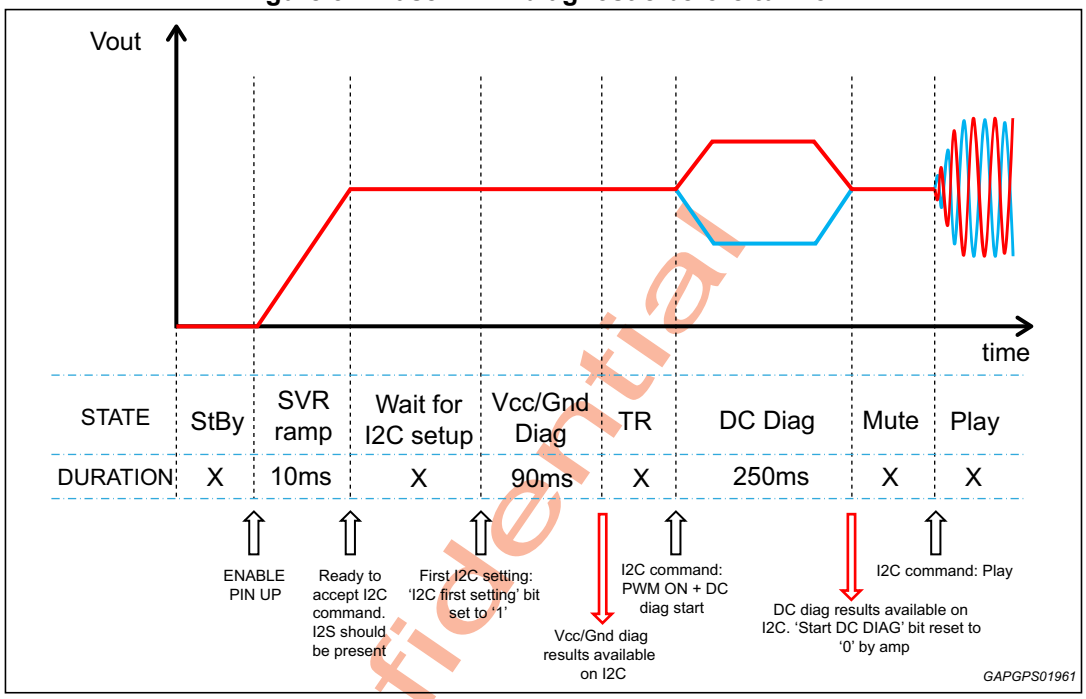


Figure 38. Case 2: AC diagnostic before turn on

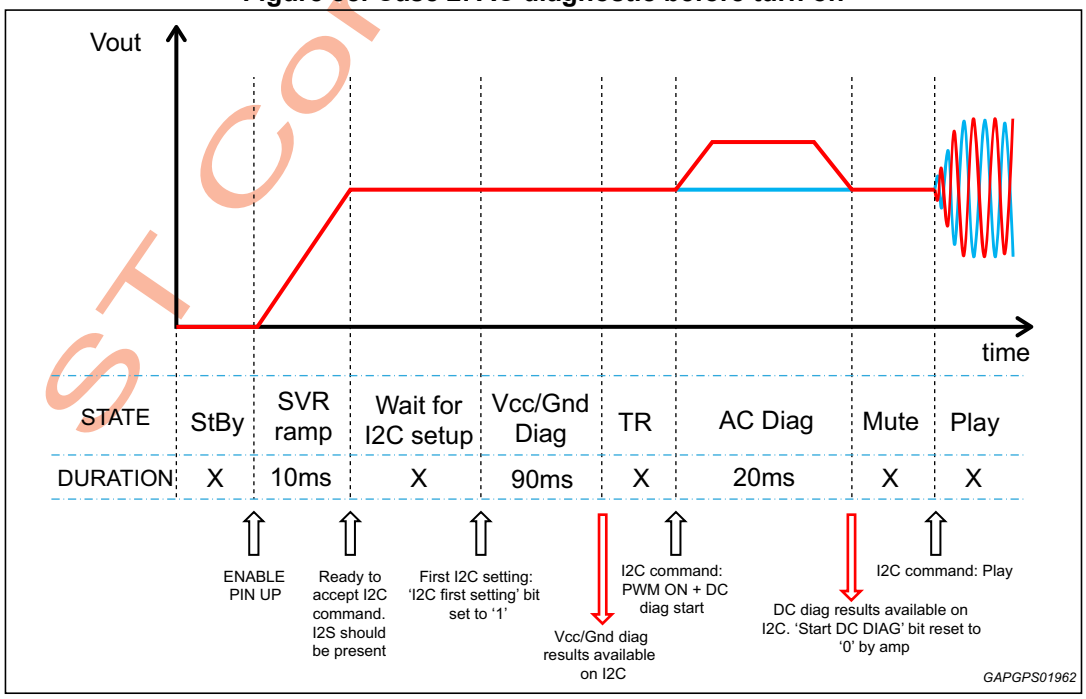
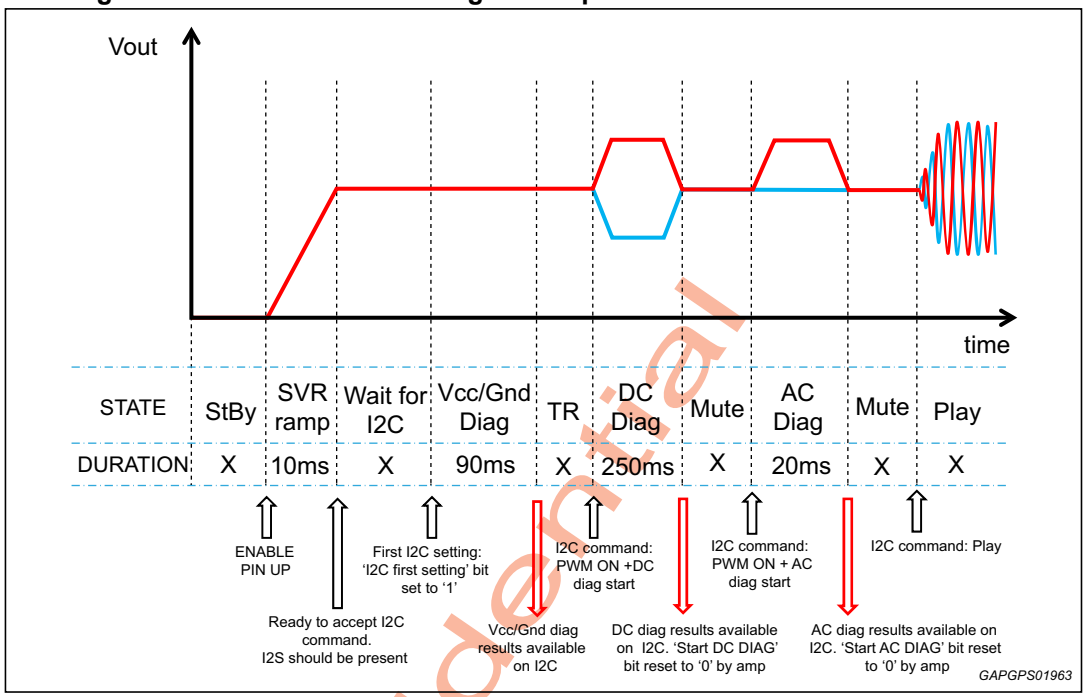
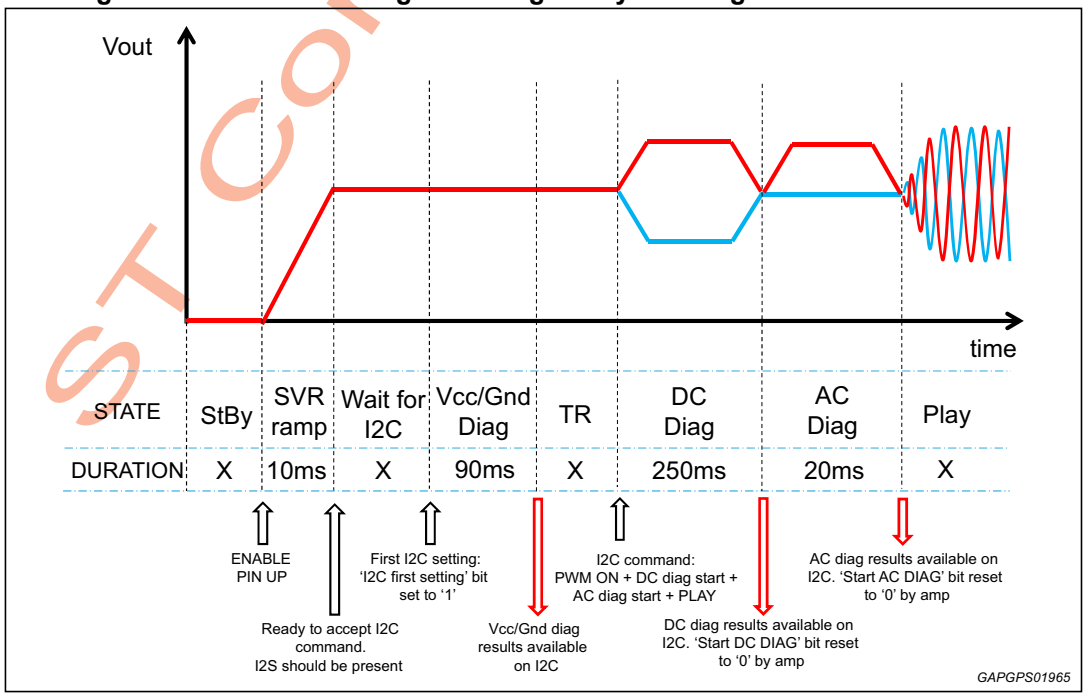


Figure 39. Case 3: DC & AC Diag with separated commands before turn on



Note: This sequence will imply a 4% deviation of diagnostic results between CH1/3 and CH2/4. More details available in the FDA801 Diagnostic user guide.

Figure 40. Case 4: DC Diag + AC Diag + Play in a single I²C bus instruction



Note: This sequence will imply a 4% deviation of diagnostic results between CH1/3 and CH2/4.

Figure 41. Case 5: Short to VCC present at turn on

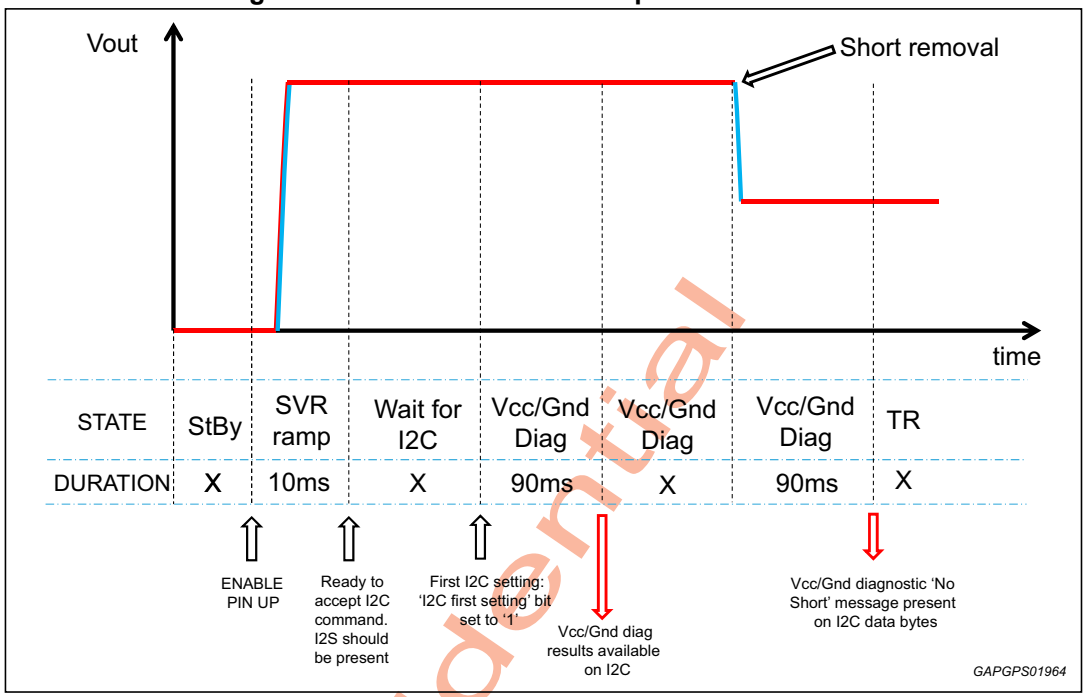


Figure 42. Case 6: DC and AC diagnostic in mute

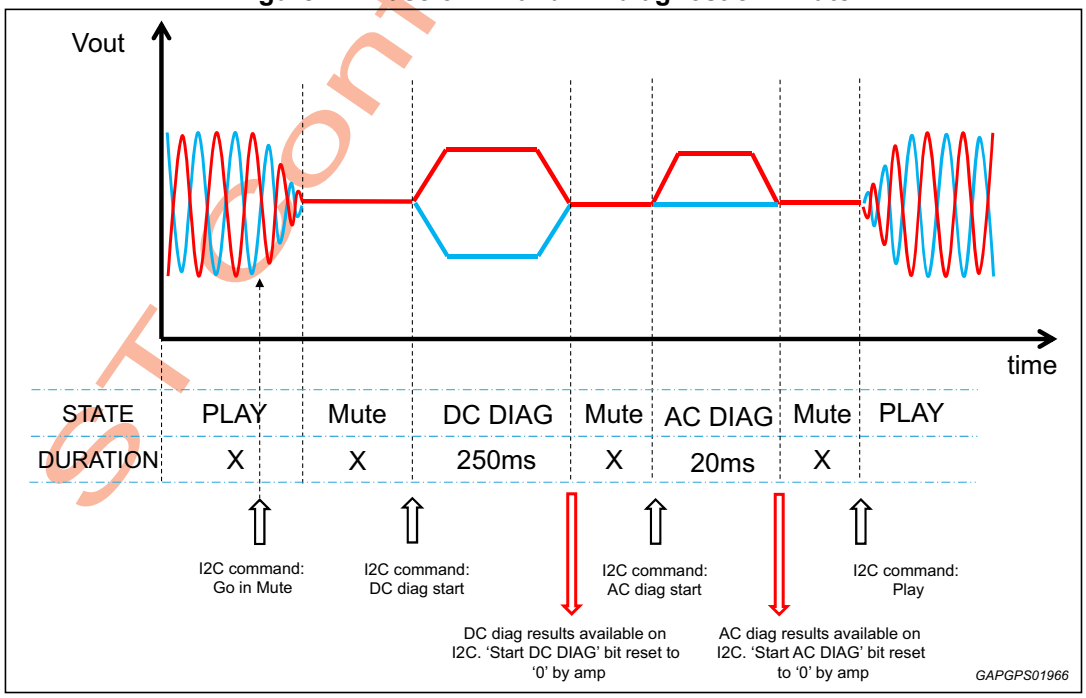


Figure 43. Case 7: Short circuit protection activation – Short to Vcc present

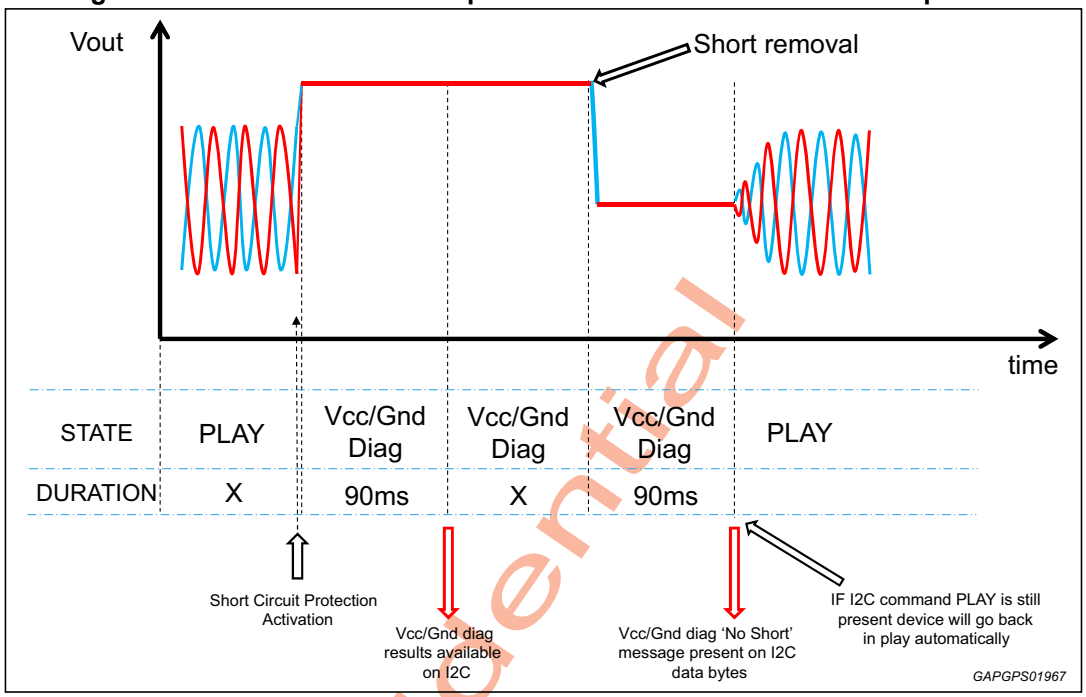
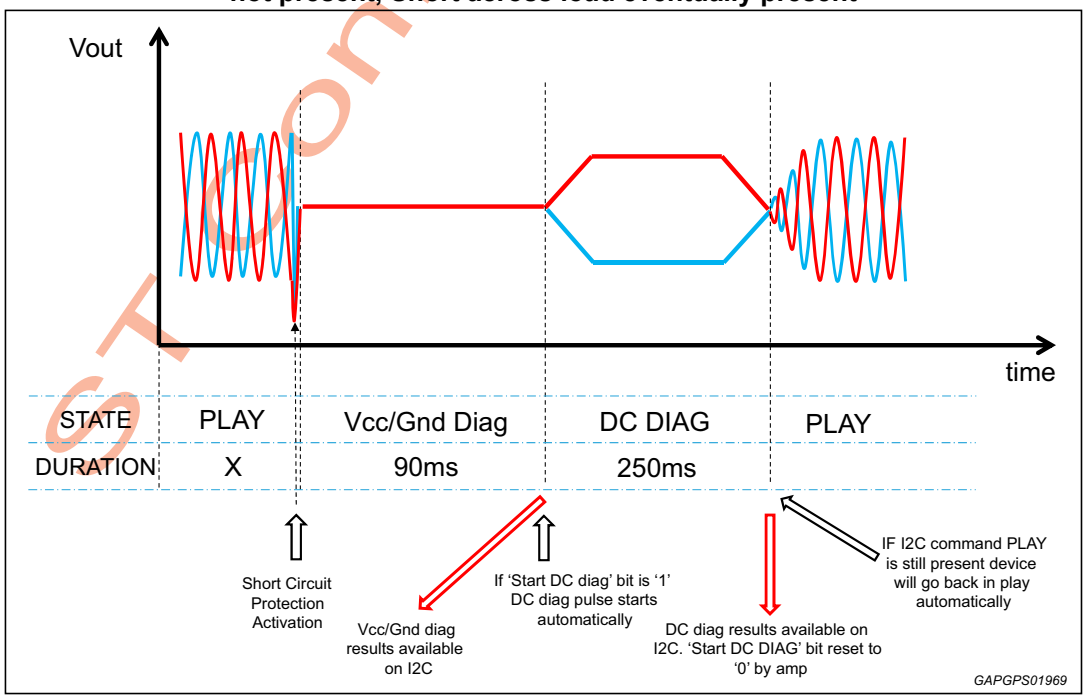


Figure 44. Case 8: Short circuit protection activation and DC diag. Short to Vcc/Gnd not present, Short across load eventually present



7.3 Digital impedance-meter (DIM)

FDA801B implements an innovative feature: a digital impedance-meter (DIM) embedded in the audio power amplifier.

More specifically it provides:

- The load resistance value after "DC diagnostic" state: DIM DC
- The magnitude and phase value after "AC diagnostic with internally generated signal" state: DIM AC

This feature goes beyond the standard failure present/not-present recognition of the diagnostic function.

The user µC can elaborate the information provided and use them for implementing a large set of functions (output equalization), without the need of dedicated external components.

7.3.1 DIM results communication via I^2C

DIM results are communicated via I2C data register from DB8 to DB19.

The DIM AC is activated running the AC diagnostic and the results are stored in modulus and phase.

Magnitude is stored in: DB9 (CH1), DB12 (CH2), DB15 (CH3), DB18 (CH4).

Phase is stored in: DB10 (CH1), DB13 (CH2), DB16 (CH3), DB19 (CH4)

The DIM function is automatically activated running the DC diagnostic and the results are stored in:

DB8 (CH1), DB11 (CH2), DB14 (CH3), DB17 (CH4).

The load resistance/AC-magnitude values written in DBx register are represented by 7 significant bits and 1 bit as a multiplier, according to the following format representation:

D7	D6	D5	D4	d3	D2	D1	D0
0 -> M=0.1 1 -> M=1.0	C[6]	C[5]	C[4]	C[3]	C[2]	C[1]	C[0]

The resistance could be calculated using this formula:

$$R = M \times K \times C[6 \div 0] \quad [\Omega]$$

A similar formula is valid for AC magnitude.

The parameter K depends on I^2C configurations, device configurations, on the model used for the resistance estimation (in case of DC DIM), etc.

Tables to calculate the K parameter (both for DC DIM and AC DIM) based on I^2C configurations are included in the Diagnostic user guide.

The phase value (in DIM AC) is given in twos complement representation and expressed in degree in a range from -127° to +127°.

The description of the procedure needed to obtain an estimation of the phase of the AC load is included in the FDA801B Diagnostic user guide as well.

7.4 Input offset detector

Input offset detector aim is to avoid any possible offset that could come from the audio signal source through I2S/TDM input stream.

For this purpose the FDA801 input offset detector performs an evaluation of the input signal and calculates if an offset with values higher that -18dBFs is present. If an input offset is detected the offset detector flag DB0-d7 goes to ‘1’.

Moreover, if high pass filter function is selected by means of IB1-d2, the FDA801 will eliminate the input offset giving a complete robustness to any disturbance or malfunction coming from the previous audio chain blocks.

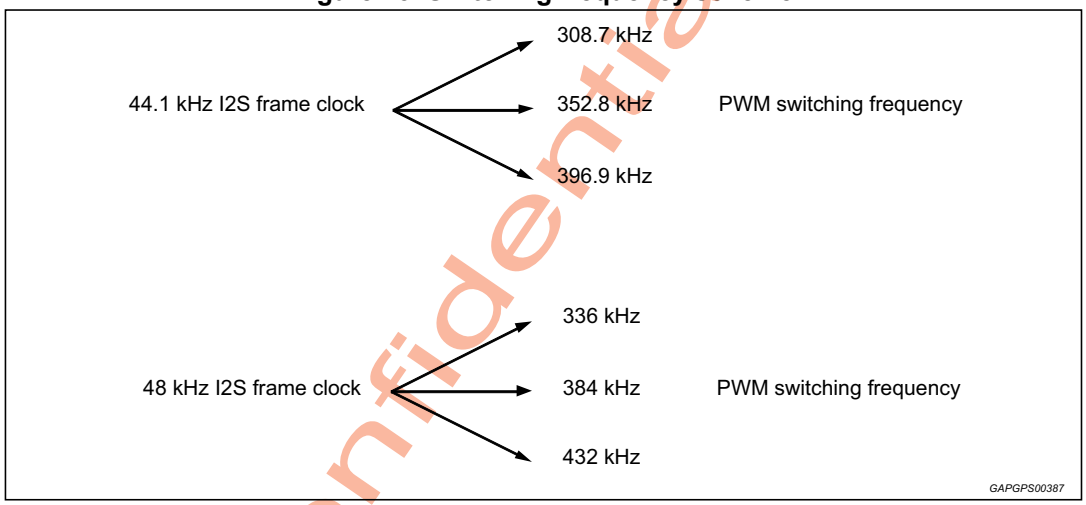
The input offset detector and high-pass filtering can be used during PLAY mode.

8 Additional features

8.1 AM operation mode

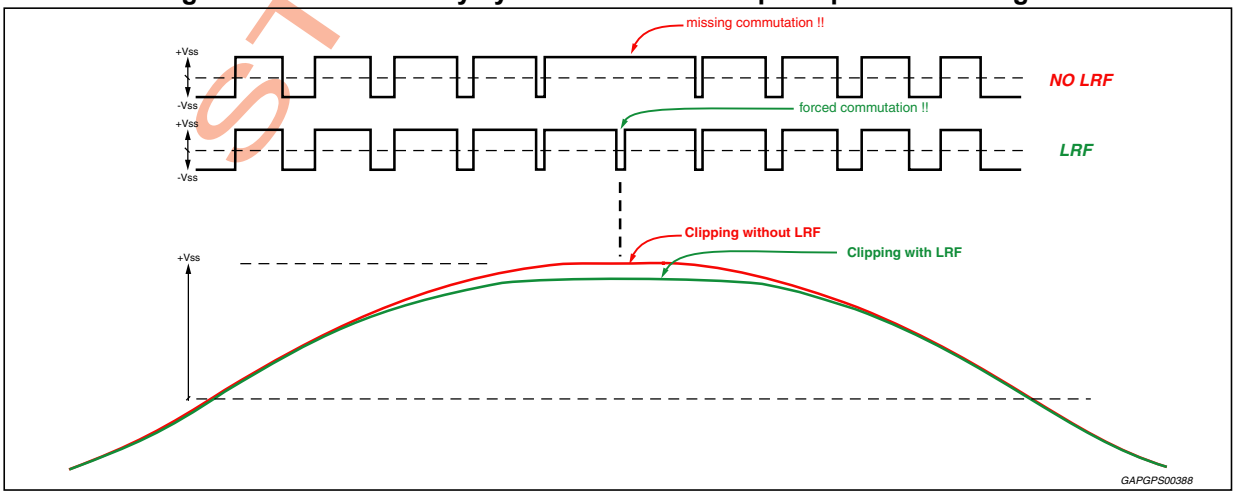
In order to avoid EM interferences when the radio is tuned on an AM station is advisable to exploit special functions provided by FDA801B. The most suitable switching frequency can be set through an I^2C interface, depending on the AM station selected by the tuner. The switching frequency can be selected just in case the input signal sampling frequency is 44.1 kHz or 48 kHz.

Figure 45. Switching frequency scheme



Actually, the spectrum of the output PWM wave can be controlled in AM band just in case it is possible to fix the switching frequency, in other words without skipping any power stage commutation (typical phenomenon for a class D amplifier close to the clipping). FDA801B offers an additional control called LRF (low radiation function). This I^2C option assures a minimum duty cycle for the PWM output square wave avoiding any missing pulses.

Figure 46. Minimum duty cycle for the PWM output square wave diagram



Consequently, by limiting the PWM duty cycle, a limitation of the output power occurs (the output power in case of usage of LRF function decreases about 10% @ 1% THD).

8.2 Noise gating

Noise gating is an automatic noise reduction feature that activates when output signal reaches inaudible levels.

When input signal levels falls below -102dBFs the system activity is automatically optimized in order to limit the output noise level as much as possible and permits the full audio chain to exploit very low noise level on the output speakers.

The noise gating process has a 100 ms observation time before turning on, in order to avoid spurious activations.

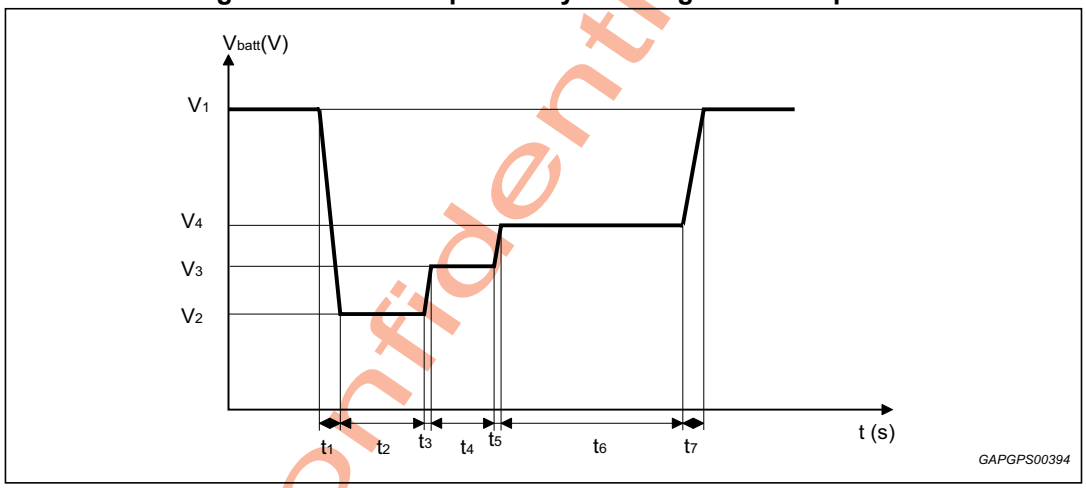
The feature is enabled by default and can be disabled selecting IB1-d5.

9 Low voltage (‘start stop’) operation

The most recent OEM specifications require automatic stop of car engine at traffic light, in order to reduce the emission of polluting substances. The engine re-start induces cranks on the battery voltage that bring the supply down to 6 V (Fig. 47-48). FDA801B allows a continuous operation when battery applied to the IC falls down to 6 V, without producing pop noise, thus supporting this new specification (the maximum output power at 6 V will be reduced according to the P_{out} curve).

Battery cranking curves supported by FDA801B are shown below, indicating the shape and durations of allowed battery transitions.

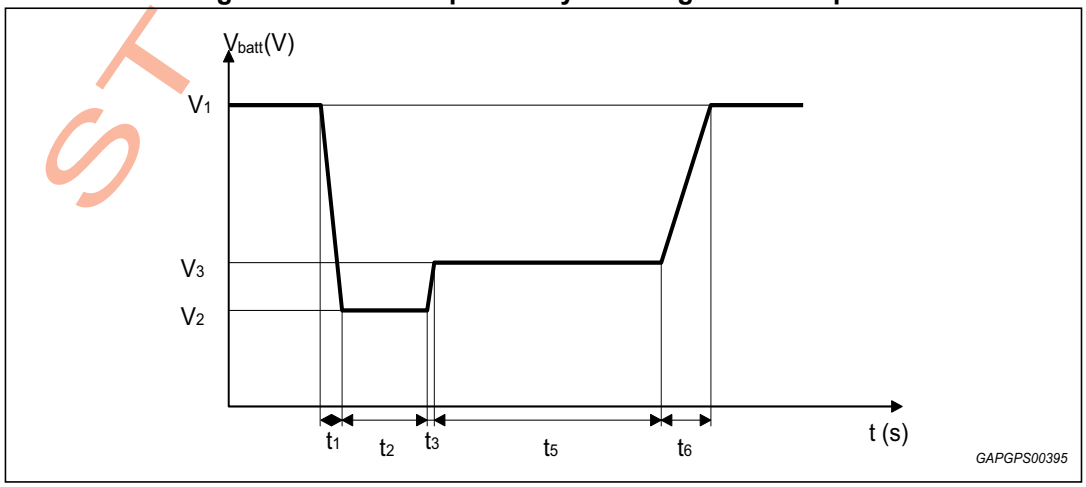
Figure 47. “Start-stop” battery cranking curve sample 1



V1 = 12 V; V2 = 6 V; V3 = 7 V; V4 = 8 V

t1 = 2 ms; t2 = 50 ms; t3 = 5 ms; t4 = 300 ms; t5 =10 ms; t6 = 1 s; t7 = 2 ms

Figure 48. “Start-stop” battery cranking curve sample 2



V1 = 12 V; V2 = 6 V; V3 = 7 V

t1 = 2 ms; t2 = 5 ms; t3 = 15 ms; t5 = 1 s; t6 = 50 ms

10 I²S bus interface

FDA801B accepts the I²S standard format that can be Time Division Multiplexed.

I²S bus is made up of four lines: the clock lines (SCK), the sync. line (WS) and two serial data lines (SD1 and SD2) where 32 bits words are sent.

Note that only the first 24 bits received per word are processed and that WS frequency has to be always the same as audio sampling frequency fs. Then, the device can support a 24-bits configuration just inserting the significant bits in the first part of the word and inserting 8 zeros at the end.

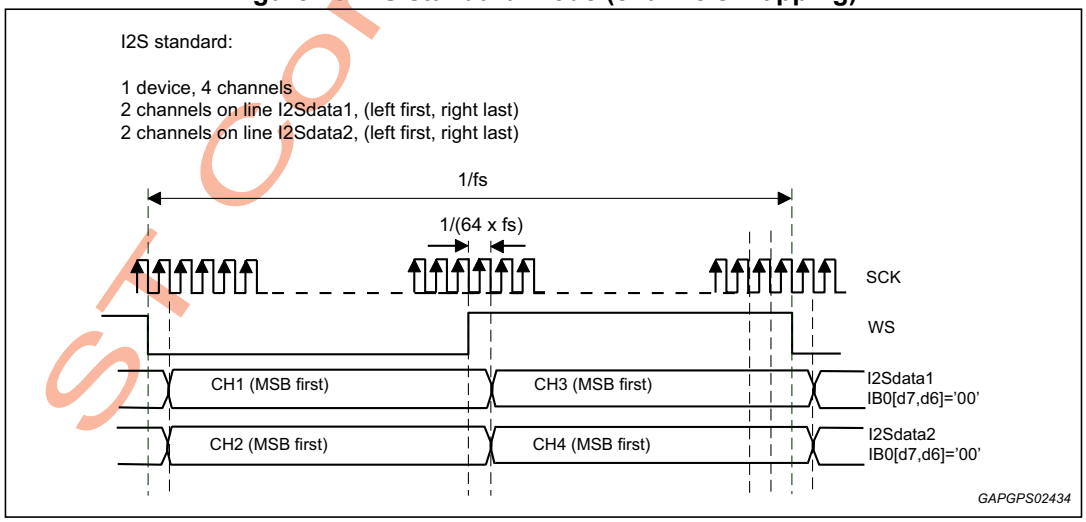
According with I²C settings, audio signals can be sent with the following data format:

- I²S standard
- TDM 4 channels
- TDM 8 channels mode 1
- TDM 8 channels mode 2

10.1 I²S standard description

With I²S standard format, data are sent as shown in *Figure 49*, where SCK frequency (f_{SCK}) is equal to 64f_s. Data LEFT1, LEFT2, RIGHT1 and RIGHT2 are respectively mapped into channels 1, 2, 3 and 4.

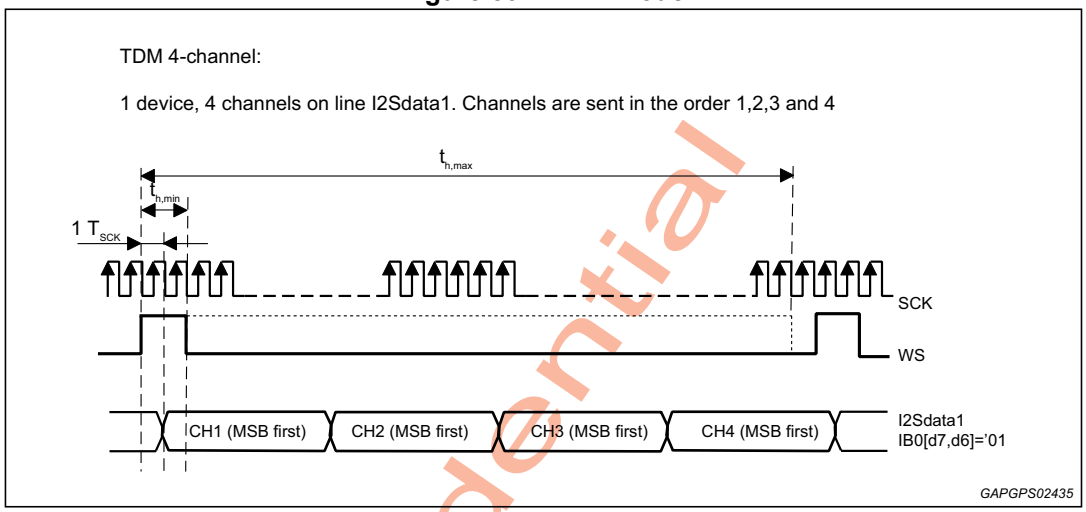
Figure 49. I²S standard mode (channels mapping)



10.2 TDM 4-channel

With TDM 4-channel mode FDA801B reads only I²Sdata1 data line where all 4 channels have to be sent as shown in *Figure 50*; f_{SCK} must be $128 f_s$.

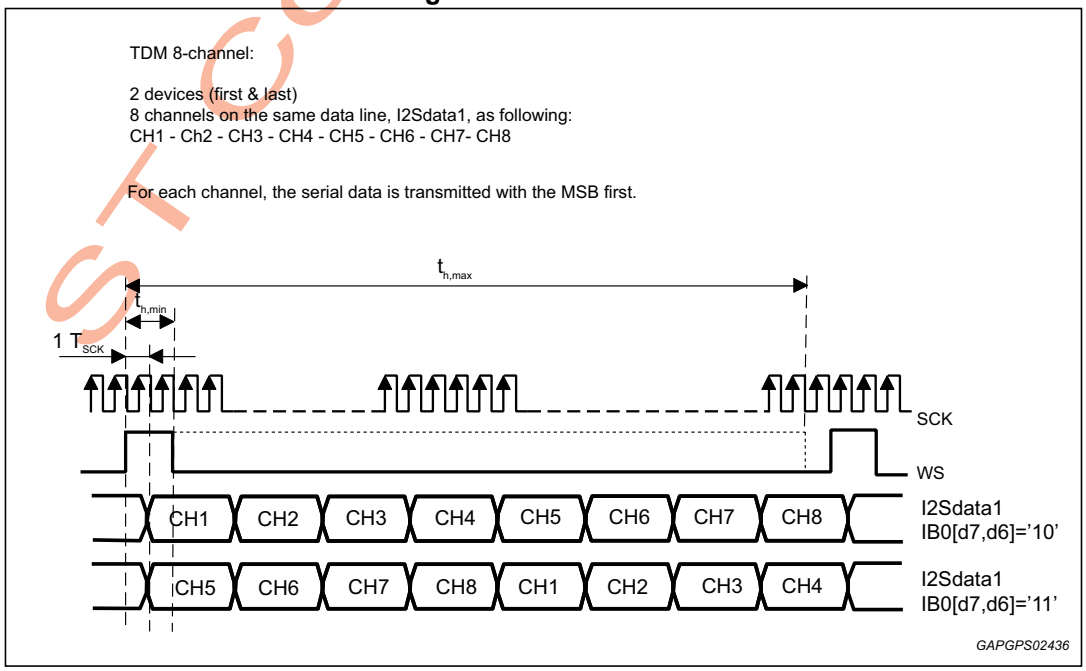
Figure 50. TDM4 mode



10.3 TDM 8-channel mode 1 and 2

With TDM 8-channel mode 1 FDA801B reads only I²Sdata1 data line, where, as shown in *Figure 51*, 8-channel data are sent; f_{SCK} must be equal to $256 f_s$.

Figure 51. TDM8 mode



Note: In TDM 4-channel and TDM 8-channel the I2Sdata2 line is not used. It should be connected to DGND.

10.4 Timings requirements

Figure 52. Audio interface timing

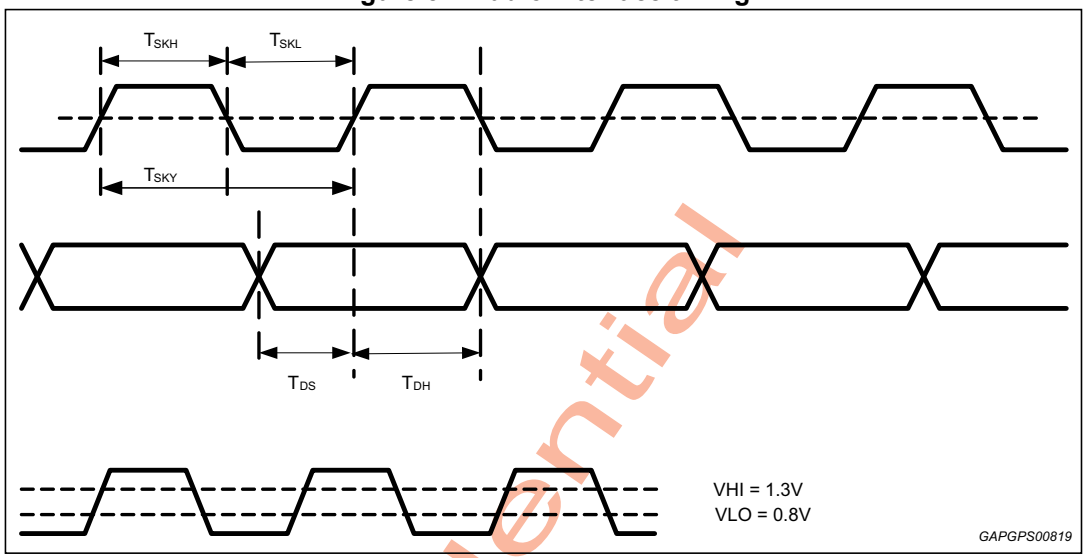


Table 10. I²S interface timing

Symbol	Parameter	note	min	max	unit
Fsck0	SCK (bit clock) frequency	-	-	24.576	MHz
-	SCK (bit clock) frequency tolerance	-	0.9Fsck0	1.1Fsck0	MHz
Tsck	SCK period	-	40.69	-	ns
-	SCK duty cycle	-	40	60	%
Tsckh	SCK high time	-	15	-	ns
Tsckl	SCK low time	-	15	-	ns
-	SCK transition time	-	-	6	ns
-	WS (word select) frequency	-	-	192	kHz
Twsh	WS high time	I2S standard	1 Tsck	63 Tsck	ns
Twsh	WS high time	TDM 4-channel	1 Tsck	127 Tsck	ns
Twsh	WS high time	TDM 8-16-channel	1 Tsck	255 Tsck	ns
Tws	WS setup time	-	8	-	ns
Twh	WS hold time	-	8	-	ns
Tds	SD13 SD24 (data inputs) setup time before SCK rising edge	-	8	-	ns
Tdh	SD13 SD24 (data inputs) hold time after SCK rising edge	-	8	-	ns

10.5 Group delay

In FDA801B the group delay is variable with the fs used, (and selected via I²C), according to the following table:

Table 11. Group delay dependency from input sampling frequency

Input sampling frequency (fs)	Delay
44.1 kHz	430 µs
48 kHz	400 µs
96 kHz	20 µs
192 kHz	10 µs

11 I²C bus interface

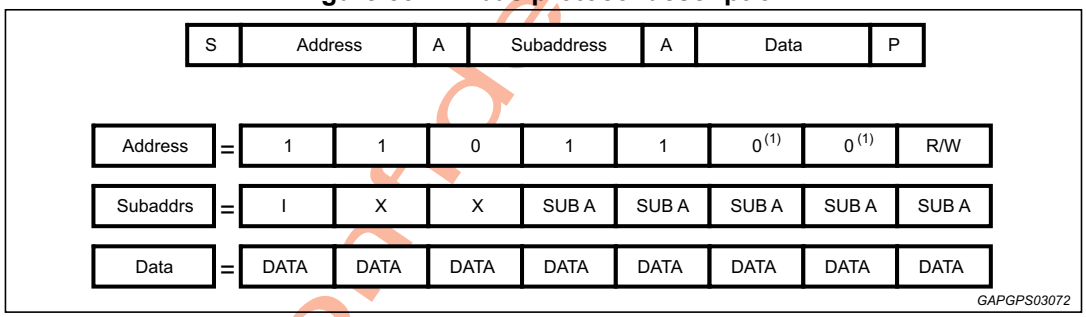
Data transmission from microprocessor to the FDA801B and viceversa takes place through the 2 wires I²C bus interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected).

When I²C bus is active any operating mode of the IC may be modified and the diagnostic may be controlled and results read back.

The protocol used for the bus is depicted in *Figure 53* and comprises:

- a start condition (S)
- a chip address byte (the LSB bit determines read/write transmission)
- a subaddress byte
- a sequence of data (N-bytes + acknowledge)
- a stop condition (P)

Figure 53. I²C bus protocol description



1. The I²C addresses are:
   Address 1 = 1101100
   Address 2 = 1101101
   Address 3 = 1101110
   Address 4 = 1101111

Description:

- S = Start
- R/W = '0' => Receive-Mode (Chip could be programmed by µP)
- I = Auto increment; when 1, the address is automatically incremented for each byte transferred
- X: not used
- A = Acknowledge
- P = Stop
- MAX CLOCK SPEED 400kbit/sec

11.1 Writing procedure

There are two possible procedures:

1. without increment: the I bit is set to 0 and the register is addressed by the subaddress. Only this register is written by the data following the subaddress byte.
2. with increment: the I bit is set to 1 and the first register write is the one addressed by subaddress. The registers are written from this address up to stop bit or the reaching of last register.

11.2 Reading procedure

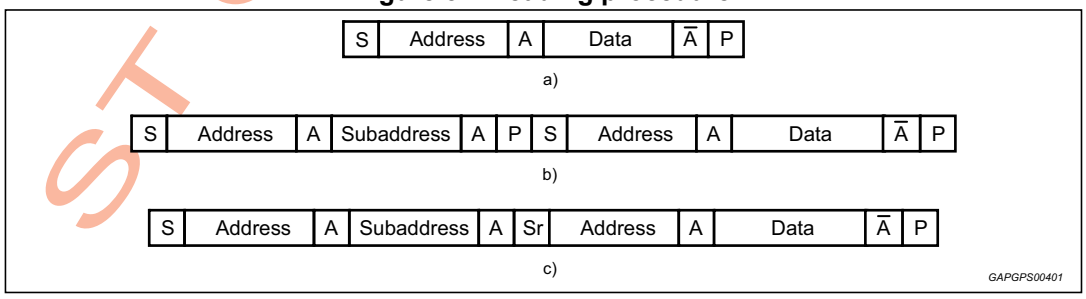
The reading procedure is made up only by the device address (sent by master) and the data (sent by slave) as reported in *Figure 54* (a). In particular when a reading procedure is performed the first register read is the last addressed in a previous access to I²C peripheral.

Hence, to read a particular register also a sort of write action (a write interrupted after the sub-address is sent) is needed to specify which register has to be read. *Figure 54* (b) shows the complete procedure to read a specific register where:

- the master performs a write action by sending just the device address and the subaddress; the transmission must be interrupted with the stop condition when the subaddress is sent.
- now, the read procedure can be performed: the master starts a new communication and sends the device address; then the slave (FDA) will respond by sending the data bits.
- the read communication is ended by the master which sends a stop condition preceded by a not-acknowledge.

Instead, performing a start immediately after the stop condition could be possible for generating the repeated start condition (Sr) which also keeps busy the I²C bus until the stop is reached (*Figure 54* (c)).

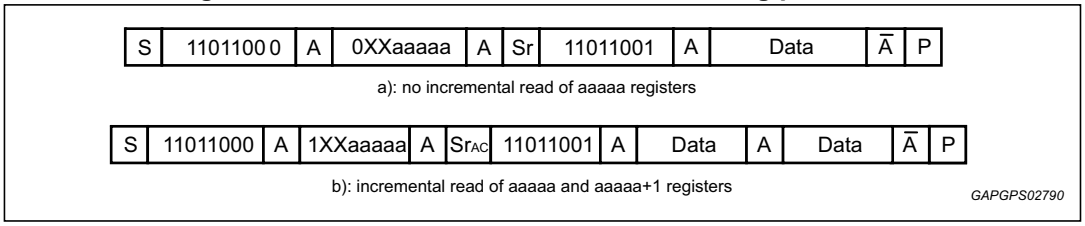
Figure 54. Reading procedure



There are two possible reading procedures:

1. without auto-increment (*Figure 55* (a)) if the "I" bit of the last I²C writing procedure has been set to 0: in this case only the register addressed by the sub-address sent in the previous writing procedure is read;
2. with auto-increment (*Figure 55* (b)) if the "I" bit of the last I²C write procedure has been set to 1: in this case the first register read is the one addressed by sub-address sent in the previous writing procedure. Only the registers from this address up to the stop bit are read.

Figure 55. Without/with auto-increment reading procedure



If a microcontroller tries to read an undefined register, FDA will return a "0xFF" data; for more details refer directly to I²C specification.

11.3 Data validity

The data on the SDA line must be stable during the high period of the clock. The HIGH and LOW state of the data line can only change when the clock signal on the SCL line is LOW.

11.4 Start and stop conditions

A start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH.
The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

11.5 Byte format

Every byte transferred to the SDA line must contain 8 bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

11.6 Acknowledge

The transmitter* puts a resistive HIGH level on the SDA line during the acknowledge clock pulse. The receiver** has to pull-down (LOW) the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during this clock pulse.

* Transmitter

= master (µP) when it writes an address to the FDA801B
= slave (FDA801B) when the µP reads a data byte from FDA801B.

** Receiver

= slave (FDA801B) when the µP writes an address to the FDA801B
= master (µP) when it reads a data byte from FDA801B.

11.7 I²C timing

This paragraph describes more in detail the I²C bus protocol used and its timings.

Please refer to *Table 12* and *Figure 56* below.

Figure 56. I²C bus interface timing

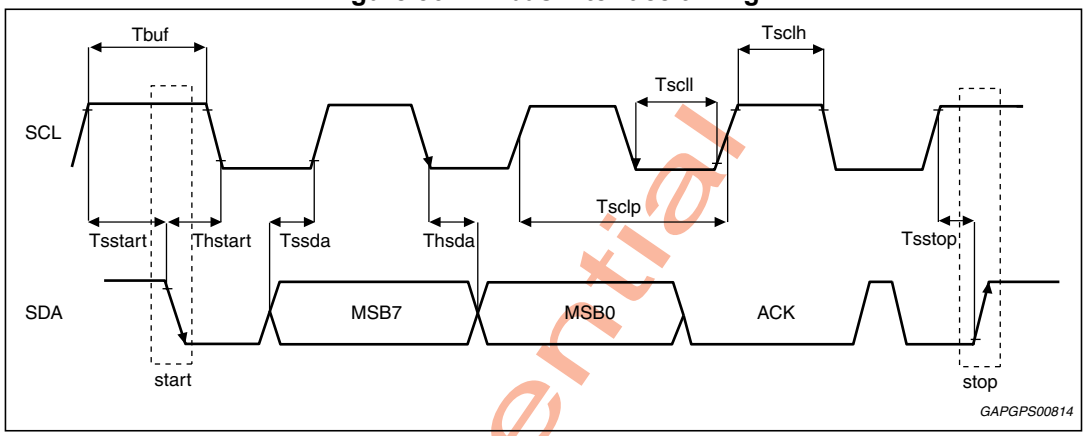


Table 12. I²C bus interface timing

Symbol	Parameter	Min	Max	Unit
Fscl	SCL (clock line) frequency	-	400	kHz
Tscl	SCL period	2500	-	ns
Tsclh	SCL high time	0.6	-	µs
Tscll	SCL low time	1.3	-	µs
Tsstart	Setup time for start condition	0.6	-	µs
Thstart	Hold time for start condition	0.6	-	µs
Tsstop	Setup time for stop condition	0.6	-	µs
Tbuf	Bus free time between a stop and a start condition	1.3	-	µs
Tssda	Setup time for data line	100	-	ns
Thsda	Hold time for data line	0(1)	-	ns
Tf	Fall time for SCL and SDA	-	300	ns

1. Device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

11.8 I²S and I²C relationship

FDA801B provides both I²C and I²S communication by means of two different digital interfaces but connected to each other interfaces and clock domains.

To program the I²C interface the I²S clock must be present, and at least 10ms should have passed from the Enable pins setting event.

In FDA801B the digital part has different clock domains:

- The I²C programming block clock is the I²C clock
- The I²S receiver clock which is the I²S clock
- The system clock which is generated by an internal PLL.

The I²C commands are not effective if I²S clock is not present. However they will remain memorized inside I²C registers.

If I²S clock is lost the digital machine goes in standby.

11.9 Main I²C functions

Several functions can be enabled/disabled by means of I²C serial communication bus. The main I²C options are:

- Amplifier gain selection (high/low gain)
- Power stage ON/OFF control channel by channel
- Parallel outputs configuration (for 2 channel applications, 2.1 applications)
- Slow/Fast Play-Mute transition
- High pass filtering for the digital input signal
- Woofer and tweeter misconnections test settings
- Low Radiation Mode (anti pulse-skipping function)
- I²S / TDM 4/8 format
- 44.1 kHz, 48 kHz, 96 kHz, 192 kHz word frame clock selection
- PWM switching frequency selection
- PWM dithering
- Thermal warning selection
- Mute/Unmute function
- Under voltage warning events
- LC filter output filter selection

Any detected fault condition will be reported in *I2C registers*, included shorts event to Vcc, GND and mixed misconnections, over voltage, over-temperature, output offset warning.

12 I²C registers

12.1 Instruction bytes- “I00xxxxx”

Table 13. IB0-ADDR: “I0000000”

Data bit	Default value	Definition
d7 d6	00	Digital input settings: **d7-d6** **Input setting** 00 I2S standard 01 TDM – 4 CHs 10 TDM – 8 CHs mode 1 11 TDM – 8 CHs mode 2
d5 d4	00	Digital input frame sync frequency (Fs): **d5-d4** **Frame sync (WS) frequency** 00 44.1 kHz 01 48 kHz 10 96 kHz 11 192 kHz
d3 d2	00	Switching frequency (with I2S frequency range 35-50kHz), expressed in kHz. **I2S Fs frequencies** **d3-d2** **44.1 kHz** **48 kHz** **96 kHz** **192 kHz** 00 308.7 336 384 384 01 352.8 384 384 384 10 396.9 432 384 384 11 396.9 432 384 384
d1	0	0 – PWM amplifier clock not dithered 1 – PWM amplifier clock dithered
d0	0	0 – PWM in phase 1 – PWM out of phase

Table 14. IB1-ADDR: "I0000001"

Data bit	Default value	Definition
d7	0	0 – CH1 and CH2 normal operation 1 – CH1 and CH2 parallel operation
d6	0	0 – CH3 and CH4 normal operation 1 – CH3 and CH4 parallel operation
d5	0	0 – Noise gate enable 1 – Noise gate disable
d4	0	0 – Low battery mute and UVLO at low level 1 – Low battery mute and UVLO at high level
d3	0	0 – Low radiation function OFF 1 – Low radiation function ON
d2	0	0 - No High-pass in the DAC 1 - High-pass in the DAC
d1	0	0 – Input offset detector disable 1 – Input offset detector enable
d0	0	0 – Output offset detector disable 1 – Output offset detector enable

Table 15. IB2-ADDR: "I0000010"

Data bit	Default value	Definition
d7	0	0 – Internal use
d6-d4	000	Temperature warning information on CD/DIAG pin: **d6-d5-d4 — Thermal info on pin** 000 — TW1 001 — TW2 010 — TW3 011 — TW4 100 — No thermal warning on CD/DIAG
d3	0	0 – NO fault information on CD/DIAG pin 1 – Fault information on CD/DIAG pin
d2	0	0 – NO Input Offset information on CD/DIAG pin 1 – Input Offset information on CD/DIAG pin
d1	0	0 – NO Output Offset information on CD/DIAG pin 1 – Output Offset information on CD/DIAG pin
d0	0	0 – NO Clipping information on CD/DIAG pin 1 – Clipping information on CD/DIAG pin

Table 16. IB3-ADDR: "I0000011"

Data bit	Default value	Definition
d7-d6	00	Mute timing setup, (values with f_{sample} = 44.1 kHz):. **d7-d6 / Type of mute / Mute time / Unit** 00 / Very Fast / 3 / ms 01 / Fast / 45 / ms 10 / Slow / 90 / ms 11 / Very Slow / 185 / ms
d5	0	0 – Low side power halving and CMC internal control (see *Table 8*) 1 – Low side power halving I2C controlled (see *Table 8*)
d4	0	Full /half power diagnostic selection (default: full)
d3	0	0 – CMC fully differential 1 – CMC single ended
d2-d1	00	**D/A conversion level controls**(1) 00 – Level internally controlled 01 – Level low 10 – Level medium 11 – Level high
d0	0	0 – Internal use

1. To be changed/used only during diagnostic. See diagnostic user guide for details on diagnostic configuration.

Table 17. IB4-ADDR: "I0000100"

Data bit	Default value	Definition
d7-d6	00	Diagnostic ramp time selection: **d7-d6** **Timing** 00 Normal 01 x2 10 x4 11 /2
d5-d4	00	Diagnostic Hold Time selection: **d5-d4** **Timing** 00 Normal 01 x2 10 x4 11 /2
d3	0	0 – Internal use
d2	0	0 – Internal use
d1	0	0 – Internal use
d0	0	0 – Internal use

Table 18. IB5-ADDR: “I0000101” - Channel 1 controls

Data bit	Default value	Definition
D7	0	AC external test flag: 0 OFF, 1 ON(1)
D6	00	CH1 gain selection: GV1 – 00 GV2 – 01 GV3 – 10 GV4 – 11
D5		
D4	0	0 – CH1 in TRISTATE (PWM OFF) 1 – CH1 with PWM ON
D3	0	0 – CH1 Speaker Diagnostic 1 – CH1 Line Driver Diagnostic
D2	0	0 – CH1 DC Diag disable 1 – CH1 DC Diag start
D1	0	0 – CH1 AC Diag disable 1 – CH1 AC Diag start (Both Internal and External)
D0	0	0 – CH1 in MUTE 1 – CH1 in PLAY

1. AC external diagnostic starts if D0, D4-D7 = 1, when D1: 0 -> 1.

Table 19. IB6-ADDR: “I0000110” - Channel 2 controls

Data bit	Default value	Definition
D7	0	AC external test flag: 0 OFF, 1 ON(1)
D6	00	CH2 gain selection: GV1 – 00 GV2 – 01 GV3 – 10 GV4 – 11
D5		
D4	0	0 – CH2 in TRISTATE (PWM OFF) 1 – CH2 with PWM ON
D3	0	0 – CH2 Speaker Diagnostic 1 – CH2 Line Driver Diagnostic
D2	0	0 – CH2 DC Diag disable 1 – CH2 DC Diag start
D1	0	0 – CH2 AC Diag disable 1 – CH2 AC Diag start (Both Internal and External)
D0	0	0 – CH2 in MUTE 1 – CH2 in PLAY

1. AC external diagnostic starts if D0, D4-D7 = 1, when D1: 0 -> 1.

Table 20. IB7-ADDR: "I0000111" - Channel 3 controls

Data bit	Default value	Definition
D7	0	AC external test flag: 0 OFF, 1 ON(1)
D6	00	CH3 gain selection: GV1 – 00 GV2 – 01 GV3 – 10 GV4 – 11
D5		
D4	0	0 – CH3 in TRISTATE (PWM OFF) 1 – CH3 with PWM ON
D3	0	0 – CH3 Speaker Diagnostic 1 – CH3 Line Driver Diagnostic
D2	0	0 – CH3 DC Diag disable 1 – CH3 DC Diag start
D1	0	0 – CH3 AC Diag disable 1 – CH3 AC Diag start (Both Internal and External)
D0	0	0 – CH3 in MUTE 1 – CH3 in PLAY

1. AC external diagnostic starts if D0, D4-D7 = 1, when D1: 0 -> 1.

Table 21. IB8-ADDR: "I0001000" - Channel 4 controls

Data bit	Default value	Definition
D7	0	AC external test flag: 0 OFF, 1 ON(1)
D6	00	CH4 gain selection: GV1 – 00 GV2 – 01 GV3 – 10 GV4 – 11
D5		
D4	0	0 – CH4 in TRISTATE (PWM OFF) 1 – CH4 with PWM ON
D3	0	0 – CH4 Speaker Diagnostic 1 – CH4 Line Driver Diagnostic
D2	0	0 – CH4 DC Diag disable 1 – CH4 DC Diag start
D1	0	0 – CH4 AC Diag disable 1 – CH4 AC Diag start (Both Internal and External)
D0	0	0 – CH4 in MUTE 1 – CH4 in PLAY

1. AC external diagnostic starts if D0, D4-D7 = 1, when D1: 0 -> 1.

Table 22. IB9-ADDR: “I0001001”

Data bit	Default value	Definition
d7	0	0 – Internal use
d6	0	0 – Internal use
d5	0	Diagnostic phase delay control ch1(1)
d4	0	Diagnostic phase delay control ch1(1)
d3	0	Diagnostic phase delay control ch1(1)
d2	0	Diagnostic phase delay control ch1(1)
d1	0	Diagnostic phase delay control ch1(1)
d0	0	Diagnostic phase delay control ch1(1)

1. Refer to AC diagnostic manuals.

Table 23. IB10-ADDR: “I0001010”

Data bit	Default value	Definition
d7	0	0 – Internal use
d6	0	0 – Internal use
d5	0	Diagnostic phase delay control ch2(1)
d4	0	Diagnostic phase delay control ch2(1)
d3	0	Diagnostic phase delay control ch2(1)
d2	0	Diagnostic phase delay control ch2(1)
d1	0	Diagnostic phase delay control ch2(1)
d0	0	Diagnostic phase delay control ch2(1)

1. Refer to AC diagnostic manuals.

Table 24. IB11-ADDR: “I0001011”

Data bit	Default value	Definition
d7	0	0 – disable PLL clock processing spread 1 – enable PLL clock processing spread
d6	0	1 – 1A additive contribution to Iprt Ib12 (d7-d6) 0 – no additive contribution to Iprt Ib12 (d7-d6)
d5	0	Diagnostic phase delay control ch3(1)
d4	0	Diagnostic phase delay control ch3(1)
d3	0	Diagnostic phase delay control ch3(1)
d2	0	Diagnostic phase delay control ch3(1)
d1	0	Diagnostic phase delay control ch3(1)
d0	0	Diagnostic phase delay control ch3(1)

1. Refer to AC diagnostic manuals.

Table 25. IB12-ADDR: “I0001100”

Data bit	Default value	Definition
d7 d6	00	D7 D6 I_{prot} 0 0 11 A 0 1 8 A 1 0 5.5 A 1 1 4.5 A
d5	0	Diagnostic phase delay control ch4(1)
d4	0	Diagnostic phase delay control ch4(1)
d3	0	Diagnostic phase delay control ch4(1)
d2	0	Diagnostic phase delay control ch4(1)
d1	0	Diagnostic phase delay control ch4(1)
d0	0	Diagnostic phase delay control ch4(1)

1. Refer to AC diagnostic manuals.

Table 26. IB13-ADDR: “I0001101”

Data bit	Default value	Definition
d7	0	Current sensing range 0 – low sensing range 1 – high sensing range
d6	0	Digital mute enable/disable 0 – Enabled 1 – Disabled
d5	0	0 – Internal use
d4	0	AC diagnostic signal level 0 – standard 1– reduced amplitude
d3	1	0 – cmdPWM peak (PWM peak activation) disabled 1 – cmdPWM peak (PWM peak activation) enabled
d2	0	0: Watchdog on I2Sws signal enable: device goes in mute if i2Sws is missed 1: Watchdog on I2Sws signal disable
d1	0	0 – Internal use
d0	0	0 – Internal use

Table 27. IB14-ADDR: "I0001110"

Data bit	Default value	Definition
d7	0	0 – Internal use
d6	0	0 – Internal use
d5	0	0 – Internal use
d4	0	0 – Internal use
d3 d2 d1	100(1)	LC filter setup(2): **d3-d2-d1 LC filter** 000 Internal 001 10 µH + 2.2 µF Out Phase 010 10 µH + 2. 2µF In Phase 011 10 µH + 3.3 µF Out Phase 100 10 µH + 3.3 µF In Phase 101 10 µH + 4.7 µF Out Phase 110 10 µH + 4.7 µF In Phase 111 Internal
d0	0	0 – FIRST setup not programmed via I2C 1 – FIRST setup programmed – ready to work

1. The optional configurations - different from 100 setting - can lead to electrical characteristics different from those declared in spec.
2. The listed configurations can be varied keeping the same LC product. However some limits on C and L have to be kept into account (the min value of L that can be used is 4.7 µH and the max C that can be used is 4.7 µF)

12.2 Data bytes - “I01xxxxx”

Table 28. DB0-ADDR: “I0100000”

Data bit	Definition
d7	Input offset detector: 0 – No DC component present on input signal 1 – DC component present on input signal
d6	Output offset detector: 0 – No DC component present on output signal 1 – DC component present on output signal
d5	0 Clipping not reached 1 Clipping reached
d4	0 No Dump pulses detected 1 Dump detected
d3	0 UVLO not detected 1 UVLO detected (NOTE: after turn-on, the first reading of this flag will be always 1)
d2	Not Used
d1	Not Used
d0	PLL lock: 0 – PLL not locked 1 – PLL locked

Table 29. DB1-ADDR: “I0100001”

Data bit	Definition
d7	0 – Thermal warning 1 not active 1 – Thermal warning 1 active
d6	0 – Thermal warning 2 not active 1 – Thermal warning 2 active
d5	0 – Thermal warning 3 not active 1 – Thermal warning 3 active
d4	0 – Thermal warning 4 not active 1 – Thermal warning 4 active
d3	Not Used
d2	Not Used
d1	Not Used
d0	Not Used

Table 30. DB2-ADDR: "I0100010" CHANNEL 1 DC outputs

Data bit	Definition
d7	0 – CH1 normal operation 1 – CH1 DC diagnostic pulse ended
d6	0 – CH1 DC diagnostic data not valid or diagnostic not activated 1 – CH1 DC diagnostic data valid
d5	0 – CH1 No overcurrent 1 – CH1 Over current protection triggered
d4	0 – Normal load on CH1 1 – Short Load on CH1
d3	0 – No Short to Vcc on CH1 1 – Short to Vcc on CH1
D2	0 – No short to GND on CH1 1 – Short to GND on CH1
d1	0 – Normal load on CH1 1 – Open Load on CH1
d0	0 – CH1 in mute 1 – CH1 in play

Table 31. DB3-ADDR: "I0100011" CHANNEL 2 DC outputs

Data bit	Definition
d7	0 – CH2 normal operation 1 – CH2 DC diagnostic pulse ended
d6	0 – CH2 DC diagnostic data not valid or diagnostic not activated 1 – CH2 DC diagnostic data valid
d5	0 – CH2 No overcurrent 1 – CH2 Over current protection triggered
d4	0 – Normal load on CH2 1 – Short Load on CH2
d3	0 – No Short to Vcc on CH2 1 – Short to Vcc on CH2
D2	0 – No short to GND on CH2 1 – Short to GND on CH2
d1	0 – Normal load on CH2 1 – Open Load on CH2
d0	0 – CH2 in mute 1 – CH2 in play

Table 32. DB4-ADDR: "I0100100" CHANNEL 3 DC outputs

Data bit	Definition
d7	0 – CH3 normal operation 1 – CH3 DC diagnostic pulse ended
d6	0 – CH3 DC diagnostic data not valid or diagnostic not activated 1 – CH3 DC diagnostic data valid
d5	0 – CH3 No overcurrent 1 – CH3 Over current protection triggered
d4	0 – Normal load on CH3 1 – Short Load on CH3
d3	0 – No Short to Vcc on CH3 1 – Short to Vcc on CH3
d2	0 – No short to GND on CH3 1 – Short to GND on CH3
d1	0 – Normal load on CH3 1 – Open Load on CH3
d0	0 – CH3 in mute 1 – CH3 in play

Table 33. DB5-ADDR: "I0100101" CHANNEL 4 DC outputs

Data bit	Definition
d7	0 – CH4 normal operation 1 – CH4 DC diagnostic pulse ended
d6	0 – CH4 DC diagnostic data not valid or diagnostic not activated 1 – CH4 DC diagnostic data valid
d5	0 – CH4 No overcurrent 1 – CH4 Over current protection triggered
d4	0 – Normal load on CH4 1 – Short Load on CH4
d3	0 – No Short to Vcc on CH4 1 – Short to Vcc on CH4
d2	0 – No short to GND on CH4 1 – Short to GND on CH4
d1	0 – Normal load on CH4 1 – Open Load on CH4
d0	0 – CH4 in mute 1 – CH4 in play

Table 34. DB6-ADDR: “I0100110” CH1 and CH2 AC diagnostic results

Data bit	Definition
d7	0 – CH1 normal operation 1 – CH1 AC diagnostic pulse ended
d6	0 – CH1 AC diagnostic data not valid or diagnostic not activated 1 – CH1 AC diagnostic data valid
d5	0 – Tweeter present on CH1 1 – No Tweeter present on CH1
d4	0 – No error-warning code 1 – error-warning code presen
d3	0 – CH2 normal operation 1 – CH2 AC diagnostic pulse ended
d2	0 – CH2 AC diagnostic data not valid or diagnostic not activated 1 – CH2 AC diagnostic data valid
d1	0 – Tweeter present on CH2 1 – No Tweeter present on CH2
d0	0 – No error-warning code 1 – error-warning code presen

Table 35. DB7-ADDR: “I0100111” CH3 and CH4 AC diagnostic results

Data bit	Definition
d7	0 – CH3 normal operation 1 – CH3 AC diagnostic pulse ended
d6	0 – CH3 AC diagnostic data not valid or diagnostic not activated 1 – CH3 AC diagnostic data valid
d5	0 – Tweeter present on CH3 1 – No Tweeter present on CH3
d4	0 – No error-warning code 1 – error-warning code presen
d3	0 – CH4 normal operation 1 – CH4 AC diagnostic pulse ended
d2	0 – CH4 AC diagnostic data not valid or diagnostic not activated 1 – CH4 AC diagnostic data valid
d1	0 – Tweeter present on CH4 1 – No Tweeter present on CH4
d0	0 – No error-warning code 1 – error-warning code presen

Table 36. DB8-ADDR:"I0101000" - CH 1 - DIM output load DC Resistance

Data bit	Definition
D7	Multiplier 'M'
D6	C[6]
D5	C[5]
D4	C[4]
D3	C[3]
D2	C[2]
D1	C[1]
D0	C[0]

Table 37. DB9-ADDR:"I0101001" - CH 1 - DIM output load AC Magnitude

Data bit	Definition
D7	Multiplier 'M'
D6	C[6]
D5	C[5]
D4	C[4]
D3	C[3]
D2	C[2]
D1	C[1]
D0	C[0]

Table 38. DB10-ADDR:"I0101010" - CH1 DIM output load AC Phase

Data bit	Definition
D7	Expressed in twos complement notation.
D6	
D5	
D4	
D3	
D2	
D1	
D0	

Table 39. DB11-ADDR:"I0101011" - CH 2 - DIM output load DC Resistance

Data bit	Definition
D7	Multiplier 'M'
D6	C[6]
D5	C[5]
D4	C[4]
D3	C[3]
D2	C[2]
D1	C[1]
D0	C[0]

Table 40. DB12-ADDR:"I0101100" - CH 2 - DIM output load AC Magnitude

Data bit	Definition
D7	Multiplier 'M'
D6	C[6]
D5	C[5]
D4	C[4]
D3	C[3]
D2	C[2]
D1	C[1]
D0	C[0]

Table 41. DB13-ADDR:"I0101101" - CH 2 - DIM output load AC Phase

Data bit	Definition
D7	Expressed in twos complement notation.
D6	
D5	
D4	
D3	
D2	
D1	
D0	

Table 42. DB14-ADDR:"I0101110" - CH 3 - DIM output load DC Resistance

Data bit	Definition
D7	Multiplier 'M'
D6	C[6]
D5	C[5]
D4	C[4]
D3	C[3]
D2	C[2]
D1	C[1]
D0	C[0]

Table 43. DB15-ADDR:"I0101111" - CH 3 - DIM output load AC Magnitude

Data bit	Definition
D7	Multiplier 'M'
D6	C[6]
D5	C[5]
D4	C[4]
D3	C[3]
D2	C[2]
D1	C[1]
D0	C[0]

Table 44. DB16-ADDR:"I0110000" - CH 3 - DIM output load AC Phase

Data bit	Definition
D7	Expressed in twos complement notation.
D6	
D5	
D4	
D3	
D2	
D1	
D0	

Table 45. DB17-ADDR:"I0110001" - CH 4 - DIM output load DC Resistance

Data bit	Definition
D7	Multiplier 'M'
D6	C[6]
D5	C[5]
D4	C[4]
D3	C[3]
D2	C[2]
D1	C[1]
D0	C[0]

Table 46. DB18-ADDR:"I0110010" - CH 4 - DIM output load AC Magnitude

Data bit	Definition
D7	Multiplier 'M'
D6	C[6]
D5	C[5]
D4	C[4]
D3	C[3]
D2	C[2]
D1	C[1]
D0	C[0]

Table 47. DB19-ADDR:"I0110011" - CH 4 - DIM output load AC Phase

Data bit	Definition
D7	Expressed in twos complement notation.
D6	
D5	
D4	
D3	
D2	
D1	
D0	

13 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

13.1 LQFP64 (10x10x1.4 mm exp. pad up) package information

Figure 57. LQFP64 (10x10x1.4 mm exp. pad up) package outline

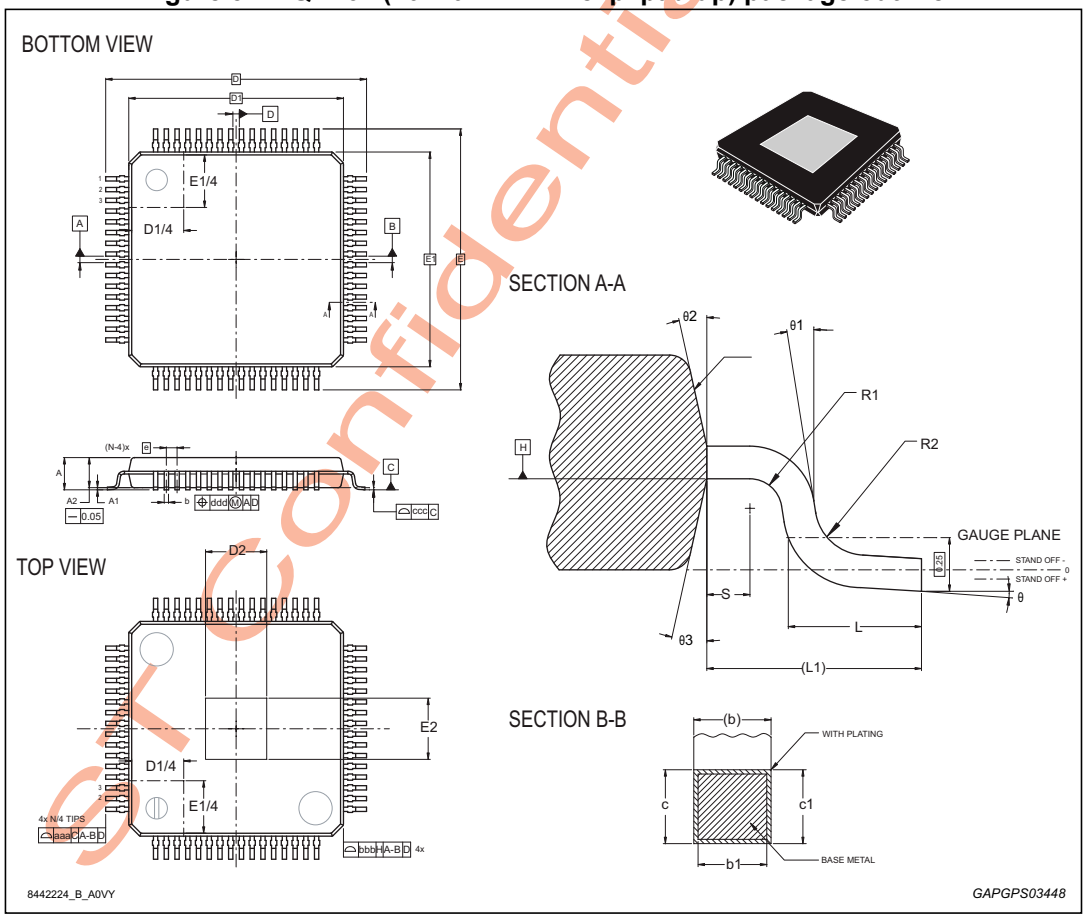


Table 48. LQFP64 (10x10x1.4 mm exp. pad up) package mechanical data

Ref	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
Θ	0°	3.5°	6°	0°	3.5°	6°
Θ1	0°	9°	12°	0°	9°	12°
Θ2	11°	12°	13°	11°	12°	13°
Θ3	11°	12°	13°	11°	12°	13°
A	-	-	1.49	-	-	0.0587
A1	-0.04	-	0.04	-0.0016	-	0.0016
A2	1.35	1.4	1.45	0.0531	0.0551	0.0571
b	-	-	0.255	-	-	0.0100
b1	0.17	0.20	0.23	0.0067	0.0079	0.0091
c	0.09	-	0.20	0.0035	-	0.0079
c1	0.09	-	0.16	0.0035	-	0.0063
D	-	12.00	-	-	0.4724	-
D1[2]	-	10.00	-	-	0.3937	-
D2[3]	-	6.00	-	-	02362	-
e	-	0.50	-	-	0.0197	-
E	-	12.00	-	-	0.4724	-
E1[2]	-	10.00	-	-	0.3937	-
E2[3]	-	6.00	-	-	0.2362	-
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1	-	1.00	-	-	0.0394	-
N	-	64.00	-	-	2.5197	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
aaa	-	0.20	-	-	0.0079	-
bbb	-	0.20	-	-	0.0079	-
ccc	-	0.08	-	-	0.0031	-
ddd	-	0.08	-	-	0.0031	-

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Dimensions D1 and E1 do not include mold flash or protrusions.
   Allowable mold flash or protrusions is “0.25 mm” per side.
3. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.

14 Revision history

Table 49. Document revision history

Date	Revision	Changes
07-Jan-2016	1	Initial release.
18-Jan-2016	2	Updated in *Table 5: Electrical characteristics* the values of V_{Mth} parameter (page 15). Updated in *Table 10: I2S interface timing on page 50* the minimum values of the Twsh parameter.
19-Apr-2016	3	Update: – Title in cover page; – *Figure 1: Block diagram on page 9*; – *Table 5: Electrical characteristics*; – *Section 3.4: Typical curves of the main electrical parameters* (caption of the figures 5, 7, 9 and 11); – *Figure 22: Frequency response (RL = 4 x 4 Ω, Po = 1 W, sine wave @ 1 kHz) on page 21*. Added: – “AEC-Q100 qualified” as first Features in cover page. – *Section 11.7: I2C timing on page 55*.