



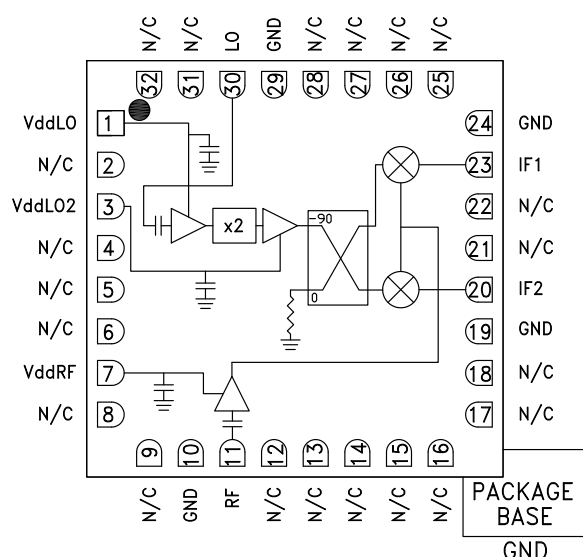
GaAs MMIC I/Q DOWNCONVERTER 21 - 25 GHz

Typical Applications

The HMC571LC5 is ideal for:

- Point-to-Point and Point-to-Multi-Point Radio
- Military Radar, EW & ELINT
- Satellite Communications

Functional Diagram



Features

- Conversion Gain: 9 dB
- Image Rejection: 18 dB
- 2 LO to RF Isolation: 35 dB
- Noise Figure: 3 dB
- Input IP3: +2 dBm
- 32 Lead 5x5mm SMT Package: 25mm²

General Description

The HMC571LC5 is a compact GaAs MMIC I/Q downconverter in a leadless RoHS compliant SMT package. This device provides a small signal conversion gain of 9 dB with a noise figure of 3.0 dB and 18 dB of image rejection across the frequency band. The HMC571LC5 utilizes an LNA followed by an image reject mixer which is driven by an active x2 multiplier. The image reject mixer eliminates the need for a filter following the LNA, and removes thermal noise at the image frequency. I and Q mixer outputs are provided and an external 90° hybrid is needed to select the required sideband. The HMC571LC5 is a much smaller alternative to hybrid style image reject mixer downconverter assemblies, and it eliminates the need for wire bonding by allowing the use of surface mount manufacturing techniques.

Electrical Specifications, $T_A = +25^\circ\text{C}$, $IF = 100\text{ MHz}$, $LO = +4\text{ dBm}$, $V_{dd} = 3.5\text{ Vdc}^*$

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range, RF	21.2 - 23.7			21 - 25			GHz
Frequency Range, LO	9 - 14			9 - 14			GHz
Frequency Range, IF	DC - 3.5			DC - 3.5			GHz
Conversion Gain (As IRM)	9	11		8	11		dB
Noise Figure		3			3		dB
Image Rejection	18	22		15	23		dB
1 dB Compression (Input)	-7	-5		-9	-6		dBm
2 LO to RF Isolation	50	60		55	40		dB
2 LO to IF Isolation	40	45		38	45		dB
IP3 (Input)	+4	+6		-1	+5		dBm
Amplitude Balance		0.8			0.3		dB
Phase Balance		5			4		Deg
Total Supply Current		125	165		125	165	mA

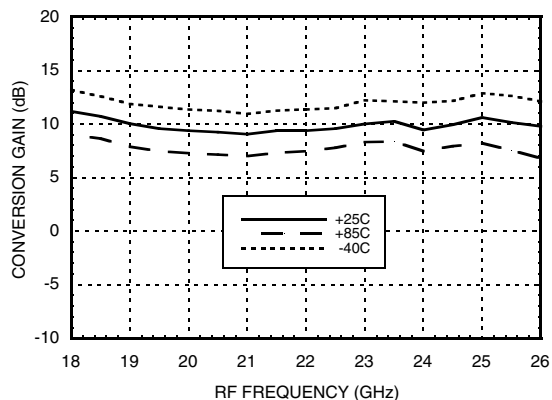
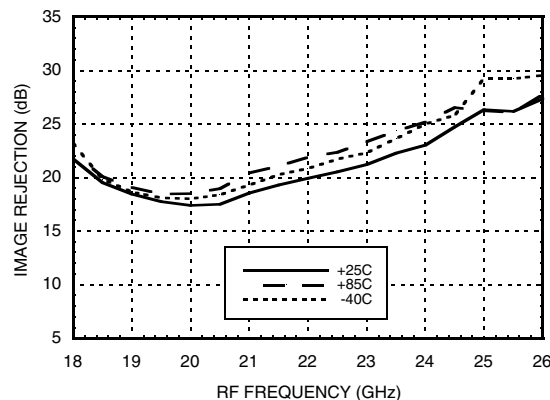
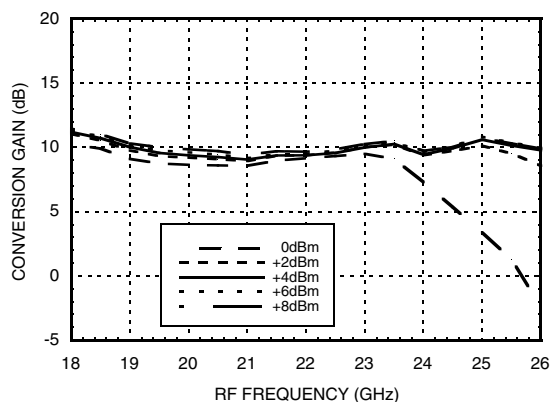
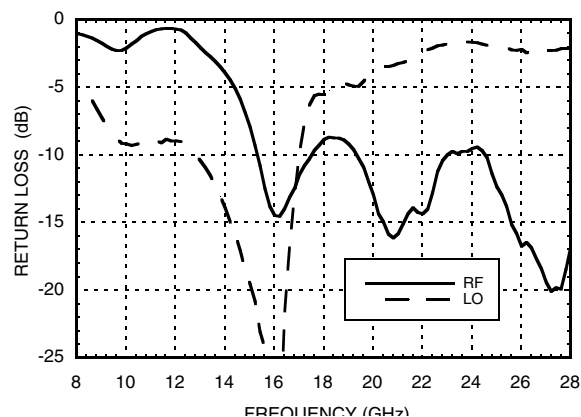
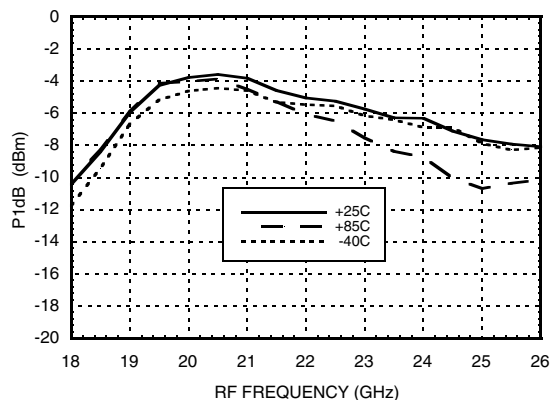
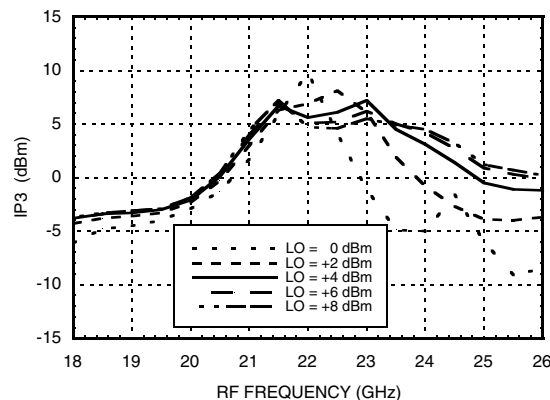
*Data taken as IRM with external IF Hybrid

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**GaAs MMIC I/Q DOWNCONVERTER
21 - 25 GHz**

Data Taken As IRM With External IF Hybrid

Conversion Gain vs. Temperature

Image Rejection vs. Temperature

Conversion Gain vs. LO Drive

Return Loss

Input P1dB vs. Temperature

Input IP3 vs. LO Drive


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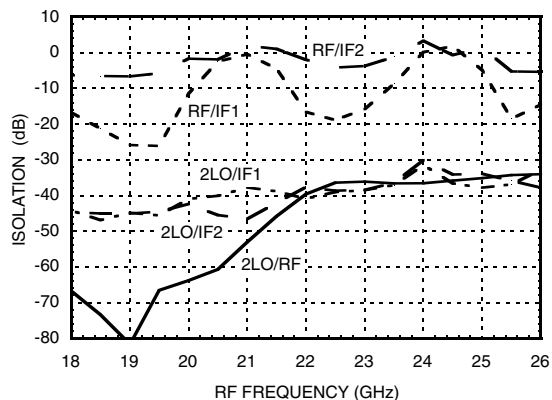
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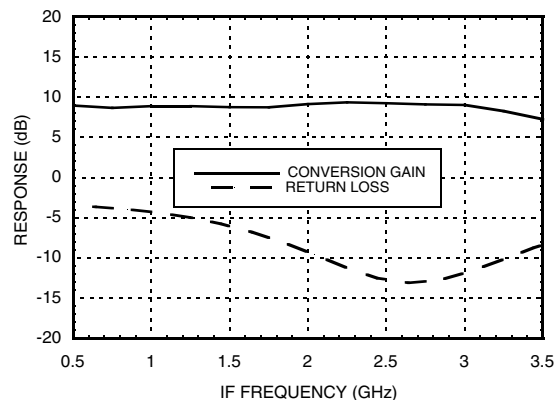
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Quadrature Channel Data Taken Without IF Hybrid

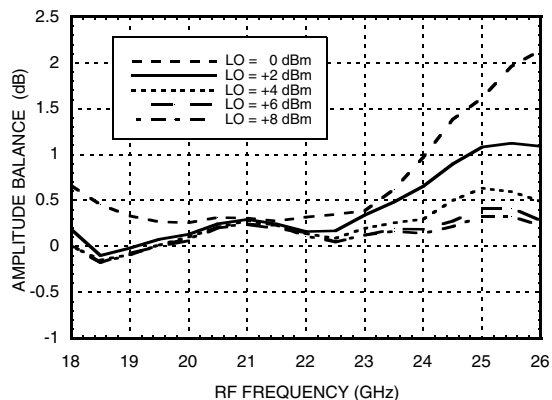
Isolations



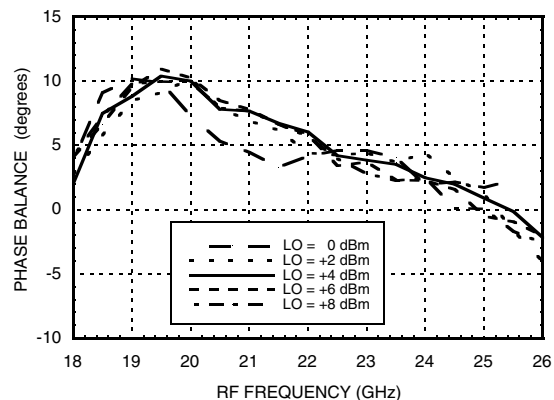
IF Bandwidth*



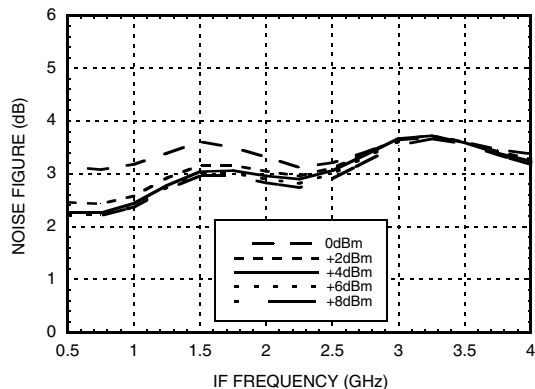
Amplitude Balance vs. LO Drive



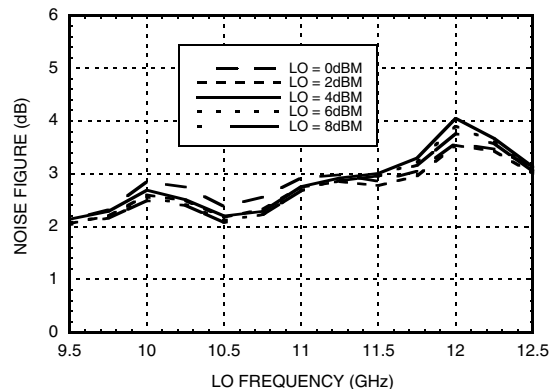
Phase Balance vs. LO Drive



Noise Figure vs. LO Drive, LO Frequency = 10.3 GHz



Noise Figure vs. LO Drive, IF Frequency = 100 MHz



* Conversion gain data taken with external IF hybrid, LO frequency fixed at 10.3 GHz and RF varied

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MxN Spurious Outputs

	nLO				
mRF	0	1	2	3	4
0	xx	31	19	25	38
1	20	32	0	31	48
2	xx	xx	72	62	43
3	xx	xx	xx	xx	81
4	xx	xx	xx	xx	xx

RF = 18 GHz @ -20 dBm

LO = 8.5 GHz @ +4 dBm

Data taken without IF hybrid

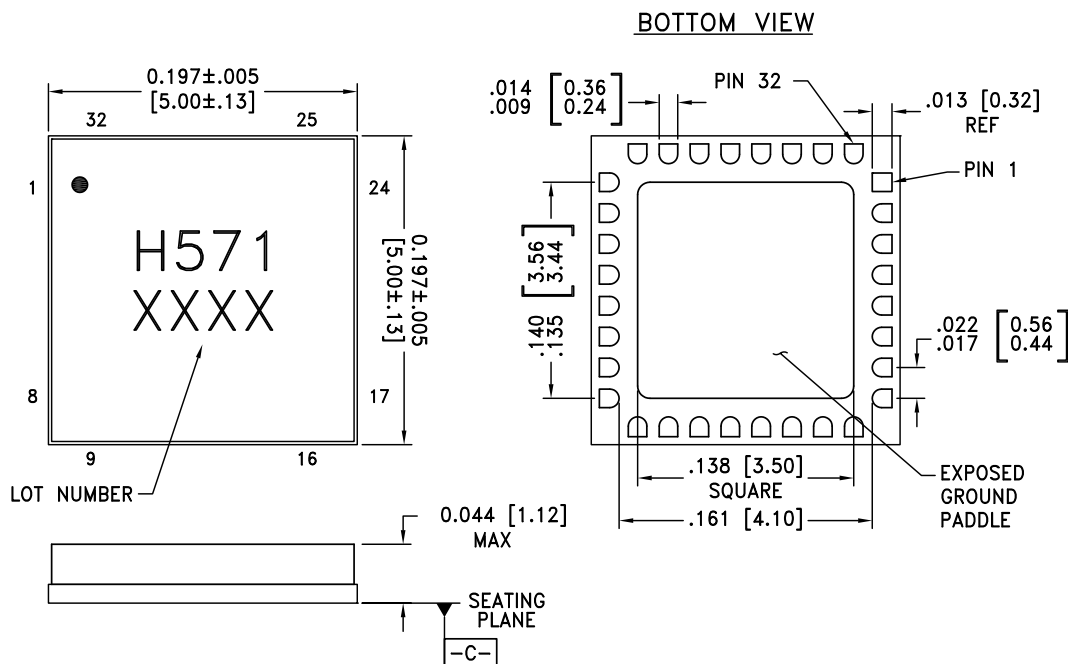
All values in dBc below IF power level (1RF -2LO = 1 GHz)

Absolute Maximum Ratings

RF	+2 dBm
LO Drive	+ 13 dBm
Vdd	5.5V
Channel Temperature	175°C
Continuous P _{diss} (T=85°C) (derate 9.56 mW/°C above 85°C)	860 mW
Thermal Resistance (R _{TH}) (channel to package bottom)	104.6 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C
ESD Sensitivity (HBM)	Class 1B



ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS


GaAs MMIC I/Q DOWNCONVERTER
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Outline Drawing

NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30 - 80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKLE
3. DIMENSIONS ARE IN INCHES [MILLIMETERS]
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking ^[2]
HMC571LC5	Alumina, White	Gold over Nickel	MSL3 ^[1]	H571 XXXX

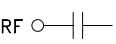
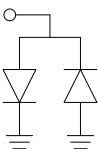
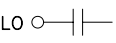
[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX

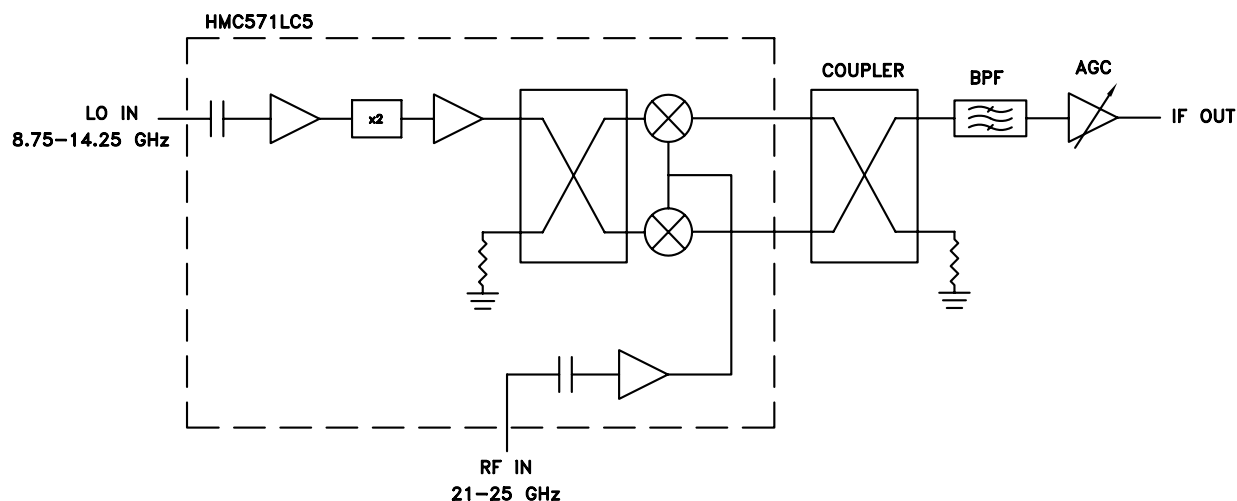


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Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	VddLO	Power supply for first stage of LO amplifier.	VddLO 
2, 4 - 6, 8, 9, 12 - 18, 21, 22, 25 - 28, 31, 32	N/C	No connection required. These pins may be connected to RF/DC ground without affecting performance.	
3	VddLO2	Power supply for second stage of LO amplifier.	VddLO2 
7	VddRF	Power supply for RF LNA.	VddRF 
10, 19, 24, 29	GND	These pins and ground paddle must be connected to RF/DC ground.	GND 
11	RF	This pin is AC coupled and matched to 50 Ohms.	RF 
20	IF2	This pin is DC coupled for applications not requiring operation to DC. This port should be DC blocked externally using a series capacitor whose value has been chosen to pass the necessary frequency range. For operation to DC, this pin must not sink / source more than 3 mA of current or part non-function and possible failure will result.	IF1, IF2 
23	IF1		
30	LO	This pin is AC coupled and matched to 50 Ohms.	LO 

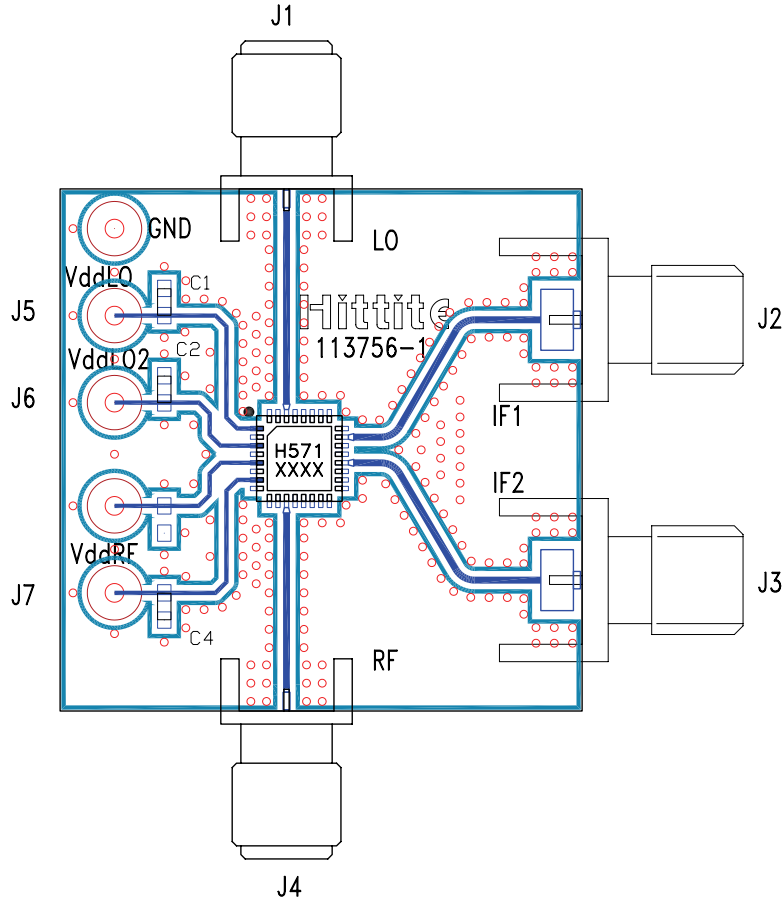
Typical Application





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Evaluation PCB



List of Materials for Evaluation PCB 113758 [1]

Item	Description
C1 - C4	Capacitor 0603, 0.01 μ F
J1, J4	PCB Mount SMA RF Connector, SRI
J2, J3	PCB Mount SMA Connector, Johnson
J5 - J7	DC Pin
U1	HMC571LC5
PCB [2]	113756 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

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