FEATURES

MitySOM-AM62 Development Board

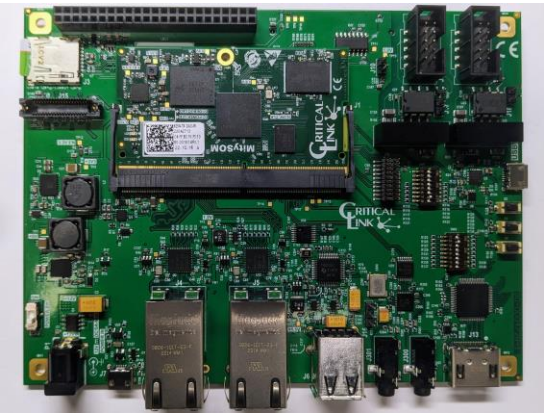
MitySOM-AM62 System on Module

Additional Hardware Included
- USB & Ethernet Cables
- AC to DC 12V 1.2A Adapter

Integrated +3.3V/+5V Power Supplies

Digital Interfaces
- HDMI Video Only Interface supporting 1080p60 (HD) video
- Audio Output and Microphone Input
- Dual 10/100/1000 MBit Ethernet Interfaces
- Micro-USB port supporting Cortex-A53 and Cortex-M4F UART Consoles
- Dual USB 2.0 Host Ports
- Micro-USB 2.0 Dual Role Interface
- Dual Electrically Isolated CAN Bus Interfaces
- Micro-SD/MMC Card Socket
- 22-pin 4-lane MIPI camera interface port

Expansion
- Dual OLDI/LCD Output Adapter
- 46-Pin AM62x Expansion Header
- Wifi/Bluetooth Module Adapter



Software and Documentation
- Linux Kernel
- uBoot
- Development Board Schematics
- Development Board Gerber Files
- Development Board BOM

Applications
- MitySOM-AM62 Evaluation
- Process Automation
- Factory Automation
- Industrial Automation
- Embedded Instrumentation
- Human Machine Interfaces
- Rich Displays
- Rapid Prototyping

DESCRIPTION

The MitySOM-AM62 Development Kit provides all the hardware and software support for system designers and developers to evaluate the Critical Link MitySOM-AM62 System on Module. The MitySOM-AM62 Development Kit comes complete with the MitySOM-AM62 module that meets your project's needs.

The MitySOM-AM62 Development Kit includes an on-board dual RS-232 to Micro-USB Port, Dual 10/100/1000 Mbit Ethernet, dual USB 2.0 Host Ports, one MIPI camera interface port, and one USB 2.0 Dual Role Device (DRD) port. The kit also includes dual electrically isolated CAN (Controller Area Network) bus ports as well as a 46-pin 0.1" header that provides several direct connections to the AM62x processor supporting GPIO, SPI, I2C, and GPMC peripherals.

The High-Definition Multimedia Interface (HDMI) supports displays up to a resolution of 2048 x 2048 through a standard connector, video only. An interface to support up to two LCD displays utilizing LVDS data and I2C control interfaces are available via an external connector interface. For audio, a standard stereo line-in and line-out 3.5mm / 1/8th jacks are provided. A standard Micro-SD card interface is available for MitySOM-AM62 boot media and/or general non-volatile data storage. The card is powered by a single 12V DC input and provides onboard +3.3V/+5V power supplies.

A block diagram of the MitySOM-AM62 Development Kit is illustrated in Figure 1 on the following page. All available processor interface pins are used directly by the MitySOM-AM62 Development Kit. Control of the onboard interface hardware and connected Expansion IO cards require proper configuration of the MitySOM-AM62 Module. While not required, it is strongly recommended that the MitySOM-AM62 software development kit and supplied API be used to manage these interfaces.

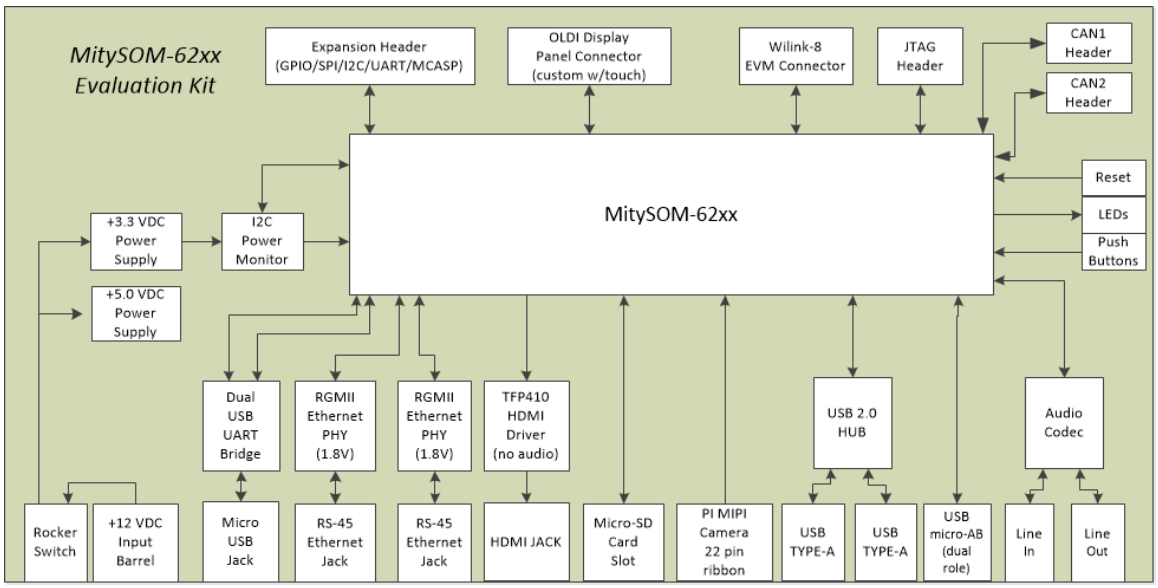


Figure 1: MitySOM-AM62 Development Kit Block Diagram

Additional details about the AM62x Sitara ARM MPU, available peripherals, and their features are provided in the datasheet on the TI website :

https://www.ti.com/tool/PROCESSOR-SDK-AM62X

Feature Descriptions

RS-232 / USB Bridge Dual Console Port 4
Audio Input/Output Description 4
2-Port USB 2.0 Interface Description 4
USB 2.0 Dual Role Device Interface Description 4
µSD/MMC Card Interface Description 4
Dual Gigabit Ethernet Interface Description 4
MIPI camera Interface Description 4
OLDI/LCD with I2C Touch Interface Description 5
HDMI (Video Only) Interface Description 5
Dual CAN Interface Description 5
Expansion Port Interface Description 5
Boot Configuration Header Description 5
TI JTAG Interface Description 6
WiFi/Bluetooth Expansion Interface Description 6
MitySOM-AM62 Current/Power Monitor 6
Control Pushbuttons 6

Electrical Interface Descriptions

Input Power – P1 8
MultiMedia Card (µSD) Interface – J2 8
2 Port USB 2.0 Type-A – J6 8
Auxiliary OLDI / LCD Interface – J15 9
HDMI Interface – J13 10
Camera MIPI Interface – J8 11
Expansion Port Interface – P3 11
Dual CAN Interface – J11 & J12 13
10/100/1000 Ethernet Interfaces – J4 and J5 13
Audio Input/Output Interface – J300 and J301 13
Boot Configuration Switches – SW1 and SW2 15
TI JTAG Interface – J9 15
WiFi/Bluetooth Expansion Port – J14 16
AM62x VPP Programming Voltage – J14 17

RS-232 / USB Bridge Dual Console Port

The MitySOM-AM62 development kit baseboard includes a CP2015 UART to USB bridge chip interfacing to UART0 (for the Cortex-A53 Console interface) and MCU_UART0 (for the Cortex M4F Console Interface). With a single micro USB connection, both console ports may be monitored using a standard terminal emulation program.

Audio Input/Output Description

Standard 3.5mm / 1/8th inch audio jacks are provided for both stereo audio output and a microphone audio input from/to a TLV320AIC26 16-bit audio CODEC connected to the MitySOM-AM62 module.

The electrical interfaces are provided via 1/8th inch jacks J300, Audio Out, and J301, Microphone In.

Linux Driver and API examples are available to support the audio functionality.

2-Port USB 2.0 Interface Description

A 2-port USB 2.0 Hub is connected to the USB0 interface of the AM62x processor of the MitySOM-AM62 module. The interface is through a dual USB-A stacked connector, J6, and the ports are configured to operate in host mode. Linux drivers are available.

USB 2.0 Dual Role Device Interface Description

The USB1 interface of the AM62x processor of the MitySOM-AM62 module is connected directly to a micro-USB port, J7, in USB Dual Role device mode. Linux drivers are available.

µSD/MMC Card Interface Description

The onboard Micro MultiMedia Card (MMC) slot uses a Micro Secure Digital (µSD) connector J3 and supports SD Standard v3.01 (TBC). It is compatible with standard (SD), SDHC (up to 32GB), and SDXC (Up to 2TB) cards. By default, the MitySOM-AM62 Development Kit boots from this interface.

U-Boot configuration information and Linux drivers are available.

Dual Gigabit Ethernet Interface Description

The on-board Ethernet interface features two network PHYs capable of running at 10/100/1000Mbit including link auto-negotiation and MII/MDIO capability. An industry-standard RJ-45 connector is provided for each external connection on J4 and J5. This Ethernet interface may be used to perform remote code download via U-Boot and FLASH upgrades on an attached MitySOM-AM62 module.

MIPI camera Interface Description

The MitySOM-AM62 Development Kit provides a 22-position flat flex cable interface to the AM62x Camera Subsystem interface, a MIPI CSI v1.3 compliant device supporting up to 4 Data Lanes at up to 2.5 Gbps per lane.

OLDI/LCD with I2C Touch Interface Description

The MitySOM-AM62 Development Kit provides a 40-position high-speed board-to-board expansion connector that connects both available OLDI interfaces (8 pairs of data lanes, 2 clock lanes) from the AM62x processor to support controlling one or two LCD displays. The interface also provides a connection to I2C1 to support communication with touch screen and/or backlight controllers.

HDMI (Video Only) Interface Description

The MitySOM-AM62 Development Kit provides a standard HDMI interface for external monitor connection. The maximum resolution supported by the display circuit is 1920x1200 (WXGA) at up to 60 Hz, 24-bit RGB 4:4:4. Nominally the display is configured for 1080p60 (HD) resolution.

Dual CAN Interface Description

The onboard CAN provides a set of CAN FD (Controller Area Network with Flexible Data-Rate) V2.0B and ISO 11898-1:2015 compliant interfaces. These interfaces are managed by the MitySOM-AM62 module directly.

The galvanic isolation is provided by a dedicated TI ISO1050 transceiver for each interface. The ISO1050 is powered by an isolated power supply with 1000V isolation from the primary supply.

Jumpers J17 (MCU_MCAN0) and J18 (MCU_MCAN1) can provide dedicated bus termination of 120Ohm. To enable termination, place shorting jumper across JPTBD.

The electrical interfaces are provided via J11 (MCU_MCAN0) and J12 (MCU_MCAN1) 10-pin shrouded headers.

Linux Driver and API examples are available to support CAN functionality.

Expansion Port Interface Description

This 46-pin port can be used for a multitude of expansion functions. GPIO, SPI, CAN, and I2C connections are available as well as AM62x GPMC 8-bit Address and Data pins with control logic. Both 1.8V from the MitySOM-AM62 module and 3.3V and +12V power supply connections are available on the connector.

Boot Configuration Header Description

The MitySOM-AM62 Development Kit provides 2 8-position dip-switches (SW1 and SW2) that are used to configure the BootMode (BM) settings of bits [3] to [15] series of the AM62x processor to determine the search order of peripherals/boot media to be used for a valid boot image.

By default, the MitySOM-AM62 Development Kit is configured to boot from the MMC/SD card.

Note that there are a total of 16 bits for the boot configuration with Boot Mode pins [0] to [2] already pulled high/low on the MitySOM-AM62 module.

TI JTAG Interface Description

A 20-pin 0.05” pitch header, J9, is available onboard for debugging the MitySOM AM62 module with a compatible JTAG Emulator.

WiFi/Bluetooth Expansion Interface Description

The WiFi/Bluetooth expansion interface, J3, is designed to be directly compatible with the Texas Instruments WL1837MODCOM8I WiFi and Bluetooth expansion card. Linux drivers are available for the TI WL1837 expansion card.

This interface can also be used for a user-designed interface card and features a 4-bit SDIO interface, 2 UART interfaces, a PCM audio interface, and multiple GPIOs.

MitySOM-AM62 Current/Power Monitor

A power/current monitor, U8, is installed in line with the +3.3V power to the MitySOM-AM62 module. Additionally, this device has a single-channel ADC that can monitor the +12V power supply voltage on the Development Board. It is accessible over the I2C1 interface to the AM62x processor.

Control Pushbuttons

Debounced normally open, contact to ground, momentary pushbuttons are included to signal the MitySOM-AM62 PMIC power button (S2), MitySOM-AM62 RESET_REQn signal (S3), and MitySOM-AM62 MCU_RESETn signal (S4).

Note: The default configuration for RESET_REQn and MCU_RESETn results in both the ARM cores resetting.

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified cards are required, please contact the Critical Link Sales Office or unit Distributors for availability and specifications.

Maximum Supply Voltage	13.2 V
Storage Temperature Range	0 to 80C

OPERATING CONDITIONS

Ambient Temperature Range	0 to 70C
Humidity	0 to 95% Non-condensing

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typical	Limit	Units (Limits)
Maximum Power Supply Output					
I_{Max}	12V Supply (AC Adapter)[1] all components			1.2	A
I_{Max}	12V Supply[2] for external components			500	mA
I_{Max}	3.3V Supply[2] for external components			1.0	A
Power Dissipation					
V_S	Supply Voltage		12±5%		V
I_S	Supply Current[3]		340[1]		mA

Notes:

1. An alternative higher amperage AC/DC 12V adapter is available upon request. Contact Critical Link for details and ordering information.
2. The maximum current supplied to external components should be limited to the specified maximum for both the 12V and 3.3V supplies.
3. Expansion card not attached, 100% Cortex-A53 utilization, USB, and Dual Ethernet are enabled and active.

ELECTRICAL INTERFACE DESCRIPTIONS

Input Power – P1

The MitySOM-AM62 Development Kit power interface, P1, requires a single +12Volt power supply. P1 uses a Würth Elektronik 694106301002 2.1/5.5 mm inner/outer diameter jack. Slide switch S1 is included to support turning on and off the main power input such that the unit may be powered off without disconnecting P1. The MitySOM-AM62 Development Kit provides reverse polarity protection on P1.

Table 1: Input Power Interface Pin Description

Signal	P1 Position
+12V	1
GND	2

MultiMedia Card (µSD) Interface – J2

The MitySOM-AM62 Development Kit provides a MMC interface that uses a standard Micro–Secure Digital (µSD) card slot for the physical interface. By default the slot is supplied with 3.3V for use with standard SD cards and the IO voltages can be lowered to 1.8V by the AM62x SOM during runtime to support higher data rates provided by SDHC cards.

Table 2: J2 Micro SD Card Connector

J6 Pin	J6 Signal	SOM Interface Signal	SOM Pin
1	DAT2	MMC1_DAT2	J10 – 171
2	CD/DAT3	MMC1_DAT3	J10 – 169
3	CMD	MMC1_CMD	J10 – 167
4	VDD	+3.3V	N/A
5	CLK	MMC1_CLK	J10 – 165
6	VSS	GND	N/A
7	DAT0	MMC1_DAT0	J10 – 175
8	DAT1	MMC1_DAT1	J10 – 173
9	Switch (B)	MMC1_SD_CD	J10 - 163
10	Switch(A)	GND	N/A

2 Port USB 2.0 Type-A – J6

The MitySOM-AM62 Development Board features a 2-port USB hub, TUSB4020BIPHP – U15, which is connected to the USB0 interface from the AM62x processor. The 2 USB ports are exposed from the Development Board on a dual USB Type-A Host-only connector, J6.

This interface is a USB 2.0 interface and supports up to 480Mbps throughput speeds and is backward compatible with Full-speed and Low-speed devices. Each port can supply a maximum of 1A of current at +5V and an overcurrent detection circuit is connected to each port individually. The pinout for both J6 is included in Table 3.

Table 3 Dual USB Host Connector Pin Out, J6

J6 Pin	J6 Signal	J6 Upper or Lower Port
1	VBUS1	Lower
2	HUB_USB1_DM	
3	HUB_USB1_DP	
4	GND	
5	VBUS2	Upper
6	HUB_USB2_DM	
7	HUB_USB2_DP	
8	GND	

Auxiliary OLDI / LCD Interface – J15

The Auxiliary OLDI / LCD interface connector provides the necessary connections to connect up to two displays as well as pins to support touchscreen controls. The interface uses a Samtec ERF-020-05.0-S-DV-L-TR board-to-board interface connector. Table 4 defines the connector, J15, pinout which contains signals that are routed directly from the MitySOM-AM62 to this connector.

Table 4: J401 Aux / LCD Interface Pin Description

Pin	Schematic Signal	SoM Pin	Type	Standard	Notes
1	OLDI_CLK0_P	44	I	LVDS	
2	OLDI_CLK1_P	45	I	LVDS	
3	OLDI_CLK0_N	46	I	LVDS	
4	OLDI_CLK1_N	43	I	LVDS	
5	GND	-	Power	-	
6	GND	-	Power	-	
7	ALDI_A0_P	56	I	LVDS	
8	OLDI_A4_P	61	I	LVDS	
9	OLDI_A0_N	54	I	LVDS	
10	OLDI_A4_N	63	I	LVDS	
11	GND	-	Power	-	
12	GND	-	Power	-	
13	OLDI_A1_P	52	I	LVDS	
14	OLDI_A5_P	51	I	LVDS	
15	OLDI_A1_N	50	I	LVDS	
16	OLDI_A5_N	49	I	LVDS	
17	GND	-	Power	-	
18	GND	-	Power	-	
19	OLDI_A2_P	62	I	LVDS	
20	OLDI_A6_P	55	I	LVDS	
21	OLDI_A2_N	64	I	LVDS	
22	OLDI_A6_N	53	I	LVDS	
23	GND	-	Power	-	
24	GND	-	Power	-	
25	ALDI_A3_P	60	I	LVDS	
26	OLDI_A7_P	57	I	LVDS	
27	OLDI_A3_N	58	I	LVDS	
28	OLDI_A7_N	59	I	LVDS	
29	GND	-	Power	-	
30	GND	-	Power	-	
31	I2C1_SCL_3V3	205	I/O	LVCMOS / OD	
32	OLDI_RESETN	-	I	LVCMOS	Connected to P3 of PCAL6408
33	I2C1_SDA_3V3	207	I/O	LVCMOS / OD	
34	OLDI_PWM	200	O	LVCMOS	EHRPWM0_A pin mux function
35	OLDI_IRQ_N	244	I	LVCMOS / OD	MCU_GPIO0_7 pin mux function
36	GND	-	Power	-	
37	GND	-	Power	-	
38	+12V	-	Power	-	
39	+3V3_VIO	-	Power	-	
40	+12V	-	Power	-	

Note: These signals are pin-muxed in the AM62x CPU.

HDMI Interface – J13

The MitySOM-AM62 Development Kit provides a 19-pin standard HDMI connector with video only, J400. Supporting HDMI 1.3, the MitySOM-AM62 can output up to a resolution of 2048 x 2048 pixels.

Table 5: J13 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	TMDS Data2+	O	HSCL	
2	Shield	Power		
3	TMDS Data2-	O	HSCL	
4	TMDS Data1+	O	HSCL	
5	Shield	Power		
6	TMDS Data1-	O	HSCL	
7	TMDS Data0+	O	HSCL	
8	Shield	Power		
9	TMDS Data0-	O	HSCL	
10	TMDS Clock+	O	HSCL	
11	Shield	Power		
12	TMDS Clock-	O	HSCL	
13	Reserved (CEC)	-		
14	Reserved	-		
15	DDC Data/SDA	I/O		Connected on I2C1 data bus, +5V
16	DDC Clock/SCL	I/O		Connected on I2C1 data bus, +5V
17	GND	Power		
18	+5.0V	Power		
19	Hot Plug Detect	I		

Camera MIPI Interface – J8

The MitySOM-AM62 Development Kit provides a 22-pin 0.5 mm pitch flat flex connector, J8, to interface with the camera subsystem of the AM62x processor on the MitySOM-AM62.

Table 6: J8 Connector Pin Assignments

Pin	Signal	Type	Standard	Notes
1	GND	-	-	
2	CSI_RX0_N	I	DPHY_RX	
3	CSI_RX0_P	I	DPHY_RX	
4	GND	-	-	
5	CSI_RX1_N	I	DPHY_RX	
6	CSI_RX1_P	I	DPHY_RX	
7	GND	-	-	
8	CSI_RXCLK_N	I	DPHY_RX	
9	CSI_RXCLK_P	I	DPHY_RX	
10	GND	-	-	
11	CSI_RX2_N	I	DPHY_RX	
12	CSI_RX2_P	I	DPHY_RX	
13	GND	-	-	
14	CSI_RX3_N	I	DPHY_RX	
15	CSI_RX3_P	I	DPHY_RX	
16	GND	-	-	
17	CAM_IO1	I/O	LVCMOS	
18	CAM_IO2	I/O	LVCMOS	
19	GND	-	-	
20	I2C1_SCL_3V3	I/O	LVCMOS / OD	
21	I2C1_SDA_3V3	I/O	LVCMOS / OD	
22	+3V3_VIO	Power	-	Max 500 mA

Expansion Port Interface – P3

The MitySOM-AM62 Development Kit provides a dual row 0.1” pitch 46-pin female general expansion connector on the top of the board. A Major League SSHS-123-D-02-GT-LF connector is used and mates with standard 0.1” dual row male headers.

This expansion interface can be used for many different add-on cards due to it having I2C, SPI, and General Purpose Memory Controller (GPMC) Address/Data pins with control signals directly from the MitySOM-AM62 module. A 3.3V and +12V supply pin are provided on the connector to support powering external cards. Table 7 provides signal descriptions for each pin.

Table 7: P3 Connector Pin Assignments

Pin	Schematic Signal	SoM Pin	Type	Standard	Notes
1	GND	-	Power	-	
2	GND	-	Power	-	
3	GPMC_AD0_BM0	154	I/O	LVCMOS 3.3V	All Boot Mode pins must be high impedance during power on / reset operations.
4	MCU_I2C0_SDA	231	I/O	LVCMOS 3.3V	
5	GPMC_AD1_BM1	148	I/O	LVCMOS 3.3V	
6	MCU_I2C0_SCL	233	I/O	LVCMOS 3.3V	
7	GPMC_AD2_BM2	150	I/O	LVCMOS 3.3V	
8	MCU_SPI0_D1	235	I/O	LVCMOS 3.3V	
9	GPMC_AD3_BM3	152	I/O	LVCMOS 3.3V	
10	MCU_SPI0_D0	237	I/O	LVCMOS 3.3V	
11	GPMC_AD4_BM4	156	I/O	LVCMOS 3.3V	
12	MCU_SPI0_CS0	239	I/O	LVCMOS 3.3V	
13	GPMC_AD5_BM5	155	I/O	LVCMOS 3.3V	
14	MCU_SPI0_CS1	241	I/O	LVCMOS 3.3V	
15	GPMC_AD6_BM6	146	I/O	LVCMOS 3.3V	
16	MCU_SPI0_CLK	243	I/O	LVCMOS 3.3V	
17	GPMC_AD7_BM7	142	I/O	LVCMOS 3.3V	
18	WKUP_I2C0_SCL	247	I/O	LVCMOS 3.3V	
19	GND	-		-	
20	WKUP_I2C_SDA	249	I/O	LVCMOS 3.3V	
21	GPMC_DIR	162	I/O	LVCMOS 3.3V	
22	VDDSHV_MCU	-	Power	+3.3V	
23	GPMC_BE1	159	I/O	LVCMOS 3.3V	
24	GND	-	Power	-	
25	GPMC_BE0	161	I/O	LVCMOS 3.3V	
26	UART0_CTSn	218	I/O	LVCMOS 3.3V	
27	GPMC_OEn	163	I/O	LVCMOS 3.3V	
28	UART0_RTSn	212	I/O	LVCMOS 3.3V	
29	GPMC_WEn	165	I/O	LVCMOS 3.3V	
30	MCASP0_AXR3	197	I/O	LVCMOS 3.3V	
31	GPMC_ADVn_ALE	164	I/O	LVCMOS 3.3V	
32	MCASP0_AXR2	199	I/O	LVCMOS 3.3V	
33	GPMC_CS0n	160	I/O	LVCMOS 3.3V	
34	EXT_RCLK1	202	I/O	LVCMOS 3.3V	
35	GPMC_CS2n	168	I/O	LVCMOS 3.3V	
36	MCAN0_RX	206	I/O	LVCMOS 3.3V	
37	GPMC_CS3n	167	I/O	LVCMOS 3.3V	
38	MCAN0_TX	208	I/O	LVCMOS 3.3V	
39	I2C1_SDA_3V3	207	I/O	LVCMOS 3.3V	
40	SPI0_CS0	215	I/O	LVCMOS 3.3V	
41	I2C1_SCL_3V3	205	I/O	LVCMOS 3.3V	
42	EXTINTn	104	I/O	LVCMOS 3.3V	Should be left NC or driven open drain as this signal is connected to PMIC interrupt.
43	GND	-	Power	-	
44	GND	-	Power	-	
45	+3V3_VIO	-	Power	+3.3V	
46	+12V	-	Power	+12V	

Note that many of these signals are pin-muxed in the CPU and may be available for a variety of functions. Review the MitySOM-AM62 datasheet for additional information.

Dual CAN Interface – J11 & J12

Table 8 lists the pin connections for each of the CAN interface connectors.

Table 8: J11 MCU_MCAN0 & J12 MCU_CAN1 Connector[2] Pin Assignments

Pin	Signal	Type	Standard	Notes
1	RESERVED	-	-	
2	RESERVED	-	-	
3	CANL	I/O		CAN Bus Signal L
4	CANH	I/O		CAN Bus Signal H
5	GND_ISOCANx[1]	Power	-	CAN Bus Isolated Ground
6	RESERVED	-	-	
7	RESERVED	-	-	
8	+5V_CANx[1]	Power	-	Isolated +5V Output, 20mA Max
9	RESERVED	-	-	
10	RESERVED	-	-	

Note 1: The ‘x’ at the end of the signal names is either a 1 or a 0 depending on which CAN interface you are using.

10/100/1000 Ethernet Interfaces – J4 and J5

The MitySOM-AM62 Development Kit provides a RJ-45 connection for a Gigabit 10/100/1000 Ethernet connection. This connection follows standard TIA/EIA-568B pin-out as shown in Table 9 below. By default, the Ethernet PHY will auto-negotiate with its link partner. The J4 connector corresponds to RGMII1 on the AM62x processor and J6 corresponds to RGMII2.

Table 9: J200 Ethernet RJ45 Pin Assignments

Pin	Signal	Type	Standard	Notes
1	TXVA_P	I/O		
2	TXVA_N	I/O		
3	TXVB_P	I/O		
4	TXVB_N	I/O		
5	TXVC_P	I/O		
6	TXVC_N	I/O		
7	TXVD_P	I/O		
8	TXVD_N	I/O		

Audio Input/Output Interface – J300 and J301

The MitySOM-AM62 Development Kit provides both an Input, biased microphone, and Output, L/R stereo speaker connections. The 3.5mm/1/8” connections are through J300 for output and J301 for input with the pin-outs shown below.

Table 10: J300 Audio Output Pin Assignments

Pin	Signal	Type	Standard	Notes
Tip	Audio Out Left	O		Unbalanced audio output
Ring	Audio Out Right	O		Unbalanced audio output
Sleeve	GND	Power		Audio Ground

Table 11: J301 Audio Input Pin Assignments

Pin	Signal	Type	Standard	Notes
Tip	Mic Bias	O		2.2V bias from TLV320AIC26
Ring	Mic Input	I		
Sleeve	GND	Power		Audio Ground

The TLV320AIC26 Audio Codec is connected to the MCASP0 interface on the AM62x processor, which is shared between this interface and the wireless / Bluetooth expansion module. You must set the J16 jumper to positions 1-2 to enable the MCASP0 pins for the Audio Codec interface.

Boot Configuration Switches – SW1 and SW2

The boot mode, as determined by the 12 Boot Mode pins, is selected on the rising edge of the PWRONRSTn Reset Input Pin of the AM62x processor which is controlled by the PMIC of the MitySOM-AM62 module. Using two 8-position dip switches, SW1 and Sw2, each boot configuration pin on the development kit is connected to a weak pull-down (47K Ohm), '0', unless a switch is turned on which will add a relatively strong pullup (470 Ohm) to the configuration pin, '1'. Table 12 describes the switch connections to the Boot Mode pins and lists the default position settings needed to boot from the MicroSD card interface.

Table 12: SW1 and SW2 Jumper Connections

Switch	Position	Default	Connection	Notes
SW1	1	OFF	N/A	
SW1	2	OFF	N/A	
SW1	3	OFF	N/A	
SW1	4	OFF	GPMC_AD3_BM3	On sets BM3 high, Off sets BM3 Low.
SW1	5	OFF	GPMC_AD4_BM4	On sets BM4 high, Off sets BM4 Low.
SW1	6	OFF	GPMC_AD5_BM5	On sets BM5 high, Off sets BM5 Low.
SW1	7	ON	GPMC_AD6_BM6	On sets BM6 high, Off sets BM6 Low.
SW1	8	OFF	GPMC_AD7_BM7	On sets BM7 high, Off sets BM7 Low.
SW2	1	OFF	VOUT_D16_BM8	On sets BM8 high, Off sets BM8 Low.
SW2	2	ON	VOUT_D17_BM9	On sets BM9 high, Off sets BM9 Low.
SW2	3	OFF	VOUT_D18_BM10	On sets BM10 high, Off sets BM10 Low.
SW2	4	OFF	VOUT_D19_BM11	On sets BM11 high, Off sets BM11 Low.
SW2	5	OFF	VOUT_D20_BM12	On sets BM12 high, Off sets BM12 Low.
SW2	6	OFF	VOUT_D21_BM13	On sets BM13 high, Off sets BM13 Low.
SW2	7	OFF	VOUT_D22_BM14	On sets BM14 high, Off sets BM14 Low.
SW2	8	OFF	VOUT_D23_BM15	On sets BM15 high, Off sets BM15 Low.

TI JTAG Interface – J9

Table 13 lists the connections to the JTAG interface connector.

Table 13: J9 JTAG Pin Assignments

Pin	Schematic Signal	SoM Pin	Type	Standard	Notes
1	TMS	230	I	LVCMOS 3.3	
2	TRST_N	234	I	LVCMOS 3.3	
3	TDI	232	I	LVCMOS 3.3	
4	GND	-	Power	-	
5	+3.3V	-	Power	-	
6	Key	-	-	-	
7	TDO	224	O	LVCMOS 3.3	
8	GND	-	Power	-	
9	N/C	-	-	-	
10	GND	-	Power	-	
11	TCK	236	I	LVCMOS 3.3	
12	GND	-	Power	-	
13	EMU0	222	I/O	LVCMOS 3.3	
14	EMU1	228	I/O	LVCMOS 3.3	
15	EMU_RSTn	226	I	LVCMOS 3.3	
16	GND	-	Power	-	
17	N/C	-	-	-	
18	N/C	-	-	-	
19	N/C	-	-	-	
20	GND	-	Power	-	

WiFi/Bluetooth Expansion Port – J14

The MitySOM-AM62 Development Kit incorporates a 100-pin expansion connector, J3, which is directly compatible with the Texas Instruments WL1837MODCOM8I WiFi and Bluetooth expansion card. This connector, MEC6-150-02-L-D-RA1, can also be utilized for a custom expansion card and has the following pinout.

Table 14: J15 Connector Pin Assignments

Pin	Signal	SOM Pin	Pin	Signal	SOM Pin
1	No Connect	N/A	2	GND	N/A
3	GND	N/A	4	WLAN_EN	187
5	+3.3V[1]	N/A	6	GND	N/A
7	+3.3V[1]	N/A	8	+1.8V	N/A
9	GND	N/A	10	No Connect	N/A
11	TP8 (WL_TX)	N/A	12	No Connect	N/A
13	TP9 (WL_RX)	N/A	14	No Connect	N/A
15	TP10 (WL_DEBUG)	N/A	16	No Connect	N/A
17	No Connect	N/A	18	GND	N/A
19	GND	N/A	20	MMC2_SDIO_CLK	173
21	No Connect	N/A	22	GND	N/A
23	No Connect	N/A	24	MMC2_SDIO_CMD	179
25	No Connect	N/A	26	MMC2_SDIO_D0	183
27	No Connect	N/A	28	MMC2_SDIO_D1	181
29	No Connect	N/A	30	MMC2_SDIO_D2	175
31	No Connect	N/A	32	MMC2_SDIO_D3	177
33	No Connect	N/A	34	WLAN_IRQ	185
35	No Connect	N/A	36	No Connect	N/A
37	GND	N/A	38	No Connect	N/A
39	No Connect	N/A	40	No Connect	N/A
41	No Connect	N/A	42	GND	N/A
43	No Connect	N/A	44	No Connect	N/A
45	No Connect	N/A	46	No Connect	N/A
47	GND	N/A	48	No Connect	N/A
49	No Connect	N/A	50	No Connect	N/A
51	No Connect	N/A	52	PCM_IF_CLK	191
53	No Connect	N/A	54	PCM_IF_FSYNC	198
55	No Connect	N/A	56	PCM_IF_DIN	203
57	No Connect	N/A	58	PCM_IF_DOUT	201
59	No Connect	N/A	60	GND	N/A
61	No Connect	N/A	62	No Connect	N/A
63	GND	N/A	64	GND	N/A
65	No Connect	N/A	66	BT_UART_IF_TX	253
67	No Connect	N/A	68	BT_UART_IF_RX	251
69	No Connect	N/A	70	BT_UART_IF_CTS	255
71	No Connect	N/A	72	BT_UART_IF_RTS	257
73	No Connect	N/A	74	No Connect	N/A
75	No Connect	N/A	76	TP11 (BT_DEBUG)	N/A
77	GND	N/A	78	No Connect	N/A
79	No Connect	N/A	80	No Connect	N/A
81	No Connect	N/A	82	No Connect	N/A
83	GND	N/A	84	No Connect	N/A
85	No Connect	N/A	86	No Connect	N/A
87	GND	N/A	88	No Connect	N/A
89	BT_EN_1V8	N/A (PCAL6408 P6)	90	No Connect	N/A
91	No Connect	N/A	92	GND	N/A
93	No Connect	N/A	94	No Connect	N/A
95	GND	N/A	96	No Connect	N/A
97	GND	N/A	98	No Connect	N/A
99	No Connect	N/A	100	No Connect	N/A

All IO signals are 1.8V logic levels and connected to the AM62x processor of the MitySOM-AM62 module. The BlueTooth UART interface pins and Audio PCM interface pins are level translated to 3.3V prior to connecting to the SOM.

The BlueTooth Audio pins (PCM_IF_CLK, PCM_IF_FSYNC, PCM_IF_DIN, PCM_IF_DOUT) are connected to the MCASP0 interface on the AM62x processor and are shared between this interface and the on-board audio CODEC. You must set the J16 jumper to positions 2-3 to enable the BlueTooth Audio interface.

AM62x VPP Programming Voltage – J14

The MitySOM-AM62 Development Kit provides a 0.1" jumper, J14, that will connect the VPP signal (pin 238) on the MitySOM-AM62 to 1.8V in order to support programming the eFuse one-time programmable (OTP) read-only memory (ROM) on the AM62x processor. Note: this jumper should not be installed during power on, and should only be installed when programming the OTP ROM on the processor.

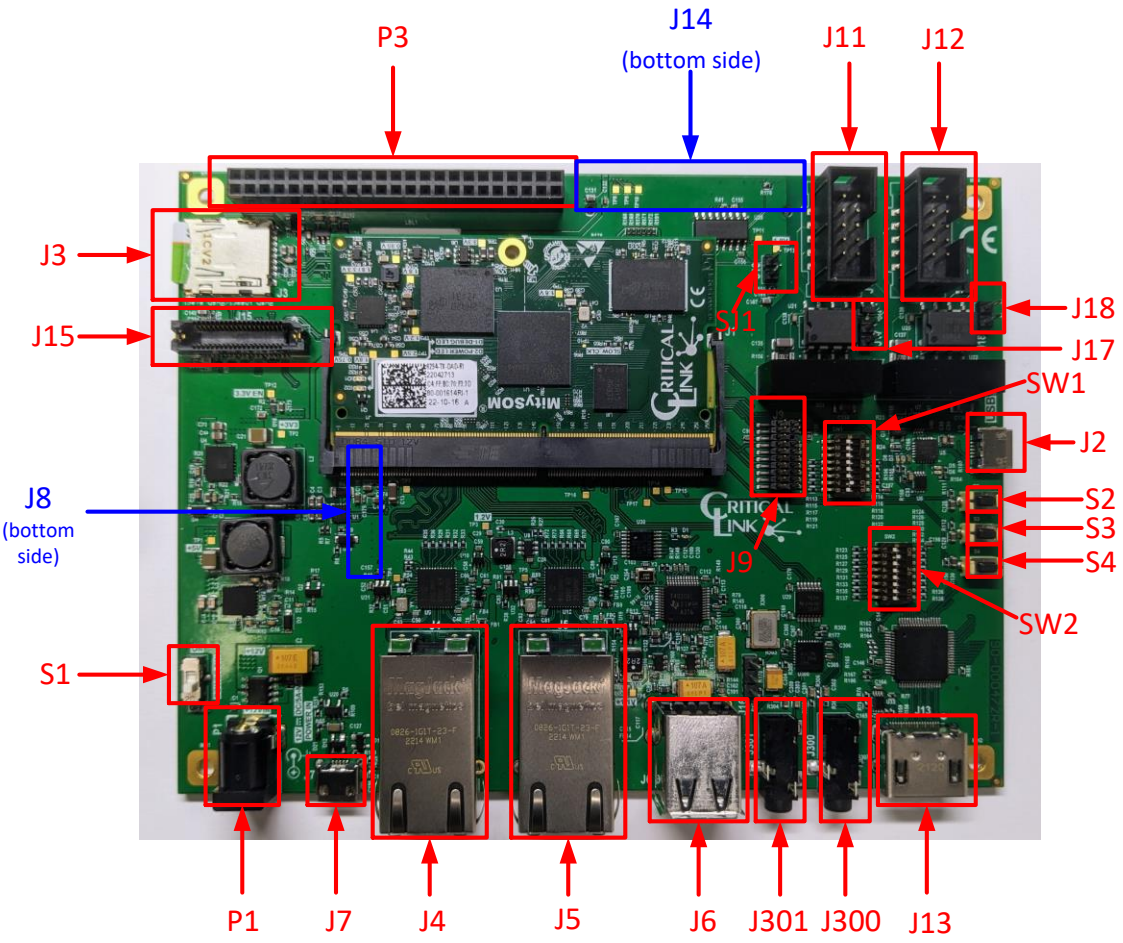
Included Components

The following table lists the components that are included with a MitySOM-AM62 Development Kit. See Table 16 for specific development kit ordering information and Table 17 for expansion kit ordering information.

Table 15: Included Items

Description	Interface Port	Qty. Included
MitySOM-AM62 Development Kit Board	n/a	Qty. 1
MitySOM-AM62 Module	J1	Qty. 1
12V 1.2A AC to DC Supply	P1	Qty. 1
Ethernet cable – 7 foot	J4, J5	Qty. 2
USB-A to MicroUSB cable	J7, J2	Qty. 2

MitySOM-AM62 Development Kit Board with MitySOM-AM62 Module



ORDERING INFORMATION

Development Kits

The following table lists the standard MitySOM-AM62 Development Kit configurations. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 16: Standard Model Numbers

Development Kit Model	Module Included	Module Operating Temp
80-001641	6231-IX-XXA-RI	-40ºC to +85º C
80-001642	6252-TX-XXD-RI	-40ºC to +85º C
80-001643	6254-TX-XXD-RI-GP	-40 ºC to +85 ºC
80-001694	6254-TX-XXD-RI	-40 ºC to +85 ºC

Expansions Kits

The following table lists the standard expansion kits for the above development kits. For shipping status, availability, and lead time of these or other configurations please contact Critical Link at info@criticallink.com.

Table 17: Standard Expansion Kit Numbers

Expansion Kit Model	Type	Interface Port
80-000540	RS485/422	J11 and J12
TI WL1837MODCOM8I	WiLink 802.11a/b/g/n w/ Bluetooth Smart Ready 4.x Dual Mode 2.4GHz, 5 GHz	J3

MECHANICAL INTERFACE DESCRIPTION

Main Board Interface / Mounting

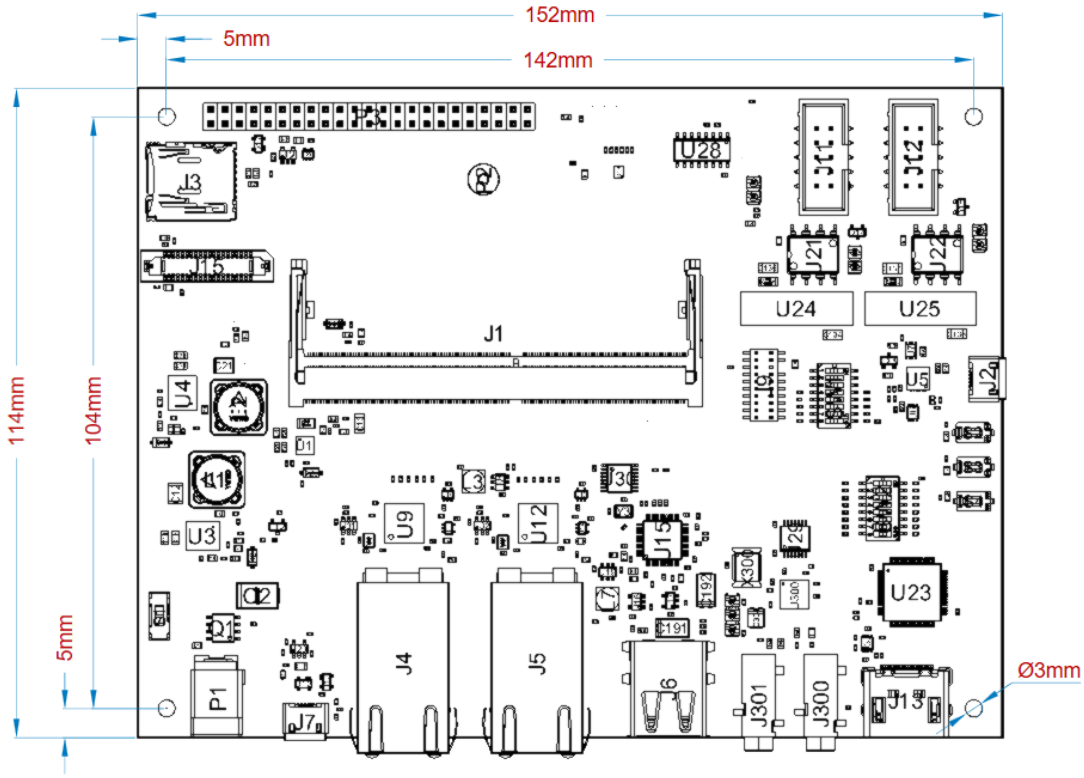


Figure 2: MitySOM-AM62 Development Kit Outline and Mounting Hole Locations (Top View, millimeters)

REVISION HISTORY

Date	Rev	Change Description
07-DEC-2022	A	Initial revision.
31-MAY-2023	B	Update for misc corrections, GP vs. HS-FS clarification.