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September 2016

FDV045P20L

P-Channel PowerTrench® MOSFET
-20 V, -1.15 A, 108 mΩ

Features

- Max $r_{DS(on)}$ = 108 mΩ at V_{GS} = -4.5 V, I_D = -1.15 A

- Max $r_{DS(on)}$ = 121 mΩ at V_{GS} = -2.5 V, I_D = -0.7 A

- Very low $r_{DS(on)}$ Mid Voltage P-channel Silicon Technology Optimised for Low Qg

- This product is optimised for fast switching applications as well as load switch applications
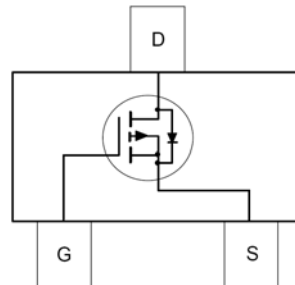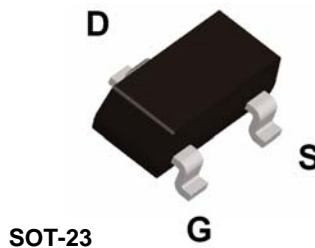
- 100% UIL Tested

- RoHS Compliant

General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been optimized for the on-state resistance and yet maintain superior switching performance.

Applications

- Active Clamp Switch

- Load Switch

SOT-23

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		-20	V
V_{GS}	Gate to Source Voltage		±8	V
I_D	-Continuous	(Note 1a)	-1.15	A
	-Pulsed	(Note 4)	-33	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	13	mJ
P_D	Power Dissipation	(Note 1a)	1.6	W
	Power Dissipation	(Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	80	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	180	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDV045P20L	FDV045P20L	SOT-23	7 "	8 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units

Off Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-18		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V			±100	nA

On Characteristics (Note 2)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-0.5	-0.9	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		3		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -4.5 V, I_D = -1.15 A		86	108	mΩ
		V_{GS} = -2.5 V, I_D = -0.7 A		97	121	
		V_{GS} = -1.8 V, I_D = -0.5 A		121	160	
		V_{GS} = -4.5 V, I_D = -1.15A, T_J = 125 °C		110	138	
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -1.15 A		3		S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1 MHz		812	1220	pF
C_{oss}	Output Capacitance			119	167	pF
C_{rss}	Reverse Transfer Capacitance			108	151	pF
R_g	Gate Resistance			20		Ω

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -10 V, I_D = -1.15 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		8.4	17	ns
t_r	Rise Time			6.5	13	ns
$t_{d(off)}$	Turn-Off Delay Time			76	122	ns
t_f	Fall Time			26	42	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to -4.5 V		7.2	10	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to -2.5 V, V_{DD} = -10 V, I_D = -1.15A		4.4	6.2	nC
Q_{gs}	Gate to Source Gate Charge			1.2		nC
Q_{gd}	Gate to Drain "Miller" Charge			1.8		nC

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.15 A (Note 2)		-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	I_F = -1.15 A, di/dt = 100 A/μs		11	20	ns
Q_{rr}	Reverse Recovery Charge			2	10	nC

Notes:
1. $R_{θJA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{θJC}$ is guaranteed by design while $R_{θCA}$ is determined by the user's board design.
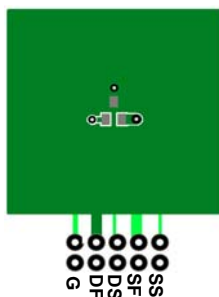
a) 80 °C/W when mounted on a 1 in^2 pad of 2 oz copper

b) 180 °C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25 °C; P-ch: L = 3 mH, I_{AS} = -3 A, V_{DD} = -20 V, V_{GS} = -6.4 V.
4. Pulsed Id refer to Fig 10 SOA curve for more details.

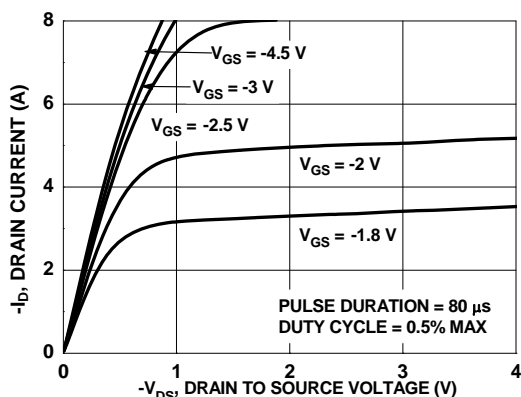## Typical Characteristics T_J = 25 °C unless otherwise noted.
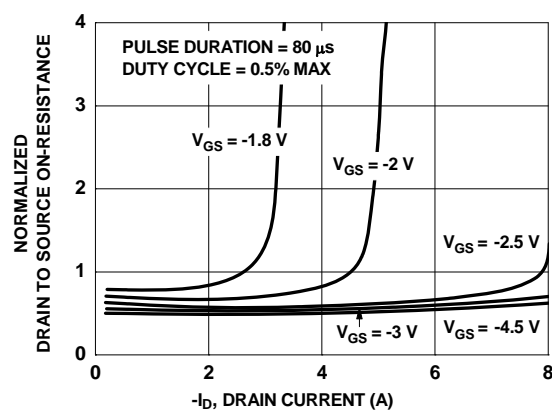
Figure 1. On Region Characteristics

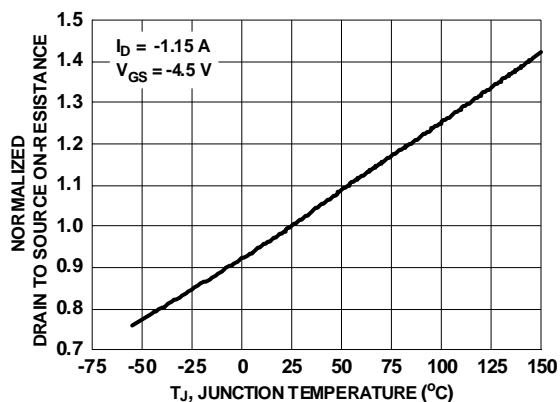**Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage**

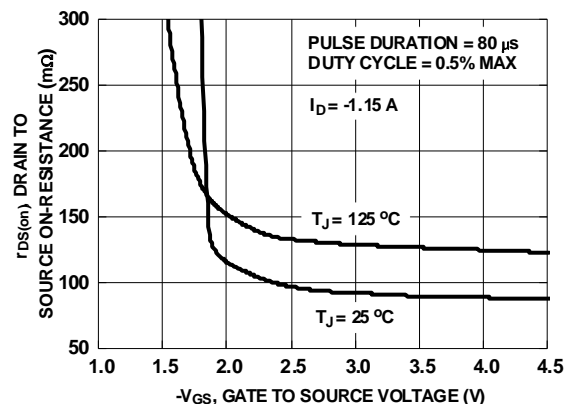**Figure 3. Normalized On Resistance vs. Junction Temperature**
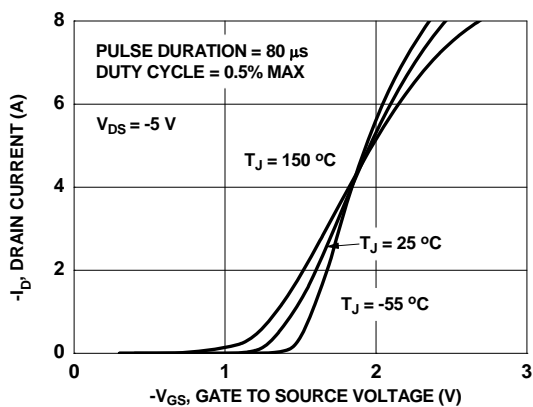
Figure 4. On-Resistance vs. Gate to Source Voltage
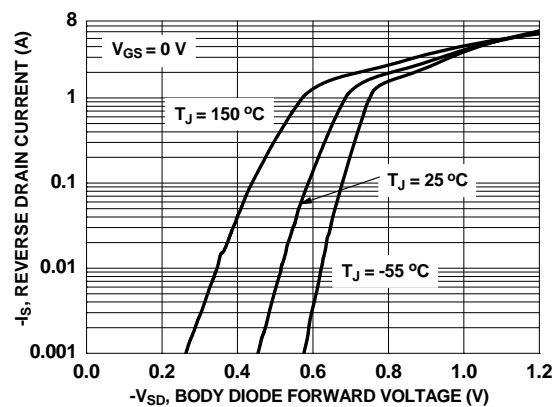
Figure 5. Transfer Characteristics

Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

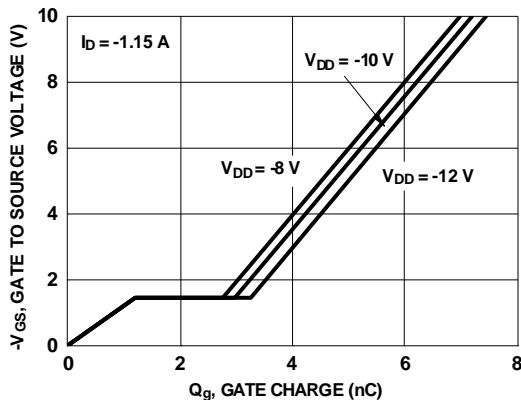## Typical Characteristics T_J = 25 °C unless otherwise noted.

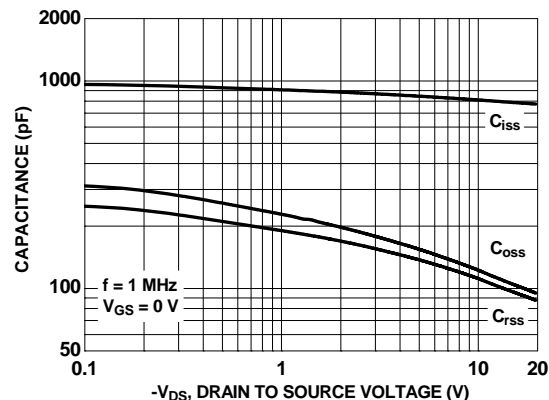**Figure 7. Gate Charge Characteristics**

Figure 8. Capacitance vs. Drain to Source Voltage
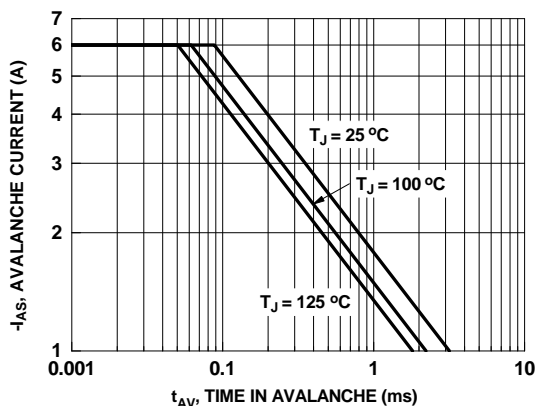

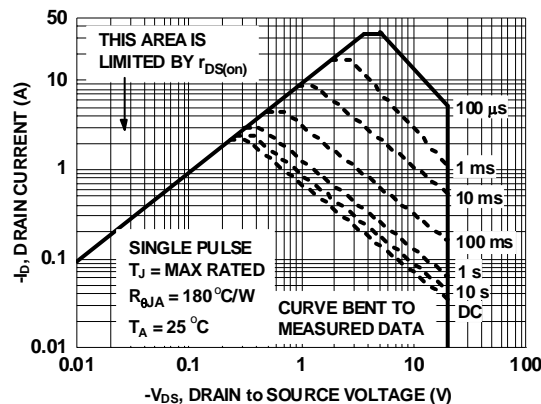
Figure 9. Unclamped Inductive Switching Capability

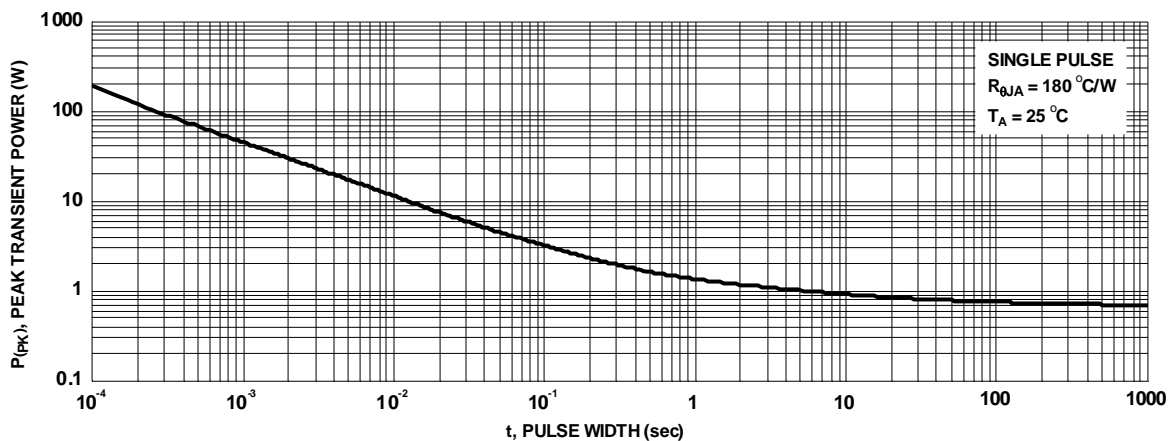**Figure 10. Forward Bias Safe Operating Area**

Figure 11. Single Pulse Maximum Power Dissipation

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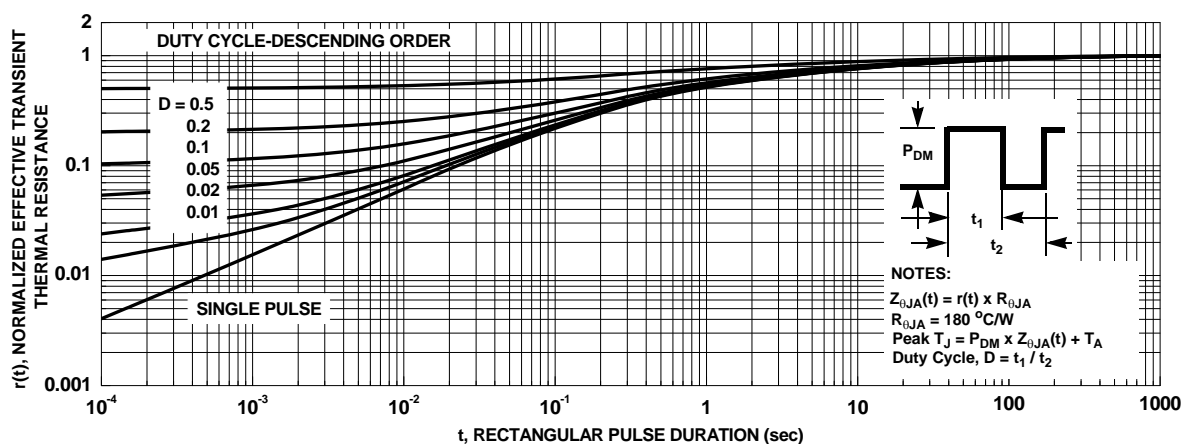**Typical Characteristics** T_J = 25 °C unless otherwise noted.

Figure 12. Junction-to-Ambient Transient Thermal Response Curve

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I77

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