

**Circuits
from the Lab™**
Reference Circuits

Circuits from the Lab™ reference circuits are engineered and tested for quick and easy system integration to help solve today's analog, mixed-signal, and RF design challenges. For more information and/or support, visit www.analog.com/CN0253.

Devices Connected/Referenced

ADG5408/	High Voltage Latch-Up Proof, 4-/8-Channel Multiplexers
ADG5409	
AD8226	Wide Supply Range, Rail-to-Rail Output Instrumentation Amplifier

A Robust, Low Power, Battery Monitoring Circuit Front End

EVALUATION AND DESIGN SUPPORT

Circuit Evaluation Boards

[CN-0253 Circuit Evaluation Board \(EVAL-CN0253-SDPZ\)](#)

[System Demonstration Platform \(EVAL-SDP-CS1Z\)](#)

Design and Integration Files

[Schematics, Layout Files, Bill of Materials](#)

CIRCUIT FUNCTION AND BENEFITS

The circuit shown in Figure 1 is a robust battery monitoring front end designed for environments where transients are likely to occur, such as in industrial or process automation environments. The circuit uses the [ADG5408](#) 8-channel CMOS multiplexer followed by the [AD8226](#) instrumentation amplifier to provide accurate voltage monitoring of individual cells at low power and low cost, and requires no additional external transient protection circuitry.

Transient overvoltage conditions may cause traditional CMOS switches to experience latch up. In junction isolation technology, the N- and P-wells of the PMOS and NMOS transistors form a parasitic silicon-controlled rectifier (SCR) circuit. An overvoltage condition triggers this SCR, causing a significant amplification of current that, in turn, leads to latch-up. Latch-up is an undesirable, high current state that can lead to device failure and can persist until the power supply is turned off.

Latch-up can occur if either the input or the output pin voltage exceeds the supply rail by more than a diode drop, or by improper power supply sequencing. If a fault occurs on the channel, and the signal exceeds the maximum rating, the fault can trigger the latch-up state in a typical CMOS part.

During circuit power up, it is also possible for voltages to occur on inputs before power is applied to the CMOS switch, especially if multiple supplies are used to power the circuit. This condition may exceed the maximum rating of the device and trigger a latch-up state.

The two multiplexers and the instrumentation amplifier (IA) used in this design have robust inputs. The [ADG5408](#) is a high voltage 8:1 multiplexer that is latch-up proof. The trench isolation technology used in the fabrication of the [ADG5408](#) prevents the latch-up state and reduces the need for external protection circuitry. Latch-up proof does not guarantee overvoltage protection and only means the switch does enter the high current SCR mode. The [ADG5408](#) also has an electrostatic discharge (ESD) rating of 8 kV human body model (ANSI/ESDA/JEDEC JS-001-2010).

The [AD8226](#) is a low cost, low power, instrumentation amplifier with robust inputs and can handle input voltages up to 40 V from the opposite supply rail, while restricting the output to within the rails. For instance, with ± 18 V supplies, the positive or negative input of the [AD8226](#) can swing between ± 22 V with no damage. All inputs of the [AD8226](#) are protected against ESD with internal diodes.

CIRCUIT DESCRIPTION

Battery monitoring systems (BMS) require the individual voltage across each battery in a battery stack to assess the state of charge (SOC) and state of health (SOH) of the battery. By multiplexing the terminals of a stack of batteries with two multiplexers, as shown in Figure 1, the voltage across each battery can be assessed.

One multiplexer is used for the positive terminal and another for the negative terminal. This differential multiplexing allows the use of a single instrumentation amplifier for up to eight channels. The amplifier then removes the common-mode voltage from each of the batteries for use by the BMS.

The [ADG5408](#) has a low on-resistance per channel, typically $13.5\ \Omega$, and a maximum of $22\ \Omega$ over temperature. With a maximum of $2\ nA$ input offset current, there is a maximum of $44\ nV$ error voltage across the channel resistances.

Rev. A

Circuits from the Lab™ circuits from Analog Devices have been designed and built by Analog Devices engineers. Standard engineering practices have been employed in the design and construction of each circuit, and their function and performance have been tested and verified in a lab environment at room temperature. However, you are solely responsible for testing the circuit and determining its suitability and applicability for your use and application. Accordingly, in no event shall Analog Devices be liable for direct, indirect, special, incidental, consequential or punitive damages due to any cause whatsoever connected to the use of any Circuits from the Lab circuits. (Continued on last page)

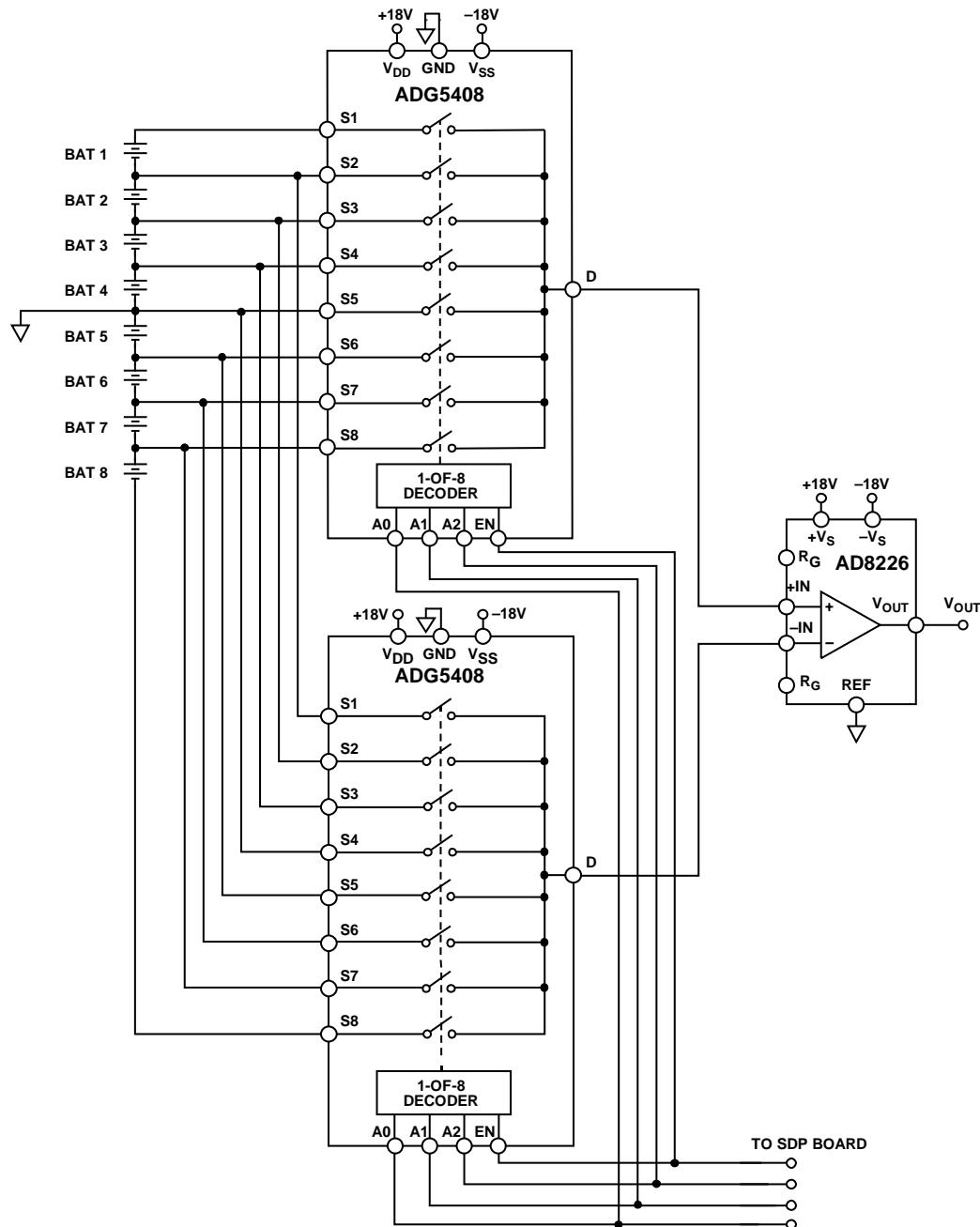


Figure 1. Robust Battery Monitoring Circuit Simplified Schematic (All Connections and Decoupling Not Shown)

10374-001

Figure 2 shows the comparison of results between a typical CMOS switch, with epitaxial layer, and the [ADG5408](#) when subjected to a latch-up test. During the test, a stress current is applied to the pin for 1 ms, called the trigger, and the current at the pin is measured after the trigger. This particular test is conducted with the switch set to open, the drain (D) set to VDD, and the source (S) set to VSS, as depicted in Figure 3. The voltage of the source is then driven beyond VSS until the required trigger current is achieved. If latch-up has not occurred, then the current at the pin returns to its pretrigger value. After latch-up has occurred, the pin continues to draw current without being driven by the trigger voltage. This can only be stopped by powering down the part.

From Figure 2, it can be seen that this typical CMOS switch reaches a latch-up current at -290 mA, while the [ADG5408](#) did not latch up until the test ended at -510 mA.

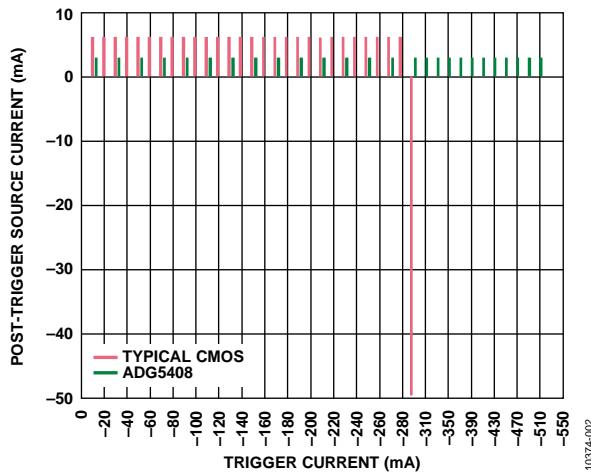


Figure 2. Post Latch-Up Trigger Current Comparison

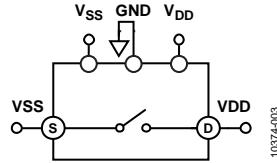


Figure 3. Latch-Up Test Configuration (Pretrigger) Common Variations

COMMON VARIATIONS

For applications where four or less batteries are used in a stack, the four differential channels of a single [ADG5409](#) can be used. The [ADG5409](#) switches four differential inputs to a single differential output and has the same latch-up proof construction as the [ADG5408](#).

CIRCUIT EVALUATION AND TEST

This circuit uses the [EVAL-CN0253-SDPZ](#) board and can be used as a standalone board, or in conjunction with the [EVAL-SDP-CS1Z](#) system demonstration platform (SDP) evaluation board. In the standalone mode, the A0, A1, A2, and EN logic levels can be controlled by links on the board or from external sources connected to the board via SMB connectors.

If computer control is desired, the [EVAL-SDP-CS1Z](#) is connected to the [EVAL-CN0253-SDPZ](#) board using 120-pin mating connectors.

Equipment Needed

- [EVAL-CN0253-SDPZ](#) board
- ± 18 V power supply
- L-ion batteries
- Digital voltmeter to measure output

If controlling the [EVAL-CN0253-SDPZ](#) board using a PC is required, additional requirements include the following:

- PC with a USB port and Windows® XP or Windows Vista® (32/64-bit) or Windows 7 (32/64-bit)
- [EVAL-SDP-CS1Z](#) SDP
- [CN-0253](#) evaluation software

Getting Started

In standalone usage only, the [EVAL-CN0253-SDPZ](#), power supplies, and test batteries are required.

To program the board with the PC, install the evaluation software. To do this, load the evaluation software by placing the [CN-0253](#) evaluation software CD in the CD drive of the PC. Using **My Computer**, locate the drive that contains the evaluation software CD and open the **Readme** file and follow the instructions for installing and using the evaluation software.

Functional Block Diagram of Test Setup

Figure 4 shows the test setup functional block diagram. The [EVAL-CN0253-SDPZ-SCH-Rev0.pdf](#) file contains the complete circuit schematics for the board. This file is contained in the [CN-0253](#) Design Support Package: (<http://www.analog.com/CN0253-DesignSupport>).

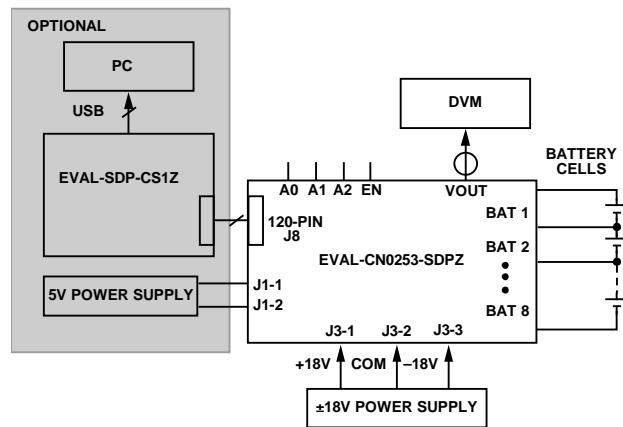


Figure 4. Test Setup Functional Block Diagram

10374-004

Setup

With the power output of the supply off, connect a +18 V power supply to the J3-1 pin (VDD_EXT), a -18 V power supply to the J3-3 pin (VSS_EXT), and the ground connection to the J3-2 pin (GND_EXT). Attach the test battery cells to the battery connections. Ensure that the link headers are retained on the battery connections that do not have batteries connected; that is, if only using four batteries, the remaining four battery connections should remain connected.

If computer control of the board is required, it is important to remove the link headers: EN, A0, A1, and A2. If using the EVAL-SDP-CS1Z, connect the EVAL-SDP-CS1Z to the EVAL-CN0253-SDPZ using the 120-pin connector. Secure the connection using the Nylon hardware.

Test

Apply power to the ± 18 V supply. Use the EN link on the board to enable the outputs from the ADG5408 multiplexers. Use the A0, A1, and A2 links on the board to select the battery for testing. The SMB connector, VOUT, can be used to connect to a separate ADC evaluation board, such as the EVAL-AD7298SDZ or manually tested using a digital voltmeter.

If computer control is required, connect the EVAL-SDP-CS1Z to the PC using the USB cable. Launch the CN-0253 evaluation software. The battery voltage can be tested as per the manual test. An additional 5 V power supply pin is provided if using the EVAL-SDP-CS1Z.

LEARN MORE

CN-0253 Design Support Package:

<http://www.analog.com/CN0253-DesignSupport>

Ardizzone, John. *A Practical Guide to High-Speed Printed-Circuit-Board Layout*, Analog Dialogue 39-09, September 2005.

Redmond, Catherine, *Winning the Battle Against Latchup in CMOS Analog Switches*, Analog Dialogue Volume 35, Number 5, October, 2001, Analog Devices.

MT-031 Tutorial, *Grounding Data Converters and Solving the Mystery of "AGND" and "DGND"*, Analog Devices.

MT-069 Tutorial, *In-Amp Input Overvoltage Protection*, Analog Devices.

MT-088 Tutorial, *Analog Switches and Multiplexers Basics*, Analog Devices.

MT-092 Tutorial, *Electrostatic Discharge (ESD)*, Analog Devices.

MT-101 Tutorial, *Decoupling Techniques*, Analog Devices.

Data Sheets and Evaluation Boards

CN-0253 Circuit Evaluation Board (EVAL-CN0253-SDPZ)

System Demonstration Platform (EVAL-SDP-CB1Z)

ADG5408 Data Sheet and Evaluation Board

ADG5409 Data Sheet and Evaluation Board

AD8226 Data Sheet and Evaluation Board

REVISION HISTORY

5/12—Rev. 0 to Rev. A

Changed 4-Channel to 8-Channel in Circuit Function and Benefits Section1

4/12—Revision 0: Initial Version

(Continued from first page) Circuits from the Lab circuits are intended only for use with Analog Devices products and are the intellectual property of Analog Devices or its licensors. While you may use the Circuits from the Lab circuits in the design of your product, no other license is granted by implication or otherwise under any patents or other intellectual property by application or use of the Circuits from the Lab circuits. Information furnished by Analog Devices is believed to be accurate and reliable. However, Circuits from the Lab circuits are supplied "as is" and without warranties of any kind, express, implied, or statutory including, but not limited to, any implied warranty of merchantability, noninfringement or fitness for a particular purpose and no responsibility is assumed by Analog Devices for their use, nor for any infringements of patents or other rights of third parties that may result from their use. Analog Devices reserves the right to change any Circuits from the Lab circuits at any time without notice but is under no obligation to do so.

©2012 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
CN10374-0-5/12(A)

