This version (31 Aug 2020 17:50) was ***approved*** by mhennerich.
The Previously approved version (10 Mar 2020 16:43) is available.

# AD-FMCOMMS8-EBZ

**Available early 2020**

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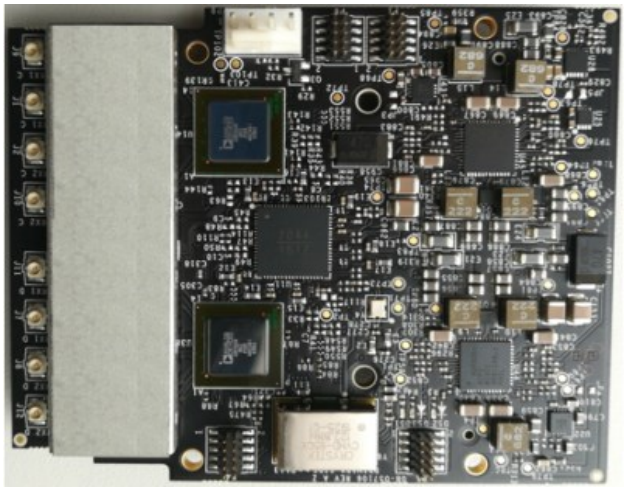
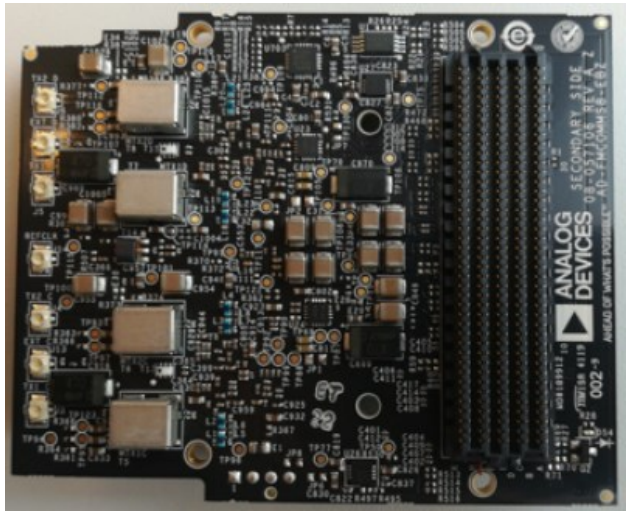
## Introduction

The AD-FMCOMMS8-EBZ is an integrated RF design containing two Analog Devices ADRV9009 wideband transceivers. By connecting to a compatible FPGA development board that supports FMC HPC mechanical connector and JESD204B bus interface it can be used for prototyping with upto 4 Transmit and Receive channels that can be synchronised in phase and frequency. Additionally it can be used with the ADRV9009-ZU11EG RF-SOM system allowing for 8 phase and frequency synchronised Transmit and Receive channels for complex multi-stream applications ensuring end-to-end deterministic latency.

The ADRV9009 Transceivers include integrated LO and phase synchronization. Overall system frequency & phase synchronization is maintained with a clock tree structure using ADI high performance low jitter HMC7044 device, making it ideal for applications requiring RF phase alignment with a large number of channels.

## Highlevel Specification



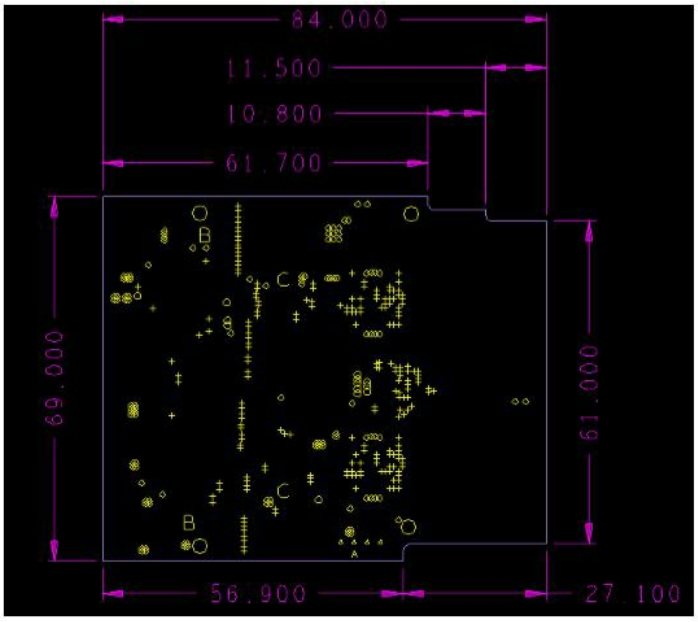


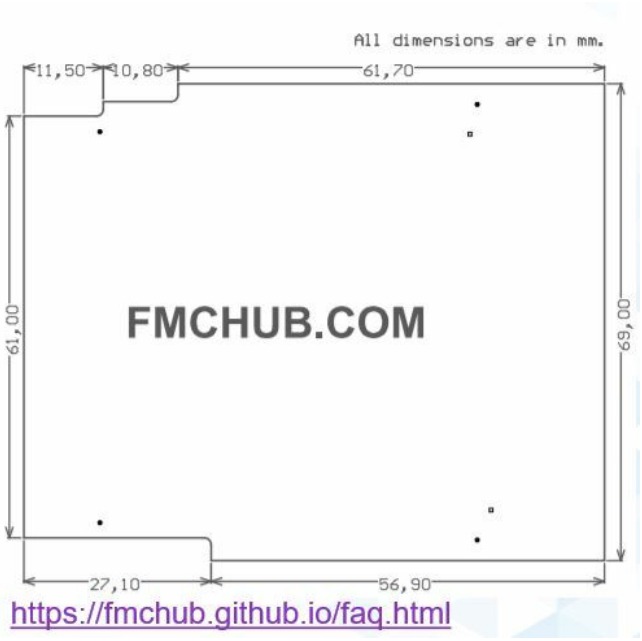

- Two ADRV9009 devices, providing (in total):
  - Quad transmitters
  - Quad receivers
  - Quad input Observation Receiver for DPD
  - Max Rx BW: 200 MHz
  - Max Tunable Tx synthesis BW: 450 MHz
  - Max Observation Rx BW: 450MHz
  - Fully integrated fractional-N RF synthesizers
  - Multi-chip phase synchronization for all RF LO and baseband clocks
  - Tuning range: 75 MHz to 6000 MHz
- FMC HPC Compatible interface
- Complies with VITA 57.1 mechanical dimensions 84mm x 69mm(not full compliance with keep out areas)
- Platform development environment support includes Industry standard Linux Industrial I/O (IIO) Applications, MATLAB®, Simulink®, and GNU Radio, and streaming interfaces for custom C, C++, python, and C# applications
- HDL reference designs and drivers to allow zero day development

## Hardware

X-Grade Rev A Schematics

X-Grade Rev A BOM

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# Getting Started

The following is leveraged directly from the ADRV9009-ZU11EG RF-SOM site.

1. Quick Start Guides
    1. FMCOMMS8 Quick Start Guide
    2. ADRV9009-ZU11EG Quick Start Guide
    3. Configure a pre-existing SD-Card
2. Linux Applications
    1. IIO Scope
        1. ADRV9009/ADRV9008 IIO Scope View
        2. ADRV9009/ADRV9008 Control IIO Scope Plugin
        3. Advanced ADRV9009/ADRV9008 Control IIO Scope Plugin
    2. FRU EEPROM Utility
3. Push custom data into/out of the ADRV9009
    1. Basic Data files and formats
    2. Stream data into/out of MATLAB
4. Design with the ADRV9009
5. Understanding the ADRV9009
    1. ADRV9009 Product page
    2. Full Datasheet and chip design package
    3. MATLAB Filter Wizard / Profile Generator for ADRV9009
6. Hardware in the Loop / How to design your own custom BaseBand
    1. GNU Radio
    2. Board Support Package for MathWorks Tools
7. Design with the ADRV9009-ZU11EG based platform
    1. Linux software
        1. ADRV9009/ADRV9008 Linux Device Driver
            1. ADRV9009/ADRV9008 Device Driver Customization
            2. Customizing the devicetree on the target
        2. JESD204 (FSM) Interface Linux Kernel Framework
        3. HMC7044 Clock Jitter Attenuator with JESD204B Linux Driver
        4. AXI-DMAC DMA Controller Linux Driver
        5. JESD204B Transmit Linux Driver
            1. JESD204B Status Utility
        6. JESD204B Receive Linux Driver
            1. JESD204B Status Utility
        7. AXI JESD204B GT HDL Linux Driver
            1. JESD204 Eye Scan
        8. AXI ADC HDL Linux Driver
        [illegible]ux Driver

2. ADRV9009/ADRV9008 No-OS System Level Design Setup
3. HDL Reference Design

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