

# ESD Protection Diode

## Low Capacitance ESD Protection for High Speed Data

### NUP2114 Series, SNUP2114

The NUP2114 surge protection is designed to protect high speed data lines from ESD. Ultra-low capacitance and high level of ESD protection makes this device well suited for use in USB 2.0 applications.

#### Features

- Low Capacitance 0.8 pF
- Low Clamping Voltage
- Stand Off Voltage: 5 V
- Low Leakage
- ESD Rating of Class 3B (Exceeding 8 kV) per Human Body model and Class C (Exceeding 400 V) per Machine Model
- Protection for the Following IEC Standards:  
IEC 61000-4-2 Level 4 ESD Protection
- UL Flammability Rating of 94 V-0
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Typical Applications

- High Speed Communication Line Protection
- USB 2.0 High Speed Data Line and Power Line Protection
- Monitors and Flat Panel Displays
- MP3
- Gigabit Ethernet
- Notebook Computers
- Digital Video Interface (DVI) and HDMI

#### MAXIMUM RATINGS (T<sub>J</sub> = 25 °C unless otherwise noted)

| Rating                                                                                    | Symbol           | Value                          | Unit |
|-------------------------------------------------------------------------------------------|------------------|--------------------------------|------|
| Operating Junction Temperature Range                                                      | T <sub>J</sub>   | -40 to +125                    | °C   |
| Storage Temperature Range                                                                 | T <sub>stg</sub> | -55 to +150                    | °C   |
| Lead Solder Temperature - Maximum (10 Seconds)                                            | T <sub>L</sub>   | 260                            | °C   |
| Human Body Model (HBM)<br>Machine Model (MM)<br>IEC 61000-4-2 Contact<br>IEC61000-4-2 Air | ESD              | 16000<br>400<br>13000<br>15000 | V    |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

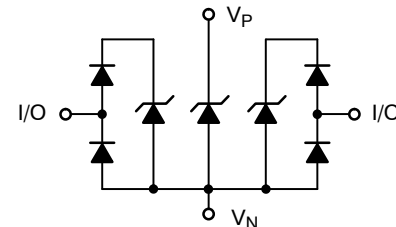
See Application Note [AND8308/D](#) for further description of survivability specs.



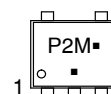
SOT-553  
CASE 463B



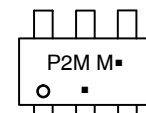
TSOP-6  
CASE 318G



#### MARKING DIAGRAMS



SOT-553

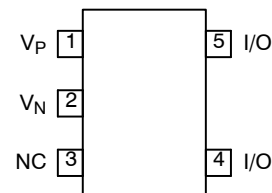


TSOP-6

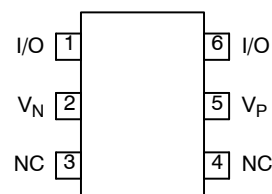
P2, P2M = Specific Device Code  
M = Date Code  
■ = Pb-Free Package

(Note: Microdot may be in either location)

#### PIN CONNECTIONS



SOT-553



TSOP-6

#### ORDERING INFORMATION

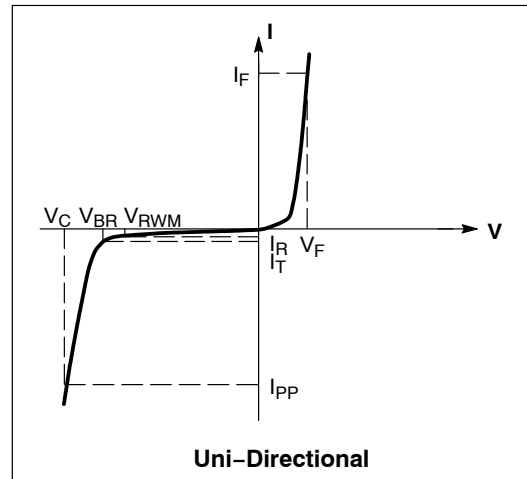
See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

| Symbol    | Parameter                                      |
|-----------|------------------------------------------------|
| $I_{PP}$  | Maximum Reverse Peak Pulse Current             |
| $V_C$     | Clamping Voltage @ $I_{PP}$                    |
| $V_{RWM}$ | Working Peak Reverse Voltage                   |
| $I_R$     | Maximum Reverse Leakage Current @ $V_{RWM}$    |
| $V_{BR}$  | Breakdown Voltage @ $I_T$                      |
| $I_T$     | Test Current                                   |
| $I_F$     | Forward Current                                |
| $V_F$     | Forward Voltage @ $I_F$                        |
| $P_{pk}$  | Peak Power Dissipation                         |
| C         | Max. Capacitance @ $V_R = 0$ and $f = 1.0$ MHz |

\* See Application Note AND8308/D for detailed explanations of datasheet parameters.



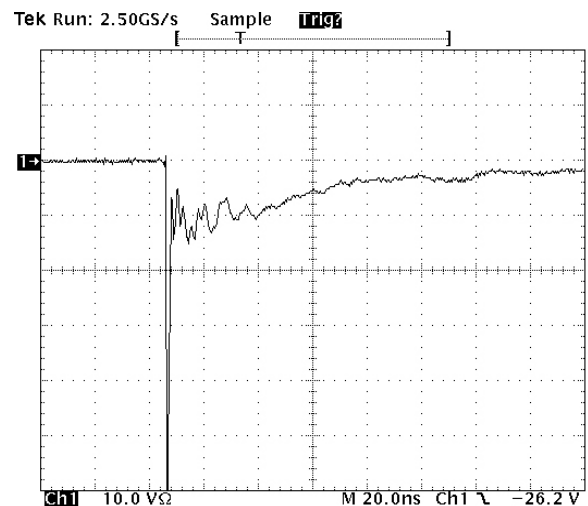
## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter                  | Symbol    | Conditions                                        | Min             | Typ  | Max | Unit          |
|----------------------------|-----------|---------------------------------------------------|-----------------|------|-----|---------------|
| Reverse Working Voltage    | $V_{RWM}$ | (Note 1)                                          |                 |      | 5.0 | V             |
| Breakdown Voltage          | $V_{BR}$  | $I_T = 1$ mA, (Note 2)                            | 5.5             | 7.5  |     | V             |
| Reverse Leakage Current    | $I_R$     | $V_{RWM} = 5$ V                                   |                 | 0.01 | 1.0 | $\mu\text{A}$ |
| Clamping Voltage           | $V_C$     | $I_{PP} = 5$ A (Note 3)                           |                 | 9.0  |     | V             |
| Clamping Voltage           | $V_C$     | $I_{PP} = 8$ A (Note 3)                           |                 | 10   |     | V             |
| Maximum Peak Pulse Current | $I_{PP}$  | 8x20 $\mu\text{s}$ Waveform                       |                 |      | 12  | A             |
| Junction Capacitance       | $C_J$     | $V_R = 0$ V, $f = 1$ MHz between I/O Pins and GND |                 | 0.8  | 1.0 | pF            |
| Junction Capacitance       | $C_J$     | $V_R = 0$ V, $f = 1$ MHz between I/O Pins         |                 |      | 0.5 | pF            |
| Clamping Voltage           | $V_C$     | @ $I_{PP} = 1$ A (Note 4)                         |                 |      | 12  | V             |
| Clamping Voltage           | $V_C$     | Per IEC 61000-4-2 (Note 5)                        | Figures 1 and 2 |      |     | V             |

1. Surge protection devices are normally selected according to the working peak reverse voltage ( $V_{RWM}$ ), which should be equal or greater than the DC or continuous peak operating voltage level.
2.  $V_{BR}$  is measured at pulse test current  $I_T$ .
3. Nonrepetitive current pulse (Pin 5 to Pin 2)
4. Surge current waveform per Figure 5.
5. Typical waveform. For test procedure see Figures 3 and 4 and Application Note AND8307/D.
6. Include S-prefix devices where applicable.



**Figure 1. ESD Clamping Voltage Screenshot**  
Positive 8 kV Contact per IEC61000-4-2



**Figure 2. ESD Clamping Voltage Screenshot**  
Negative 8 kV Contact per IEC61000-4-2

## IEC 61000-4-2 Spec.

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|-------|-------------------|------------------------|----------------------|----------------------|
| 1     | 2                 | 7.5                    | 4                    | 2                    |
| 2     | 4                 | 15                     | 8                    | 4                    |
| 3     | 6                 | 22.5                   | 12                   | 6                    |
| 4     | 8                 | 30                     | 16                   | 8                    |

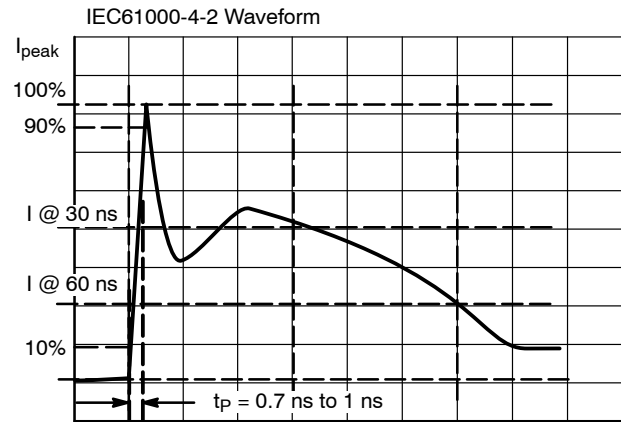


Figure 3. IEC61000-4-2 Spec

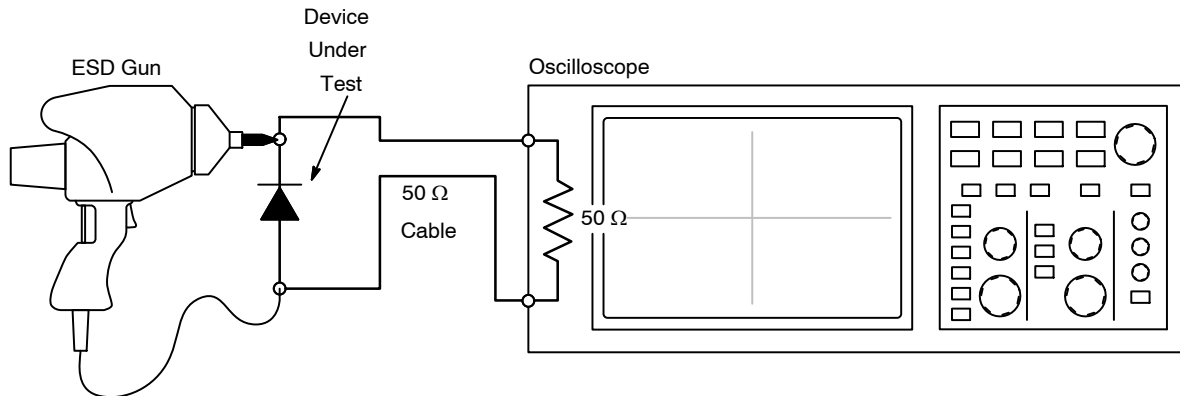


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D - Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to AND8307/D.

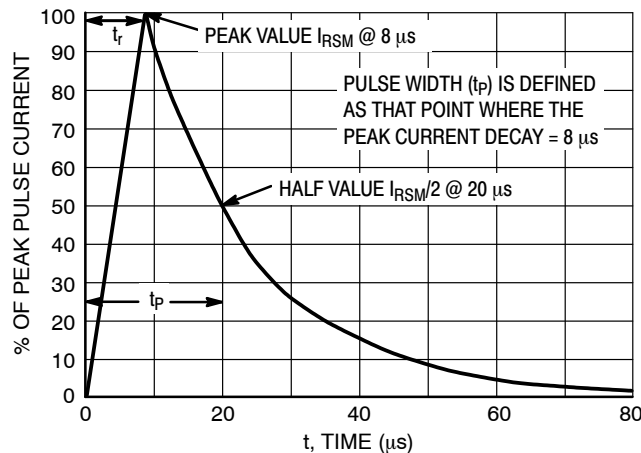


Figure 5. 8 x 20  $\mu$ s Pulse Waveform

## NUP2114 Series, SNUP2114

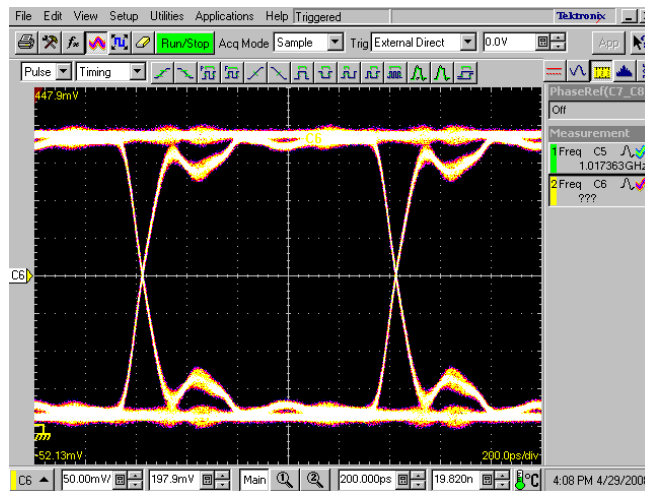


Figure 6. 500 MHz Data Pattern

### ORDERING INFORMATION

| Device            | Marking | Package              | Shipping <sup>†</sup> |
|-------------------|---------|----------------------|-----------------------|
| NUP2114UPXV5T1G   | P2      | SOT-553<br>(Pb-Free) | 4 000 / Tape & Reel   |
| NUP2114UCMR6T1G   | P2M     | TSOP-6<br>(Pb-Free)  | 3 000 / Tape & Reel   |
| SNUP2114UCMR6T1G* | P2M     | TSOP-6<br>(Pb-Free)  | 3 000 / Tape & Reel   |

<sup>†</sup> For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

\* S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

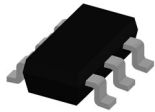
# NUP2114 Series, SNUP2114

## REVISION HISTORY

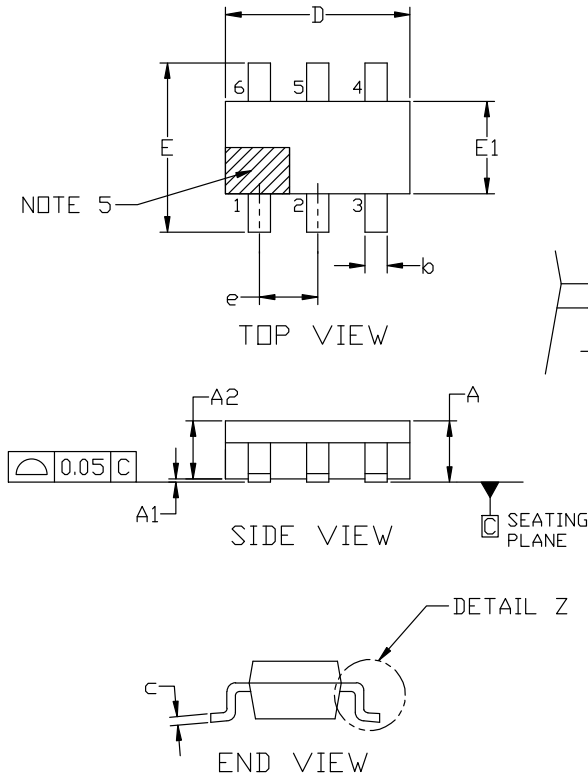
|   |                                                 |            |
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| 4 | Rebranded the document to <b>onsemi</b> format. | 11/24/2025 |
|---|-------------------------------------------------|------------|

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



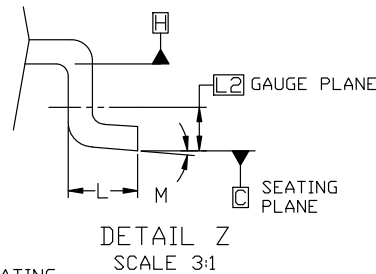

**TSOP-6 3.00x1.50x0.90, 0.95P**  
**CASE 318G**  
**ISSUE W**

DATE 26 FEB 2024

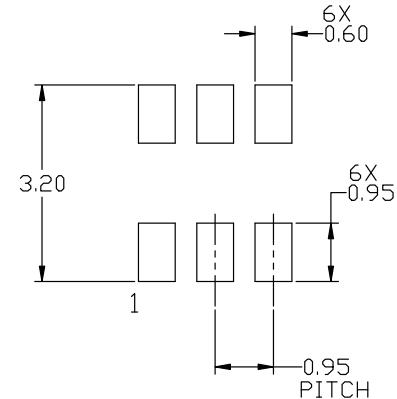


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE



| MILLIMETERS |          |      |      |
|-------------|----------|------|------|
| DIM         | MIN      | NOM  | MAX  |
| A           | 0.90     | 1.00 | 1.10 |
| A1          | 0.01     | 0.06 | 0.10 |
| A2          | 0.80     | 0.90 | 1.00 |
| b           | 0.25     | 0.38 | 0.50 |
| c           | 0.10     | 0.18 | 0.26 |
| D           | 2.90     | 3.00 | 3.10 |
| E           | 2.50     | 2.75 | 3.00 |
| E1          | 1.30     | 1.50 | 1.70 |
| e           | 0.85     | 0.95 | 1.05 |
| L           | 0.20     | 0.40 | 0.60 |
| L2          | 0.25 BSC |      |      |
| M           | 0°       | ---  | 10°  |


**RECOMMENDED MOUNTING FOOTPRINT**

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

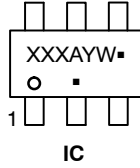
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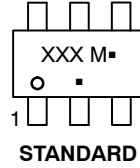
TSOP-6 3.00x1.50x0.90, 0.95P  
CASE 318G  
ISSUE W

DATE 26 FEB 2024

GENERIC  
MARKING DIAGRAM\*



IC



STANDARD

XXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

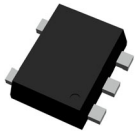
XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

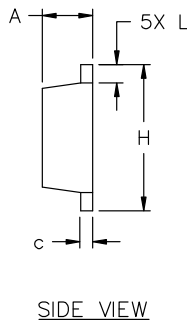
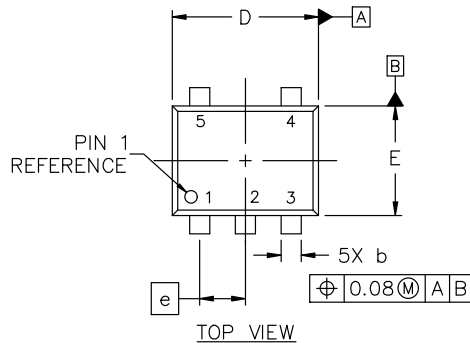
|                                                                                                   |                                                                                                               |                                                                                                              |                                                                                                      |                                                                                                            |                                                                                                       |
|---------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------|
| STYLE 1:<br>PIN 1. DRAIN<br>2. DRAIN<br>3. GATE<br>4. SOURCE<br>5. DRAIN<br>6. DRAIN              | STYLE 2:<br>PIN 1. EMITTER 2<br>2. BASE 1<br>3. COLLECTOR 1<br>4. EMITTER 1<br>5. BASE 2<br>6. COLLECTOR 2    | STYLE 3:<br>PIN 1. ENABLE<br>2. N/C<br>3. R BOOST<br>4. Vz<br>5. V in<br>6. V out                            | STYLE 4:<br>PIN 1. N/C<br>2. V in<br>3. NOT USED<br>4. GROUND<br>5. ENABLE<br>6. LOAD                | STYLE 5:<br>PIN 1. EMITTER 2<br>2. BASE 2<br>3. COLLECTOR 1<br>4. EMITTER 1<br>5. BASE 1<br>6. COLLECTOR 2 | STYLE 6:<br>PIN 1. COLLECTOR<br>2. COLLECTOR<br>3. BASE<br>4. EMITTER<br>5. COLLECTOR<br>6. COLLECTOR |
| STYLE 7:<br>PIN 1. COLLECTOR<br>2. COLLECTOR<br>3. BASE<br>4. N/C<br>5. COLLECTOR<br>6. EMITTER   | STYLE 8:<br>PIN 1. Vbus<br>2. D(in)<br>3. D(in)+<br>4. D(out)+<br>5. D(out)<br>6. GND                         | STYLE 9:<br>PIN 1. LOW VOLTAGE GATE<br>2. DRAIN<br>3. SOURCE<br>4. DRAIN<br>5. DRAIN<br>6. HIGH VOLTAGE GATE | STYLE 10:<br>PIN 1. D(OUT)+<br>2. GND<br>3. D(OUT)-<br>4. D(IN)-<br>5. VBUS<br>6. D(IN)+             | STYLE 11:<br>PIN 1. SOURCE 1<br>2. DRAIN 2<br>3. DRAIN 2<br>4. SOURCE 2<br>5. GATE 1<br>6. DRAIN 1/GATE 2  | STYLE 12:<br>PIN 1. I/O<br>2. GROUND<br>3. I/O<br>4. I/O<br>5. VCC<br>6. I/O                          |
| STYLE 13:<br>PIN 1. GATE 1<br>2. SOURCE 2<br>3. GATE 2<br>4. DRAIN 2<br>5. SOURCE 1<br>6. DRAIN 1 | STYLE 14:<br>PIN 1. ANODE<br>2. SOURCE<br>3. GATE<br>4. CATHODE/DRAIN<br>5. CATHODE/DRAIN<br>6. CATHODE/DRAIN | STYLE 15:<br>PIN 1. ANODE<br>2. SOURCE<br>3. GATE<br>4. DRAIN<br>5. N/C<br>6. CATHODE                        | STYLE 16:<br>PIN 1. ANODE/CATHODE<br>2. BASE<br>3. EMITTER<br>4. COLLECTOR<br>5. ANODE<br>6. CATHODE | STYLE 17:<br>PIN 1. EMITTER<br>2. BASE<br>3. ANODE/CATHODE<br>4. ANODE<br>5. CATHODE<br>6. COLLECTOR       |                                                                                                       |

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**SOT-553-5 1.60x1.20x0.55, 0.50P**  
**CASE 463B**  
**ISSUE D**

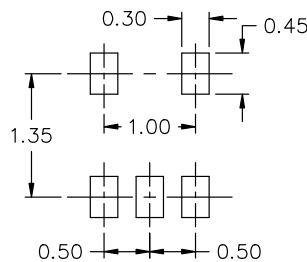
DATE 21 FEB 2024



## NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NOM. | MAX. |
| A   | 0.50        | 0.55 | 0.60 |
| b   | 0.17        | 0.22 | 0.27 |
| c   | 0.08        | 0.13 | 0.18 |
| D   | 1.55        | 1.60 | 1.65 |
| E   | 1.15        | 1.20 | 1.25 |
| e   | 0.50 BSC    |      |      |
| H   | 1.55        | 1.60 | 1.65 |
| L   | 0.10        | 0.20 | 0.30 |



## RECOMMENDED MOUNTING FOOTPRINT\*

- \* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

**GENERIC MARKING DIAGRAM\***


XX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:  
PIN 1. BASE  
2. EMITTER  
3. BASE  
4. COLLECTOR  
5. COLLECTOR

STYLE 2:  
PIN 1. CATHODE  
2. COMMON ANODE  
3. CATHODE 2  
4. CATHODE 3  
5. CATHODE 4

STYLE 3:  
PIN 1. ANODE 1  
2. N/C  
3. ANODE 2  
4. CATHODE 2  
5. CATHODE 1

STYLE 4:  
PIN 1. SOURCE 1  
2. DRAIN 1/2  
3. SOURCE 1  
4. GATE 1  
5. GATE 2

STYLE 5:  
PIN 1. ANODE  
2. EMITTER  
3. BASE  
4. COLLECTOR  
5. CATHODE

STYLE 6:  
PIN 1. EMITTER 2  
2. BASE 2  
3. EMITTER 1  
4. COLLECTOR 1  
5. COLLECTOR 2/BASE 1

STYLE 7:  
PIN 1. BASE  
2. EMITTER  
3. BASE  
4. COLLECTOR  
5. COLLECTOR

STYLE 8:  
PIN 1. CATHODE  
2. COLLECTOR  
3. N/C  
4. BASE  
5. EMITTER

STYLE 9:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. ANODE  
5. ANODE

|                         |                                        |                                                                                                                                                                                  |
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| <b>DESCRIPTION:</b>     | <b>SOT-553-5 1.60x1.20x0.55, 0.50P</b> | <b>PAGE 1 OF 1</b>                                                                                                                                                               |

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