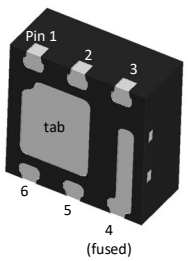
MOSFET

OptiMOS™ 5 Power-Transistor, 30 V

PG-VSON-6



Features

- Lowest on-resistance $R_{DS(on)}$ in a 2x2 package
- Optimized for highest performance and power density
- 100% avalanche tested
- Superior thermal resistance for a 2x2 package
- N-channel
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

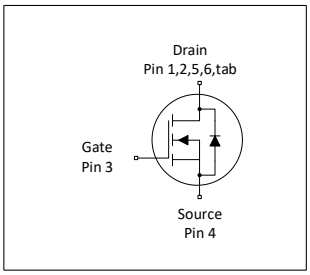


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	30	V
$R_{DS(on),max}$	3.6	mΩ
I_D	81	A
Q_{oss}	8.2	nC
Q_G(0V..4.5V)	7.2	nC

Type / Ordering Code	Package	Marking	Related Links
ISK036N03LM5	PG-VSON-6	3603	-

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1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- - -	- - -	81 51 16.5	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=4.5 V, T_A=25 °C, R_{thJA}=60 °C/W[2]
Pulsed drain current[3]	$I_{D,pulse}$	-	-	323	A	T_C=25 °C
Avalanche energy, single pulse[4]	E_{AS}	-	-	7	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-16	-	16	V	-
Power dissipation	P_{tot}	- -	- -	39 2.1	W	T_C=25 °C T_A=25 °C, R_{thJA}=60 °C/W[2]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-

2 Thermal characteristics

at T_j=25 °C, unless otherwise specified

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	1.6	3.2	°C/W	-
Device on PCB, 6 cm² cooling area[2]	R_{thJA}	-	-	60	°C/W	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.
[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.
[3] See Diagram 3 for more detailed information
[4] See Diagram 13 for more detailed information

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3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.2	1.6	2.0	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=24 V, V_{GS}=0 V, T_j=25 °C V_{DS}=24 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=16 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	2.6 3.3	3.6 4.6	mΩ	V_{GS}=10 V, I_D=20 A V_{GS}=4.5 V, I_D=20 A
Gate resistance[1)]	R_G	-	0.7	1.2	Ω	-
Transconductance	g_{fs}	-	96	-	S	|V_{DS}|≥2|I_D|$R_{DS(on)max}$, I_D=20 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	1010	1300	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	270	350	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	32	56	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	7.7	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	1.4	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	14.6	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	1.5	-	ns	V_{DD}=15 V, V_{GS}=4.5 V, I_D=20 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	2.5	3.4	nC	V_{DD}=15 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	1.6	2.2	nC	V_{DD}=15 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate to drain charge	Q_{gd}	-	1.8	2.7	nC	V_{DD}=15 V, I_D=20 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	2.7	3.9	nC	V_{DD}=15 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge total	Q_g	-	7.2	9.0	nC	V_{DD}=15 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.5	-	V	V_{DD}=15 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge total	Q_g	-	15.2	20.2	nC	V_{DD}=15 V, I_D=20 A, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	8.2	10.9	nC	V_{DD}=15 V, V_{GS}=0 V

[1)] Defined by design. Not subject to production test.
[2)] See figure 16 for gate charge parameter definition. Defined by design, not subject to production test

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Table 7 Reverse diode

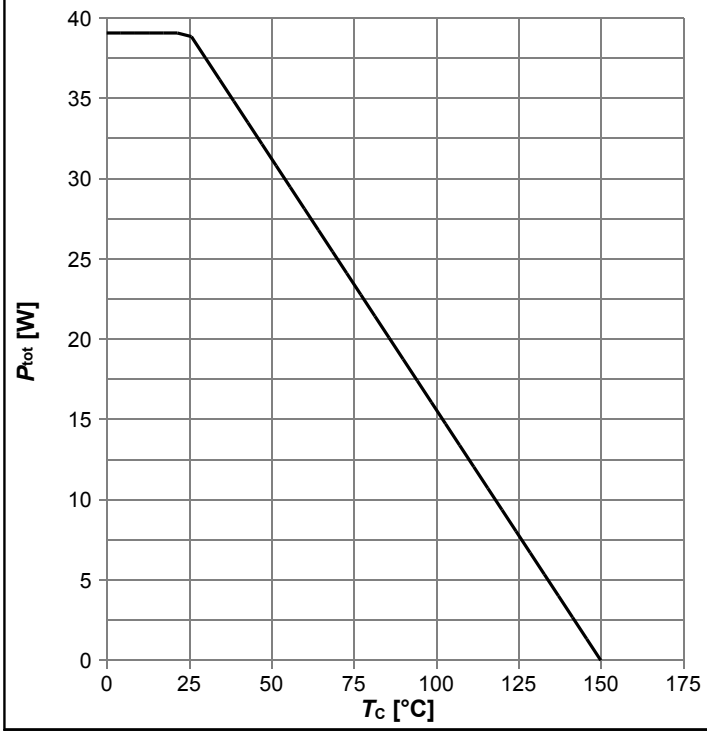
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	37	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	323	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.79	1.0	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	25.8	51.6	ns	V_R=15 V, I_F=20 A, di_F/dt=100 A/µs
Reverse recovery charge[1)]	Q_{rr}	-	17.0	34	nC	V_R=15 V, I_F=20 A, di_F/dt=100 A/µs

[1)] Defined by design. Not subject to production test.

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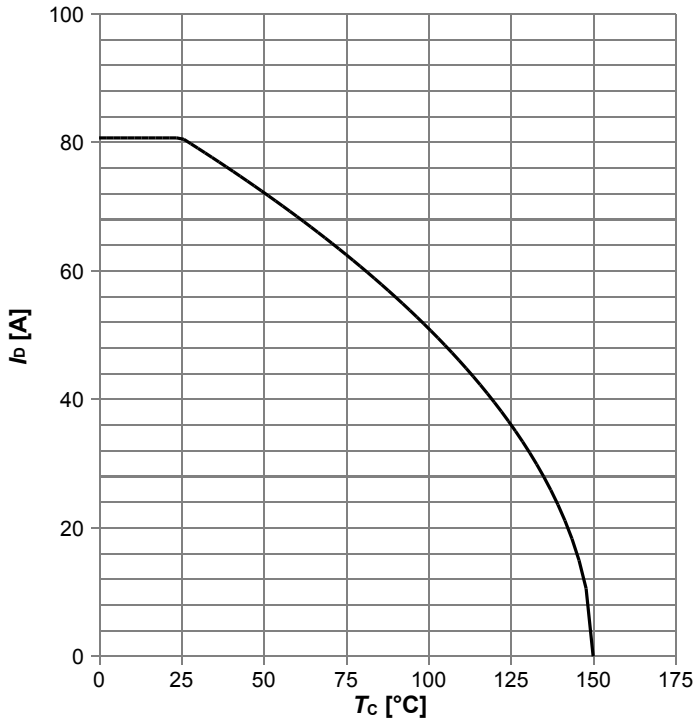
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



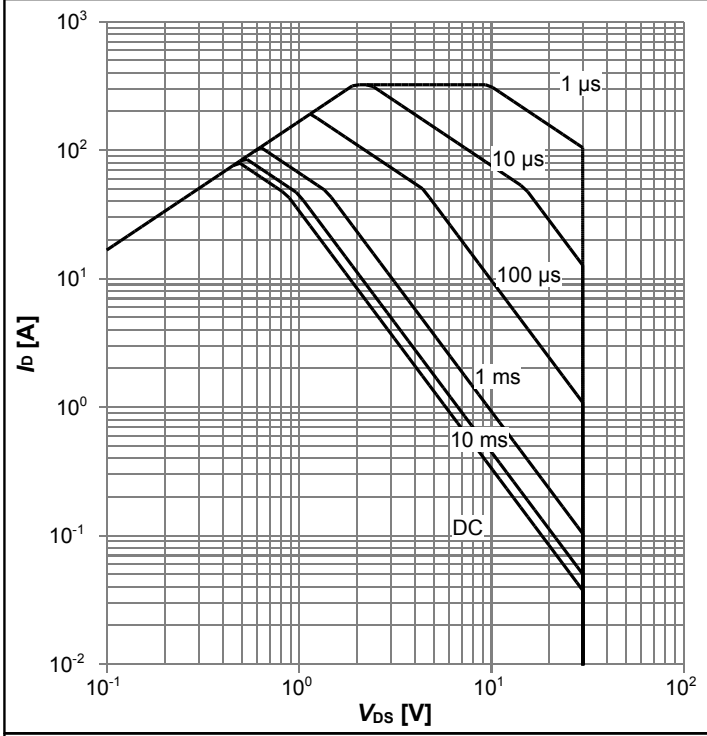
$P_{tot}=f(T_C)$

Diagram 2: Drain current



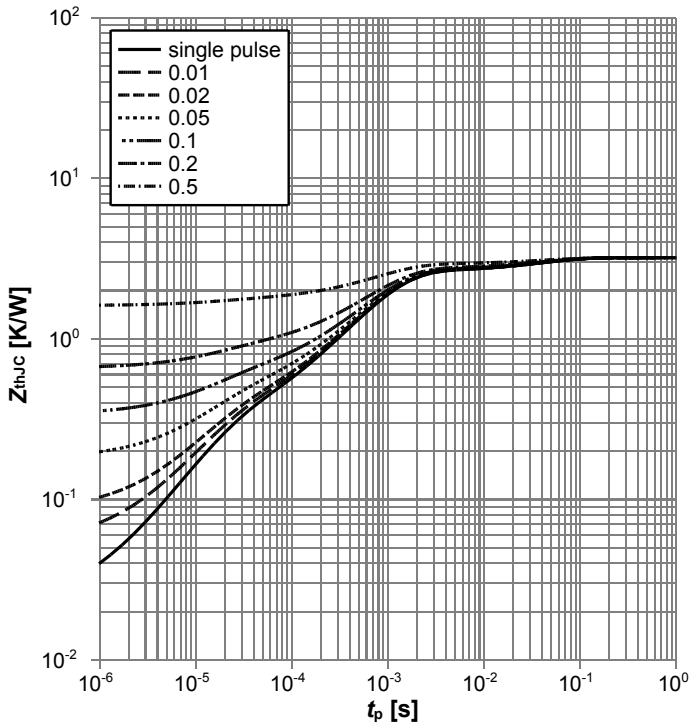
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



$I_D=f(V_{DS})$; T_C=25 °C; D=0; parameter: t_p

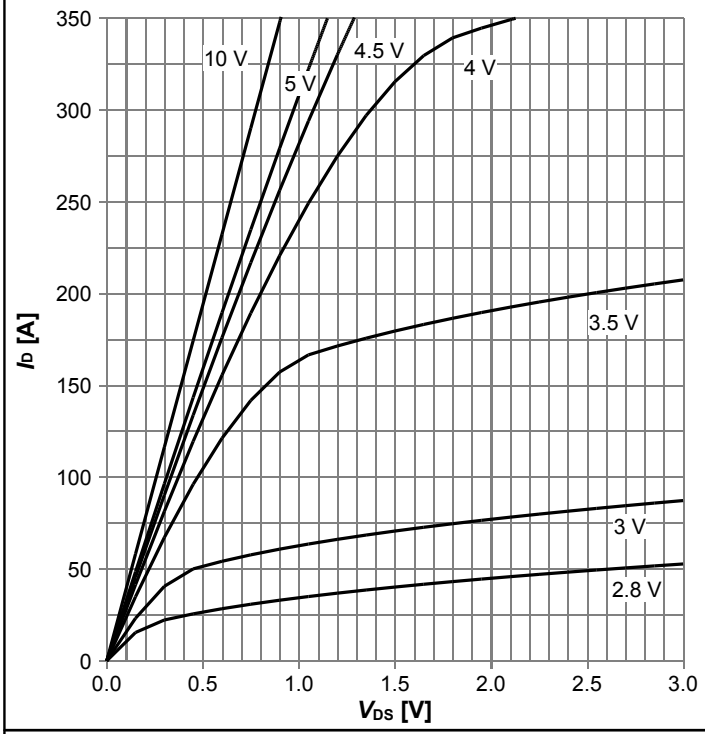
Diagram 4: Max. transient thermal impedance



$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

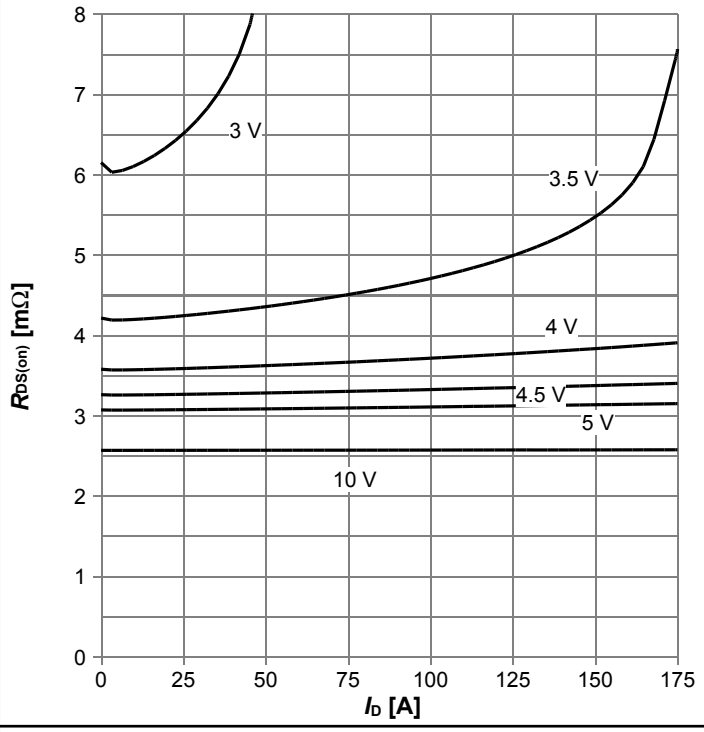
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Diagram 5: Typ. output characteristics



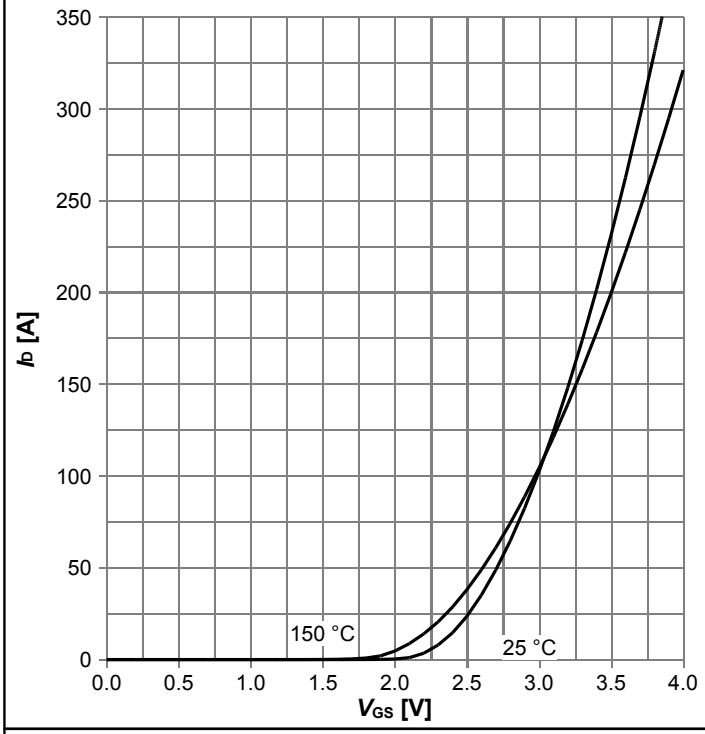
$I_D=f(V_{DS})$, $T_j=25$ °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



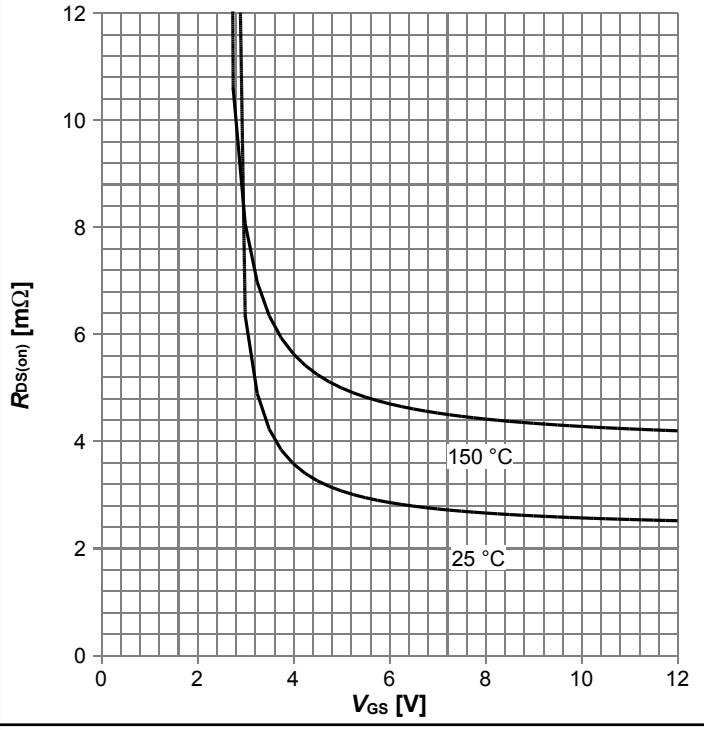
$R_{DS(on)}=f(I_D)$, $T_j=25$ °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

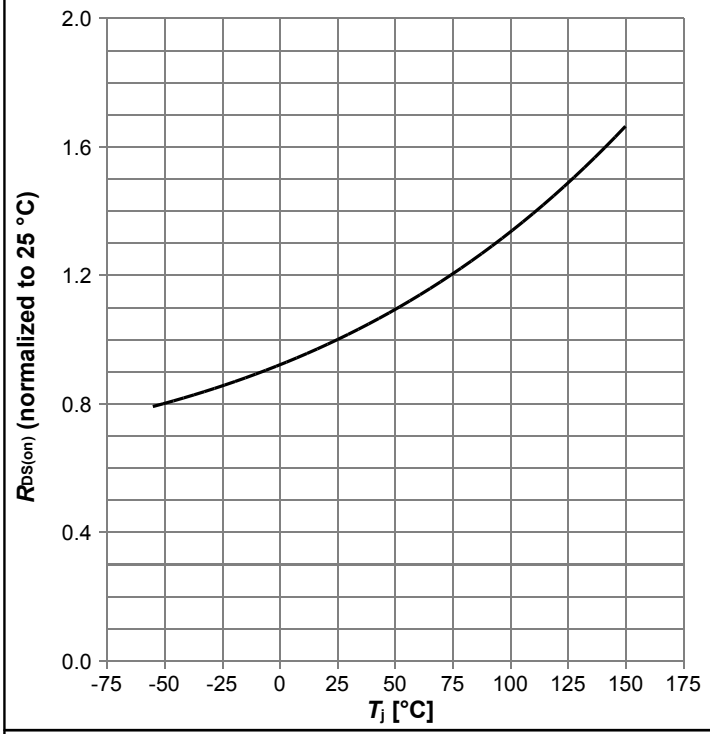
Diagram 8: Typ. drain-source on resistance



$R_{DS(on)}=f(V_{GS})$, $I_D=20$ A; parameter: T_j

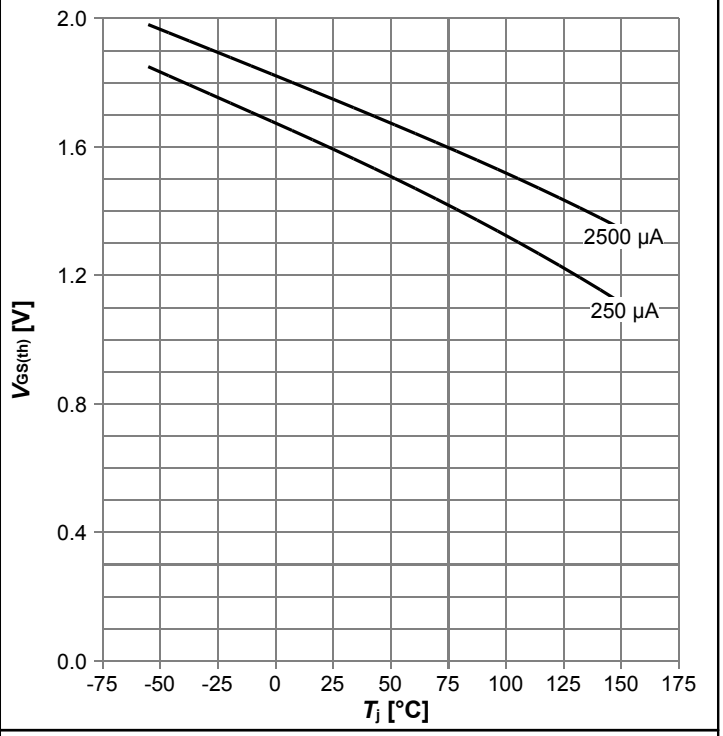
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Diagram 9: Normalized drain-source on resistance



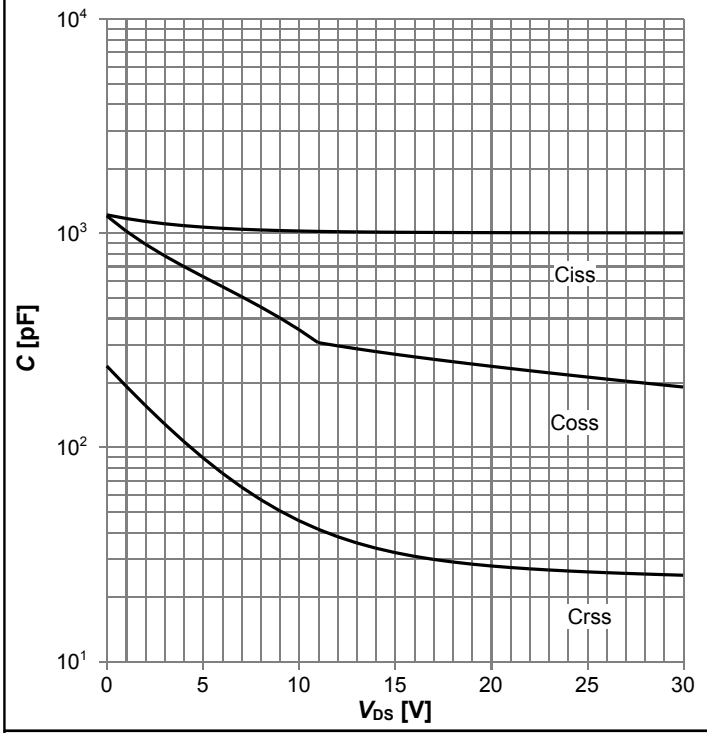
$R_{DS(on)}$=f(T_j), I_D=20 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



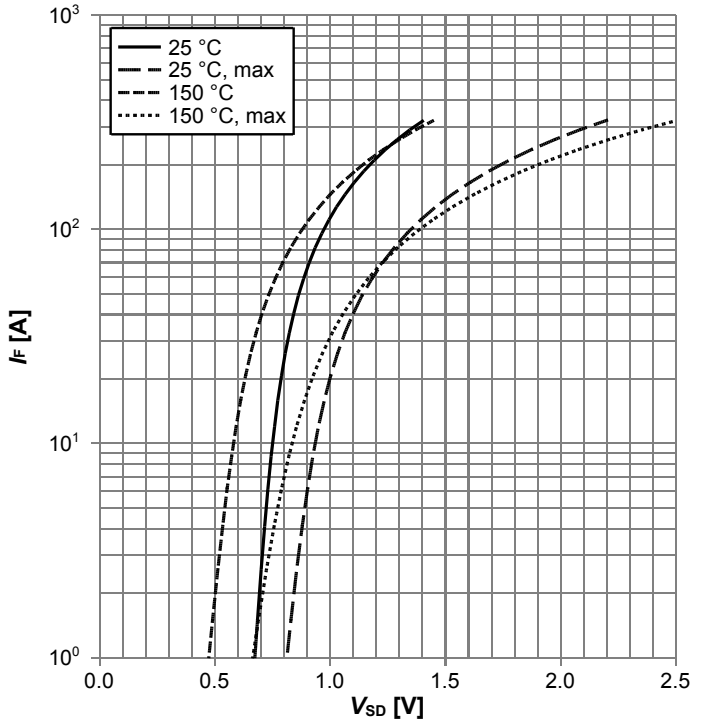
$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

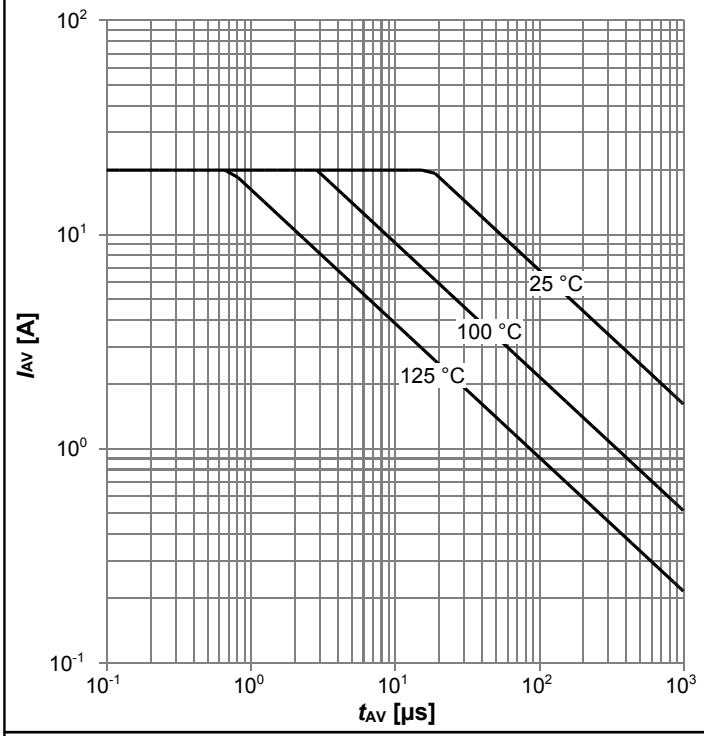
Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

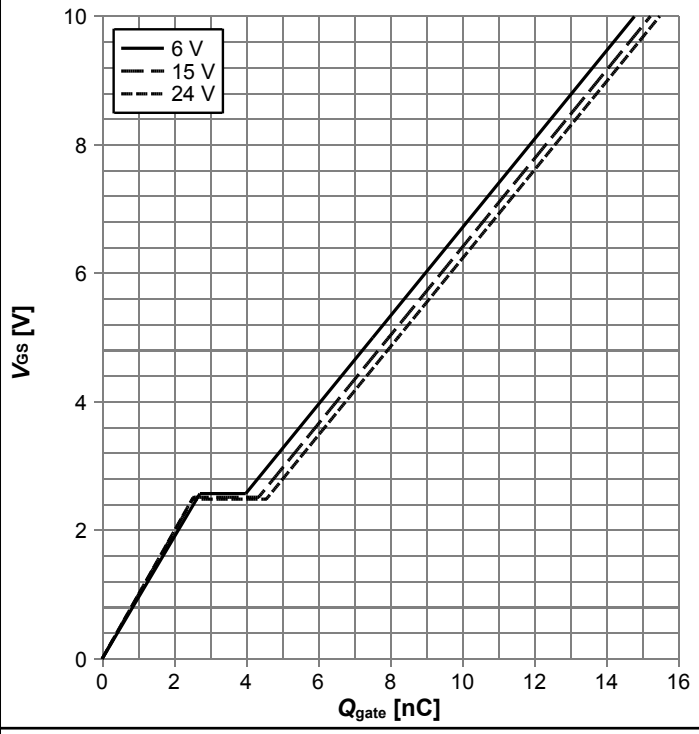
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Diagram 13: Avalanche characteristics



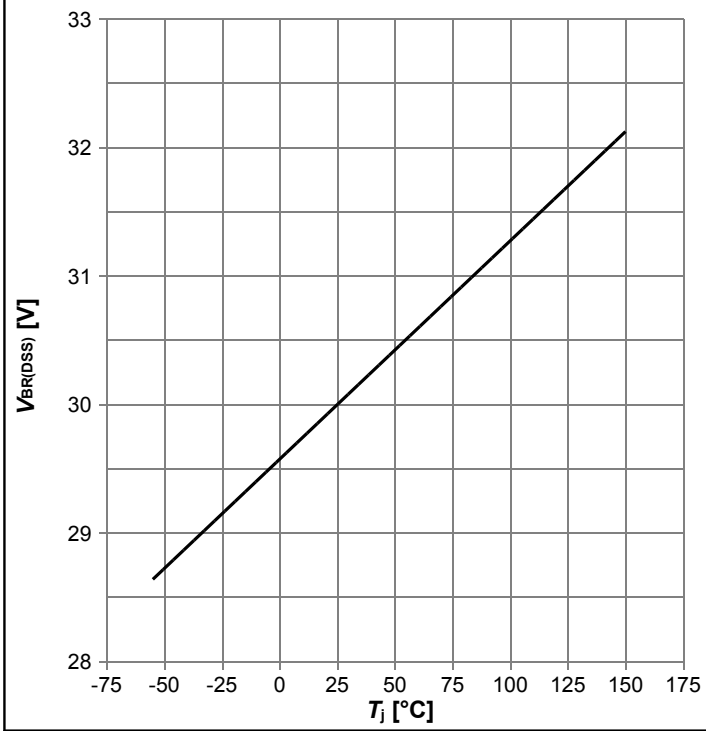
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



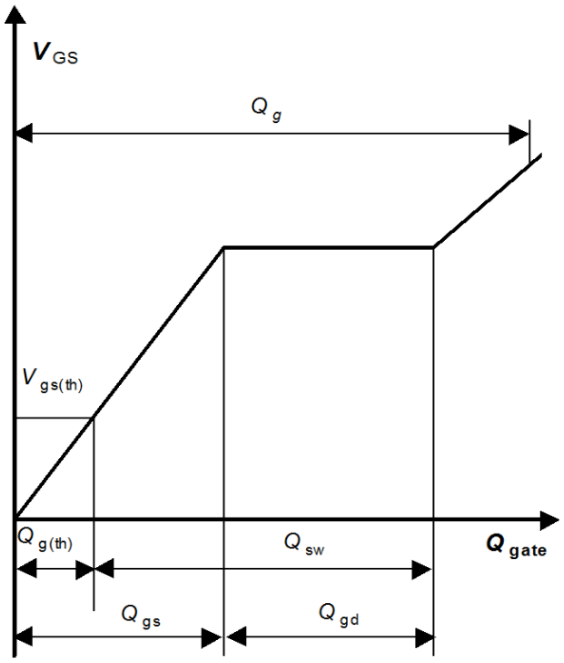
V_{GS}=f(Q_{gate}), I_D=20 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



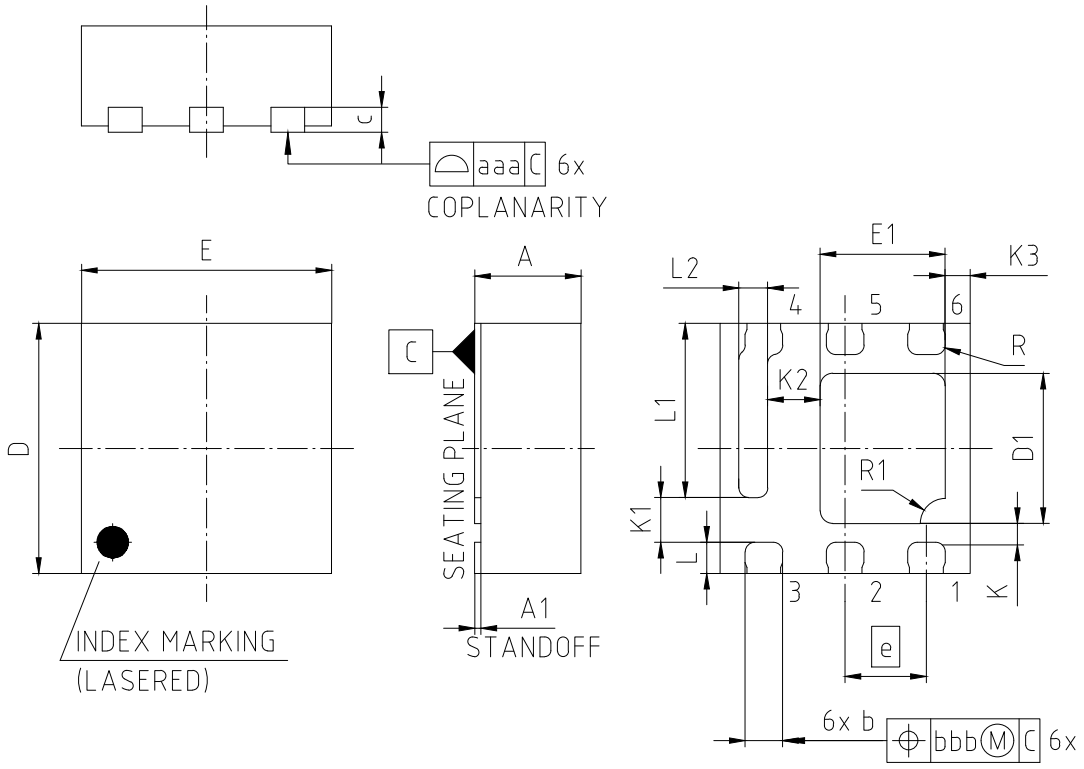
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram Gate charge waveforms



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5 Package Outlines



PACKAGE - GROUP NUMBER:	PG-VSON-6-U02				
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	---	0.90	**L**	0.20	0.30
A1	---	0.05	**L1**	1.29	1.49
b	0.20	0.40	**L2**	0.13	0.33
c	(0.20)		**R**	(0.08)	
D	1.90	2.10	**R1**	(0.20)	
D1	1.10	1.30	**N**	6	
E	1.90	2.10	**aaa**	0.08	
E1	0.90	1.10	**bbb**	0.10	
e	0.65				
K	0.05	---			
K1	0.26	---			
K2	0.42	---			
K3	0.10	0.30			

NOTE:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-VSON-6, dimensions in mm

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Revision History

ISK036N03LM5

Revision: 2024-01-08, Rev. 2.2

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2020-11-26	Release of final version
2.1	2023-06-05	Update RthJC, Ptot, current rating, RDS(on)typ, Gfs, Capacitances and Gate charges.
2.2	2024-01-08	Update POD drawing

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