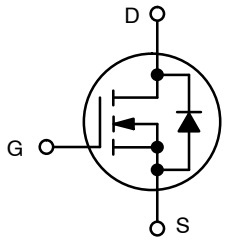
Power MOSFET
60 V, 22 A, 39 mΩ, Single N-Channel

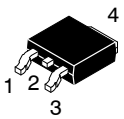
NVD5867NL

$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
60 V	39 mΩ @ 10 V	22 A
	50 mΩ @ 4.5 V	



N−CHANNEL MOSFET

Features
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- High Current Capability
- Avalanche Energy Specified
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant



DPAK
CASE 369AA
STYLE 2

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	60	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3)	Steady State	T_C = 25°C	I_D	22	A
		T_C = 100°C		16	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	43	W
		T_C = 100°C		21	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	Steady State	T_A = 25°C	I_D	6.0	A
		T_A = 100°C		4.0	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)		T_A = 25°C	P_D	3.3	W
		T_A = 100°C		1.7	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	85	A
Current Limited by Package (Note 3)	T_A = 25°C		$I_{Dmaxpkg}$	30	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 175	°C
Source Current (Body Diode)			I_S	36	A
Single Pulse Drain−to−Source Avalanche Energy (T_J = 25°C, V_{DD} = 50 V, V_{GS} = 10 V, $I_{L(pk)}$ = 19 A, L = 0.1 mH, R_G = 25 Ω)			E_{AS}	18	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

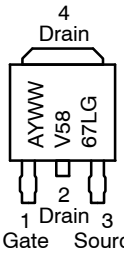
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case (Drain) (Note 1)	$R_{\theta JC}$	3.5	°C/W
Junction−to−Ambient − Steady State (Note 2)	$R_{\theta JA}$	45	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location*
Y = Year
WW = Work Week
V5867L = Device Code
G = Pb−Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION
See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				60		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25°C			1.0	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5	1.8	2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.2		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 11 A			26	39	mΩ
		V_{GS} = 4.5 V, I_D = 11 A			33	50	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 11 A			8.0		S
CHARGES, CAPACITANCES AND GATE RESISTANCES							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 25 V			675		pF
Output Capacitance	C_{oss}				68		
Reverse Transfer Capacitance	C_{rss}				47		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 22 A			15		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.0		
Gate−to−Source Charge	Q_{GS}				2.2		
Gate−to−Drain Charge	Q_{GD}				4.3		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 22 A			7.6		nC
Gate Resistance	R_G				1.3		Ω
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(on)}$	V_{GS} = 10 V, V_{DD} = 48 V, I_D = 22 A, R_G = 2.5 Ω			6.5		ns
Rise Time	t_r				12.6		
Turn−Off Delay Time	$t_{d(off)}$				18.2		
Fall Time	t_f				2.4		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.87	1.2	V
			T_J = 125°C		0.78		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 22 A			17		ns
Charge Time	ta				13		
Discharge Time	tb				4.0		
Reverse Recovery Charge	Q_{RR}				12		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL PERFORMANCE CURVES

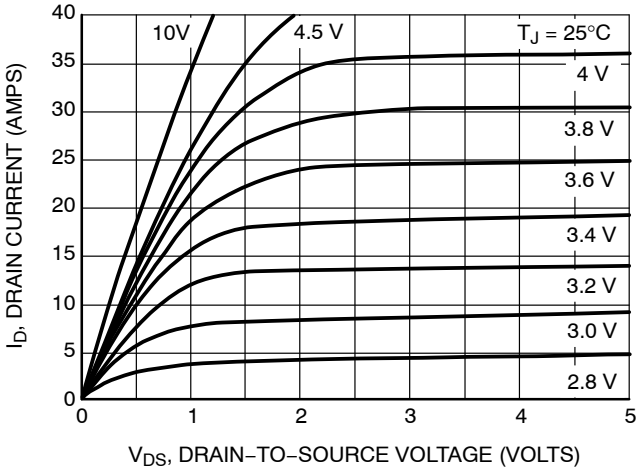

Figure 1. On−Region Characteristics

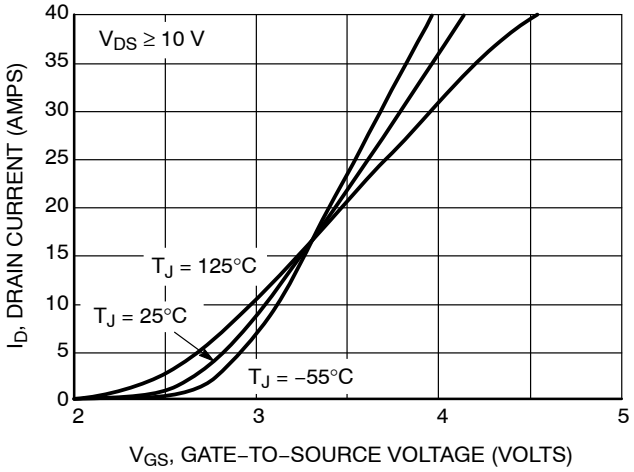

Figure 2. Transfer Characteristics

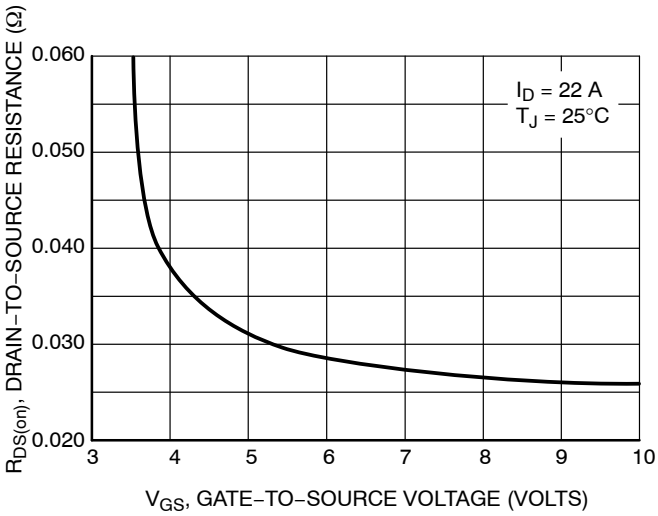

Figure 3. On−Resistance vs. Gate−to−Source Voltage

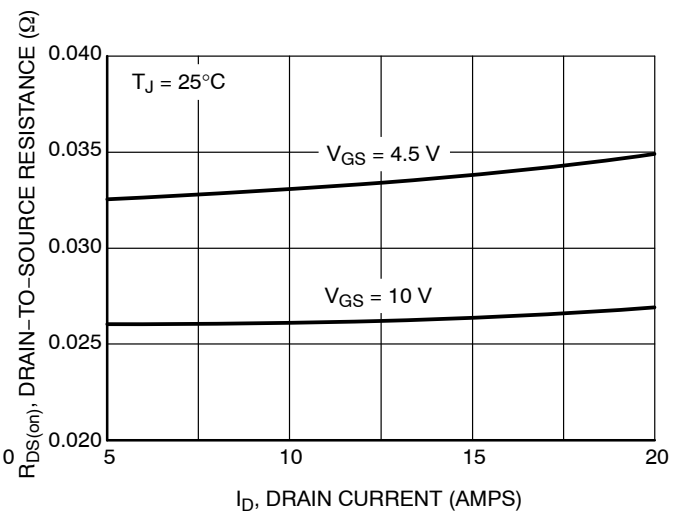

Figure 4. On−Resistance vs. Drain Current and Gate Voltage

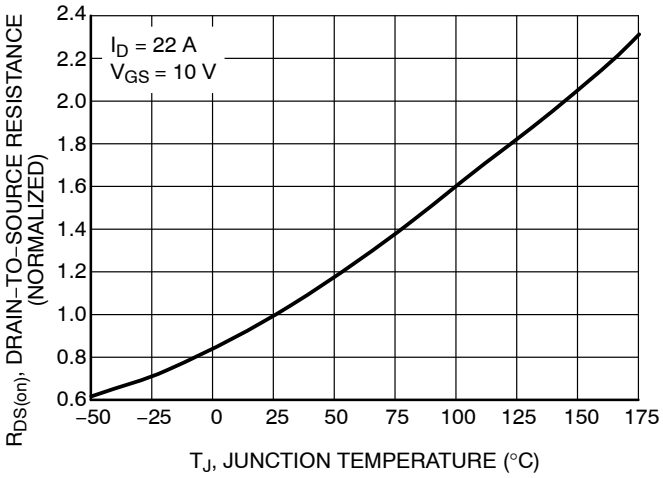

Figure 5. On−Resistance Variation with Temperature

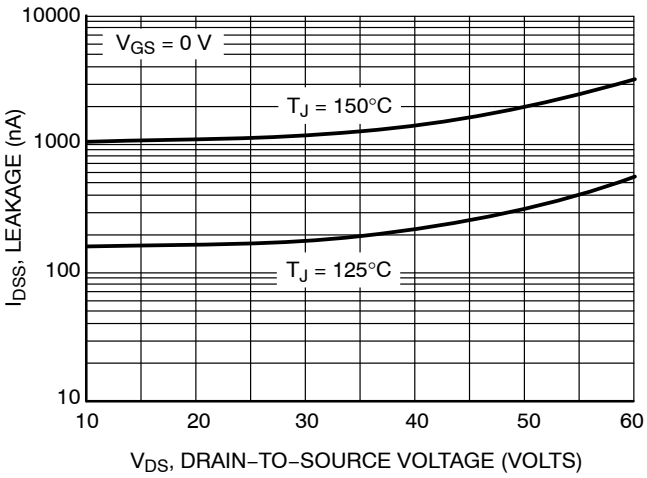

Figure 6. Drain−to−Source Leakage Current vs. Drain Voltage

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TYPICAL PERFORMANCE CURVES

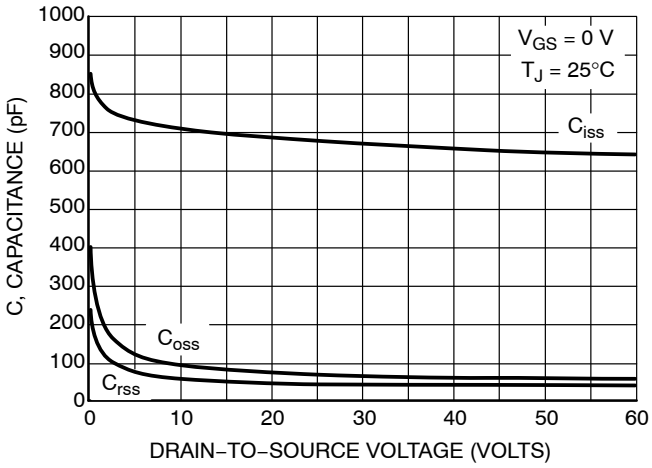

Figure 7. Capacitance Variation

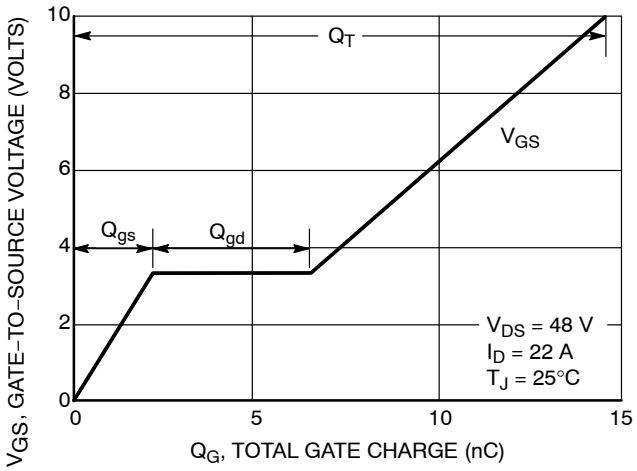

Figure 8. Gate−To−Source Voltage vs. Total Charge

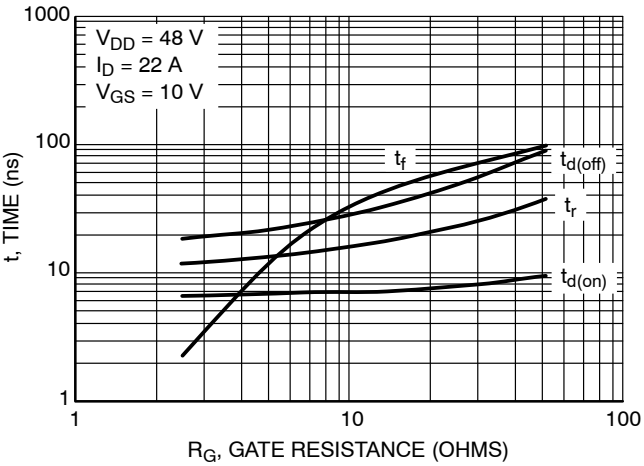

Figure 9. Resistive Switching Time Variation vs. Gate Resistance

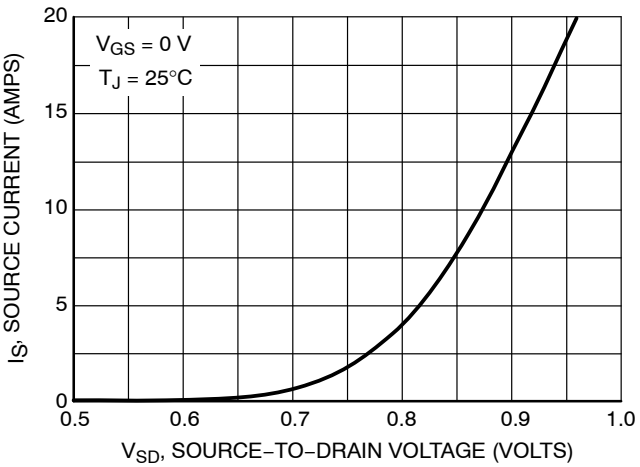

Figure 10. Diode Forward Voltage vs. Current

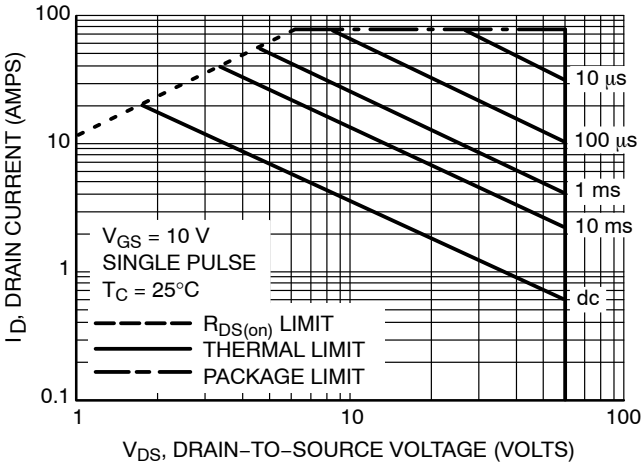

Figure 11. Maximum Rated Forward Biased Safe Operating Area

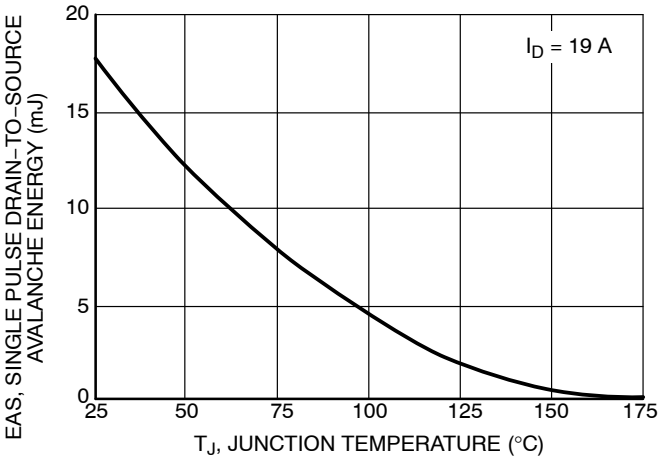

Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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TYPICAL PERFORMANCE CURVES

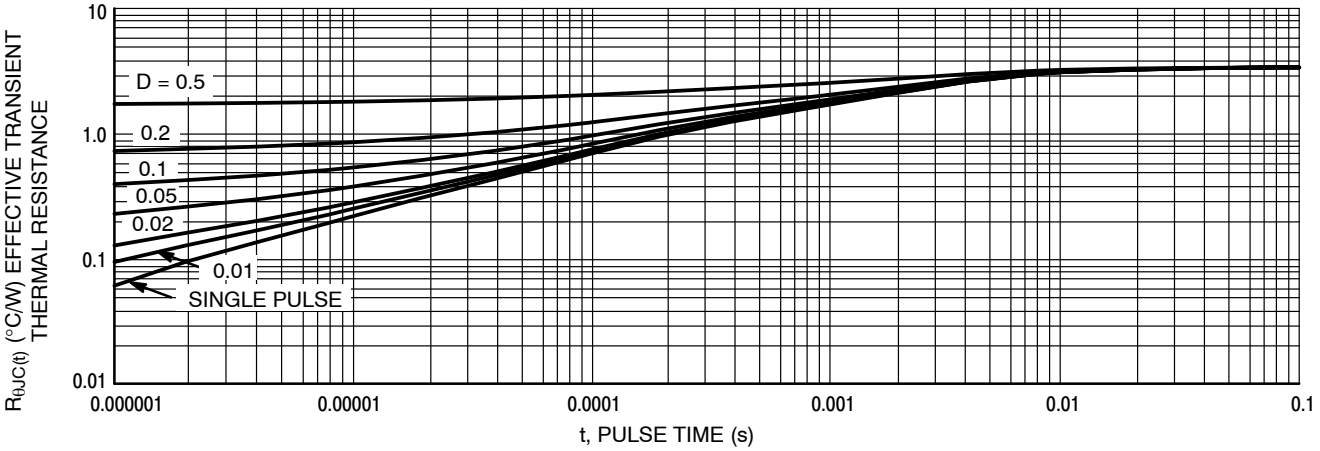

Figure 13. Thermal Response

ORDERING INFORMATION

Order Number	Package	Shipping†
NVD5867NLT4G	DPAK (Pb−Free)	2500 / Tape & Reel
SVD5867NLT4G	DPAK (Pb−Free)	2500 / Tape & Reel
SVD5867NLT4G−UM	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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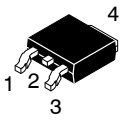


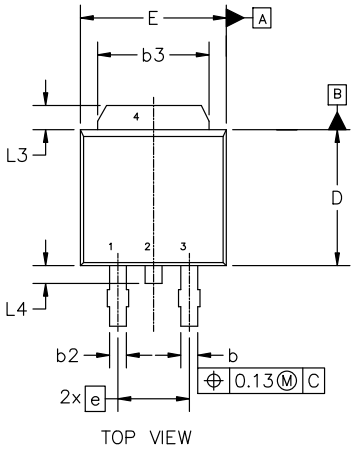
SCALE 1:1

DPAK−3 6.10x6.54x2.28, 2.29P
CASE 369AA
ISSUE C

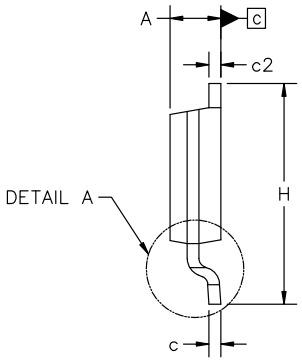
DATE 14 MAY 2026

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.28	2.38
A1	0.00	−−−	0.13
b	0.63	0.76	0.89
b2	0.76	0.95	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.74 REF		
L2	0.51 BSC		
L3	0.89	−−−	1.27
L4	−−−	−−−	1.01
Z	3.93	−−−	−−−

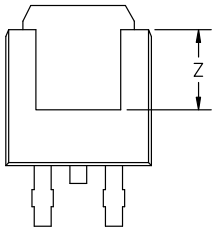
NOTES
1. DIMENSION AND TOLERANCING PER ASME Y14.5 2018
2. CONTROLLING DIMENSION: MILLIMETERS
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION b3, L3, AND Z
4. DIMENSION D AND E DO NOT INCLUDED MOLD FLASH, PROTRUSION, OR BURRS.
5. DIMENSION D AND E ARE DETERMINED AT OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H



TOP VIEW

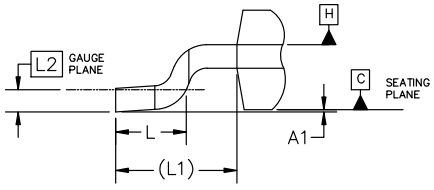


SIDE VIEW

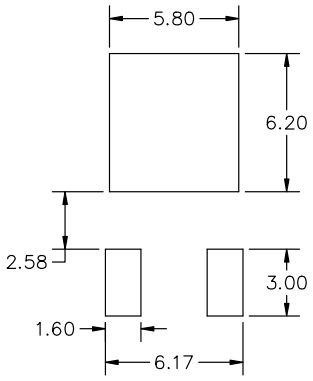


TOP VIEW

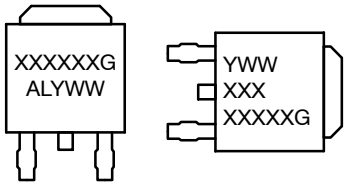
RECOMMENDED
MOUNTING FOOTPRINT



DETAIL A
ROTATED 90° CW



GENERIC
MARKING DIAGRAM*



IC **Discrete**

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DPAK−3 6.10x6.54x2.28, 2.29P**	**PAGE 1 OF 1**

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