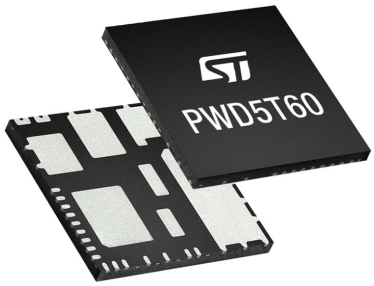
PWD5T60

Datasheet

Compact high-voltage three-phase power stage with integrated gate driver



VFQFPM12x12x0.95mm

Features

- Power driver integrating gate driver and high-voltage power MOSFETs:
  - $R_{DS(on)}$ = 1.38 Ω
  - BV_{DSS} = 500 V
- Wide input supply voltage range from 9 V to 20 V
- Integrated zero-drop bootstrap diodes
- Comparator for fast overcurrent protection with Smart ShutDown functionality
- Overtemperature protection
- 3.3 V, 5 V TTL/CMOS inputs with hysteresis
- Matched propagation delay for all channels
- UVLO function on low-side and high-side
- Interlocking and deadtime functions
- Dedicated enable pin
- Very compact and simplified layout

Product status link

PWD5T60

Product label

SUSTAINABLE TECHNOLOGY

Applications

- 3-phase inverters
- Fans and pumps
- Home and industrial appliances
- Refrigerator compressors

Description

The PWD5T60 is a is a three-phase high-density power driver integrating gate driver and six N-channel power MOSFETs. The PWD5T60 is the optimal solution for motor drive applications such as fans, pumps and small appliances.

The integrated power MOSFETs have $R_{DS(on)}$ of 1.38 Ω and 500 V blocking voltage. The high integration of the device allows to efficiently drive loads with reduced footprint, making PWD5T60 the optimal solution for space constrained applications.

The device has dedicated input pins for each output and a shutdown pin. The logic inputs are CMOS/TTL compatible down to 3.3 V for easy interfacing with control devices. Matched delays between low-side and high-side sections guarantee no cycle distortion and allow high-frequency operation.

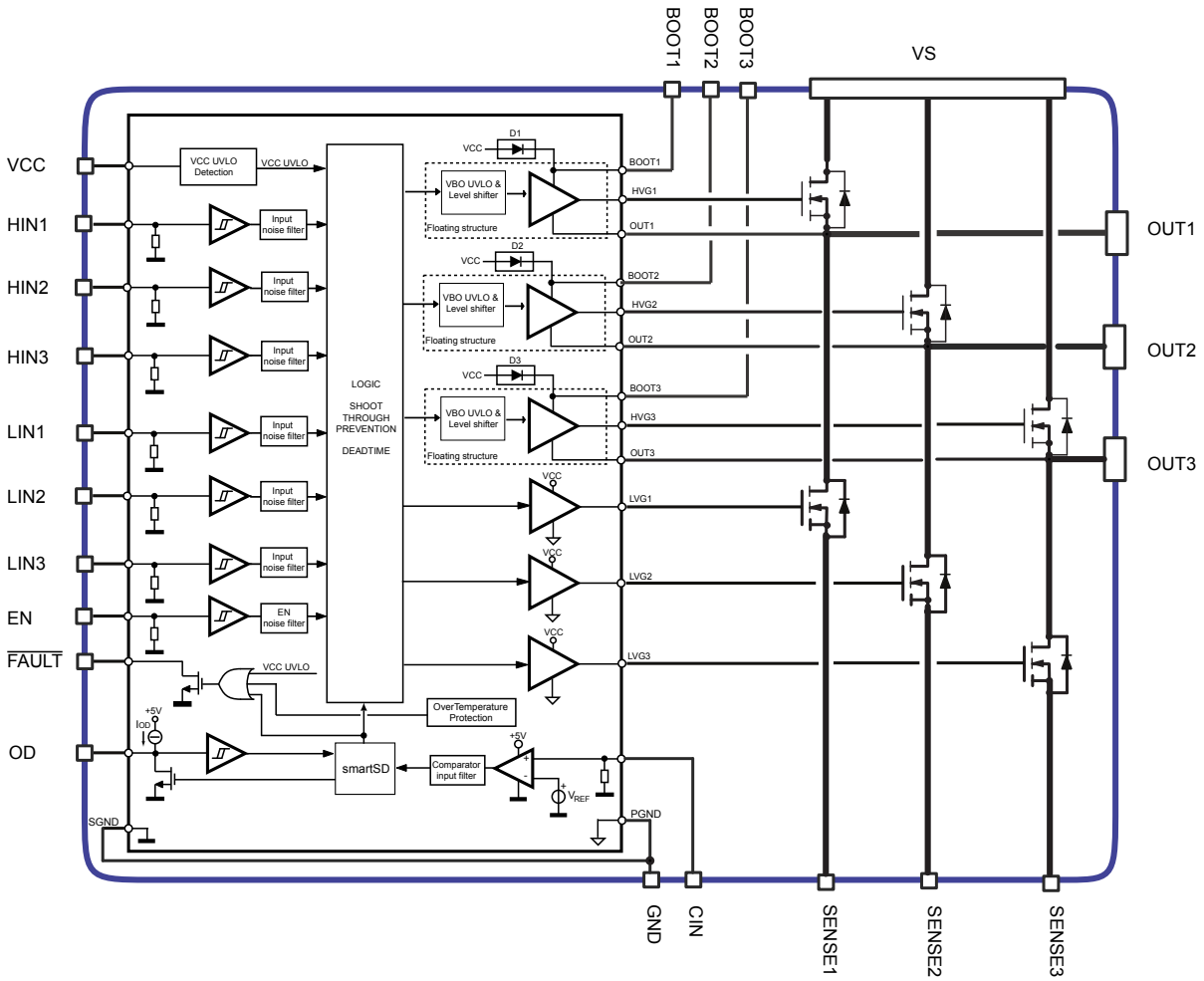
Robustness is a distinctive factor of PWD5T60. Prevention from cross conduction is ensured by interlocking and deadtime functions and a comparator featuring advanced smart ShutDown function ensures fast and effective protection against overload and overcurrent.

The dedicated UVLO protections on both low-side and high-side prevent the power switches from operating in low efficiency or dangerous conditions, enabling optimal and fail-safe operation.

The zero-drop integrated bootstrap diodes as well as all of the embedded features enable the design of compact and simple PCB layout, and reduce the overall bill of material and application cost. The device is available in a compact VFQFPN 12x12x0.95 mm.

1 Block diagram

Figure 1. **PWD5T60 block diagram**



2 Pin description and connection diagram

Figure 2. **PWD5T60 pin connection**

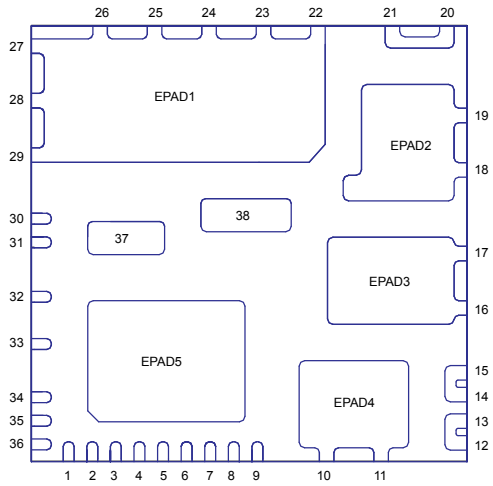


Table 1. **Pin description**

Pin #	Pin Name	Type	Function
1	HIN3	Logic input	High-side driver logic input 3
2	LIN1	Logic input	Low-side driver logic input 1
3	LIN2	Logic input	Low-side driver logic input 2
4	LIN3	Logic input	Low-side driver logic input 3
5	$\overline{\text{FAULT}}$	Open-drain output	Fault output
6	CIN	Analog input	Comparator positive input
7	EN	Logic input	Enable input, active high
8	OD	Open-drain output	SmartSD timing open-drain output, unlatch and restart input
9, EPAD5	GND	Power supply	Ground for gate driver IC and low-side gate drive return
10, 11, 30 (1), 37, EPAD4	OUT1	Power	Half-bridge 1 output
12, 13	SENSE1	Power	Half-bridge 1 sense (low-side MOSFET source)
14, 15	SENSE2	Power	Half-bridge 2 sense (low-side MOSFET source)
16, 17, 38, EPAD3	OUT2	Power	Half-bridge 2 output
18, 19, EPAD2	OUT3	Power	Half-bridge 3 output
20, 21	SENSE3	Power	Half-bridge 3 sense (low-side MOSFET source)
22-29, EPAD1	Supply	Power supply	High voltage supply (high-side MOSFET drain)
31	BOOT1	Power supply	Bootstrap supply voltage 1
32	BOOT2	Power supply	Bootstrap supply voltage 2
33	BOOT3	Power supply	Bootstrap supply voltage 3
34	VCC	Power supply	Driver low side and logic supply voltage
35	HIN1	Logic input	High-side driver logic input 1
36	HIN2	Logic input	High-side driver logic input 2

1. *Internally connected. Use for bootstrap capacitor connection only.*

3 Electrical data

3.1 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in Table 2 may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability. All voltages referred to ground (GND) unless otherwise specified.

Table 2. Absolute maximum ratings

Symbol	Parameter	Test Condition	Min	Max	Unit
VCC	Power supply voltage		-0.3	21	V
VCC-SENSEx	VCC to SENSE pin voltage		-0.3	25	V
V_{BOx}	BOOT to OUT pin		-0.3	21	V
BV_{DSS}	MOSFETs blocking Voltage	T_J = 25°C		500	V
I_D	Drain current (per MOSFET)	DC @T_{CB} = 25 °C (1)		3.5	A
		DC @T_{CB} = 100 °C (1) (2)		2	A
		Pulse @T_{CB} = 25 °C (1) (2) (3)		14	A
SR_{OUT}	Full bridge outputs slew rate (10% - 90%)	(2)		40	V/ns
V_{OUTx}	Output voltage		V_{BOOTx} - 21	500	V
V_{BOOTx}	Bootstrap voltage		-0.3	520	V
V_{CIN}	Comparator input voltage		-0.3	20	V
V_i	Logic input voltage (4)		- 0.3	15	V
V_{OD}	Open-drain voltage (OD, $\overline{FAULT}$)		-0.3	21	V
V_{FAULT}	$\overline{FAULT}$ pin voltage		- 0.3	21	V
V_{ISO}	Isolation Voltage (1 min) (2)			2500	V_{RMS}
T_J	Junction temperature		-40	125	°C
T_{stg}	Storage temperature		-50	150	°C
P_{TOT}	Total power dissipation (5)	T_{amb} = 25°C JEDEC board (6) (7)		5.2	W
ESD	Human Body Model		2 (8)		kV

1. *T_{CB} is the temperature of the case-bottom pad.*
2. *Not tested in production.*
3. *The value specified by the pulse duration limited by maximum junction temperature.*
4. *EN, LINx and HINx pins.*
5. *Value calculated basing on thermal resistance, power uniformity distributed over the six power MOSFETs, still air.*
6. *The device mounted on a FR4 2s2p board as JESD51-5/7.*
7. *Actual applicative board max. dissipation could be higher or lower depending on the layout and cooling techniques.*
8. *Pins 12, 13, 14, 15, 20 and 21 have HBM ESD value ± 1.75 kV*

3.2 Recommended operating conditions

All voltages referred to ground (GND) unless otherwise specified.

Table 3. Recommended operating conditions

Symbol	Parameter	Min	Max	Unit
VCC	Power supply voltage	9	20	V
V_{BO} (1)	Floating supply voltage	8.5	20	V
V_{OUT}	DC Output voltage	-10 (2)	400	V
V_{CIN}	Comparator input voltage	0	15	V
V_i	Logic input voltage	0	15	V
V_{OD}	Open-drain voltage (OD, $\overline{FAULT}$)	0	20	V
V_{FAULT}	$\overline{FAULT}$ pin voltage	0	20	V
f_{SW} (3)	Maximum switching frequency		30	kHz
PW (4)	Minimum input pulse width	300		ns

1. *$V_{BO} = V_{BOOT} - V_{OUT}$*
2. *LVG off. VCC = 9 V. Logic is operational if $V_{BOOT} > 5$ V.*
3. *Actual maximum f_{SW} depends on power dissipation.*
4. *Pulse width on LIN or HIN pins propagated to gate driver outputs.*

3.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(J\text{-}CT)}$	Thermal resistance junction-to-case top	7	°C/W
$R_{th(J\text{-}CB)}$	Thermal resistance junction-to-case bottom	0.32	°C/W

4 Electrical characteristics

4.1 Driver

HIN is referred to channels HIN1, HIN2, HIN3; LIN is referred to channels LIN1, LIN2, LIN3.

Table 5. Electrical characteristics

VCC = 15 V; T_J = +25 °C, unless otherwise specified

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Low-side section supply						
VCC_{thON}	VCC UVLO turn on threshold		8.7	9.2	9.7	V
VCC_{thOFF}	VCC UVLO turn off threshold		8.2	8.7	9.2	V
VCC_{hys}	VCC UVLO hysteresis		0.4	0.5	0.6	V
I_{QCCU}	VCC under-voltage quiescent supply current	VCC = 7 V; EN = 5 V; CIN = SGND LVG & HVG: OFF		430	744	µA
I_{QCC}	VCC quiescent supply current	EN = 5 V; CIN = SGND LVG & HVG: OFF		1125	1650	µA
High-side floating section supply (1)						
V_{BOthON}	V_{BO} UVLO turn on threshold		8.2	8.7	9.2	V
$V_{BOthOFF}$	V_{BO} UVLO turn off threshold		7.7	8.2	8.7	V
V_{BOhys}	V_{BO} UVLO hysteresis		0.4	0.5	0.6	V
I_{QBOU}	V_{BO} under-voltage quiescent supply current	VCC = V_{BO} = 6.5 V; EN = 5 V; CIN = SGND LVG OFF; HVG = ON		25	62	µA
I_{QBO}	V_{BO} quiescent supply current	V_{BO} = 15 V EN = 5 V; CIN = SGND LVG OFF; HVG = ON		84	150	µA
I_{LK}	High voltage leakage current	BOOT = HVG = OUT = 520 V			15	µA
R_{Dboot}	Bootstrap Diode on resistance			200		Ω
Logic Inputs						
V_{il}	Low level logic threshold voltage		0.8		1.4	V
V_{ih}	High level logic threshold voltage		1.8		2.3	V
V_{hyst}	Logic input threshold hysteresis		0.8	0.9	1.2	V
V_{SSDh}	SmartSD restart threshold		3.6	4.1	4.4	V
V_{SSDl}	SmartSD unlatch threshold			0.56	0.75	V
I_{LINh}	LIN logic “1” input bias current	V_{LINx} = 15 V	120	150	200	µA
I_{LINl}	LIN logic “0” input bias current	V_{LINx} = 0 V			1	µA
I_{HINh}	HIN logic “1” input bias current	V_{HINx} = 15 V	120	150	200	µA
I_{HINl}	HIN logic “0” input bias current+	V_{HINx} = 0			1	µA
R_{PD_IN}	Logic input pull-down resistor		75	100	125	kΩ
I_{ENh}	EN logic “1” input bias current	V_{EN} = 15 V	110	150	200	µA
I_{ENl}	EN logic “0” input bias current	V_{EN} = 0 V			1	µA
R_{PD_EN}	EN pull-down resistor		75	100	125	kΩ

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Sense comparator (2) and **$\overline{\text{FAULT}}$**						
V_{REF}	Internal voltage reference		430	480	530	mV
C_{INhyst}	Comparator input hysteresis		40	70		mV
C_{IN_PD}	Comparator input pull-down current	V_{CIN} = 1 V	7	10	13	µA
I_{OD}	OD internal current source		2.5	5	7.5	µA
R_{ON_OD}	OD On resistance	I_{OD} = 16 mA	19	25	36	W
I_{OL_OD}	OD low level sink current	V_{OD} = 400 mV	11	16	21	mA
I_{SAT_OD}	OD saturation current	V_{OD} = 5 V		108		mA
V_{FLOAT_OD}	OD floating voltage level	OD connected only to an external capacitance	4.5	4.9	5.4	V
R_{ON_F}	$\overline{\text{FAULT}}$ On resistance	I_{FAULT} = 8 mA		50	100	W
I_{OL_F}	$\overline{\text{FAULT}}$ low level sink current	V_{FAULT} = 400 mV	4	8	12	mA
t_{OD}	Comparator propagation delay	R_{pu} = 100 kΩ to 5 V; Voltage step on CIN = 0 to 3.3 V; 50% CIN to 90% OD	350	475	590	ns
t_{CIN-F}	Comparator triggering to $\overline{\text{FAULT}}$	Voltage step on CIN = 0 to 3.3 V; 50% CIN to 90% $\overline{\text{FAULT}}$	360	475	590	ns
$t_{CINoffMOS}$	Comparator triggering to low-side MOSFET turn-off propagation delay	Voltage step on CIN = 0 to 3.3 V; OUT 500 Ω to 5 V, VS = 5 V 50% CIN to 10% OUT	730	840	950	ns
t_{FCIN}	Comparator input filter time		360	475	590	ns
SR	OD Slew rate	C_L = 1 nF; R_{pu} = 33 kΩ to 5 V; 90% to 10% OD	20	60	100	V/µs
Over temperature protection						
T_{TSD}	Shut down temperature (3) (4)		120	135	150	°C
T_{HYS}	Temperature hysteresis (3) (4)			20		°C
Dynamic characteristics						
t_{FIN}	LIN, HIN input filter time		30	40	50	ns
t_{FEN}	EN input filter time		200	300	400	ns
DT	Deadtime		200	300	400	ns
MDT	Matching deadtime (5)			0	50	ns

1. *$V_{BO} = V_{BOOT} - V_{OUT}$*
2. *Comparator is disabled when VCC is in UVLO condition*
3. *Characterization data, not tested in production.*
4. *The temperature sensor is located in the driver.*
5. *MDT = $| DT_{LH} - DT_{HL} |$*

4.2 Power MOSFETs

HIN is referred to channels HIN1, HIN2, HIN3; LIN is referred to channels LIN1, LIN2, LIN3.

Table 6. Electrical characteristics

VCC = 15 V; T_J = +25 °C, unless otherwise specified.

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(BR)DS}$	Drain-source breakdown voltage	I_D = 1 mA (1)	600			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V EN = SENSE = GND			1	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 250 µA (1)	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	I_D = 1.75 A; V_{GS} = 10 V;	-	1.38	1.75	Ω
I_{AS}	Avalanche current, repetitive or not repetitive	Pulse width limited by T_J max. (1)			1	A
E_{AS}	Single pulse avalanche energy	Starting T_J = 25 °C, I_D = I_{AS}, V_{DD} = 50 V (1)			132	mJ
V_{SD}	Diode forward on voltage	EN = SENSE = GND I_{SD} = 3.5 A;	-	-	1.6	V

1. *Tested at wafer level before packaging.*

5 Device characterization values

The PWD5T60 integrates six 500 V N-channel power MOSFETs in three phase full bridge configuration.

Table 7, Table 8. Inductive load switching characteristics and electrical characteristics curves contained in this section represent typical values based on characterization and simulation results and are not subject to the production test.

Table 7. Power MOSFETs

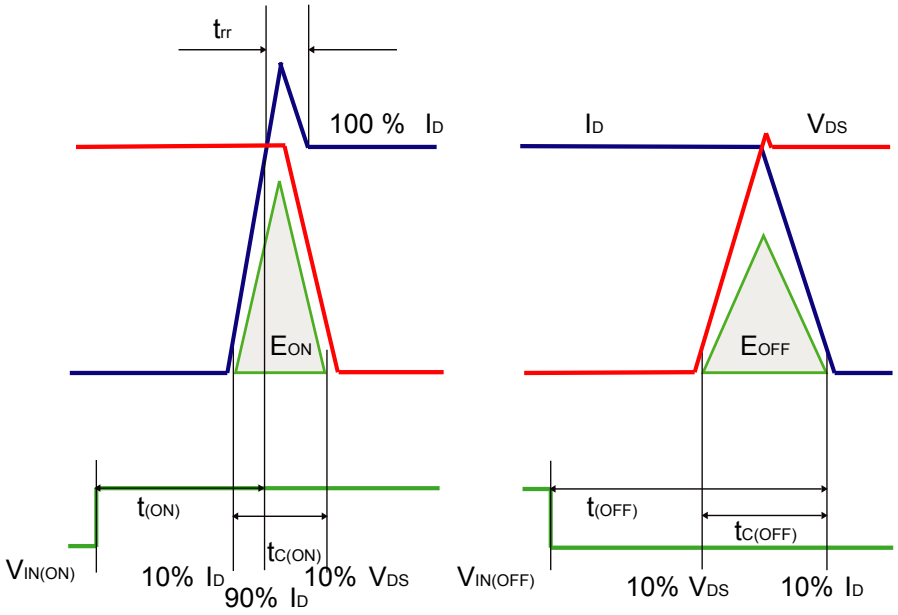
Symbol	Parameter	Test condition	Min	Typ	Max	Unit
MOSFET Dynamic						
Q_g	Total gate charge	V_{GS} = 10 V, T_J = 25 °C V_{DS} = 480 V, I_D = 3.5 A	-	5.3	-	nC
Source-Drain diode						
t_{rr}	Diode reverse recovery time	I_{SD} = 3.5 A, T_J = 25 °C di/dt = 100 A/µs, V_{DS} = 60 V	-	58	-	ns
Q_{rr}	Diode reverse recovery charge		-	109	-	µC
I_{RRM}	Diode reverse recovery current		-	4	-	A
t_{rr}	Diode reverse recovery time	I_{SD} = 3.5 A, T_J = 150 °C di/dt = 100 A/µs, V_{DS} = 60 V	-	109	-	ns
Q_{rr}	Diode reverse recovery charge		-	309	-	µC
I_{RRM}	Diode reverse recovery current		-	5	-	A

Table 8. Inductive load switching characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$t_{(ON)}$ (1)	Turn-on time	VS = 300 V, VCC = V_{BO} = 15 V, I_D = 1.75 A See Figure 3	-	390	-	ns
$t_{C(ON)}$ (2)	Crossover time (on)		-	150	-	ns
$t_{(OFF)}$ (1)	Turn-off time		-	165	-	ns
$t_{C(OFF)}$ (2)	Crossover time (off)		-	40	-	ns
t_{SD}	Shutdown to high/low-side propagation delay		-	HS: 75 LS: 85	-	ns
E_{on}	Turn-on switching losses		-	75	-	µJ
E_{off}	Turn-off switching losses		-	8	-	µJ

1. *$t_{(ON)}$ and $t_{(OFF)}$ include the propagation delay time of the internal driver.*
2. *$t_{C(ON)}$ and $t_{C(OFF)}$ are the switching times of MOSFET itself under the internally given gate driving conditions.*

Figure 3. **Switching time definition**



(a) turn-on (b) turn-off

Figure 4. **Normalized gate threshold voltage vs temperature**

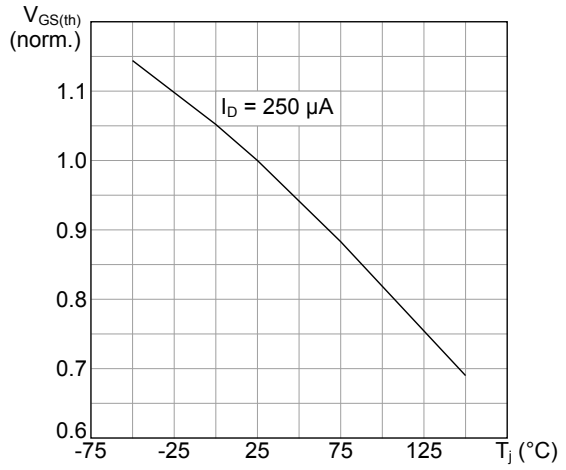


Figure 5. **Normalized drain-source breakdown voltage vs. temperature**

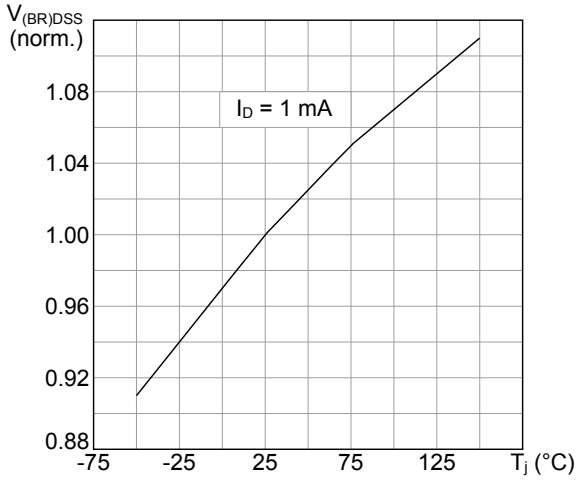


Figure 6. **Static drain-source on-resistance**

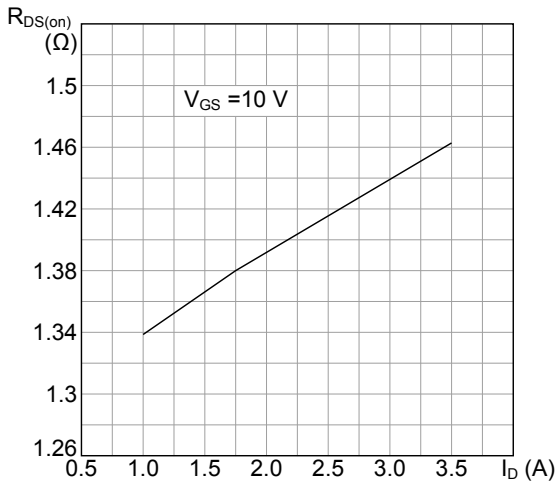


Figure 7. **Normalized on-resistance vs temperature**

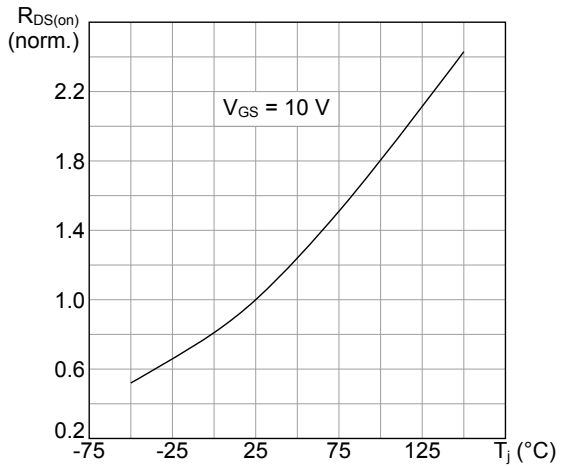


Figure 8. **Transfer characteristics**

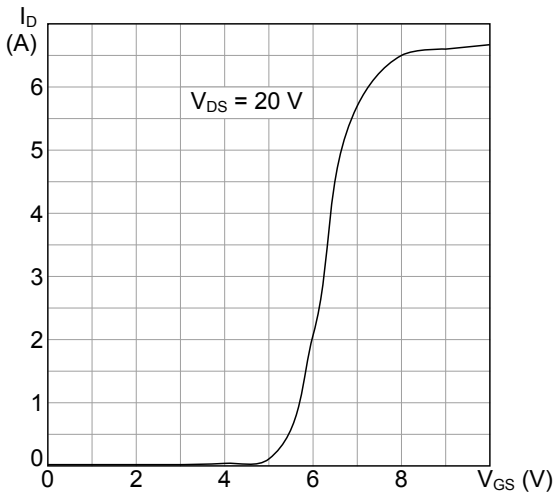


Figure 9. **Output characteristics**

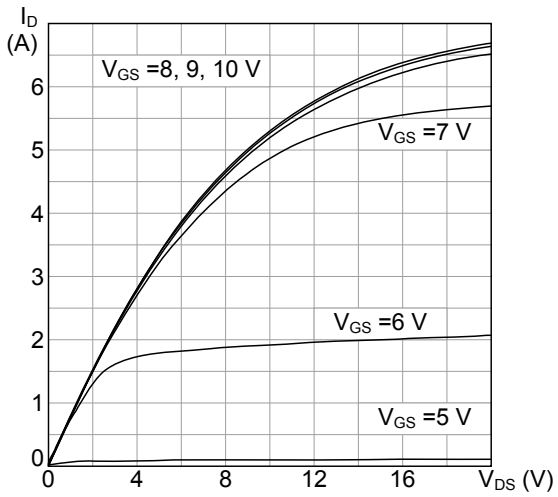
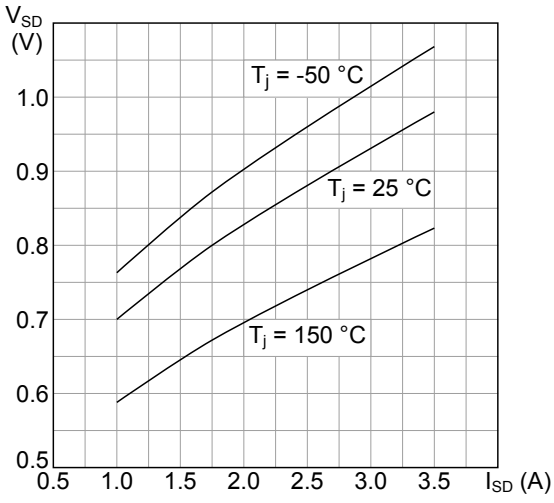


Figure 10. **Static source-drain diode forward characteristics**



6 Functional description

6.1 Inputs and outputs

The device is controlled through the following logic inputs:

- EN: enable input, active high;
- LIN: low-side driver inputs, active high;
- HIN: high-side driver inputs, active high.

Table 9. Inputs truth table (applicable when the device is not in UVLO or SmartSD protection)

	Input pins			Output pins	
	EN	LIN	HIN	LVG	HVG
	L	X	X	OFF	OFF
	H	L	L	OFF	OFF
	H	H	L	**ON**	OFF
	H	L	H	OFF	**ON**
Interlocking	H	H	H	OFF	OFF

Note: X : Do not care.

The $\overline{\text{FAULT}}$ and OD pins are open-drain outputs.

The $\overline{\text{FAULT}}$ signal is set low in case VCC UVLO is detected, or in case the SmartShutDown comparator triggers an event. It is only used to signal a UVLO or SmartSD activation to external circuits, and its state does not affect the behavior of other functions or circuits inside the driver.

The OD behavior is explained in Section 6.5.

6.2 Deadtime

The deadtime feature, in companion with the interlocking feature, guarantees that driver outputs of the same channel are not high simultaneously and at least a DT time passes between the turn-off of one driver's output and the turn-on of the companion output of the same channel. If a deadtime longer than the internal DT is applied to the LIN and HIN inputs by the external controller, the internal DT is ignored and the outputs follow the deadtime determined by the inputs.

6.3 VCC UVLO protection

Undervoltage protection is available on VCC and BOOT supply pins. In order to avoid intermittent operation, a hysteresis sets the turn-off threshold with respect to the turn-on threshold.

When VCC voltage goes below the $V_{CCthOFF}$ threshold, all the outputs are switched off, both LVG and HVG. When VCC voltage reaches the V_{CCthON} threshold, the driver returns to normal operation and sets the LVG outputs according to actual input pin status; HVG is also set according to input pin status if the corresponding V_{BO} section is not in UVLO condition. The $\overline{FAULT}$ output is kept low when VCC is in UVLO condition. The following figures show some examples of typical operation conditions.

Figure 11. VCC power ON and UVLO, LVG timing

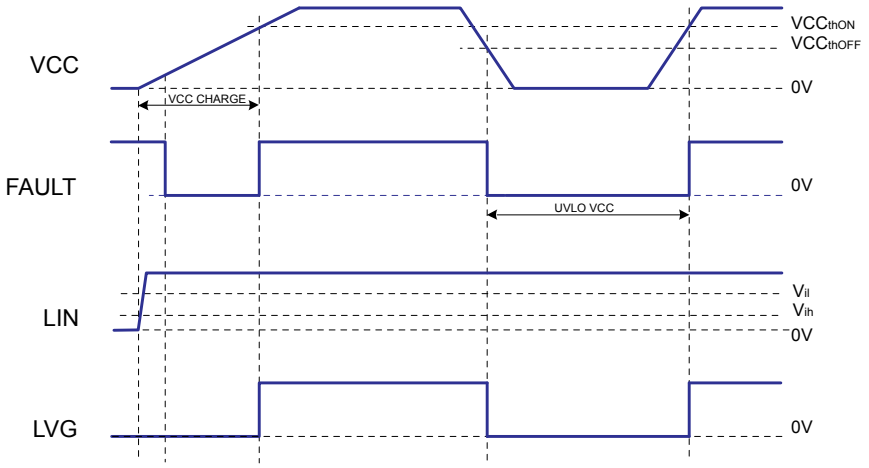
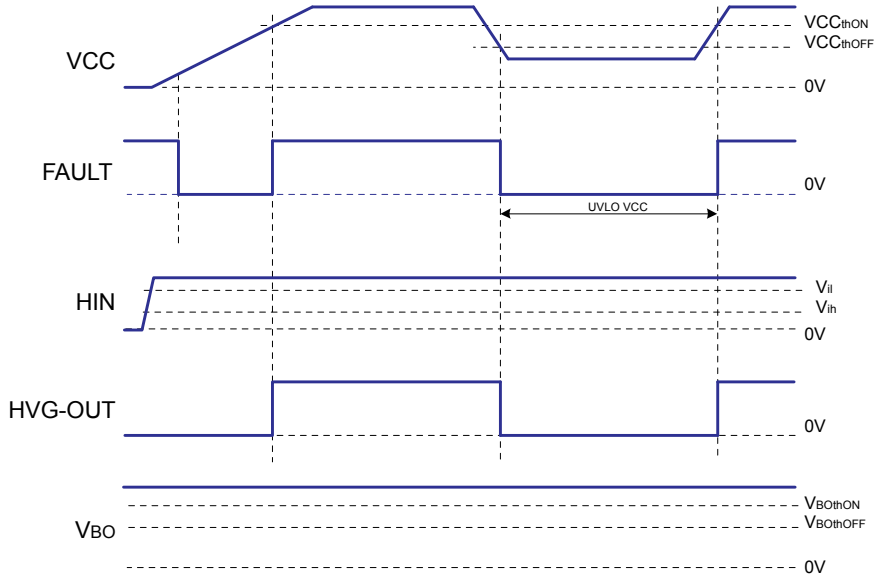


Figure 12. VCC power ON and UVLO, HVG timing

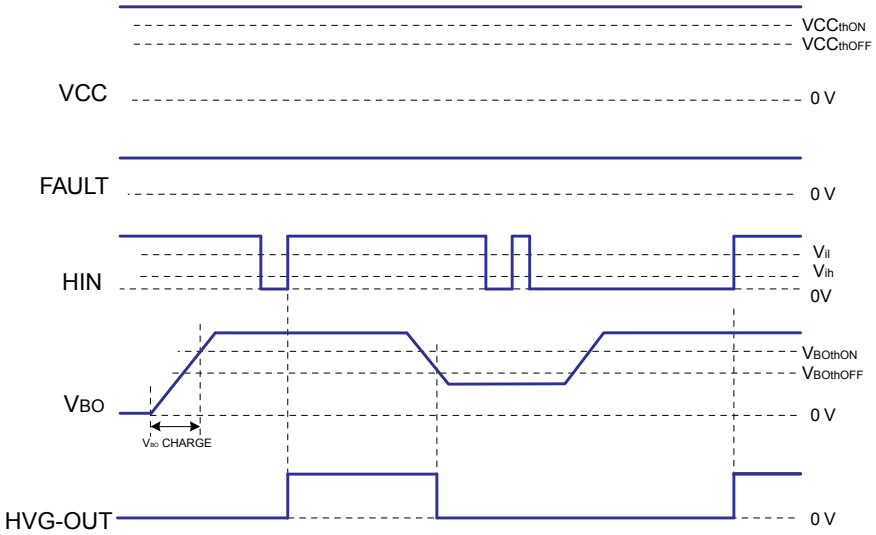


6.4 V_{BO} UVLO protection

Dedicated undervoltage protection is available on each bootstrap section between BOOTx and OUTx supply pins. In order to avoid intermittent operation, a hysteresis sets the turn-off threshold with respect to the turn-on threshold.

When the V_{BO} voltage goes below the $V_{BOthOFF}$ threshold, the HVG output of the corresponding bootstrap section is switched off. When the V_{BO} voltage reaches the V_{BOthON} threshold, the device returns to normal operation and the output remains off up to the next input pin transition that requests HVG to turn on.

Figure 13. V_{BO} power-ON and UVLO timing



6.5 Comparator and Smart shutdown

The PWD5T60 integrates a comparator committed to the fault protection function, thanks to the SmartShutDown (SmartSD) circuit.

The SmartSD architecture allows immediate turn-off of the gate driver outputs in the case of overload or overcurrent condition, by minimizing the propagation delay between the fault detection event and the actual output switch-off. In fact, the time delay between the fault detection and the output turn-off is not dependent on the value of the external components connected to the OD pin, which are only used to set the duration of disable time after the fault.

This provides the possibility to increase the duration of the output disable time after the fault event up to very large values without increasing the delay time of the protection. The duration of the disable time is determined by the values of the external capacitor C_{OD} and of the optional pull-up resistor connected to the OD pin.

The comparator has an internal voltage reference V_{REF} connected to the inverting input, while the non-inverting input is available on the CIN pin. The comparator's CIN input can be connected to an external shunt resistor in order to implement a fast and simple overcurrent protection function. The output signal of the comparator is filtered from glitches shorter than t_{FCIN} and then fed to the SmartSD logic.

If the impulse on the CIN pin is higher than V_{REF} and wider than t_{FCIN}, the SmartSD logic is triggered and immediately sets all of the driver outputs to low-level (OFF).

At the same time, $\overline{FAULT}$ is forced low to signal the event (for example to an MCU input) and OD starts to discharge the external C_{OD} capacitor used to set the duration of the output disable time of the fault event.

The $\overline{FAULT}$ pin is released and driver outputs restart following the input pins as soon as the *output disable time* expires.

The overall disable time is composed of two phases:

- The OD *unlatch time* (t_1 in Figure 14), which is the time required to discharge the C_{OD} capacitor down to the V_{SSDI} threshold. The discharge starts as soon as the SSD comparator is triggered.

- The OD *Restart time* (t_2 in Figure 14), which is the time required to recharge the C_{OD} capacitor up to the V_{SSDh} threshold. The recharge of C_{OD} starts when the OD internal MOSFET is turned-off, which happens when the fault condition has been removed (CIN < V_{REF} - C_{INhyst}) and the voltage on OD reaches the V_{SSDl} threshold. This time normally covers most of the overall output disable time.

If no external pull-up is connected to OD, the external C_{OD} capacitor is discharged with a time constant defined by C_{OD} and the internal MOSFET's characteristic (Equation 1), and the Restart time is determined by the internal current source I_{OD} and by C_{OD} (Equation 2).

Equation 1

$$t_1 \cong R_{ON\_OD} \cdot C_{OD} \cdot \ln\left(\frac{V_{OD}}{V_{SSDl}}\right) \quad (1)$$

Equation 2

$$t_2 \cong \frac{C_{OD} \cdot V_{SSDh}}{I_{OD}} \cdot \ln\left(\frac{V_{SSDl} - V_{OD}}{V_{SSDh} - V_{OD}}\right) \quad (2)$$

Where $V_{OD} = V_{FLOAT\_OD}$

In case the OD pin is connected to VCC by an external pull-up resistor R_{OD_ext}, the OD discharge time is determined by the external network R_{OD_ext} C_{OD} and by the internal MOSFET's R_{ON_OD} (Equation 3), while the Restart time is determined by current in R_{OD_ext} (Equation 4).

Equation 3

$$t_1 \cong C_{OD} \cdot \left(R_{OD\_ext} // R_{ON\_OD}\right) \cdot \ln\left(\frac{V_{OD} - V_{on}}{V_{SSDl} - V_{on}}\right) \quad (3)$$

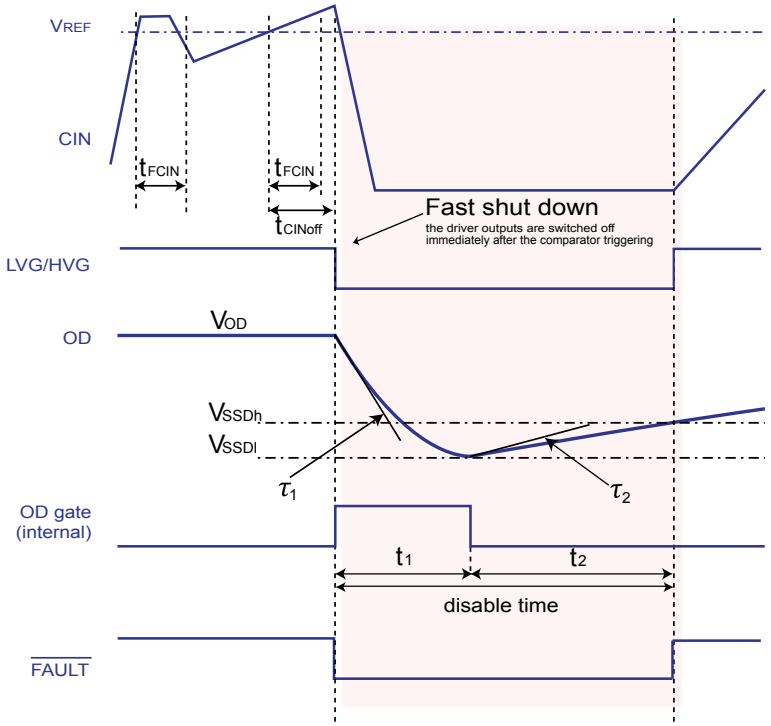
Equation 4

$$t_2 \cong C_{OD} \cdot R_{OD\_ext} \cdot \ln\left(\frac{V_{SSDl} - V_{OD}}{V_{SSDh} - V_{OD}}\right) \quad (4)$$

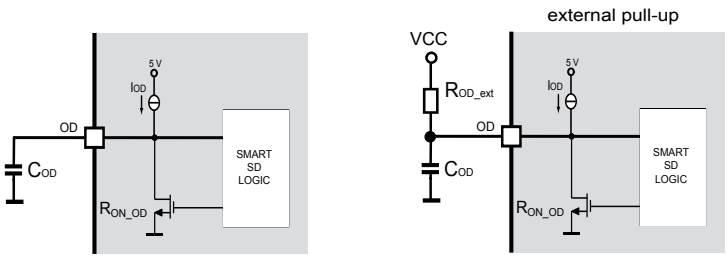
where:

$$V_{on} = \frac{R_{ON\_OD}}{R_{OD\_ext} + R_{ON\_OD}} \cdot VCC \;\; ; \quad V_{OD} = VCC$$

Figure 14. **Smart shutdown timing waveforms**



SMART SHUTDOWN CIRCUIT



6.6 Overtemperature protection

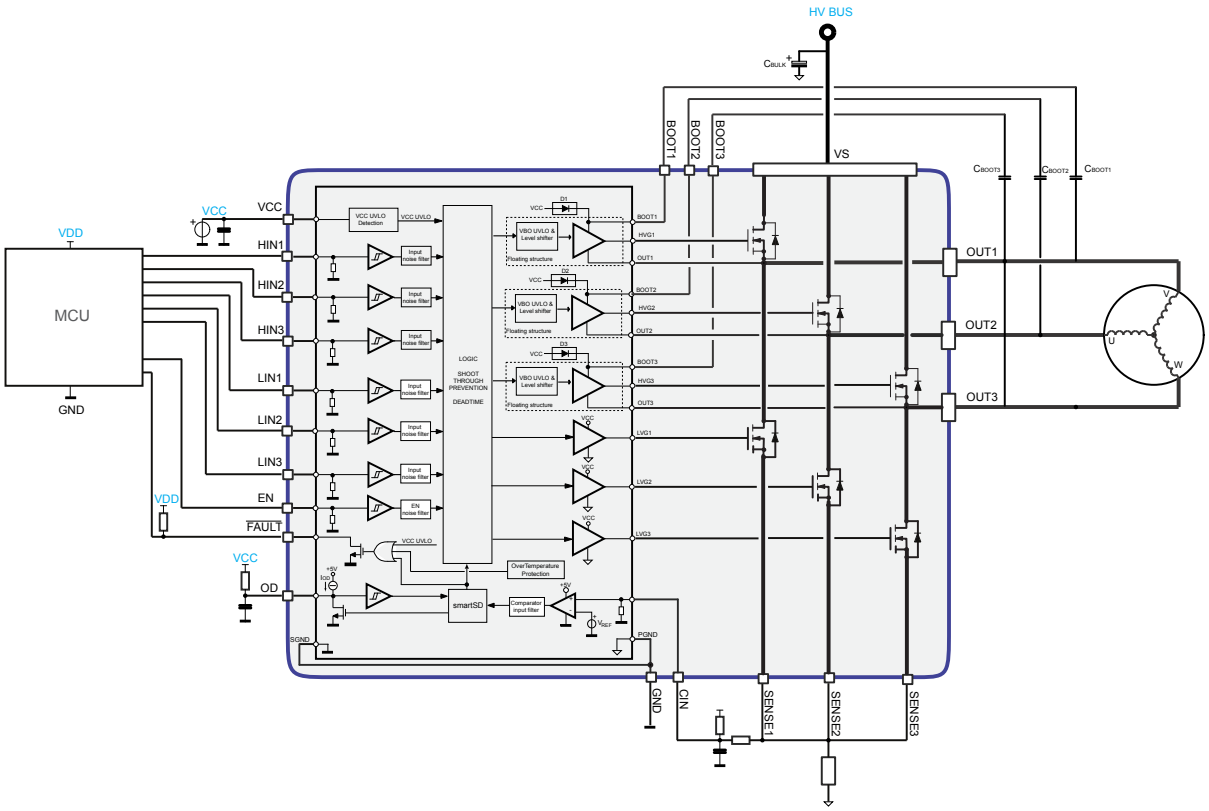
The device integrates an overtemperature protection, which turns and keeps all MOSFETs off when T_J exceeds T_{TSD}.

Overtemperature protection is signaled externally setting the $\overline{FAULT}$ pin low.

Once T_J falls below (T_{TSD} - T_{HYS}) the $\overline{FAULT}$ pin is released and the MOSFETs are set according to the logic input values.

7 Typ application

Figure 15. **Typical application 3-phase single-shunt**



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

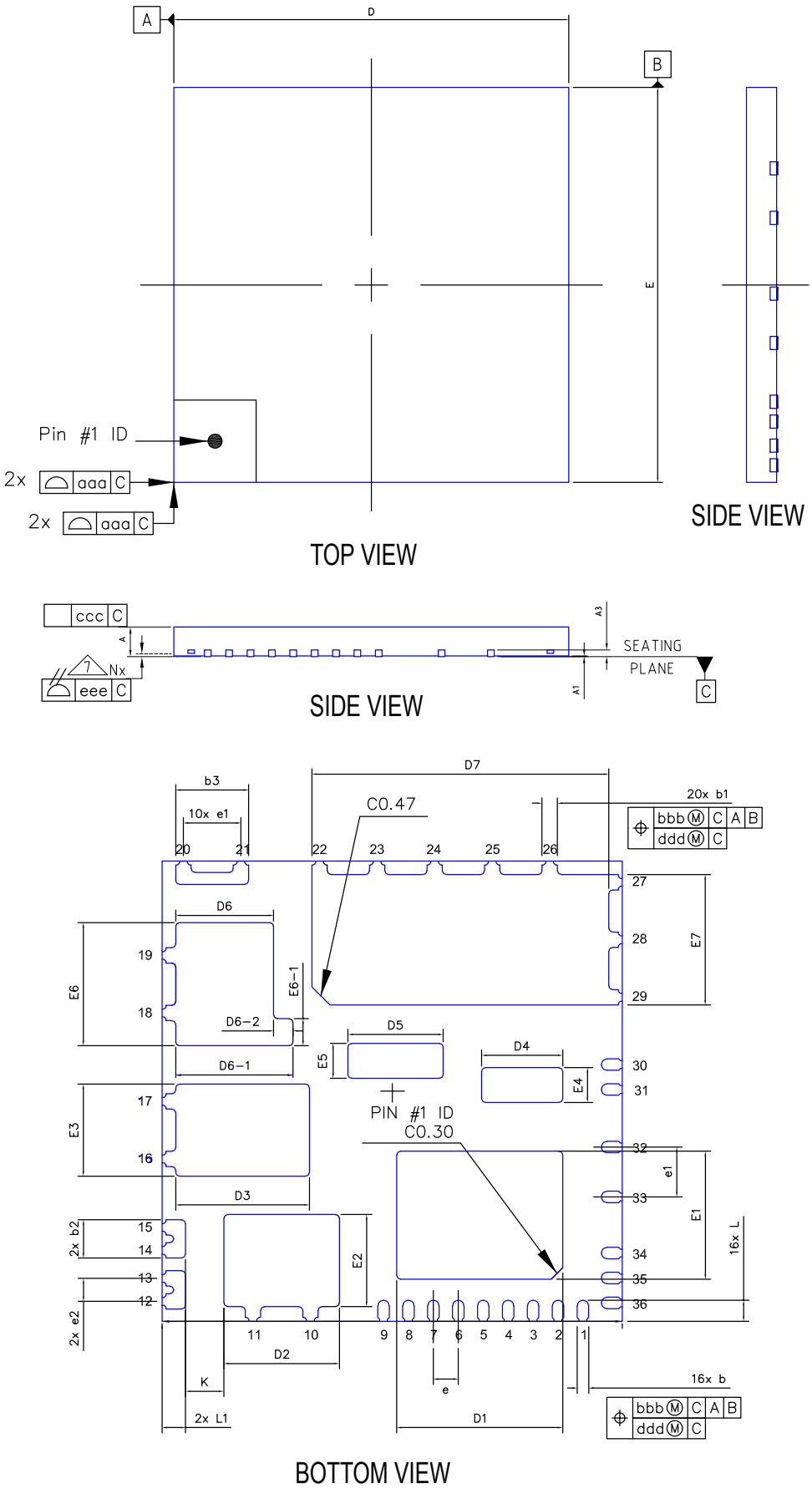
8.1 VFQFPN 12x12x0.95 mm, 36 leads, 0.65 mm pitch, package information

Table 10. Package dimensions

Symbol	Dimensions [mm]		
	Min.	Typ.	Max
A	0.80	0.90	1.00
A1	0.000	0.020	0.050
A3		0.203 REF	
b	0.25	0.30	0.35
b1	0.35	0.40	0.45
b2	0.95	1.00	1.05
b3	1.85	1.90	1.95
D		12.00 BSC	
E		12.00 BSC	
e		0.65 BSC	
e1		1.50 BSC	
e2		0.60 BSC	
e3		1.30 BSC	
D1	4.231	4.331	4.431
E1	3.236	3.336	3.436
D2	2.916	3.016	3.116
E2	2.300	2.400	2.500
D3	3.388	3.488	3.588
E3	2.300	2.400	2.500
D4	2.020	2.120	2.220
E4	0.812	0.912	1.012
D5	2.388	2.488	2.588
E5	0.812	0.912	1.012
D6	2.452	2.552	2.652
D6-1	2.956	3.056	3.156
D6-2	0.404	0.504	0.604
E6	3.108	3.208	3.308
E6-1	0.605	0.705	0.805
D7	7.640	7.740	7.840
E7	3.300	3.400	3.500
K	0.900	1.000	1.100
L	0.450	0.550	0.650

Symbol	Dimensions [mm]		
	Min.	Typ.	Max
L1	0.508	0.608	0.708
	TOLERANCE		
aaa	0.150		
bbb	0.100		
ccc	0.100		
ddd	0.050		
eee	0.080		

Figure 16. **Package outline**

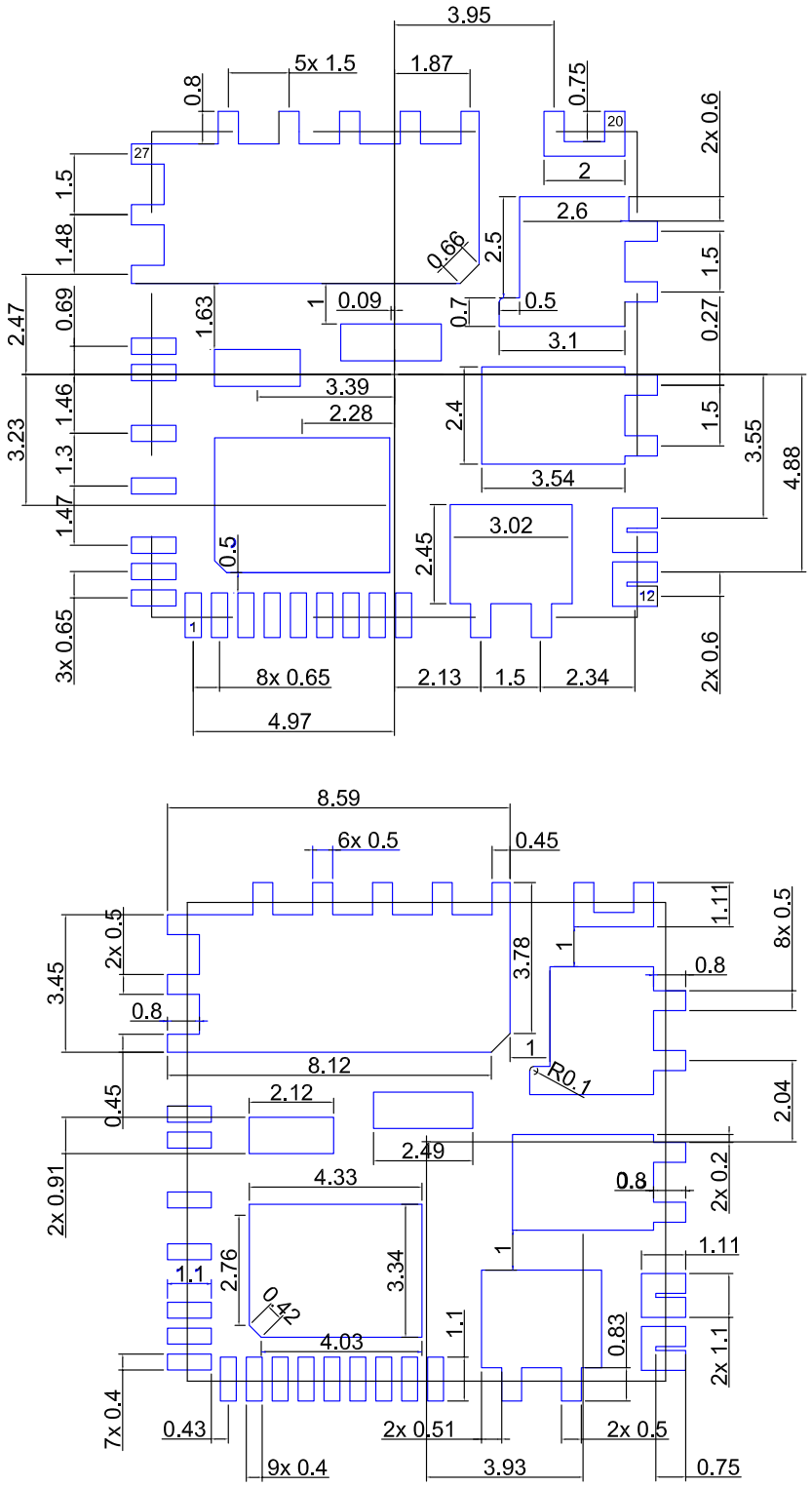


8.2 Suggested footprint

The PWD5T60 footprint for the PCB layout is usually defined based on several design factors as assembly plant technology capabilities and board component density.

For easy device usage and evaluation, ST provides the following footprint design, which is suitable for the largest variety of PCBs.

Figure 17. Suggested footprint (top view)



9 Ordering information

Table 11. **Order code**

Order code	Package	Package marking	Packaging
PWD5T60	VFQFPN 12x12x0.95 mm, 36 leads, 0.65 mm pitch	PWD5T60	Tray
PWD5T60TR	VFQFPN 12x12x0.95 mm, 36 leads, 0.65 mm pitch	PWD5T60	Tape & reel

Revision history

Table 12. **Document revision history**

Date	Version	Changes
15-Jan-2024	1	Initial release.
18-Jun-2024	2	Updated Table 3 (removed the note of the V_{OUT} maximum value), Table 2 (updated note 3) and Table 5 (correct the typo of the t_{OD} and t_{CIN-F} typical value, removed DT and MDT test conditions).

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