Datasheet

Serial EEPROM Series Standard EEPROM

SPI BUS EEPROM

BR25G256xxx-5A Series

General Description

BR25G256xxx-5A Series is a 256 Kbit serial EEPROM of SPI BUS Interface.

Features

- SPI BUS Mode (CPOL, CPHA) = (0, 0), (1, 1)
- Page Size: 64 Byte
- Bit Format: 32768 x 8 bit
- 64 Byte Write Lockable Identification Page (ID Page)
- Address Auto Increment Function at Read Operation
- Auto Erase and Auto End Function at Data Rewrite
- Write Protect Block Setting by Software
  Memory Array 1/4, 1/2, Whole
- HOLD Function by the HOLDB Pin
- Prevention of Write Mistake
  Write Prohibition at Power On
  Write Prohibition by the WPB Pin
  Write Prohibition Block Setting
  Prevention of Write Mistake at Low Voltage
- Data at Shipment
  Memory Array: FFh
  ID Page : FFh
  Status Register WPEN, BP1, BP0: 0, 0, 0
  Lock Status LS: 0

Applications

- Ordinary Electronic Equipment (such as AV Equipment, OA Equipment, Telecommunication Equipment, Home Electronic Appliances, Amusement Equipment, etc.).

Typical Application Circuit

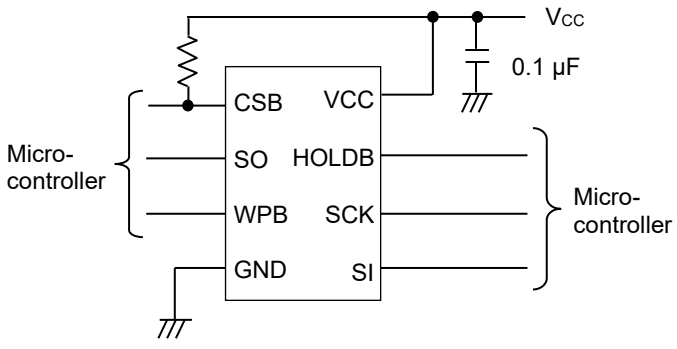


Figure 1. Typical Application Circuit

Key Specifications

- Supply Voltage: 1.6 V to 5.5 V
- Ambient Operating Temperature: -40 °C to +85 °C
- Clock Frequency: 20 MHz (Max)
- Write Time: 3.5 ms (Max)
- Write Cycles:
  4 Million Times (Ta = 25 °C)
- Data Retention:
  200 Years (Ta = 55 °C)

Packages

	W (Typ) x D (Typ) x H (Max)
SOP-J8	4.9 mm x 6.0 mm x 1.65 mm
TSSOP-B8	3.0 mm x 6.4 mm x 1.2 mm
MSOP8	2.9 mm x 4.0 mm x 0.9 mm
VSON08AX2030	2.0 mm x 3.0 mm x 0.6 mm

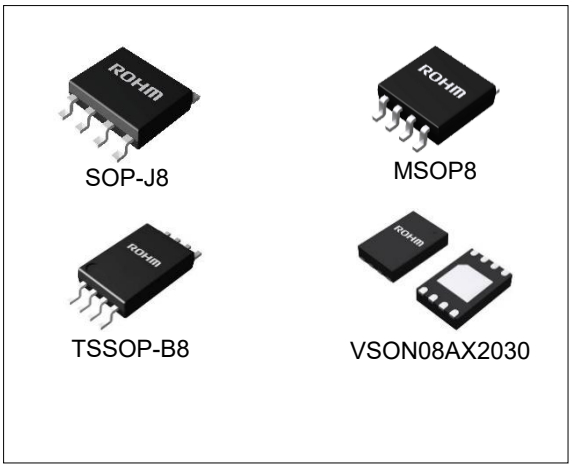


Figure 2

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Pin Configurations

(TOP VIEW)

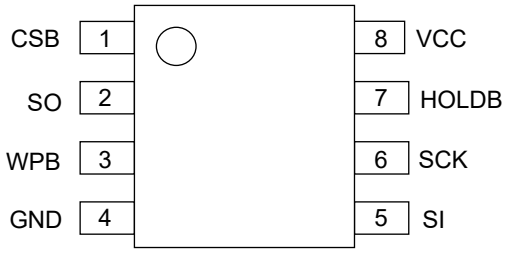


Figure 3-(a). Pin Configuration
(SOP-J8, TSSOP-B8, MSOP8)

(TOP VIEW)

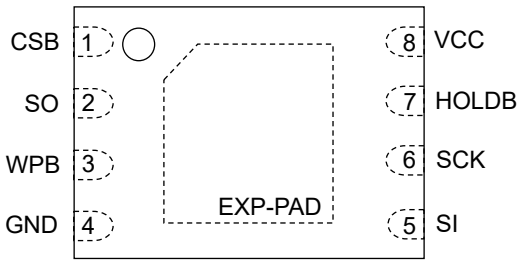


Figure 3-(b). Pin Configuration
(VSON08AX2030)

Pin Description

Pin No.	Pin Name	Input/Output	Descriptions
1	CSB	Input	Chip select input
2	SO	Output	Serial data output
3	WPB	Input	Write protect input
4	GND	-	All input/output reference voltage, 0 V
5	SI	Input	Serial data input
6	SCK	Input	Serial clock input
7	HOLDB	Input	Hold input
8	VCC	-	Power supply
-	EXP-PAD	-	Leave as OPEN or connect to GND

Block Diagram

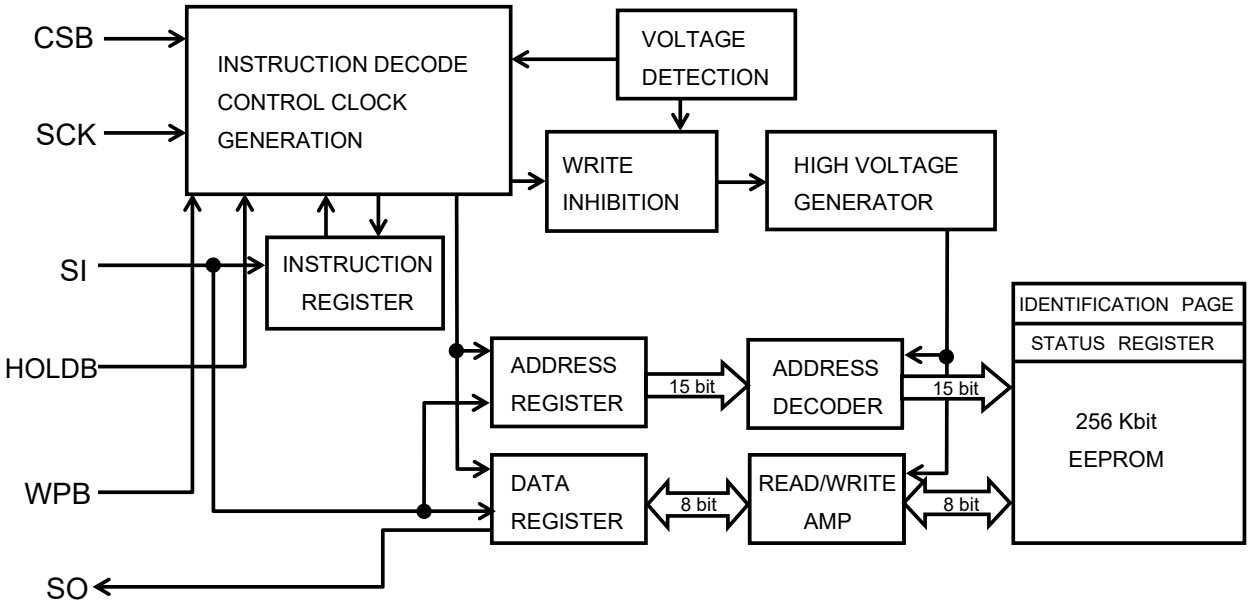


Figure 4. Block Diagram

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Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Remark
Supply Voltage	V_{CC}	-0.3 to +6.5	V	Ta = 25 °C
Terminal Voltage	-	-0.3 to V_{CC}+1.0	V	Ta = 25 °C. The maximum value of terminal voltage is not over than 6.5 V. When the pulse width is 50 ns or less, the minimum value of terminal voltage is -1.0 V.
Electro Static Discharge (Human Body Model)	V_{ESD}	-3000 to +3000	V	Ta = 25 °C
Maximum Output Low Current (SO)	I_{OLMAX}	10	mA	Ta = 25 °C
Maximum Output HIGH Current (SO)	I_{OHMAX}	-10	mA	Ta = 25 °C
Maximum Junction Temperature	Tjmax	150	°C	-
Storage Temperature Range	Tstg	-65 to +150	°C	-

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s*(Note 3)*	2s2p*(Note 4)*	
SOP-J8				
Junction to Ambient	θ_{JA}	149.3	76.9	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	18	11	°C/W
TSSOP-B8				
Junction to Ambient	θ_{JA}	251.9	152.1	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	31	20	°C/W
MSOP8				
Junction to Ambient	θ_{JA}	284.1	135.4	°C/W
Junction to Top Characterization Parameter*(Note 2)*	Ψ_{JT}	21	11	°C/W

(Note 1) Based on JESD51-2A (Still-Air)
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

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Thermal Resistance (Note 5) - continued

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 7)	2s2p(Note 8)	
VSON08AX2030				
Junction to Ambient	θ_{JA}	299.5	77.8	°C/W
Junction to Top Characterization Parameter(Note 6)	Ψ_{JT}	42	18	°C/W

(Note 5) Based on JESD51-2A(Still-Air)
(Note 6) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 7) Using a PCB board based on JESD51-3.
(Note 8) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 9)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ 0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 9) This thermal via connect with the copper pattern of layers 1,2, and 4. The placement and dimensions obey a land pattern.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	1.6	-	5.5	V
Ambient Operating Temperature	Ta	-40	-	+85	°C
Bypass Capacitor(Note 10)	C	0.1	-	-	µF

(Note 10) Connect a bypass capacitor between the IC's VCC and GND pin.

Input/Output Capacitance (Ta = 25 °C, f = 5 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input Capacitance(Note 11)	C_{IN}	-	-	8	pF	V_{IN} = GND
Output Capacitance(Note 11)	C_{OUT}	-	-	8	pF	V_{OUT} = GND

(Note 11) Not 100 % Tested.

Memory Cell Characteristics (V_{CC} = 1.6 V to 5.5 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Write Cycles(Note 12, 13)	-	4,000,000	-	-	Times	Ta = 25 °C
Data Retention(Note 12)	-	200	-	-	Years	Ta = 55 °C

(Note 12) Not 100 % Tested.
(Note 13) The Write Cycles is defined for unit of 4 data bytes with the same address bits of WA14 to WA2.

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Electrical Characteristics (Unless otherwise specified, Ta = -40 °C to +85 °C, V_{CC} = 1.6 V to 5.5 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Input High Voltage 1	V_{IH1}	0.7V_{CC}	-	V_{CC} +1.0	V	1.7 V ≤ V_{CC} ≤ 5.5 V
Input High Voltage 2	V_{IH2}	0.8V_{CC}	-	V_{CC} +1.0	V	1.6 V ≤ V_{CC} < 1.7 V
Input Low Voltage 1	V_{IL1}	-0.3*(Note 14)*	-	+0.3V_{CC}	V	1.7 V ≤ V_{CC} ≤ 5.5 V
Input Low Voltage 2	V_{IL2}	-0.3*(Note 14)*	-	+0.2V_{CC}	V	1.6 V ≤ V_{CC} < 1.7 V
Output Low Voltage 1	V_{OL1}	0	-	0.4	V	I_{OL} = 3.0 mA, 2.5 V ≤ V_{CC} ≤ 5.5 V
Output Low Voltage 2	V_{OL2}	0	-	0.2	V	I_{OL} = 1.0 mA, 1.6 V ≤ V_{CC} < 2.5 V
Output High Voltage 1	V_{OH1}	0.8V_{CC}	-	V_{CC}	V	I_{OH} = -2.0 mA, 2.5 V ≤ V_{CC} ≤ 5.5 V
Output High Voltage 2	V_{OH2}	0.8V_{CC}	-	V_{CC}	V	I_{OH} = -400 µA, 1.6 V ≤ V_{CC} < 2.5 V
Input Leakage Current	I_{LI}	-1	-	+1	µA	V_{IN} = 0 V to V_{CC}
Output Leakage Current	I_{LO}	-1	-	+1	µA	V_{OUT} = 0 V to V_{CC}, CSB = V_{CC}
Supply Current (WRITE) *(Note 15)*	I_{CC1}	-	-	1.7	mA	V_{CC} = 5.5 V, f_{SCK} = 20 MHz, $t_{E/W}$ = 3.5 ms V_{IH}/V_{IL} = 0.9V_{CC} /0.1V_{CC}, SO = OPEN
Supply Current (READ) *(Note 15)*	I_{CC2}	-	-	1.0	mA	V_{CC} = 1.6 V, f_{SCK} = 5 MHz V_{IH}/V_{IL} = 0.9V_{CC} /0.1V_{CC}, SO = OPEN
	I_{CC3}	-	-	1.5	mA	V_{CC} = 2.5 V, f_{SCK} = 5 MHz V_{IH}/V_{IL} = 0.9V_{CC} /0.1V_{CC}, SO = OPEN
	I_{CC4}	-	-	3.0	mA	V_{CC} = 5.5 V, f_{SCK} = 5 MHz V_{IH}/V_{IL} = 0.9V_{CC} /0.1V_{CC}, SO = OPEN
	I_{CC5}	-	-	2.0	mA	V_{CC} = 2.5 V, f_{SCK} = 10 MHz V_{IH}/V_{IL} = 0.9V_{CC} /0.1V_{CC}, SO = OPEN
	I_{CC6}	-	-	4.0	mA	V_{CC} = 5.5 V, f_{SCK} = 10 MHz V_{IH}/V_{IL} = 0.9V_{CC} /0.1V_{CC}, SO = OPEN
	I_{CC7}	-	-	8.0	mA	V_{CC} = 5.5 V, f_{SCK} = 20 MHz V_{IH}/V_{IL} = 0.9V_{CC} /0.1V_{CC}, SO = OPEN
Standby Current	I_{SB}	-	-	2.5	µA	V_{CC} = 5.5 V CSB = HOLDB = WPB = V_{CC}, SCK = SI = V_{CC} or 0 V, SO = OPEN

(Note 14) When the pulse width is 50 ns or less, it is -1.0 V.
(Note 15) The average value during operation.

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AC Characteristics (Unless otherwise specified, Ta = -40 °C to +85 °C, C_{L1} = 30 pF, V_{CC} = 1.6 V to 5.5 V)

Parameter	Symbol	1.6 V ≤ V_{CC} < 1.7 V			1.7 V ≤ V_{CC} < 2.5 V			2.5 V ≤ V_{CC} < 4.5 V			4.5 V ≤ V_{CC} ≤ 5.5 V			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SCK Frequency	f_{SCK}	0.01	-	5	0.01	-	5	0.01	-	10	0.01	-	20	MHz
SCK High Time	t_{SCKWH}	80	-	-	80	-	-	40	-	-	20	-	-	ns
SCK Low Time	t_{SCKWL}	80	-	-	80	-	-	40	-	-	20	-	-	ns
CSB High Time	t_{CS}	85	-	-	85	-	-	40	-	-	20	-	-	ns
CSB Setup Time	t_{CSS}	60	-	-	60	-	-	30	-	-	15	-	-	ns
CSB Hold Time	t_{CSH}	80	-	-	60	-	-	30	-	-	15	-	-	ns
SCK Setup Time	t_{SCKS}	60	-	-	60	-	-	30	-	-	15	-	-	ns
SCK Hold Time	t_{SCKH}	60	-	-	60	-	-	30	-	-	15	-	-	ns
SI Setup Time	t_{DIS}	20	-	-	20	-	-	10	-	-	5	-	-	ns
SI Hold Time	t_{DIH}	30	-	-	20	-	-	10	-	-	5	-	-	ns
Data Output Delay Time1	t_{PD1}	-	-	70	-	-	50	-	-	30	-	-	20	ns
Data Output Delay Time2 (C_{L2} = 100 pF)	t_{PD2}	-	-	80	-	-	60	-	-	40	-	-	20	ns
Output Hold Time	t_{OH}	0	-	-	0	-	-	0	-	-	0	-	-	ns
Output Disable Time	t_{OZ}	-	-	80	-	-	80	-	-	40	-	-	20	ns
HOLDB Setting Setup Time	t_{HFS}	0	-	-	0	-	-	0	-	-	0	-	-	ns
HOLDB Setting Hold Time	t_{HFH}	40	-	-	40	-	-	30	-	-	15	-	-	ns
HOLDB Release Setup Time	t_{HRS}	0	-	-	0	-	-	0	-	-	0	-	-	ns
HOLDB Release Hold Time	t_{HRH}	60	-	-	60	-	-	30	-	-	15	-	-	ns
Time from HOLDB to Output High-Z	t_{HOZ}	-	-	80	-	-	80	-	-	40	-	-	20	ns
Time from HOLDB to Output Change	t_{HPD}	-	-	100	-	-	80	-	-	40	-	-	20	ns
SCK Rise Time *(Note 16)*	t_{RC}	-	-	2	-	-	2	-	-	2	-	-	2	µs
SCK Fall Time *(Note 16)*	t_{FC}	-	-	2	-	-	2	-	-	2	-	-	2	µs
Output Rise Time *(Note 16)*	t_{RO}	-	-	40	-	-	40	-	-	20	-	-	10	ns
Output Fall Time *(Note 16)*	t_{FO}	-	-	40	-	-	40	-	-	20	-	-	10	ns
Write Time	$t_{E/W}$	-	-	3.5	-	-	3.5	-	-	3.5	-	-	3.5	ms

(Note 16) Not 100 % Tested.

AC Characteristics Condition

Parameter	Symbol	Conditions	Unit
Load Capacitance1	C_{L1}	30	pF
Load Capacitance2	C_{L2}	100	pF
Input Rise Time	-	50	ns
Input Fall Time	-	50	ns
Input Voltage	-	0.2V_{CC} / 0.8V_{CC}	V
Input/Output Judgment Voltage	-	0.3V_{CC} / 0.7V_{CC}	V

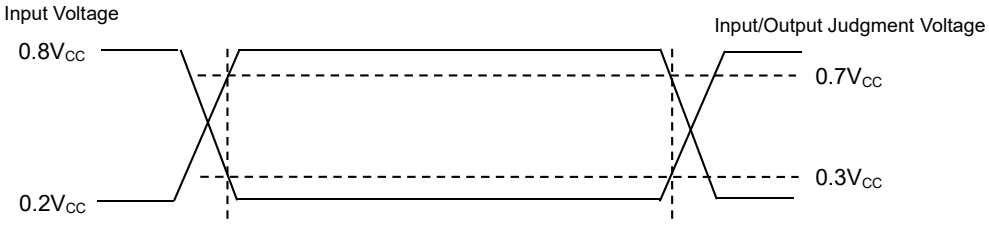


Figure 5. Input/Output Judgment Voltage

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Input/Output Timing

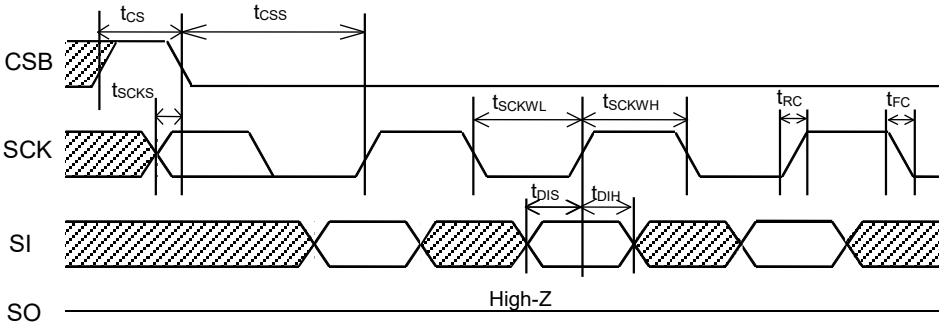


Figure 6-(a). Input Timing

SI is taken into IC inside in sync with data rise edge of SCK. Input address and data from the Most Significant Bit MSB.

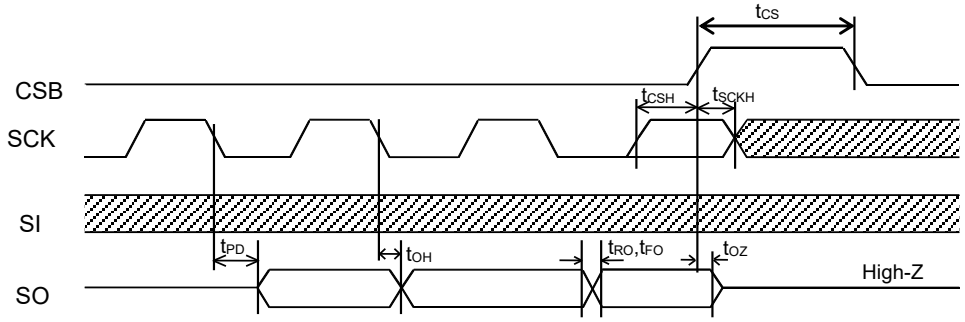


Figure 6-(b). Input/Output Timing

SO is output in sync with data fall edge of SCK. Data is output from the Most Significant Bit MSB.

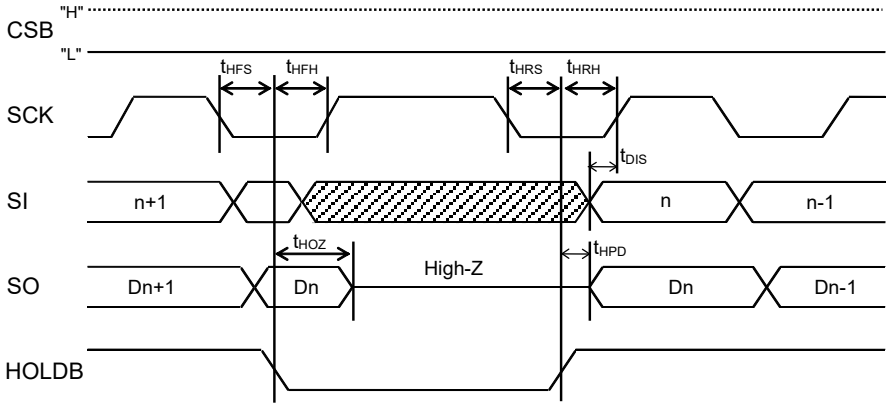


Figure 6-(c). HOLD Timing

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Typical Performance Curves

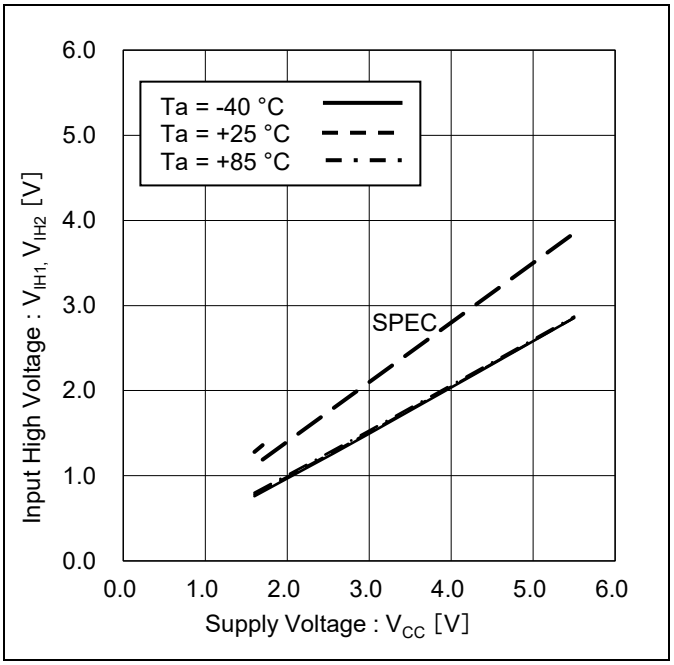


Figure 7. Input High Voltage 1,2 vs Supply Voltage
(CSB, SCK, SI, HOLDB, WPB)

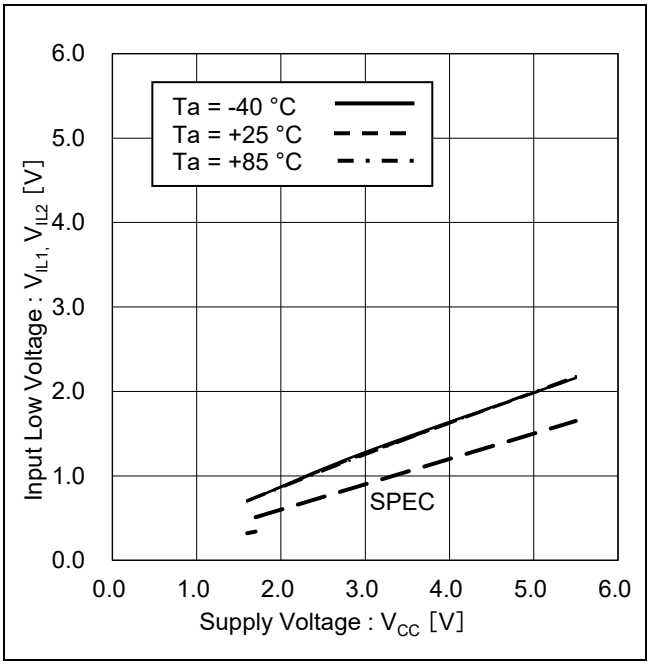


Figure 8. Input Low Voltage 1,2 vs Supply Voltage
(CSB, SCK, SI, HOLDB, WPB)

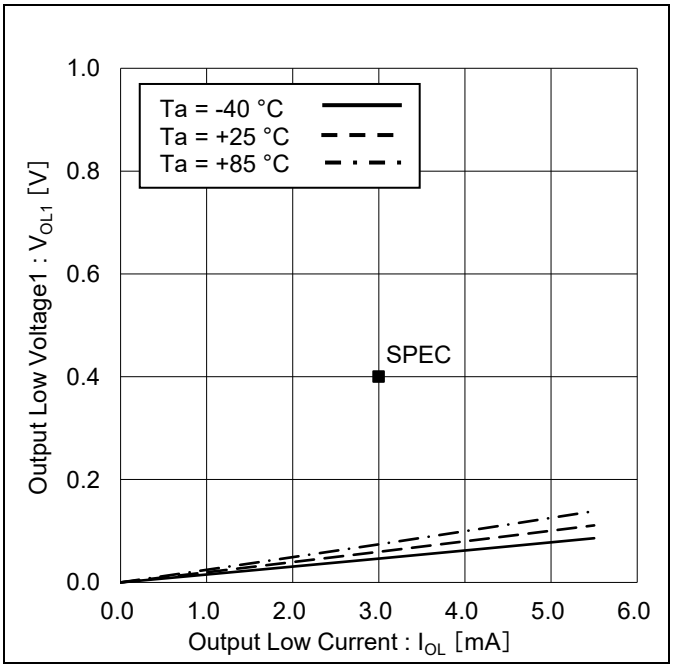


Figure 9. Output Low Voltage1 vs Output Low Current
(V_{CC} = 2.5 V)

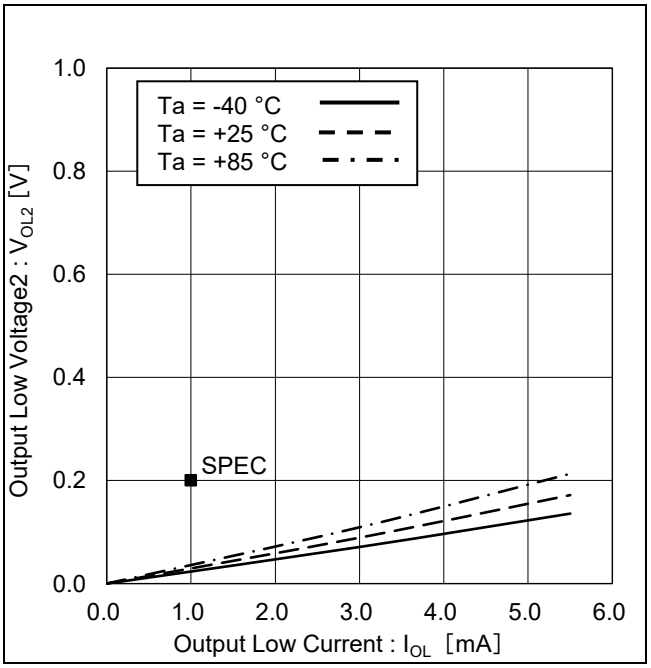


Figure 10. Output Low Voltage2 vs Output Low Current
(V_{CC} = 1.6 V)

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Typical Performance Curves - continued

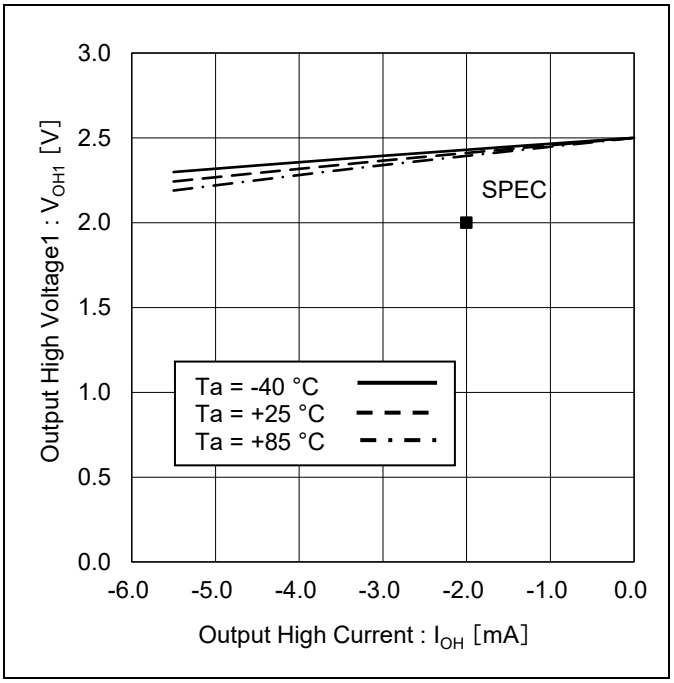


Figure 11. Output High Voltage1 vs Output High Current
(V_{CC} = 2.5 V)

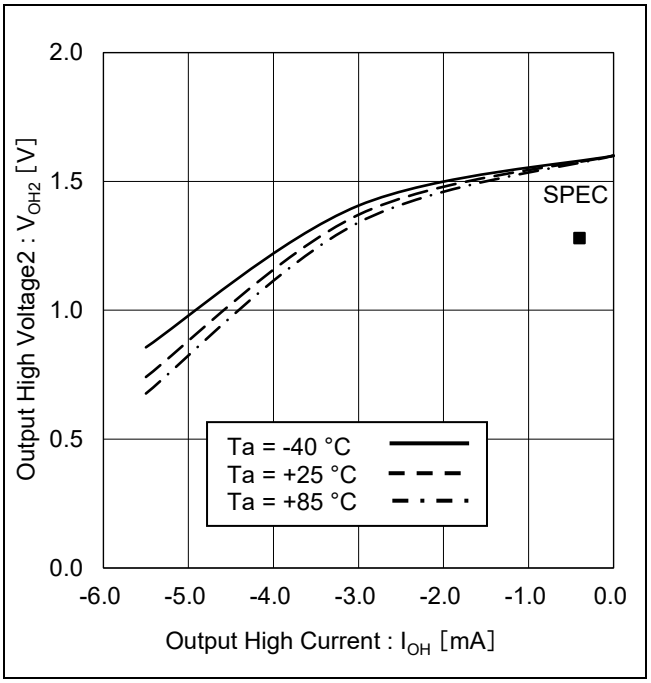


Figure 12. Output High Voltage2 vs Output High Current
(V_{CC} = 1.6 V)

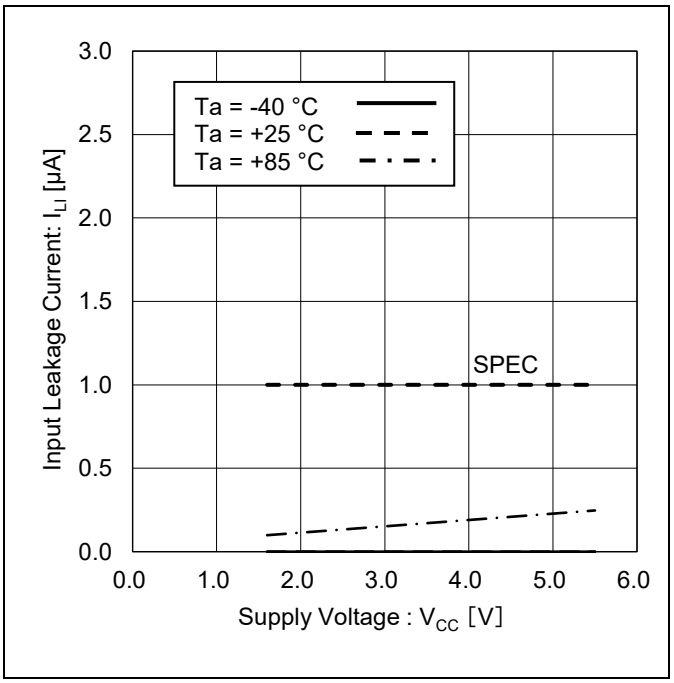


Figure 13. Input Leakage Current vs Supply Voltage
(CSB, SCK, SI, HOLDB, WPB)

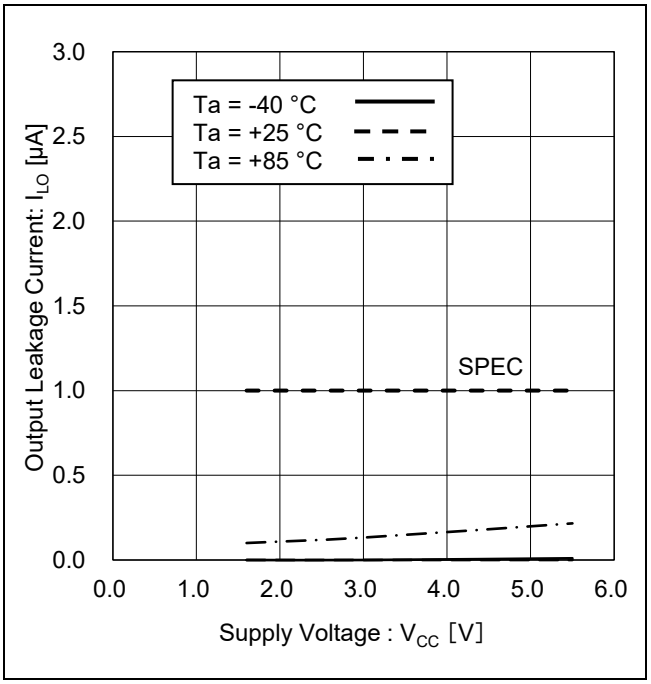


Figure 14. Output Leakage Current vs Supply Voltage
(SO)

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Typical Performance Curves - continued

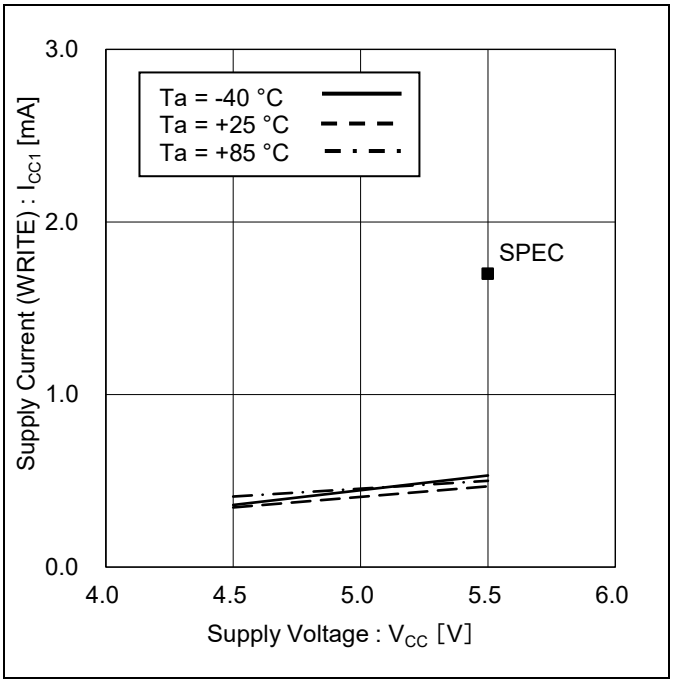


Figure 15. Supply Current (WRITE) vs Supply Voltage

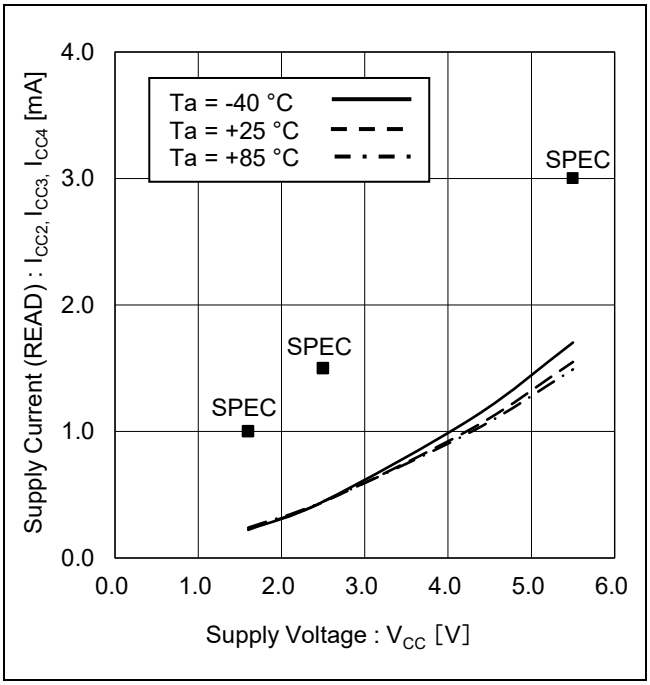


Figure 16. Supply Current (READ) vs Supply Voltage

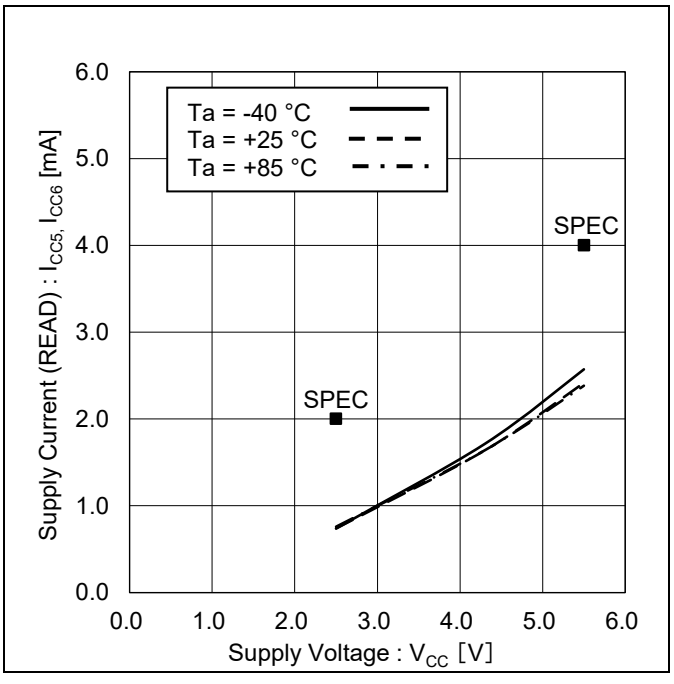


Figure 17. Supply Current (READ) vs Supply Voltage

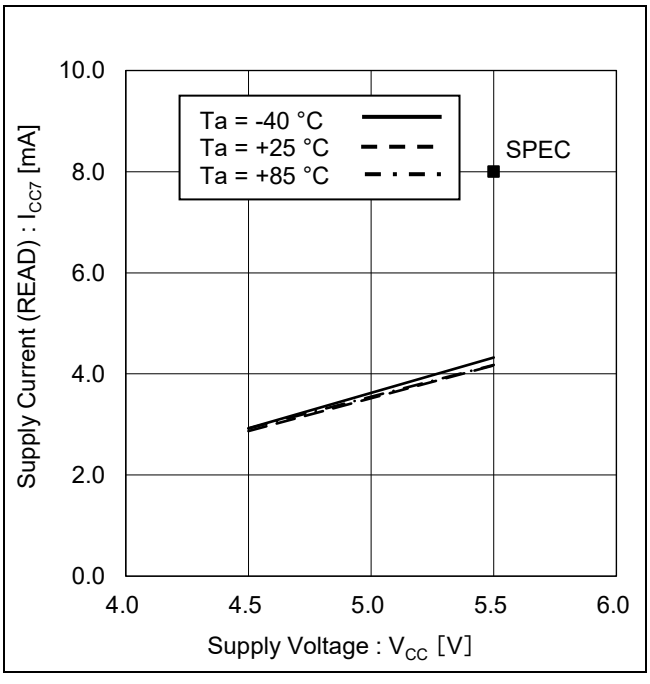


Figure 18. Supply Current (READ) vs Supply Voltage

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Typical Performance Curves - continued

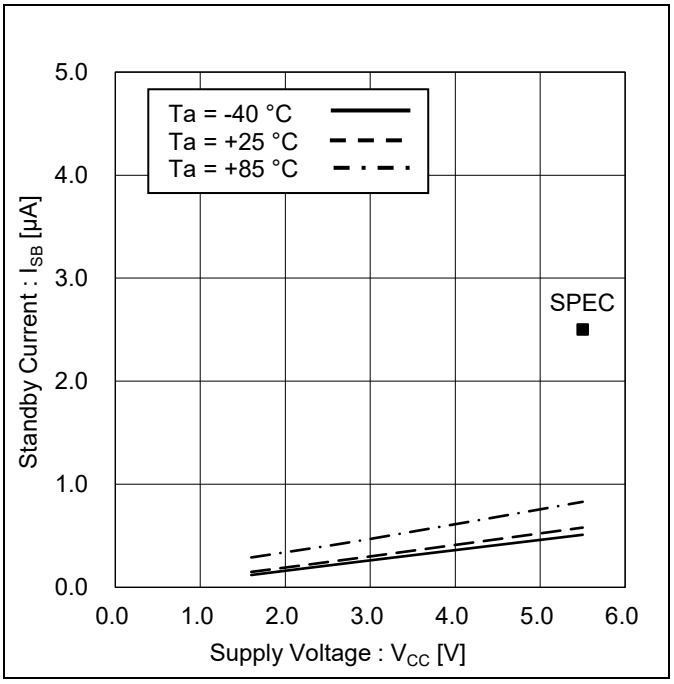


Figure 19. Standby Current vs Supply Voltage

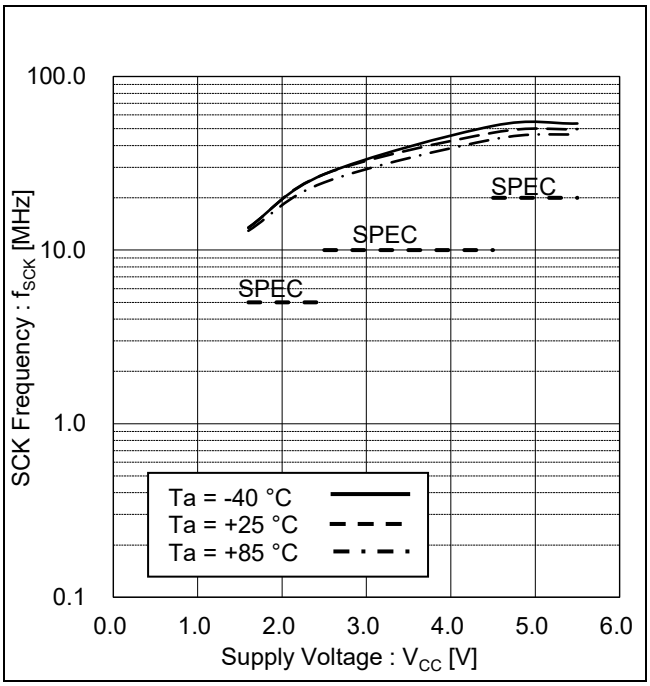


Figure 20. SCK Frequency vs Supply Voltage

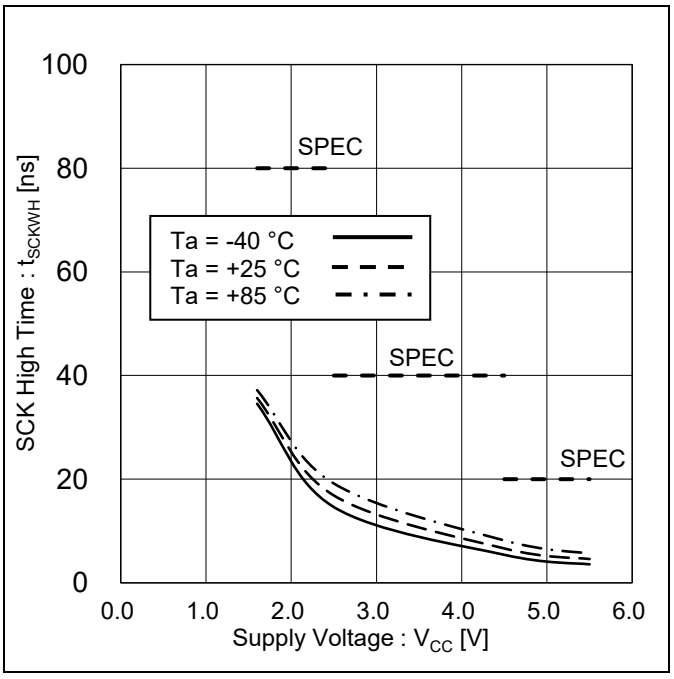


Figure 21. SCK High Time vs Supply Voltage

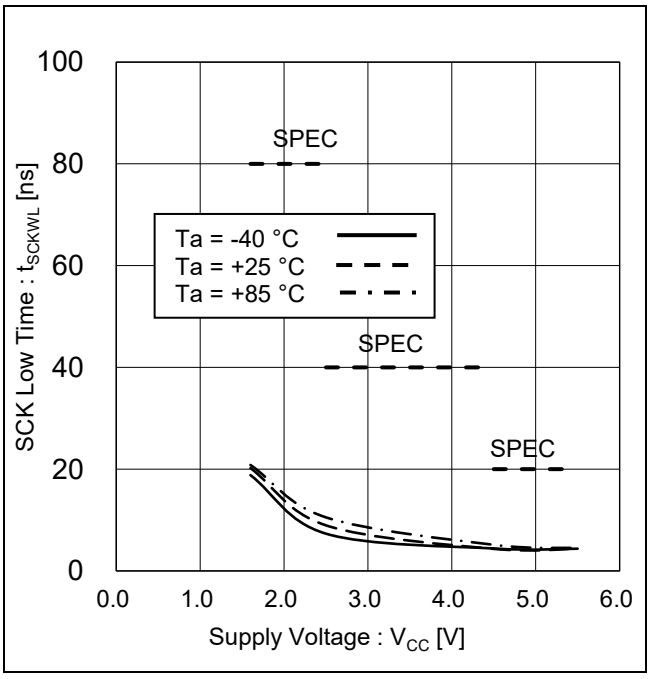


Figure 22. SCK Low Time vs Supply Voltage

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Typical Performance Curves - continued

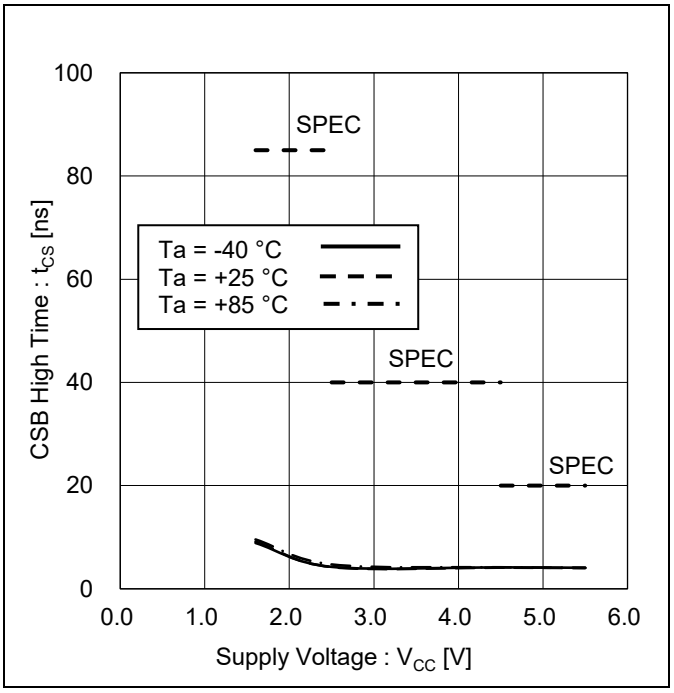


Figure 23. CSB High Time vs Supply Voltage

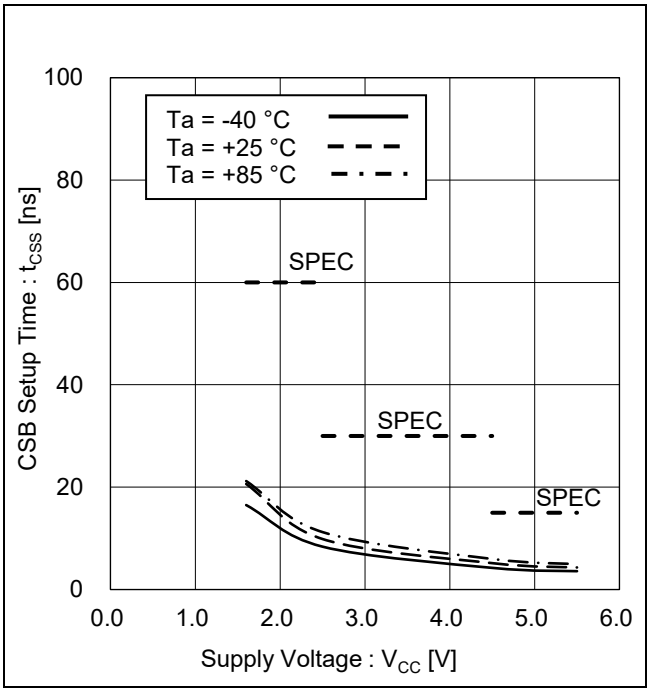


Figure 24. CSB Setup Time vs Supply Voltage

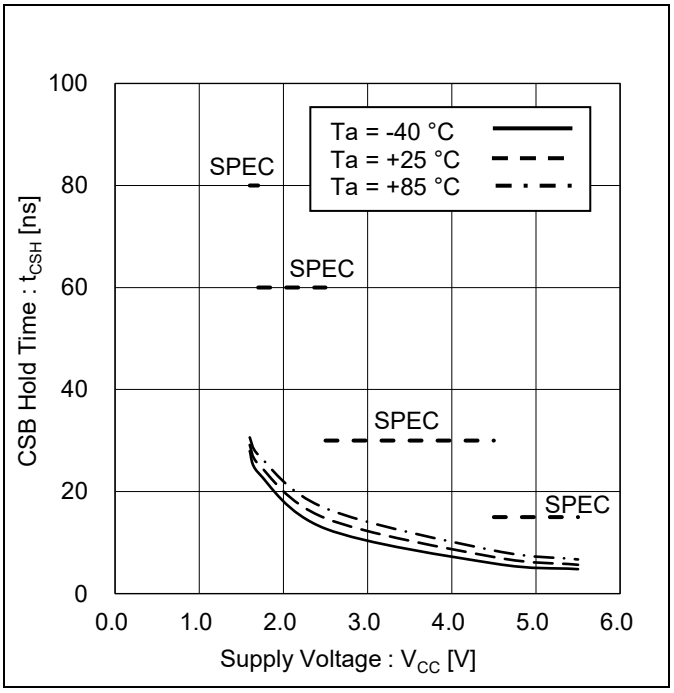


Figure 25. CSB Hold Time vs Supply Voltage

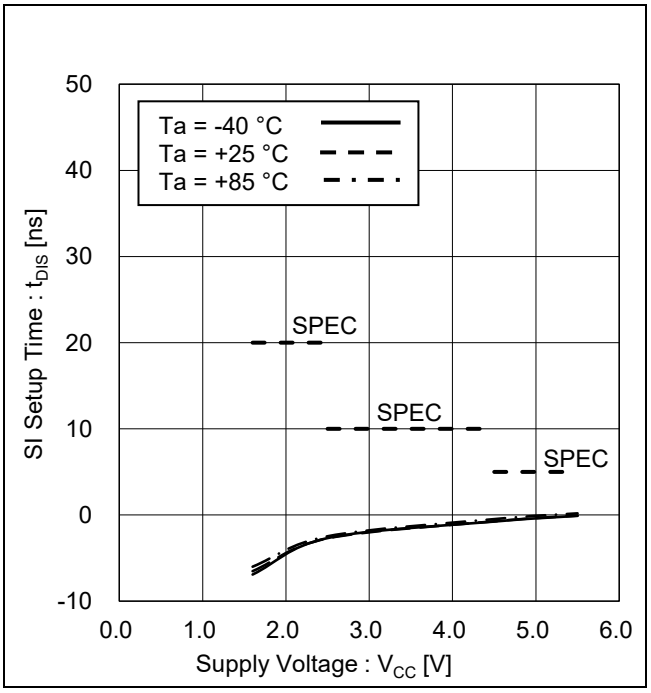


Figure 26. SI Setup Time vs Supply Voltage

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Typical Performance Curves - continued

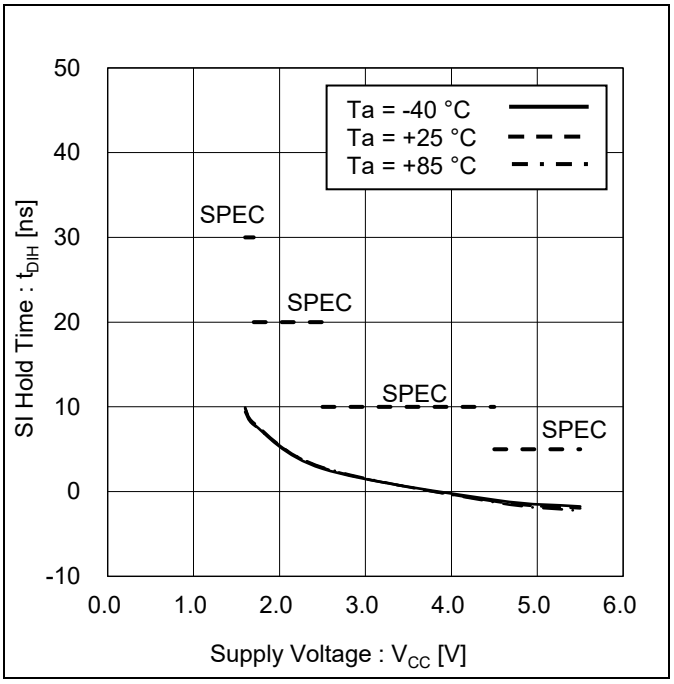


Figure 27. SI Hold Time vs Supply Voltage

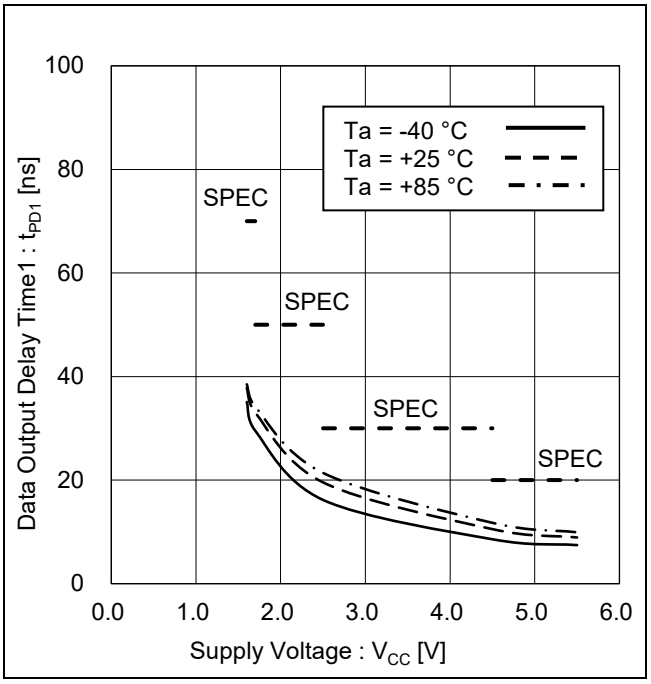


Figure 28. Data Output Delay Time1 vs Supply Voltage

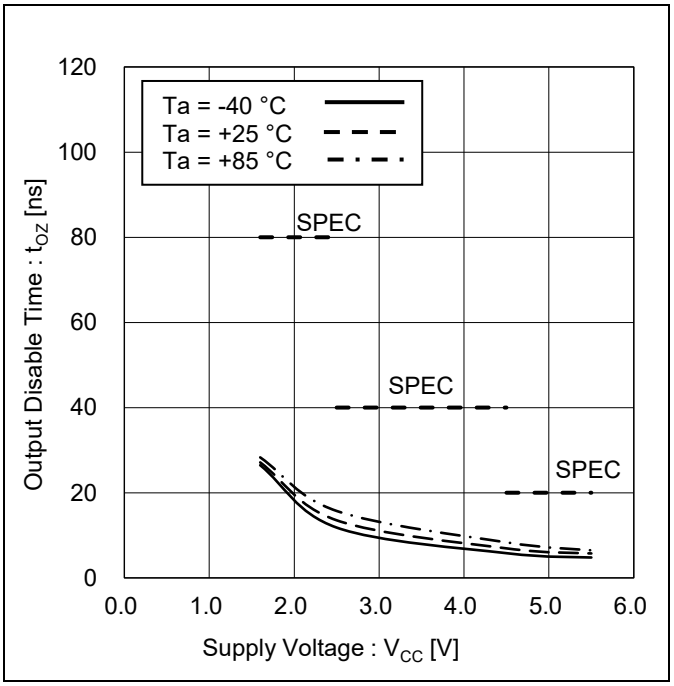


Figure 29. Output Disable Time vs Supply Voltage

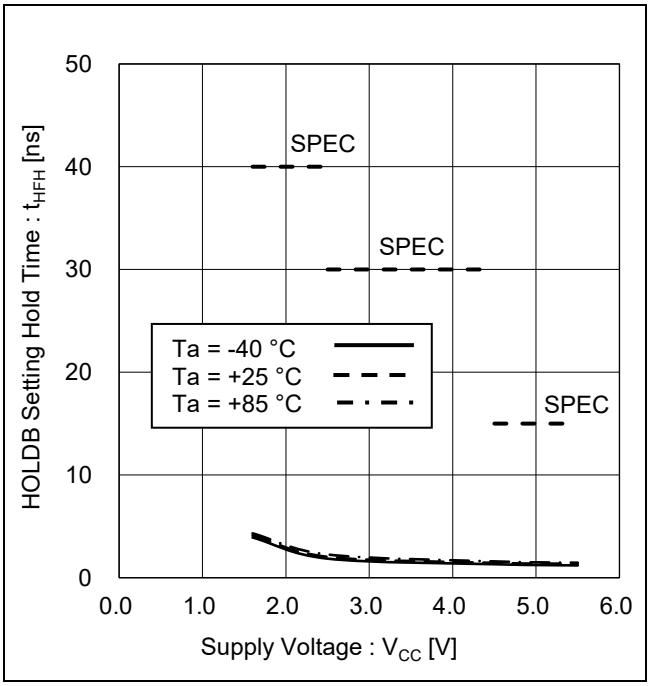


Figure 30. HOLDB Setting Hold Time vs Supply Voltage

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Typical Performance Curves - continued

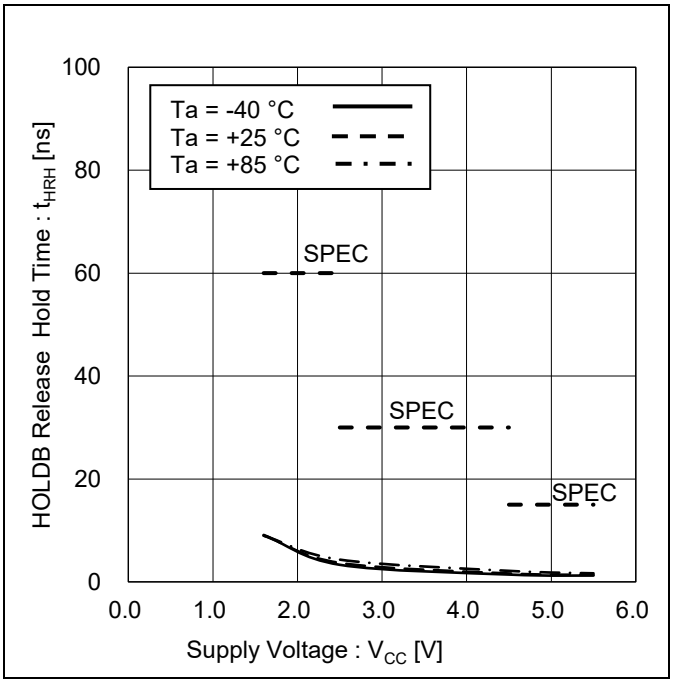


Figure 31. HOLDB Release Hold Time vs Supply Voltage

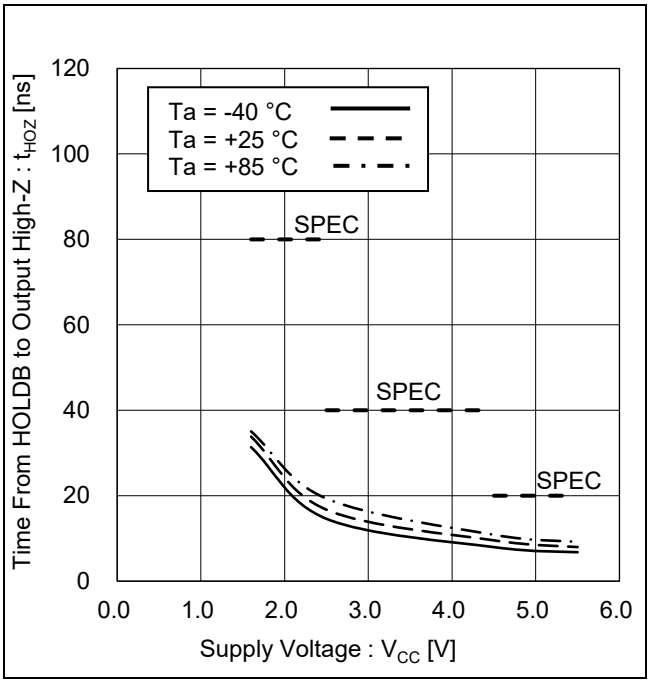


Figure 32. Time from HOLDB to Output High-Z vs Supply Voltage

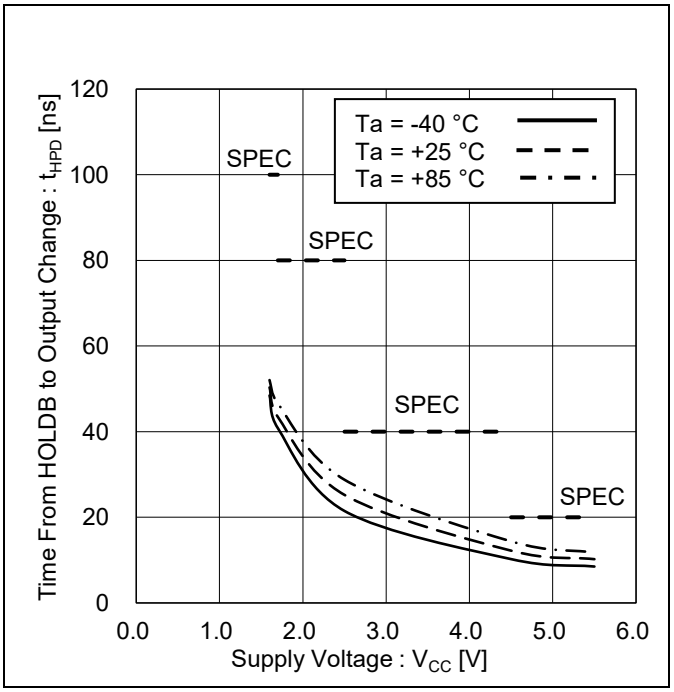


Figure 33. Time from HOLDB to Output Change vs Supply Voltage

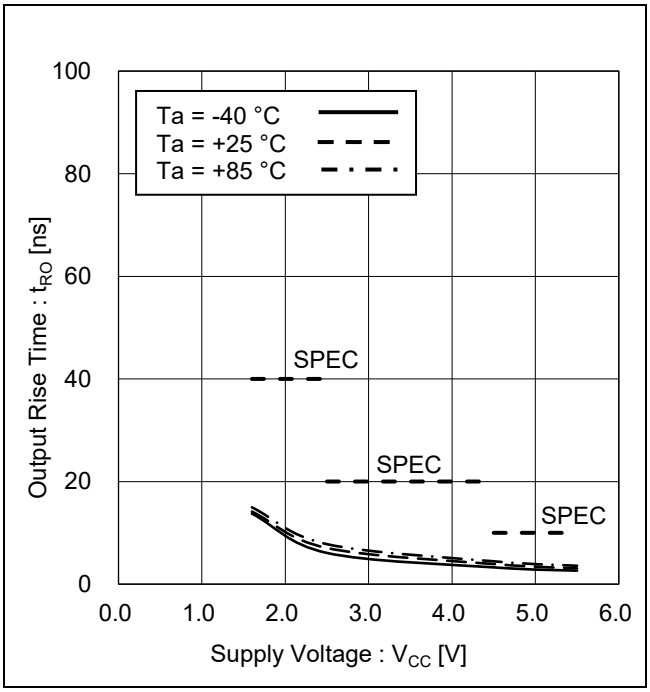


Figure 34. Output Rise Time vs Supply Voltage

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Typical Performance Curves - continued

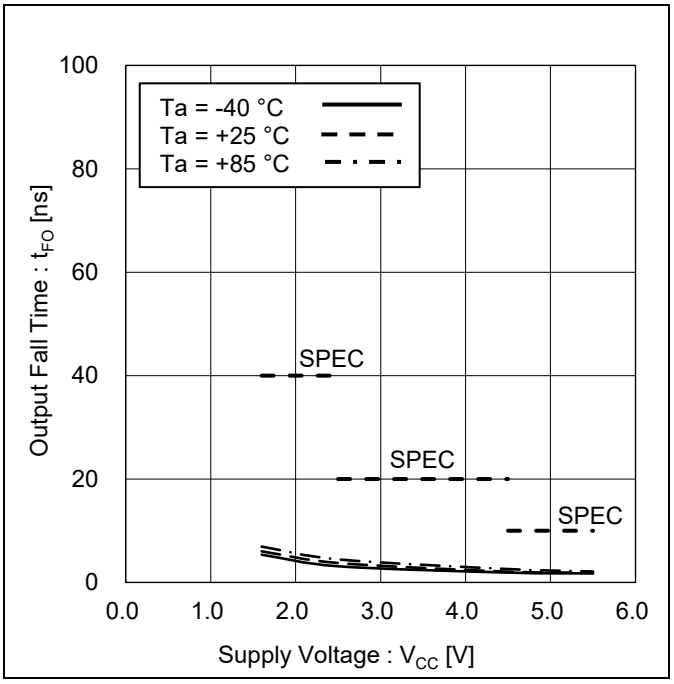


Figure 35. Output Fall Time vs Supply Voltage

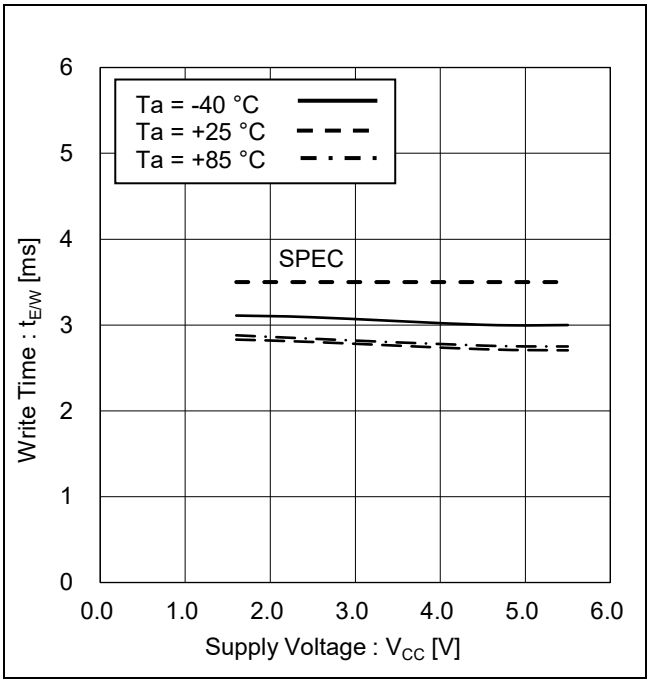


Figure 36. Write Time vs Supply Voltage

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Function Explanation

1. Status Register

This IC has the Status Registers. Status Register are of 8 bits and express the following parameters.
WPEN, BP0 and BP1 can be set by Write Status Register command. These 3 bits are memorized into the EEPROM, therefore are valid even when supply voltage is turned off.
Write Cycles and Data Retention of Status Register are same as characteristics of the EEPROM.
WEN can be set by Write Enable command and Write Disable command. WEN becomes write disable status when supply voltage is turned off. $\overline{R}$/B is for write confirmation, therefore cannot be set externally.
The values of Status Register can be read by Read Status Register command.

Table 1. Status Register

D7	D6	D5	D4	D3	D2	D1	D0
WPEN	0	0	0	BP1	BP0	WEN	$\overline{R}$/B

Table 2. Function of Status Register

bit	Memory Location	Function	Content
WPEN	EEPROM	Pin Enable/Disable designation bit for the WPB pin WPEN = 0 = Invalid, WPEN = 1 = Valid	WPEN bit enables/disables the function of the WPB pin.
BP1 BP0	EEPROM	EEPROM Write Disable Block designation bit	BP1 and BP0 bits designate the Write Disable Block of EEPROM. Refer to Table 3. Write Disable Block Setting.
WEN	Register	Write Enable/Write Disable Confirmation bit WEN = 0 = Prohibited WEN = 1 = Permitted	WEN bit indicates the status of write enable or write disable for WRITE, WRSR, WRID, LID.
$\overline{R}$/B	Register	Write Cycle Status ($\overline{READY}$/BUSY) Confirmation bit $\overline{R}$/B = 0 = READY, $\overline{R}$/B = 1 = BUSY	$\overline{R}$/B bit indicates the status of READY or BUSY of the write cycle.

Table 3. Write Disable Block Setting

Status Register		Protected Block	Protected Addresses
BP1	BP0		
0	0	None	None
0	1	Upper 1/4	6000h to 7FFFh
1	0	Upper 1/2	4000h to 7FFFh
1	1	Whole Memory	0000h to 7FFFh, ID Page

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Function Explanation - continued

2. Write Protect Mode by the WPB pin

By setting WPB = Low with WPEN = 1, Write Status Register command is disabled. Only when WPEN bit is set “1”, the WPB pin functions become valid. However, when write cycle is in execution, no interruption can be made.

Table 4. Write Protect Mode

WPEN bit	WPB pin	Instruction	
		WRSR	WRITE/WRID/LID
0	X	Writable	Writable
1	High	Writable	Writable
1	Low	Write Protected	Writable

WPB is normally fixed to High or Low for use, but when WPB is controlled so as to cancel Write Status Register command, pay attention to the following WPB Valid Timing.

Write Status Register command is executed, by setting WPB = Low in cancel valid area, command can be cancelled. The Data area (from 7th fall of SCK to 16th rise of SCK) becomes the cancel valid area. However, once write is started, any input cannot be cancelled. WPB input becomes Don’t Care, and cancellation becomes invalid.

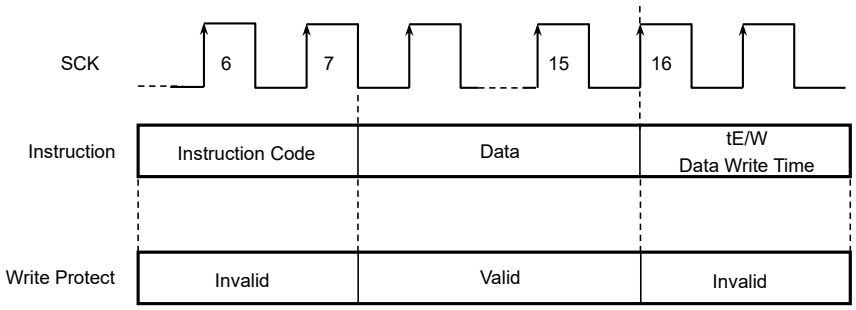


Figure 37. WPB Valid Timing (WRSR)

3. Hold Mode by the HOLDB pin

By the HOLDB pin, serial communication can be stopped temporarily (HOLD status). The HOLDB pin carries out serial communications normally when it is High. To get in HOLD status, at serial communication, when SCK = Low, set the HOLDB pin Low.

At HOLD status, SCK and SI become Don’t Care, and SO becomes high impedance (High-Z).

To release the HOLD status, set HOLDB = High, when SCK = Low. After that, communication can be restarted from the point before the HOLD status. For example, when HOLD status is made after WA5 address input at Read command, after release of HOLD status, by starting WA4 address input, Read command can be restarted. When in HOLD status, leave CSB = Low. When it is set CSB = High in HOLD status, the IC is reset, therefore communication after that cannot be restarted.

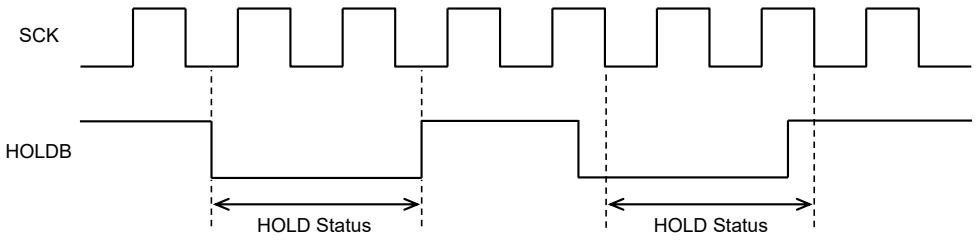


Figure 38. HOLD Status

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Function Explanation - continued

4. ID Page

This IC has 64 byte Write Lockable Identification Page (ID Page) in addition to Memory Array.
By setting Lock Status (LS) bit to “1” with Lock ID Page command, it is prohibited to write to ID page permanently.
It is not reversible to set from ID Page Lock Status (LS = “1”) to ID Page Lock Release status (LS = “0”).

Table 5. Function of Lock Status

bit	Memory Location	Function	Content
LS	EEPROM	ID Page Lock/Release Status designation bit LS = 0 = ID Page Lock Release LS = 1 = ID Page Lock	LS bit can set Lock Status to ID Page.

5. ECC Function

This IC has ECC bits for Error Correction to each 4 data bytes with the same address bits of WA14 to WA2. In the Read operation, even if there is 1 bit data error in the 4 bytes, IC corrects to correct data by ECC function and outputs data corrected. Even if write operation is started with only 1 byte data input, this IC rewrites the data of 4 bytes with the same address bits of WA14 to WA2 and the data of ECC bits added to these 4 bytes data. In order to maximize Write Cycles specified, it is recommended to write with data input of each 4 bytes with the same address bits of WA14 to WA2.

Table 6. Example of 4 data bytes with the same address bits of WA14 to WA2 (Address 0000h, 0001h, 0002h, 0003h)

Same Address Bits from WA14 to WA2													Non-Common		Address
WA 14	WA 13	WA 12	WA 11	WA 10	WA 9	WA 8	WA 7	WA 6	WA 5	WA 4	WA 3	WA 2	WA 1	WA 0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001h
0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0002h
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0003h

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Instruction Mode

After setting the CSB pin from High to Low, to execute each command, input Instruction Code, Address and Data from the Most Significant Bit MSB.

Table 7. Instruction Mode

Instruction	Content	Instruction Code (8 bit)	Address (MSB) / Data (8 bit)	Address (LSB) (8 bit)	Data (8 bit)
WREN	Write Enable	0000 0110	-	-	-
WRDI	Write Disable	0000 0100	-	-	-
READ	Read	0000 0011	WA15 to WA8 *(Note 17)*	WA7 to WA0	D7 to D0 Output
WRITE	Write	0000 0010	WA15 to WA8 *(Note 17)*	WA7 to WA0	D7 to D0 Input
RDSR	Read Status Register	0000 0101	D7 to D0 Output *(Note 18)*	-	-
WRSR	Write Status Register	0000 0001	D7 to D0 Input *(Note 18)*	-	-
RDID	Read ID Page	1000 0011	0000 0000	00WA5 to WA0	D7 to D0 Output
WRID	Write ID Page	1000 0010	0000 0000	00WA5 to WA0	D7 to D0 Input
RDLS	Read Lock Status	1000 0011	0000 0100	0000 0000	D7 to D0 Output *(Note 19)*
LID	Lock ID page	1000 0010	0000 0100	0000 0000	D7 to D0 Input *(Note 19)*

(Note 17) WA15 = Don't Care
(Note 18) Refer to Figure 45 and Figure 46
(Note 19) Refer to Figure 49 and Figure 50

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Timing Chart

1. Write Enable Command (WREN)

It is set to write enable status by Write Enable command. As for this command, set CSB to Low, and then input the Instruction Code of Write Enable command. This command is accepted at the 7th rise of SCK. Even with input over 7 clocks, command becomes valid.

Before carrying out Write command, Write Status Register command, Write ID Page command and Lock ID Page command, it is necessary to set write enable status by the Write Enable command.

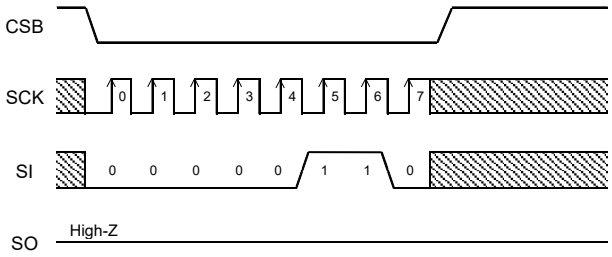


Figure 39. Write Enable Command

2. Write Disable Command (WRDI)

It is set to write disable status, WEN bit becomes to “0”, by Write Disable command. As for this command, set CSB to Low, and then input the Instruction Code of Write Disable command. This command is accepted at the 7th rise of SCK. Even with input over 7 clocks, command becomes valid.

If Write command, Write Status Register command, Write ID Page command or Lock ID Page command is input in the write disable status, commands are cancelled. And even in the write enable status, once Write command, Write Status Register command, Write ID Page command or Lock ID Page is executed, it gets in the write disable status.

After power on, this IC is in write disable status.

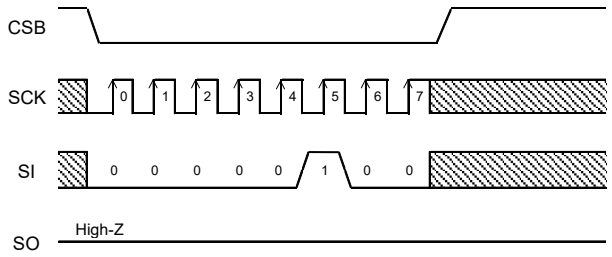


Figure 40. Write Disable Command

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Timing Chart - continued

3. Read Command (READ)

By Read command, data of EEPROM can be read. As for this command, set CSB to Low, then input address after Instruction Code of Read command. This IC starts data output of the designated address. Data output is started from SCK fall of 23 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8 bit), by continuing input of SCK, data of the next address can be read. Increment read can read all the addresses of EEPROM Array. After reading data of the most significant address, by continuing increment read, data of the least significant address is read.

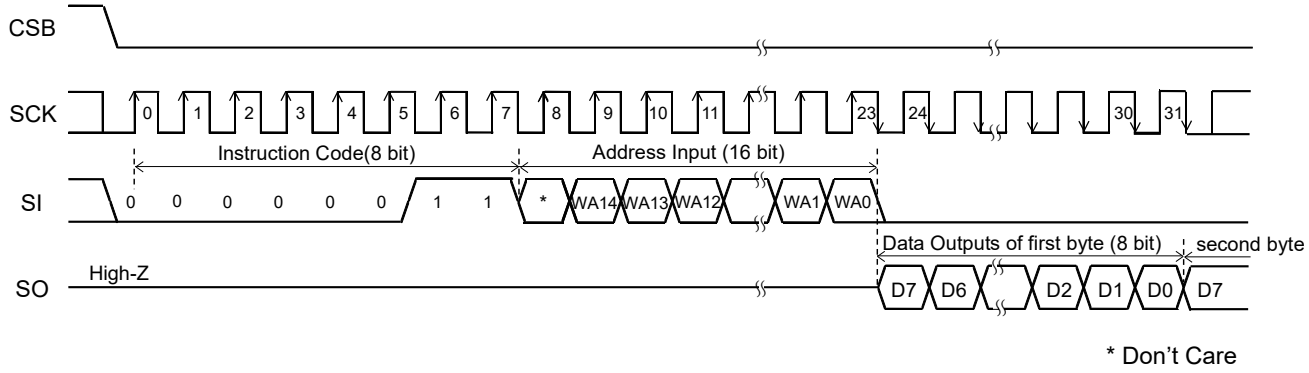


Figure 41. Read Command

4. Write Command (WRITE)

By Write command, data of EEPROM can be written. As for this command, set CSB to Low, then input address and data after Instruction Code of Write command. Then, by making CSB to High, the IC starts write operation. The write time of EEPROM requires time of $t_{E/W}$ (Max 3.5 ms). To start write operation, set CSB Low to High after taking the last data (D0), and before the next SCK clock starts. At other timing, Write command is not executed, and this Write command is cancelled.

During write operation, other than Read Status Register command is not accepted.

This IC has Page Write function, and after input of data for 1 byte (8 bit), by continuing data input without setting CSB High to Low, data up to 64 byte can be written for one $t_{E/W}$. In Page Write, the addressed lower 6 address bits are incremented internally at every time when data of 1 byte is inputted and data is written to respective addresses. When the data input exceeds the last address byte of the page, address rolls over to the first address byte of the same page. It is not recommended to input data over 64 byte, it is recommended to input data in 64 byte. In case of the data input over 64 byte, it is explained in Table 9.

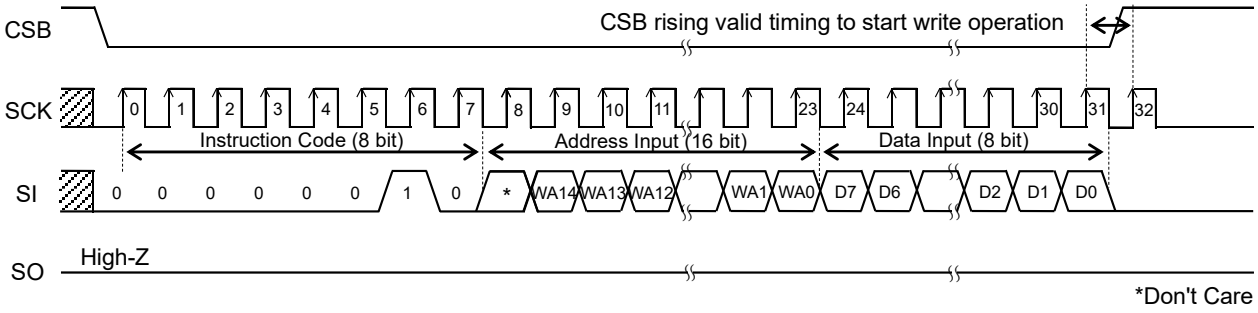


Figure 42. Write Command (Byte Write)

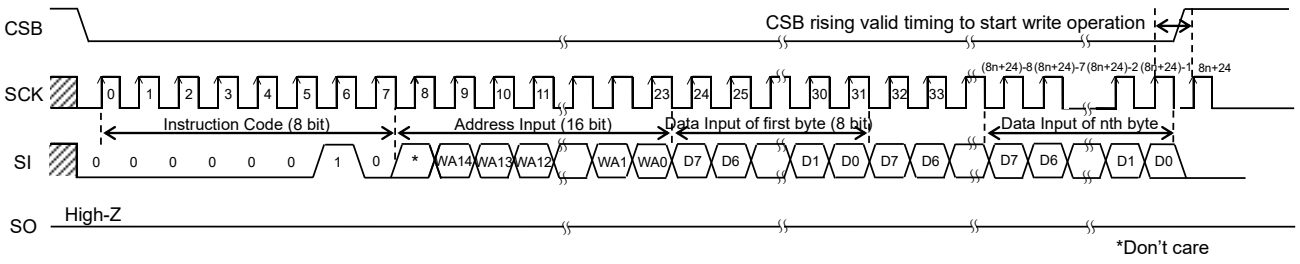


Figure 43. Write Command (Page Write)

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Timing Chart - continued

5. Page Write Function

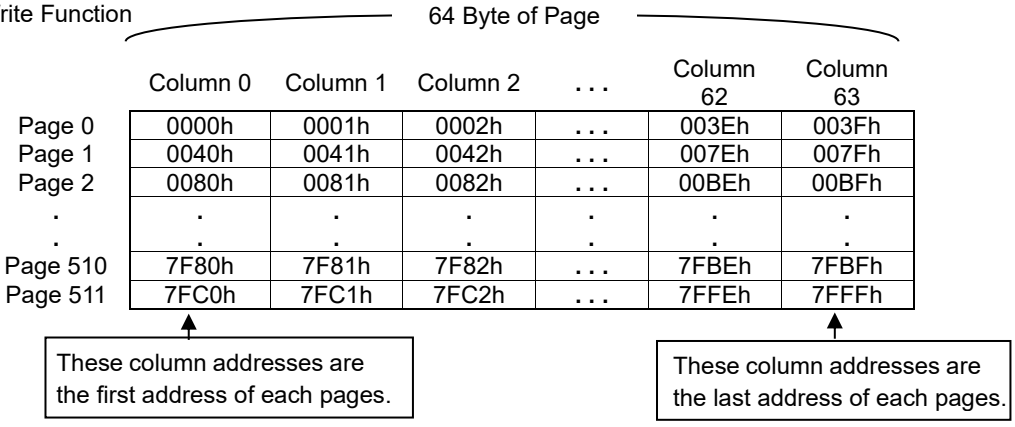


Figure 44. EEPROM physical address for Page Write command (64 Byte)

(1) In case of Page Write command with 64 byte or lower data input

Table 8. Example of Page Write with 2 byte data input

No.	4 Byte group	Group 0				. . .	. . .	Group 15			
	Addresses of Page 0	0000h	0001h	0002h	0003h	0004h	. . .	003Ch	003Dh	003Eh	003Fh
1	Previous Data	00h	01h	02h	03h	04h	. . .	3Ch	3Dh	3Eh	3Fh
2	Input data for Page Write (2 Byte)	AAh	55h	-	-	-	. . .	-	-	-	-
3	The Data after Write operation	AAh	55h	02h	03h	04h	. . .	3Ch	3Dh	3Eh	3Fh

No.1: These data are EEPROM data before Write operation.
No.2: Inputted 2 byte data AAh, 55h from address 0000h.
No.3: If Write operation is executed with the data of No.2, the data are changed from the data of No.1 to the data of No.3.The data of address 0000h, 0001h are changed to data AAh, 55h, the data of address 0002h, 0003h, the 4 byte group of Group 0, are over-written to data 02h, 03h.
When Write command is cancelled, EEPROM data keep No.1.

(2) In case of Page Write command with more than 64 byte data input

Table 9. Example of Page Write with 66 byte data input

No.	4 Byte group	Group 0				. . .	. . .	Group 15			
	Addresses of Page 0	0000h	0001h	0002h	0003h	0004h	. . .	003Ch	003Dh	003Eh	003Fh
1	Previous Data	00h	01h	02h	03h	04h	. . .	3Ch	3Dh	3Eh	3Fh
2	Input data for Page Write (66 Byte)	55h	AAh	55h	AAh	55h	. . .	55h	AAh	55h	AAh
		FFh	00h	-	-	-	. . .	-	-	-	-
3	The Data after Write operation	FFh	00h	02h	03h	55h	. . .	55h	AAh	55h	AAh

No.1: These data are initial EEPROM data before Write operation.
No.2: Inputted 66 byte data 55h, AAh, - - , 55h, AAh, FFh, 00h from address 0000h.
The data of address 0000h, 0001h are set to data 55h, AAh first. The data of address 0002h, 0003h are set to data 55h, AAh. After inputting data to Maximum byte (003Fh), the data address 0000h, 0001h are set to data FFh, 00h again. No data input to address 0002h, 0003h again.
No.3: If Page Write operation is executed with the data of No.2, the data are changed from the data of No.1 to the data of No.3. The data of address 0000h, 0001h are changed to FFh, 00h inputted data later, not to 55h, AAh inputted data first. The data of address 0002h, 0003h, the 4 byte group of Group 0, are over-written to 02h, 03h of Previous Data, not to 55h, AAh inputted data first. The data of other addresses are changed to 55h, AAh - - , 55h, AAh.
When Write command is cancelled, EEPROM data keep No.1.

(3) Roll Over

In Page Write command, when data is set to the last address of a page (e.g. address “003Fh” of page 0), the next data will be set to the first address of the same page (e.g. address “0000h” of page 0). Page Write address increment is available in the same page including the address designated at first.

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Timing Chart - continued

6. Read Status Register Command (RDSR)

By Read Status register command, data of status register can be read. As for this command, set CSB to Low, then input Instruction Code of Read Status Register command. This IC starts data output of the status register. Data output is started from SCK fall of 7 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8 bits), by continuing input of SCK, this IC repeats to output data of the status register.
Even if in write operation, Read Status Register command can be executed.

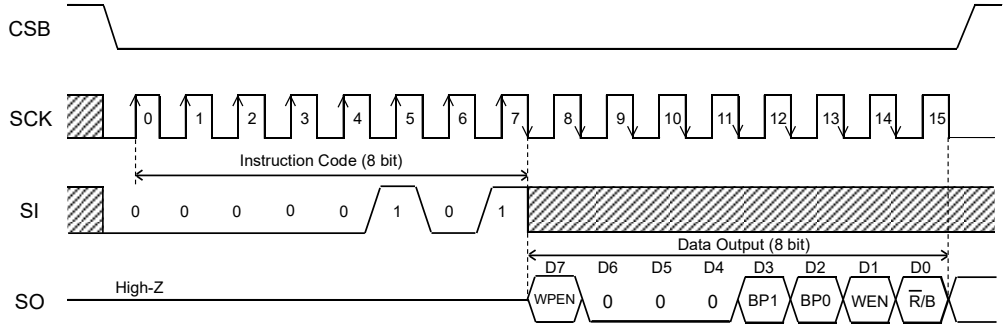


Figure 45. Read Status Register Command

7. Write Status Register Command (WRSR)

Write Status Register command can write status register data. The data can be written by this command are 3 bits, that is, WPEN (D7), BP1 (D3) and BP0 (D2) among 8 bits of status register. As for this command, set CSB to Low, and input Instruction Code of Write Status Register command, and input data. Then, by making CSB to High, this IC starts write operation. Write Time requires time of $t_{E/W}$ as same as Write command. As for CSB rise, start CSB after taking the last data bit (D0), and before the next SCK clock starts. At other timing, command is cancelled.
To the write disabled block, write cannot be made, and only read can be made.
During write operation, other than Read Status Register command is not accepted.

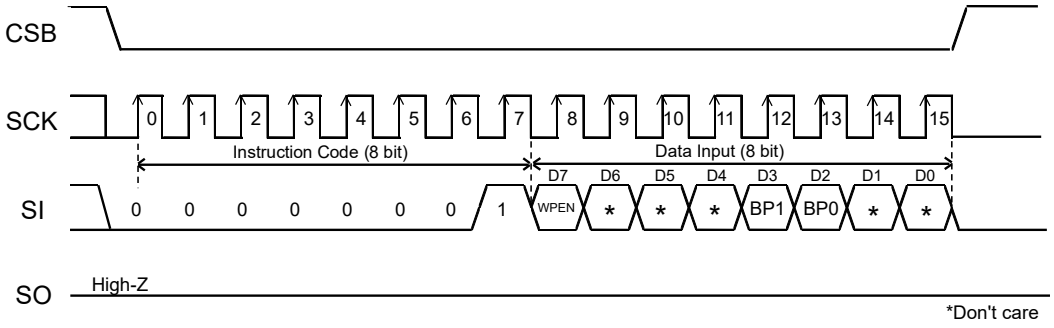


Figure 46. Write Status Register Command

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Timing Chart - continued

8. Read ID Page Command (RDID)

By Read ID Page command, data of ID Page can be read. As for this command, set CSB to Low, then input address after Instruction Code of Read ID Page command. By inputting lower address bits WA5 to WA0, it is possible to address to 64 byte ID Page. Data output is started from SCK fall of 23 clock, and from D7 to D0 sequentially. This IC has increment read function. After output of data for 1 byte (8 bits), by continuing input of SCK, data of the next address can be read. After reading data of the most significant address of ID Page, by continuing increment read, data of the least significant address of ID Page is read.

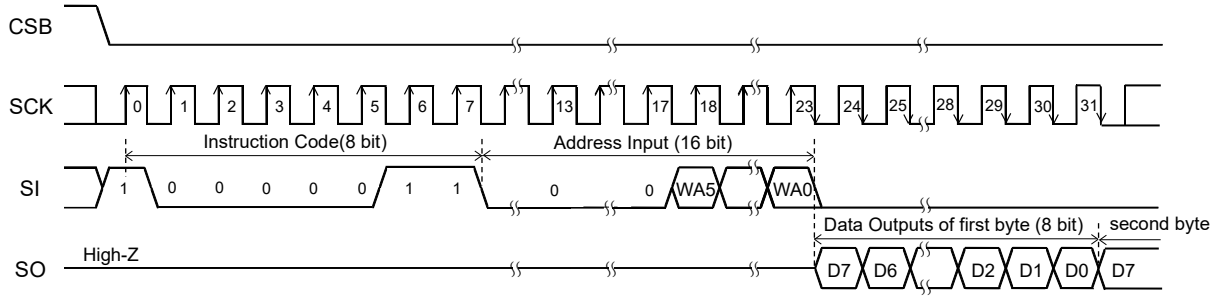


Figure 47. Read ID Page Command

9. Write ID Page Command (WRID)

By Write ID Page command, data of ID Page can be written. As for this command, set CSB to Low, then input address and data after Instruction Code of Write ID Page command. By inputting lower address bits WA5 to WA0, it is possible to address to 64 byte ID Page. Then, by making CSB to High, the IC starts write operation. To start write operation, set CSB Low to High after taking the last data (D0), and before the next SCK clock starts. At other timing, Write ID Page command is not executed, and this Write ID Page command is cancelled. The write time of EEPROM requires time of $t_{E/W}$ (Max 3.5 ms).

During write operation, other than Read Status Register command is not accepted.

In case of Lock Status (LS) bit “1”, Write ID Page command can’t be executed.

Write ID Page command has Page Write Function same as Write command.

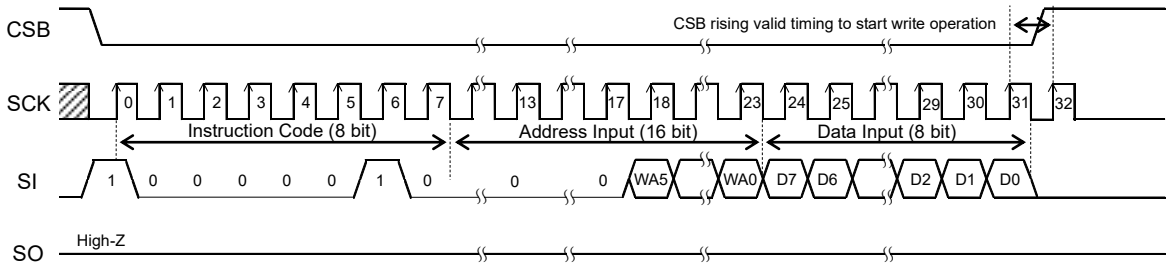


Figure 48. Write ID Page Command

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Timing Chart - continued

10. Read Lock Status Command (RDLS)

By Read Lock Status command, data of Lock Status can be read. As for this command, set CSB to Low, then input address after Instruction Code of Read Lock Status command. Data output is started from SCK fall of 23 clock, and from D7 to D0 sequentially. The data D0 indicates Lock Status bit. The data D7 to D1 are Don't Care. This IC has increment read function. After output of data for 1 byte (8 bits), by continuing input of SCK, this IC repeats to output data of the Lock Status byte. In case of Lock Status (LS) bit "1", ID Page is locked, Write ID Page command can't be executed. In case of LS bit "0", ID Page is released to lock, Write ID Page command can be executed.

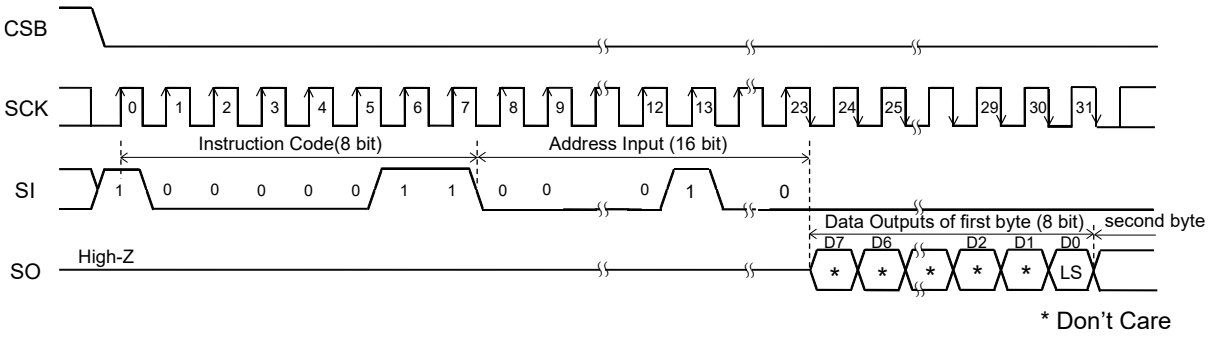


Figure 49. Read Lock Status Command

11. Lock ID Page Command (LID)

By Lock ID Page command, data of Lock Status can be written. In case of Lock Status (LS) bit "1", Lock ID Page command can't be executed permanently. As for this command, set CSB to Low, then input address and data after Instruction Code of Lock ID Page command. To start write operation, set CSB Low to High after taking the last data (D0), and before the next SCK clock starts. At other timing, Lock ID Page command is not executed, and this Lock ID Page command is cancelled. The write time of EEPROM requires time of $t_{E/W}$ (Max 3.5 ms).
During write operation, other than Read Status Register command is not accepted.

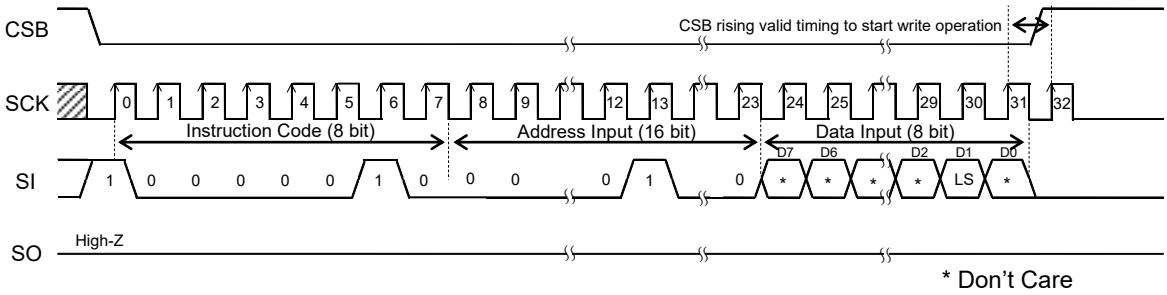


Figure 50. Lock ID Page Command

At Standby State

1. Standby Current

Set CSB = High, and be sure to set SCK, SI, WPB and HOLDB inputs = Low or High. Do not input intermediate voltage.

2. Timing

As shown in Figure.51, at standby, when SCK is High, even if CSB is fallen, SI status is not read at fall edge. SI status is read at SCK rise edge after fall of CSB. At standby and at power ON/OFF, set CSB = High status.

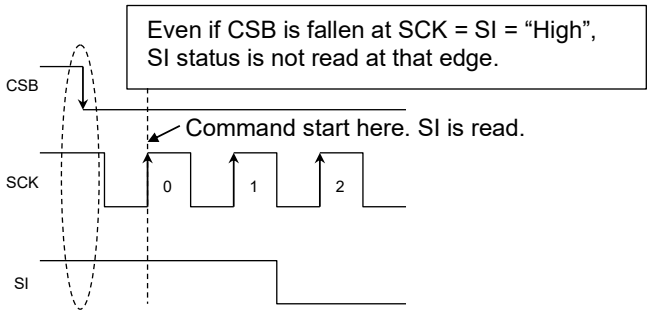


Figure 51. Operating Timing

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Method To Cancel Each Command

1. READ, RDID, RDLS
   Method to cancel: cancel by CSB = High

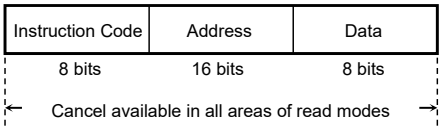


Figure 52. READ, RDID, RDLS Cancel Valid Timing

2. RDSR
   Method to cancel: cancel by CSB = High

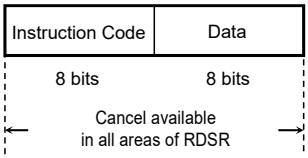


Figure 53. RDSR Cancel Valid Timing

3. WRITE, WRID, LID
   a: Instruction Code, Address Input Area
   Cancellation is available by CSB = High.
   b: Data Input Area (D7 to D1 input area)
   Cancellation is available by CSB = High.
   c: Data Input Area (D0 area)
   When CSB is started, write starts.
   After CSB rise, cancellation cannot be made by any means.
   d: $t_{E/W}$ Area
   Cancellation is available by CSB = High. However, when write starts (CSB is started) in the area c, cancellation cannot be made by any means. And by inputting on SCK clock, cancellation cannot be made. In page write mode, there is write enable area at every 8 clocks.

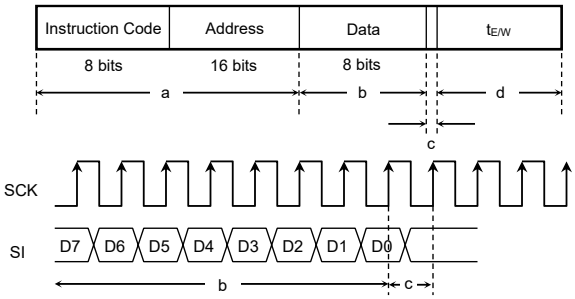


Figure 54. WRITE, WRID, LID Cancel Valid Timing

Note 1) If V_{CC} is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
Note 2) If CSB is started at the same timing as that of the SCK rise, write execution/cancel becomes unstable, therefore, it is recommended to fall in SCK = Low area. As for SCK rise, assure timing of t_{CSS}/t_{CSH} or higher.

4. WRSR
   a: From Instruction code to 15th rising of SCK
   Cancel by CSB = High.
   b: From 15th rising of SCK to 16th rising of SCK (write enable area)
   When CSB is started, write starts.
   c: After 16th rising of SCK
   Cancel by CSB = High.
   However, when write starts (CSB is started) in the area b, cancellation cannot be made by any means. And, by inputting on SCK clock, cancellation cannot be made.

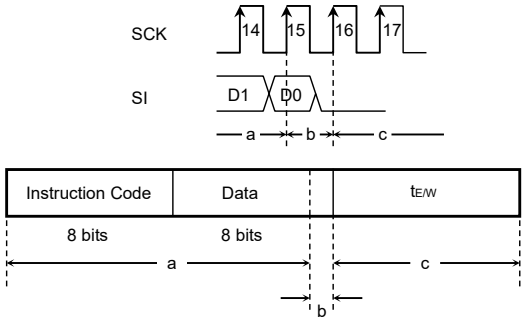


Figure 55. WRSR Cancel Valid Timing

Note 1) If V_{CC} is made OFF during write execution, designated address data is not guaranteed, therefore write it once again.
Note 2) If CSB is started at the same timing as that of the SCK rise, write execution/cancel becomes unstable, therefore, it is recommended to fall in SCK = Low area. As for SCK rise, assure timing of t_{CSS}/t_{CSH} or higher.

5. WREN/WRDI
   a: From instruction code to 7th rising of SCK
   Cancel by CSB = High.
   b: Cancellation is not available when CSB is started after 7th clock.

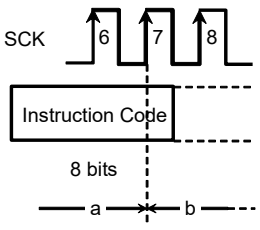


Figure 56. WREN/WRDI Cancel Valid Timing

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Application Examples

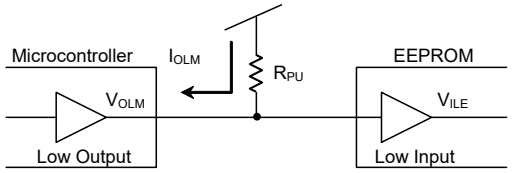
High Speed Operation

In order to realize stable high speed operations, pay attention to the following input/output pin conditions.

1. Pull Up, Pull Down Resistance for Input Pins

When to attach pull up, pull down resistance to EEPROM input pins, select an appropriate value for the microcontroller V_{OL}, I_{OL} from V_{IL} characteristics of this IC.

2. Pull Up Resistance



V_{ILE} : V_{IL} of EEPROM
V_{OLM} : V_{OL} of Microcontroller
I_{OLM} : I_{OL} of Microcontroller

Figure 57. Pull Up Resistance

$$R_{PU} \geq \frac{V_{CC}-V_{OLM}}{I_{OLM}} \quad (1)$$

$$V_{OLM} \leq V_{ILE} \quad (2)$$

Example) When V_{CC} = 5 V, V_{ILE} = 1.5 V, V_{OLM} = 0.4 V, I_{OLM} = 2 mA, from the equation (1).

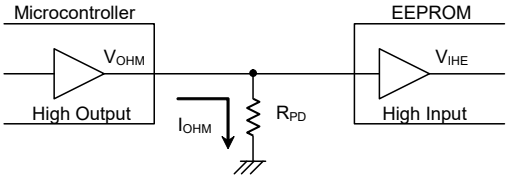
$$R_{PU} \geq \frac{5-0.4}{2\times10^{-3}}$$

$$R_{PU} \geq 2.3 \ [\text{k}\Omega]$$

With the value of R_{PU} to satisfy the above equation, V_{OLM} becomes 0.4 V or lower, and with V_{ILE} (= 1.5 V), the equation (2) is also satisfied.

And, in order to prevent malfunction, mistake write at power ON/OFF, be sure to make the CSB pin pull up.

3. Pull Down Resistance



V_{IHE} : V_{IH} of EEPROM
V_{OHM} : V_{OH} of Microcontroller
I_{OHM} : I_{OH} of Microcontroller

Figure 58. Pull Down Resistance

$$R_{PD} \geq \frac{V_{OHM}}{I_{OHM}} \quad (3)$$

$$V_{OHM} \geq V_{IHE} \quad (4)$$

Example) When V_{CC} = 5 V, V_{OHM} = V_{CC}-0.5 V, I_{OHM} = 0.4 mA, V_{IHE} = V_{CC} x 0.7 V, from the equation (3),

$$R_{PD} \geq \frac{5-0.5}{0.4\times10^{-3}}$$

$$R_{PD} \geq 11.3 \ [\text{k}\Omega]$$

Further, by amplitude V_{IHE}, V_{ILE} of signal input to EEPROM, operation speed changes. By inputting signal of amplitude of V_{CC}/GND level to input, more stable high speed operations can be realized. On the contrary, when amplitude of 0.8V_{CC} /0.2V_{CC} is input, operation speed becomes slow.*(Note 20)*
In order to realize more stable high speed operation, it is recommended to make the values of R_{PU}, R_{PD} as large as possible, and make the amplitude of signal input to EEPROM close to the amplitude of V_{CC} /GND level.

(Note 20) At this moment, operating timing guaranteed value is guaranteed.

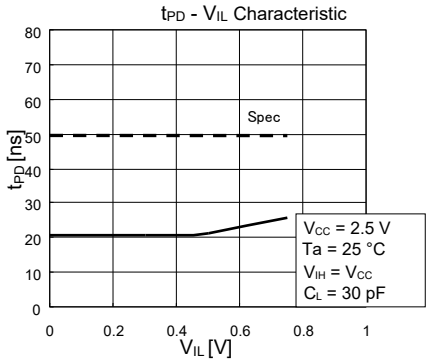


Figure 59. V_{IL} dependency of Data Output Delay Time t_{PD}

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Application Examples - continued

4. SO Load Capacitance Condition

Load capacitance of the SO Pin affects upon delay characteristic of SO output. (Data Output Delay Time, Time from HOLDB to High-Z) In order to make output delay characteristic into higher speed, make SO load capacitance small. In concrete, “Do not connect many devices to SO bus”, “Make the wire between the controller and EEPROM short”, and so forth.

5. Other Cautions

Make the wire length from the Microcontroller to EEPROM input signal same length, in order to prevent setup/hold violation to EEPROM, owing to difference of wire length of each input.

I/O Equivalence Circuits

1. Input (CSB, SCK, SI, HOLDB, WPB)

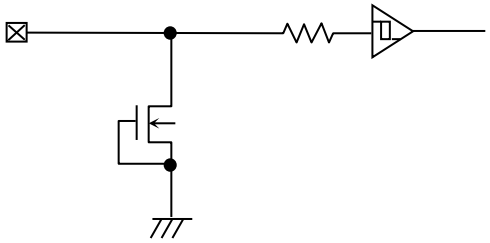


Figure 60. Input Equivalent Circuit (CSB, SCK, SI, HOLDB, WPB)

2. Output (SO)

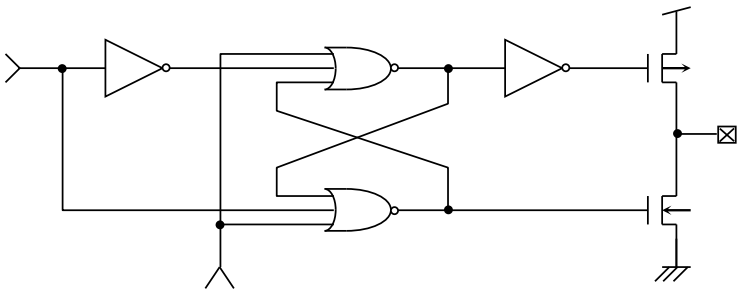


Figure 61. Output Equivalent Circuit (SO)

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Caution on Power-up Conditions

At power-up, as the V_{CC} rises, the IC's internal circuits may go through unstable low voltage area, making the IC's internal circuit not completely reset, hence, malfunction like miswriting and misread may occur. To prevent it, this IC is equipped with Power-on Reset circuit. In order to ensure its operation, at power-up, please observe the conditions below. In addition, set the power supply rise so that the supply voltage constantly increases from V_{BOT} to V_{CC} level. Furthermore, t_{INIT} is the time from the power become stable to the start of the first command input.

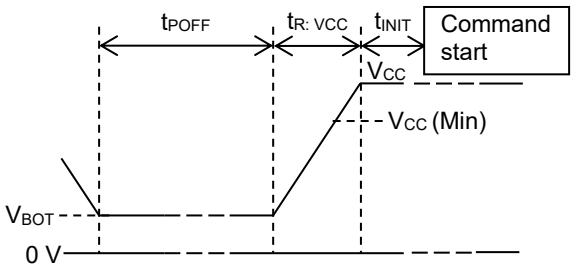


Figure 62. Rise Waveform Diagram

Power-Up Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage at Power OFF	V_{BOT}	-	-	0.3	V
Power OFF Time *(Note 21)*	t_{POFF}	1	-	-	ms
Initialize Time *(Note 21)*	t_{INIT}	0.1	-	-	ms
Supply Voltage Rising Time *(Note 21)*	$t_{R: VCC}$	0.001	-	100	ms

(Note 21) Not 100 % Tested.

At power ON/OFF, set CSB = High (= V_{CC}).
When CSB is Low, this IC gets in input accept status (active). If power is turned on in this status, noises and the likes may cause malfunction, mistake write or so. To prevent these, at power ON, set CSB = High. (When CSB is in High status, all inputs are canceled.)

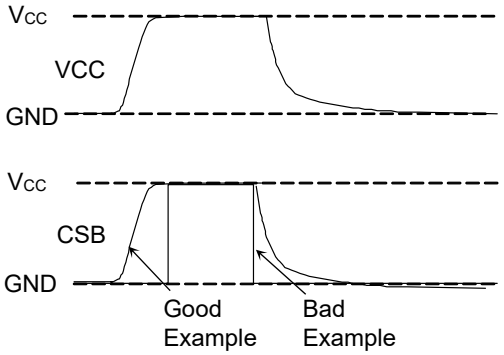


Figure 63. CSB Timing at power ON/OFF

(Good example) the CSB Pin is pulled up to V_{CC}.
At power OFF, take 1 ms or higher before supply. If power is turned on without observing this condition, the IC internal circuit may not be reset, which please note.

(Bad example) the CSB Pin is Low at power ON/OFF.
In this case, CSB always becomes Low (active status), and EEPROM may have malfunction, mistake write owing to noises and the likes.
Even when CSB input is High-Z, the status becomes like this case, which please note.

Low Voltage Malfunction Prevention Function

LVCC circuit prevents data rewrite operation at low power, and prevents write error. At LVCC voltage (Typ = 1.2 V) or below, data rewrite is prevented.

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Noise Countermeasures

1. VCC Noise (bypass capacitor)
   When noise or surge gets in the power source line, malfunction may occur, therefore, for removing these, it is recommended to attach a bypass capacitor (0.1 µF) between IC VCC and GND. At that moment, attach it as close to IC as possible. And, it is also recommended to attach a bypass capacitor between board VCC and GND.

2. SCK Noise
   When the rise time (t_{RC}) of SCK is long, and a certain degree or more of noise exists, malfunction may occur owing to clock bit displacement. To avoid this, a Schmitt trigger circuit is built in SCK input. The hysteresis width of this circuit is set about 0.2 V, if noises exist at SCK input, set the noise amplitude 0.2 Vp-p or below. And it is recommended to set the rise time (t_{RC}) of SCK 100 ns or below. In the case when the rise time is 100 ns or higher, take sufficient noise countermeasures. Make the clock rise, fall time as small as possible.

3. WPB Noise
   During execution of Write Status Register command, if there exist noises on the WPB pin, mistake in recognition may occur and forcible cancellation may result, which please note. To avoid this, a Schmitt trigger circuit is built in WPB input. In the same manner, a Schmitt trigger circuit is built in CSB input, SI input and HOLDB input too.

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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

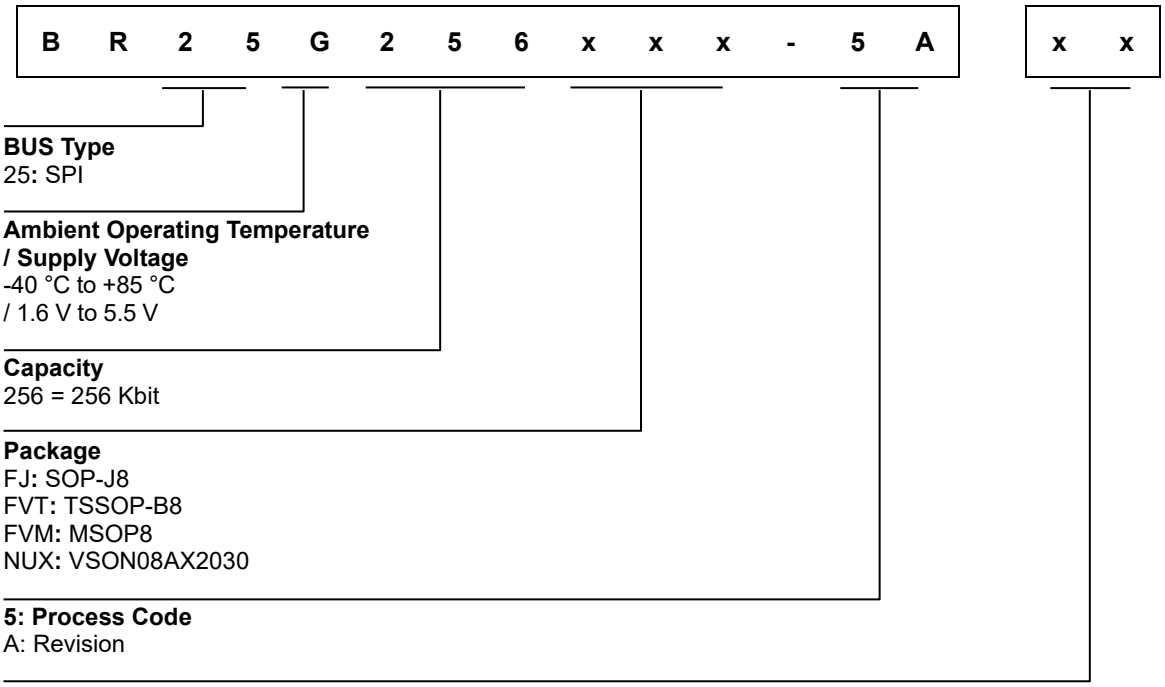
10. **Regarding the Input Pin of the IC**
    In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

11. **Ceramic Capacitor**
    When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

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Ordering Information



Lineup

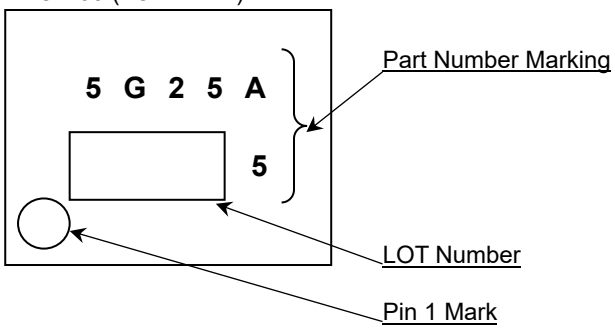
Package		Orderable Part Number	
Type	Quantity		
SOP-J8	Reel of 2500	BR25G256FJ	-5AE2
TSSOP-B8	Reel of 3000	BR25G256FVT	-5AE2
MSOP8	Reel of 3000	BR25G256FVM	-5ATR
VSON08AX2030	Reel of 4000	BR25G256NUX	-5ATR

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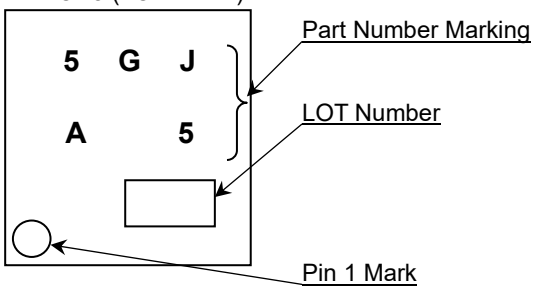
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Marking Diagrams

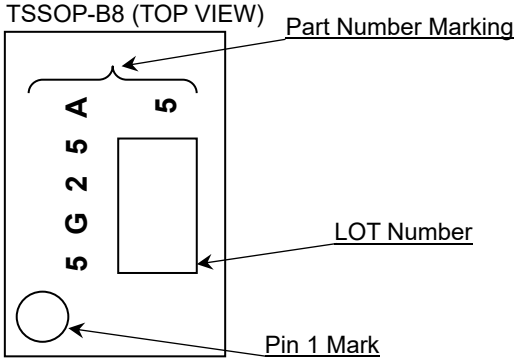
SOP-J8 (TOP VIEW)



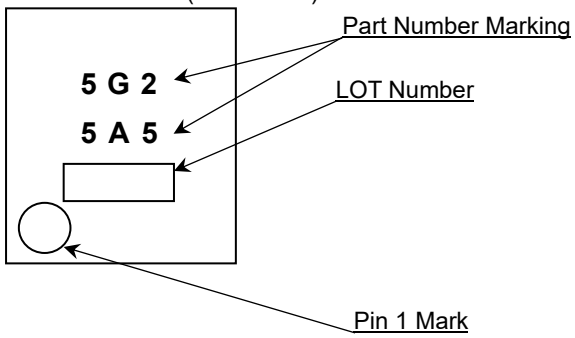
MSOP8 (TOP VIEW)



TSSOP-B8 (TOP VIEW)



VSON08AX2030 (TOP VIEW)

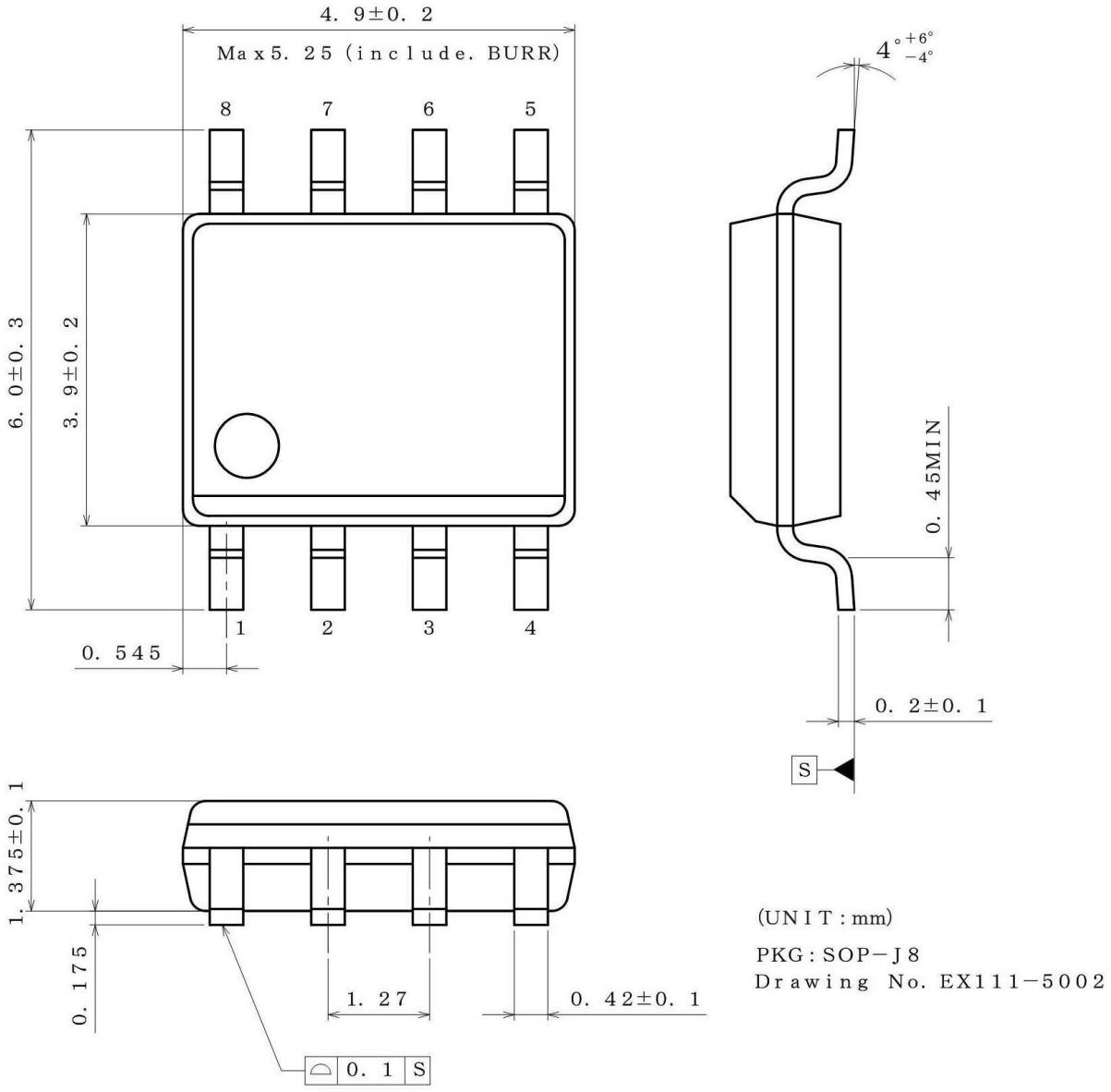


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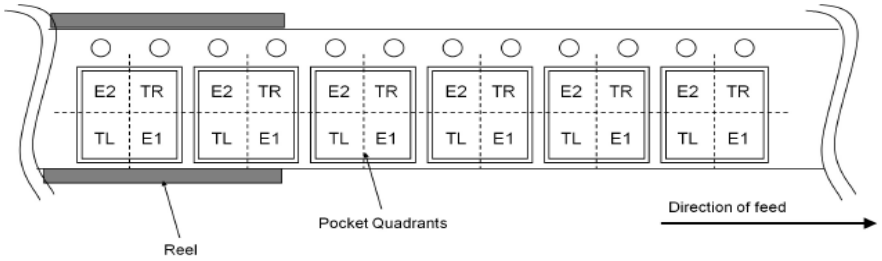
Physical Dimension and Packing Information

Package Name	SOP-J8



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand

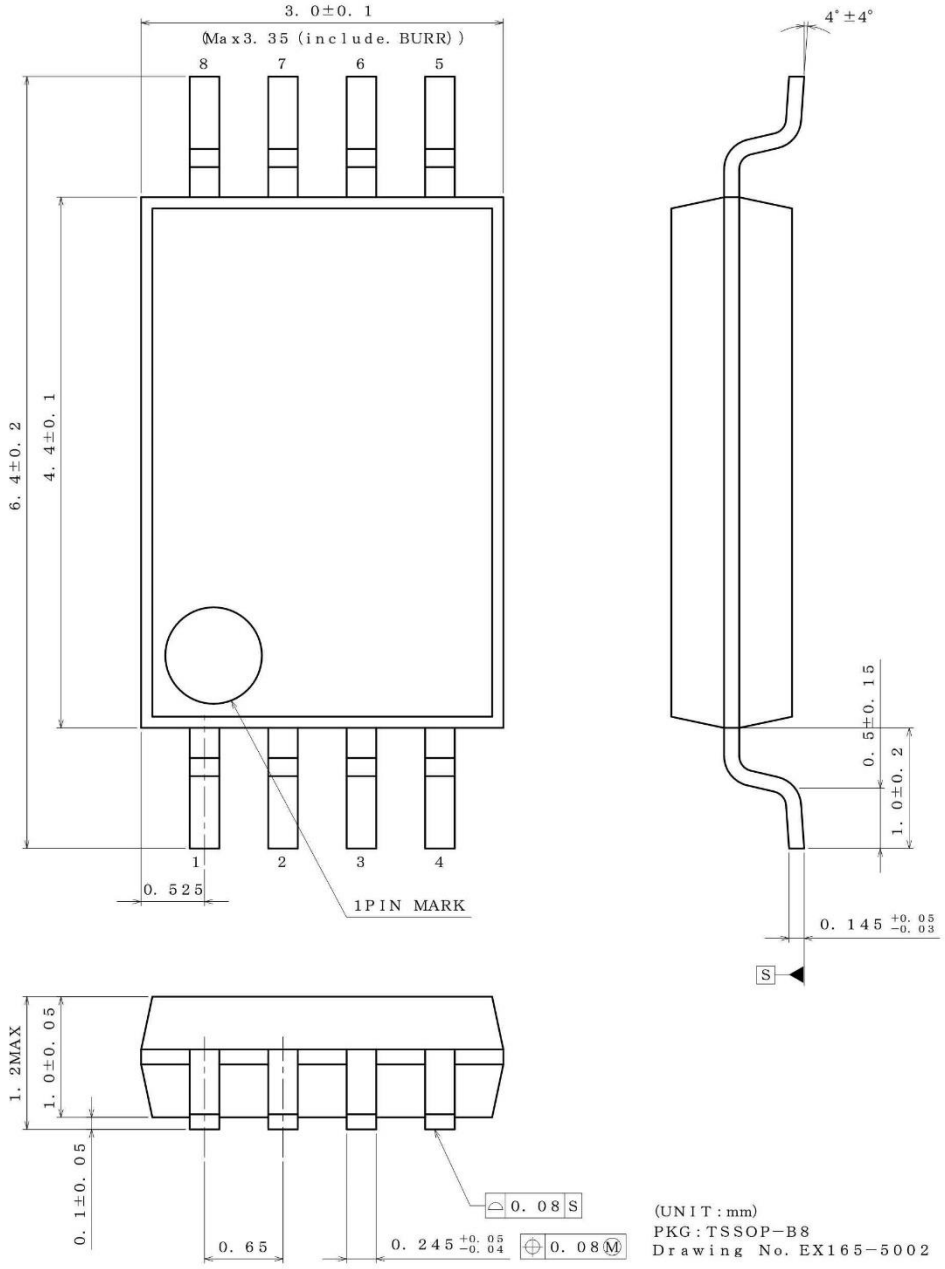


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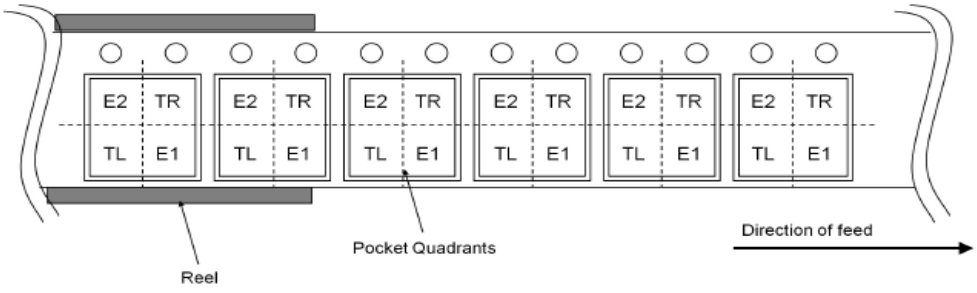
Physical Dimension and Packing Information - continued

Package Name	TSSOP-B8



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand

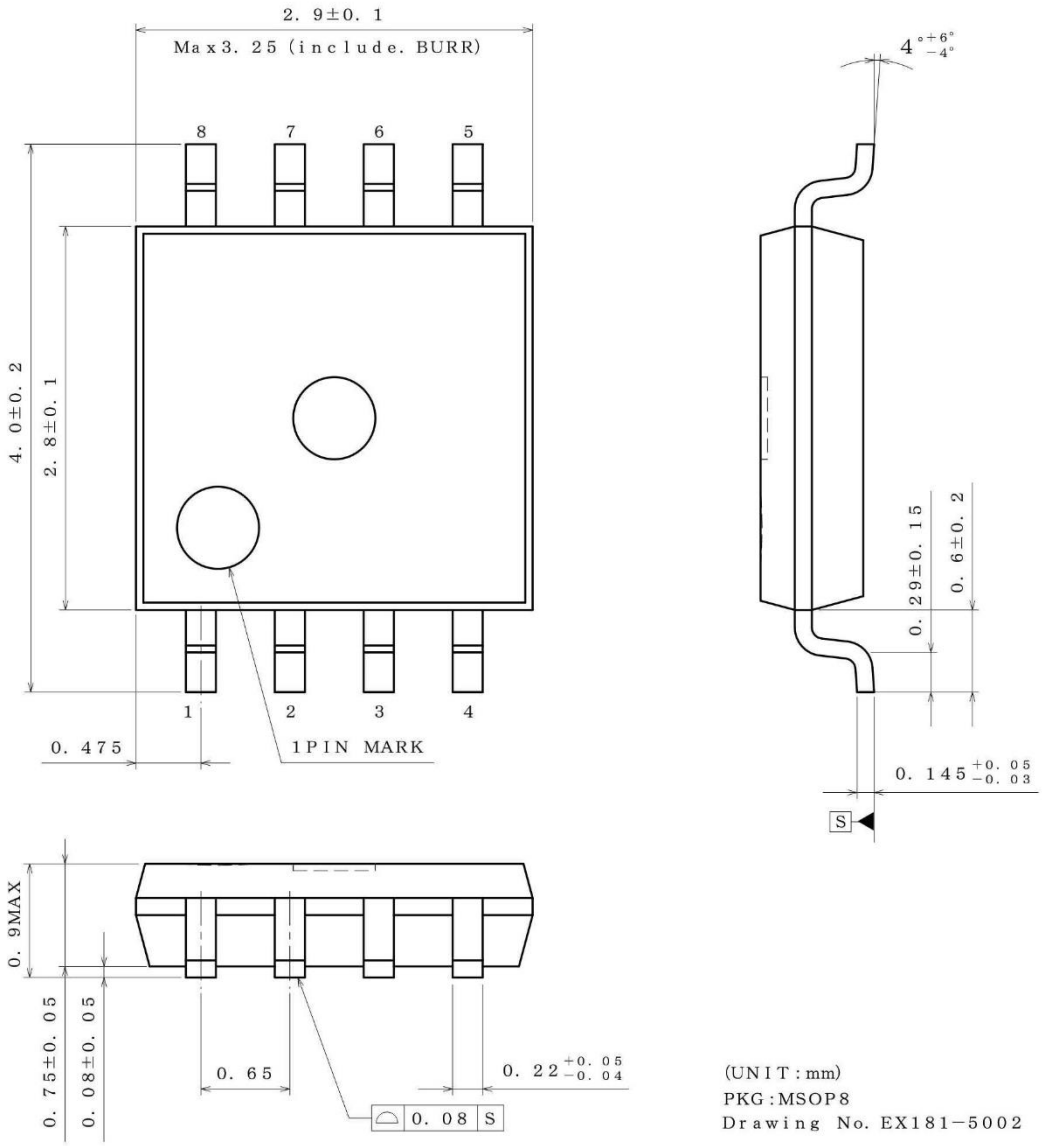


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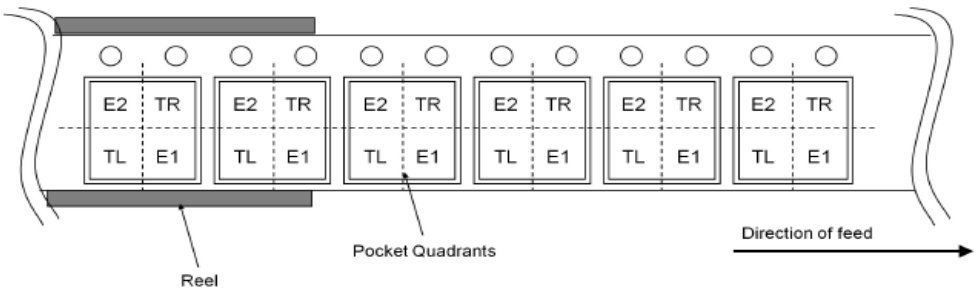
Physical Dimension and Packing Information - continued

Package Name	MSOP8



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)

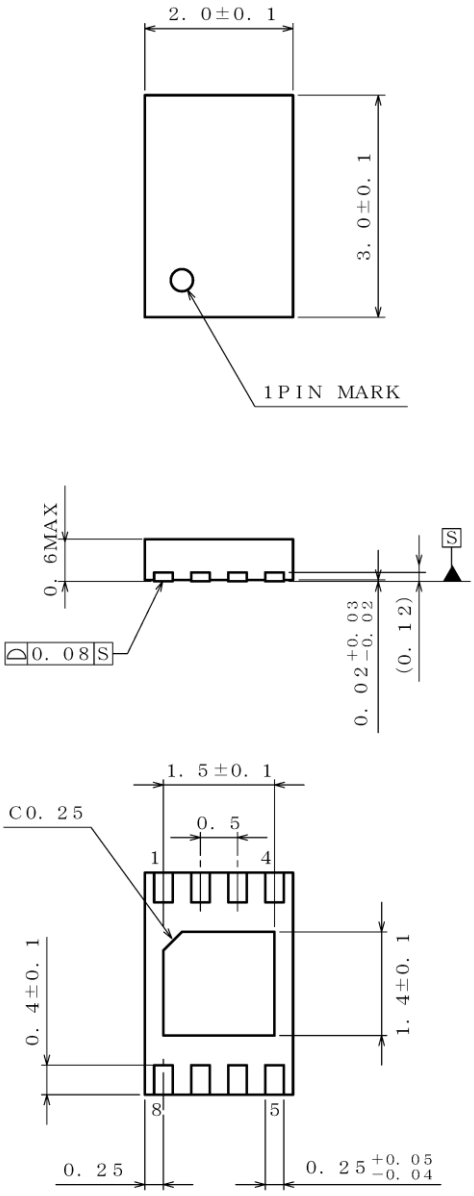


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Physical Dimension and Packing Information - continued

Package Name	VSON08AX2030

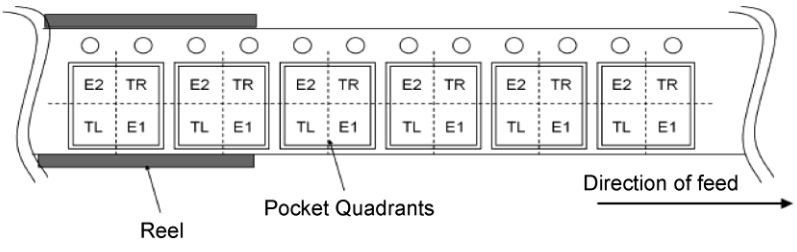


(UNIT : mm)

PKG : VSON08AX2030
Drawing No. : EX087−5001

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	TR The direction is the pin 1 of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand



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Revision History

Date	Revision	Changes
02.Jun.2022	001	New Release
10.Sep.2025	002	Change VSON008X2030 to VSON08AX2030.

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Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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2. ROHM shall not have any obligations where the claims, actions or demands arising from the combination of the Products with other articles such as components, circuits, systems or external equipment (including software).

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