# SiT5721

1 to 60 MHz Emerald™ Platform Stratum 3E DCOCXO

## Description

The SiT5721 is the industry's first digitally controlled OCXO (DCOCXO), enabling output frequency tuning via I²C interface with ±5 ppt (±0.005 ppb) resolution. The device delivers ±5 ppb over-temp stability, ±0.04 ppb/°C frequency slope (dF/dT) and Stratum 3E compliance in the smallest 9 mm x 7 mm package.

Leveraging SiTime's unique DualMEMS® and TurboCompensation® temperature sensing technology, the SiT5721 is engineered for the best dynamic performance, delivering the most stable timing in the presence of environmental stressors – airflow, temperature perturbation, vibration, shock, and electromagnetic interference (EMI).

The SiT5721's environmental robustness enables unmatched ease-of-use and reduces system manufacturing overhead:

- Highly flexible location on the PCB
- Minimal shielding for thermal isolation

SiT5721 can be factory-programmed to any nominal output frequency between 1 MHz and 60 MHz. It is supported by the SiT6731 evaluation board.

## Features

- Any frequency between 1 MHz and 60 MHz, in 1 Hz steps
- ±0.04 ppb/°C frequency slope typical (dF/dT)
- ±5 ppb frequency stability over temperature
- Up to 85°C operating temperature range
- 1.4E-11 ADEV at 10 second averaging time
- Digital frequency pulling via I²C
  - Up to ±10 ppm pull range
  - ±5 ppt pulling resolution
- Exceptional dynamic stability under airflow and rapid temperature changes
- Excellent holdover over a wide range of conditions
- Integrated regulators for on-chip power-supply noise filtering and excellent PSRR
- GR-1244 Stratum 3E compliant
- Resistant to shock and vibration
- 3.3 V supply voltage
- LVCMOS or clipped sinewave output

## Applications

- 4G/5G radio
- Base Stations
- Digital Switching
- Time and Frequency Measurement
- IEEE 1588
- Test and measurement

### 9 mm x 7 mm Package

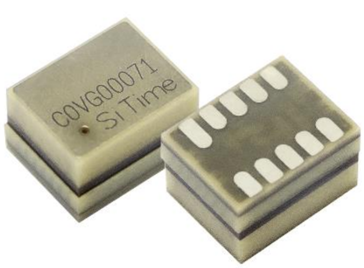


**Figure 1. Top and bottom view**

### Package Pinout

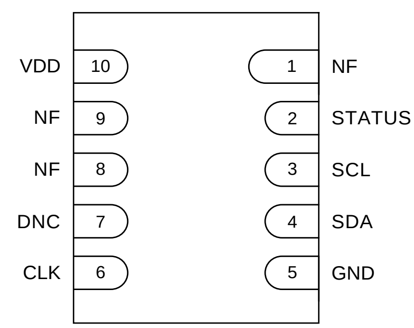


**Figure 2. Pin Assignments (Bottom view)**

## Ordering Information

**SiT5721 A C - K W 3 33 - T - 19.123456 T**

**Part Family**
"SiT5721"

**Revision Letter**
"A" is the revision

**Temperature Range[1]**
"I": Industrial, -40°C to 85°C
"C": Extended Commercial, -20°C to 70°C

**Output Waveform[2]**
"-": LVCMOS
"C": Clipped Sinewave

**Package Size**
"K": 9 mm x 7 mm

**Frequency Stability**
"W": for ±5 ppb
"X": for ±8 ppb

**I²C Address Mode**
Values: 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F

Set bits 3:0 of device I²C address to the Hex value of the ordering code.

**Packaging[3,4]**
"F": 24 mm Tape & Reel, <250 units
"X": 24 mm Tape & Reel, 250 units
"N": 24 mm Tape & Reel, 500 units
(blank): bulk

**Frequency**
1.000000 to 60.000000 MHz

**Pull Range**
"T": ±6.25 ppm
"R": ±10 ppm

**Supply Voltage**
"33": 3.3 V ±5%

**Notes:**
1. Contact SiTime for other temperature range options.
2. "-" corresponds to the default rise/fall time for LVCMOS output as specified in Table 2 (Output Characteristics). Contact SiTime for other rise/fall time options for best EMI.
3. Bulk is available for sampling only.

### Table 1. Ordering Codes for Supported Tape & Reel Packaging Method[4]

| Device Size | 24 mm T&R (<250 units) | 24 mm T&R (250 units) | 24 mm T&R (500 units) |
|---|---|---|---|
| 9 mm x 7 mm | F | X | N |

**Note:**
4. 10 unit minimum order quantity for tape and reel packaging.

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## Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage. Typical values are at 25°C and 3.3 V VDD. All measurements are specified with 15 pF load unless otherwise stated.

### Table 2. Output Characteristics

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Frequency Coverage** | | | | | | |
| **Nominal Output Frequency Range** | F_nom | 1 | – | 60 | MHz | |
| **Frequency Stability** | | | | | | |
| **Frequency Stability over Temperature** | F_stab | -5 | – | +5 | ppb | Referenced to (fmax + fmin)/2 over the specified temperature range. Contact SiTime for 3 ppb or tighter frequency stability. Measured after 48 hours of operation. |
| | | -8 | – | +8 | ppb | |
| **Frequency vs. Temperature Slope** | dF/dT | -0.12 | ±0.04 | +0.12 | ppb/°C | Steady airflow <3 m/s, 1°C/min ramp rate |
| **Dynamic Frequency Change to Temperature Ramp** | F_dynamic | -0.002 | ±0.0007 | +0.002 | ppb/s | Steady airflow <3 m/s, 1°C/min ramp rate |
| **Initial Tolerance** | F_init | -300 | – | +300 | ppb | Offset from nominal frequency (F_nom) after 2 reflows, measured at 25°C. |
| **Hysteresis Over Temperature** | F_Hys | -0.8 | ±0.11 | +0.8 | ppb | Over -40 to 85°C, measured as maximum frequency deviation from center of hysteresis eye, 1°C/min ramp rate |
| **One-day Aging** | F_1d | – | ±0.7 | ±1.6 | ppb | After 60-days operation, 50°C |
| **One-month Aging** | F_1m | – | ±32 | ±57 | ppb | After 30-days operation, 50°C |
| **One-year Aging** | F_1y | – | ±110 | ±230 | ppb | After 30-days operation, 50°C |
| **Ten-year Aging** | F_10y | – | ±220 | ±394 | ppb | After 30-days operation, 50°C |
| **Total Stability – 20 years** | F_20y_stab | -1 | – | +1 | ppm | Better than Stratum 3E stability of ±4.6 ppm over 20 years per GR-1244-CORE. Inclusive of initial tolerance, frequency stability over temperature, 20-year Aging, and variations to supply voltage and output load. Typically called free running accuracy |
| **Supply Voltage Sensitivity** | F_Vdd | – | ±0.3 | – | ppb | $V_{DD}$ ±5% |
| **Output Load Sensitivity** | F_load | – | ±0.2 | – | ppb | LVCMOS output, 15 pF ±10% |
| | | – | ±0.1 | – | ppb | Clipped sinewave output, 10 kΩ \|\| 10 pF ±10% |
| **Start-up Characteristics** | | | | | | |
| **Start-up Time** | T_start | – | 2.5 | 3.5 | ms | Time to first pulse |
| **OE Time** | T_oe | – | | 680 | ns | Time to first pulse after OE pin reaches 70% of $V_{DD,}$ 10 MHz |
| **Warm-up Time** | T_warmup | – | 20 | 150 | s | Time to within ±10 ppb of final frequency. Final frequency measured at one hour. Device powered on for 48 hours then powered off for 1 hour prior to measurement. |
| | | – | – | 45 | ms | Time to within ±200 ppb of final frequency. Final frequency measured at one hour. Device powered on for 48 hours then powered off for 1 hour prior to measurement. |
| **LVCMOS Output Characteristics** | | | | | | |
| **Duty Cycle** | DC | 45 | – | 55 | % | |
| **Rise/Fall Time** | Tr, Tf | – | 2.2 | 3 | ns | 10% - 90% VDD |
| **Output Voltage High – CLK Pin** | $V_{OH}$ | 90% | – | – | $V_{DD}$ | $I_{OH}$ = ±3 mA, ($V_{DD}$ = 3.3 V) |
| **Output Voltage Low – CLK Pin** | $V_{OL}$ | – | – | 10% | $V_{DD}$ | $I_{OL}$ = ±3 mA, ($V_{DD}$ = 3.3 V) |
| **Status Pin Output Characteristics** | | | | | | |
| **Output Voltage High** | $V_{OH\_P2}$ | $V_{DD}$ -0.4 | – | – | V | $I_{OH}$ = ±8 mA |
| **Output Voltage Low** | $V_{OL\_P2}$ | – | – | 0.4 | V | $I_{OL}$ = ±8 mA |
| **Clipped Sinewave Output Characteristics** | | | | | | |
| **Output Voltage Level** | $V_{\_OUT}$ | 0.8 | – | 1.2 | V | Measured peak-to-peak swing at any $V_{DD}$ – 10 kΩ \|\| 10 pF ±10% |
| **Rise/Fall Time** | Tr, Tf | – | 3.9 | 4.6 | ns | 20%–80% $V_{OUT}$ |

### Table 3. DC Characteristics

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Supply Voltage** | | | | | | |
| **Supply Voltage** | $V_{DD}$ | 3.14 | 3.3 | 3.47 | V | Contact SiTime for other voltage options |
| **Power Consumption** | | | | | | |
| **Power Consumption – Warm-up** | Pwr_warmup | – | – | 2.3 | W | |
| **Power Consumption – Steady State** | Pwr_steady | – | 0.95 | 1.1 | W | At +25°C |
| **Temperature Range** | | | | | | |
| **Operating Temperature Range** | T_use | -20 | – | +70 | °C | Extended commercial |
| | | -40 | – | +85 | °C | Industrial. Contact SiTime for -55°C and 95°C support |

### Table 4. Input Characteristics

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Frequency Tuning Range – I²C mode** | | | | | | |
| **Pull Range** | PR | ±6.25 | – | – | ppm | Contact SiTime for pull ranges up to ±3200 ppm |
| | | ±10 | – | – | ppm | |
| **Absolute Pull Range**[5] | APR | ±5.25 | – | – | ppm | Over operating temperature range (T_rated). Digitally controlled mode for PR = ±6.25 ppm |
| | | ±9 | – | – | ppm | Over operating temperature range (T_rated). Digitally controlled mode for PR = ±10 ppm |
| **I²C Interface Characteristics** [6] | | | | | | |
| **Bus Frequency** | F_I2C | – | 100 | – | kHz | |
| | | – | 400 | – | kHz | Contact SiTime for higher bus frequencies |
| **Input Voltage Low** | VIL_I2C | – | – | 30% | $V_{DD}$ | |
| **Input Voltage High** | VIH_I2C | 70% | – | – | $V_{DD}$ | |
| **Output Voltage Low** | VOL_I2C | – | – | 0.4 | V | ±20 mA |
| **Output Fall Time** | Tf_I2C | | | 5 | ns | 70%–30% $V_{OUT}$, C = 50 pF |
| **Input Leakage Current** | $I_L$ | | | 650 | nA | SDA pin, logic High |
| **Pull-Up Equivalent Resistor** | RPU | 25 | 40 | 55 | kΩ | Internal pull up to $V_{DD}$ |
| **Input Capacitance** | $C_{IN}$ | – | 6 | – | pF | |

**Notes:**

5. APR = PR – Total Stability.
6. I²C master must support clock stretching.

### Table 5. Jitter & Phase Noise

| Parameters | Symbol | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| **Jitter** | | | | | | |
| **RMS Period Jitter** | T_jitt_per | – | 1 | 1.3 | ps | F_nom = 10 MHz, population 10k |
| **RMS Phase Jitter (random)** | T_phj | – | 0.4 | 0.55 | ps | F_nom = 10.3 MHz, Integration bandwidth = 12 kHz to 5 MHz |
| **Allan Deviation** | | | | | | |
| $\tau = 1\ second$ | AD_1s | – | 1.6E-11 | – | | Measured after 48 hours operation. |
| $\tau = 10\ seconds$ | AD_10s | – | 1.4E-11 | – | | |
| $\tau = 100\ seconds$ | AD_100s | – | 1.6E-11 | – | | |
| $\tau = 1,000\ seconds$ | AD_1000s | – | 2.5E-11 | – | | |
| $\tau = 10,000\ seconds$ | AD_10000s | – | 1.4E-10 | – | | |
| **Phase Noise** | | | | | | |
| **1 Hz offset** | | – | -81 | -78 | dBc/Hz | Reference F_nom = 10.3 MHz |
| **10 Hz offset** | | – | -109 | -106 | dBc/Hz | |
| **100 Hz offset** | | – | -128 | -125 | dBc/Hz | |
| **1 kHz offset** | | – | -147 | -145 | dBc/Hz | |
| **10 kHz offset** | | – | -152 | -149 | dBc/Hz | |
| **100 kHz offset** | | – | -152 | -149 | dBc/Hz | |
| **1 MHz offset** | | – | -164 | -161 | dBc/Hz | |
| **5 MHz offset** | | – | -165 | -160 | dBc/Hz | |

### Table 6. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| **Storage Temperature** | -55 | 105 | °C |
| **$V_{DD}$** | -0.5 | 4 | V |
| **Soldering Temperature (follow standard Pb-free soldering guidelines)** | – | 260 | °C |

### Table 7. Thermal Considerations

| Package | θJA[7] (°C/W) |
|---|---|
| **Stacked-PCB 9.0 mm x 7.0 mm** | 110 |

General guidelines for the thermal design of the PCB are the following:

1) The power and ground planes should be continuous in the 9 x 7 mm area directly under the device.
2) Thermal vias should not be added to 9 x 7 mm area directly under the device.
3) The thermal properties of the PCB should be designed such that the steady state device power is limited to 1.6 W at -40°C.

For more details on recommendations for thermal design Contact SiTime.

### Table 8. Environmental Compliance[8]

| Parameter | Condition/Test Method |
|---|---|
| **Mechanical Shock** | MIL-STD-883F, Method2002 |
| **Mechanical Vibration** | MIL-STD-883F, Method2007, Condition A<br>JEDEC JESD22-B103, Condition 1 |
| **Temperature Cycle** | JESD22, MethodA104 |
| **Solderability** | MIL-STD-883F, Method2003 |
| **Moisture Sensitivity Level** | MSL3 |
| **Washability** | Non-washable |

**Note:**

7. The presented θJA is for a device on a JESD51-7 2s2p compliant board in still air. θJA is a function of board design and ambient environments.
8. This device is RoHS and REACH compliant Pb-free and is Halogen-free and Antimony-free.

## Pin-out (Bottom View)

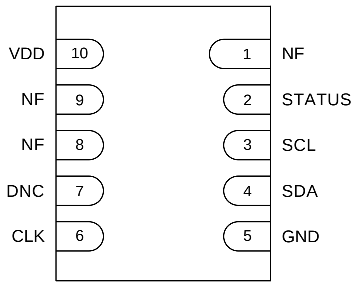



**Figure 3. Size 9 mm x 7 mm**

### Table 9. Pin Assignments

| Package Size | Pin 1 | Pin 2 | Pin 3 | Pin 4 | Pin 5 | Pin 6 | Pin 7 | Pin 8 | Pin 9 | Pin 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| 9 mm x 7 mm | NF | STATUS | SCL | SDA | GND | CLK | DNC | NF | NF | VDD |

### Table 10. Pin Description

| Symbol | I/O | Internal Pull-up/Pull Down Resistor | Function |
|---|---|---|---|
| NF | No Function | - | Solder to pads. Connect to VDD [9] |
| STATUS | Output | - | H: Device in normal operation.<br>L: After startup, indicates oven has not reached steady state. After steady state is achieved, indicates device internal error. |
| SCL | Input | - | $I^2C$ Serial Clock Input [10] |
| SDA | Input/Output | - | $I^2C$ Serial Data [10] |
| GND | Ground | - | Connect to ground [11] |
| DNC | Do Not Connect | - | Solder to pads. Do not connect [12] |
| CLK | Output | - | LVCMOS, or clipped sinewave oscillator output |
| VDD | Power | - | Connect to VDD |

**Notes:**

9. SiTime recommends electrical connection to VDD. Use narrow traces (e.g. 4 to 6 mil) to avoid significant heat dissipation through these pads.
10. I2C address is a factory programmable option.
11. 0.1 µF capacitor in parallel with a 10 µF capacitor are required between VDD and GND.
12. Connecting DNC pin to VDD or ground may cause the device to malfunction.

## Test Circuit Diagrams

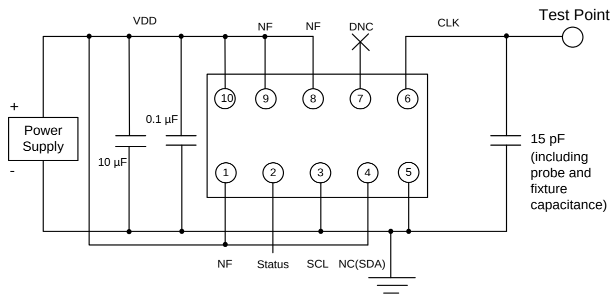



**Figure 4. LVCMOS Test Circuit (No I²C Control)**

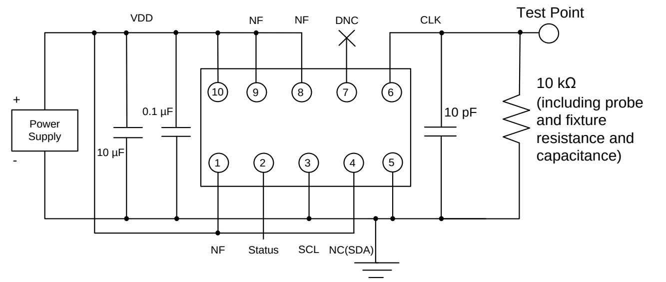



**Figure 5. Clipped Sinewave Test Circuit (No I²C Control)**

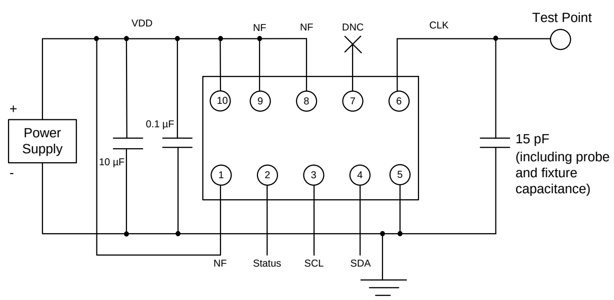



**Figure 6. LVCMOS Test Circuit (I²C Control)**

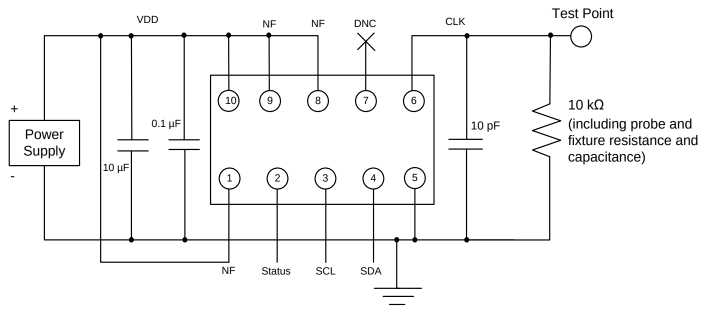



**Figure 7. Clipped Sinewave Test Circuit (I²C Control)**

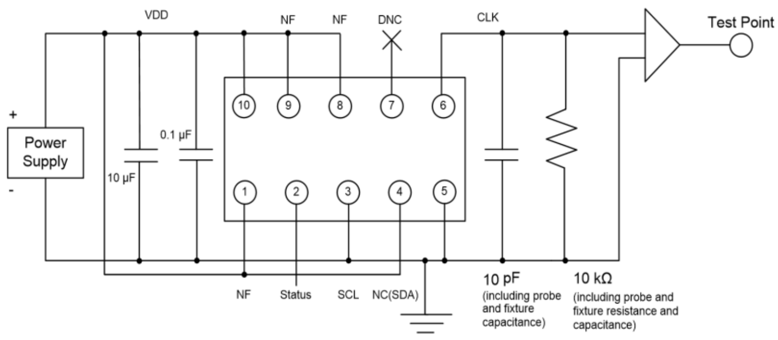



**Figure 8. Phase Noise Clipped Sine Test Circuit (No I²C Control)**

## Waveforms

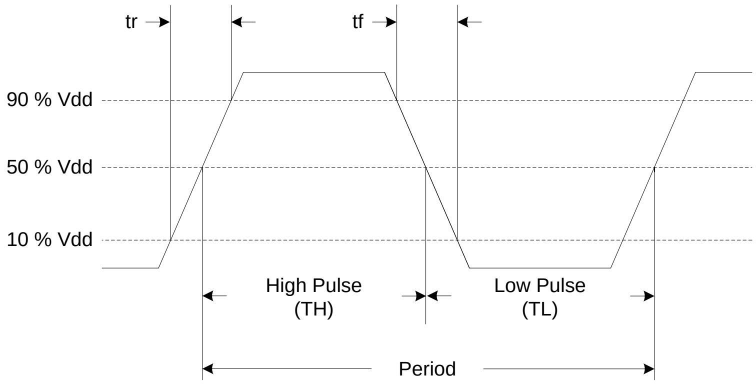



**Figure 9. LVCMOS Waveform Diagram[13]**

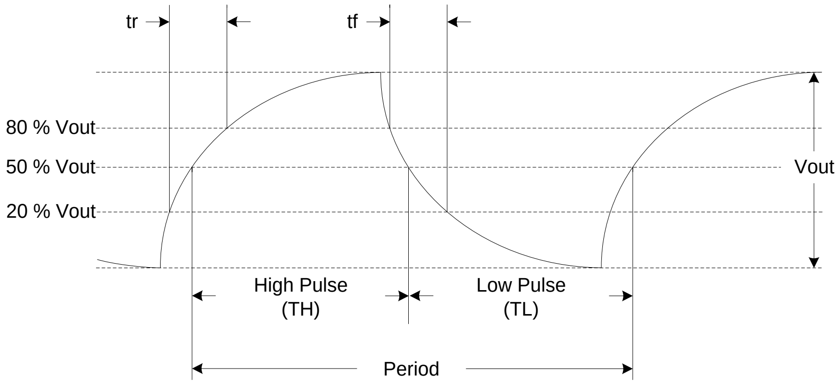



**Figure 10. Clipped Sinewave Waveform Diagram[13]**

**Note:**

13. Duty Cycle is computed as Duty Cycle = TH/Period.

## Timing Diagrams

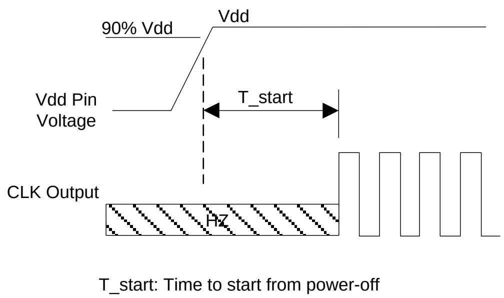



**Figure 11. Startup Timing**

## Typical Performance Plots

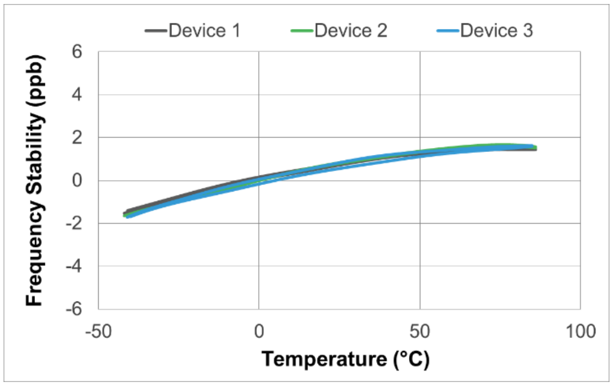



**Figure 12. Frequency Stability**

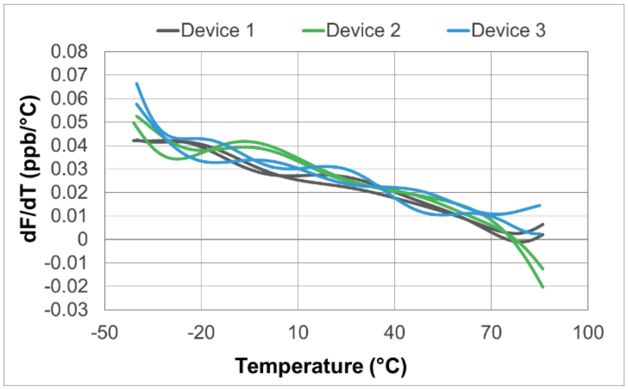



**Figure 13. Frequency Slope**

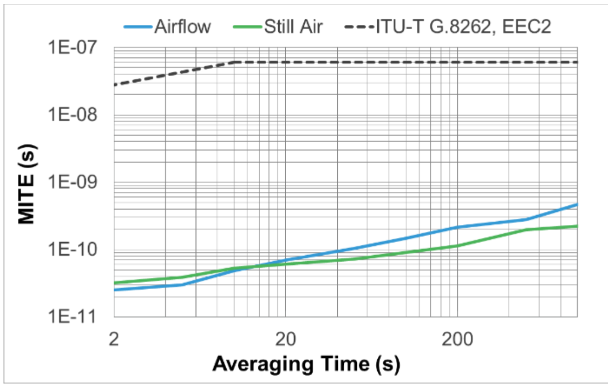



**Figure 14. MTIE**

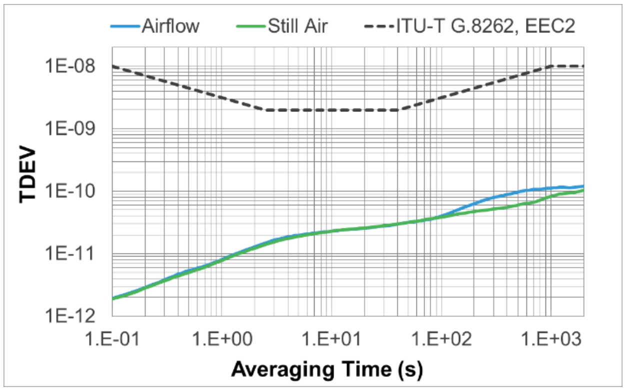



**Figure 15. TDEV**

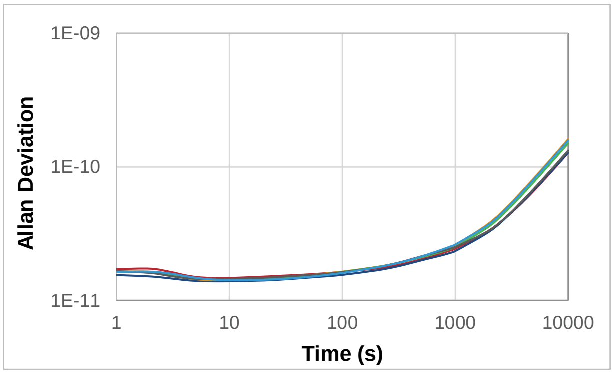



**Figure 16. ADEV Still Air**

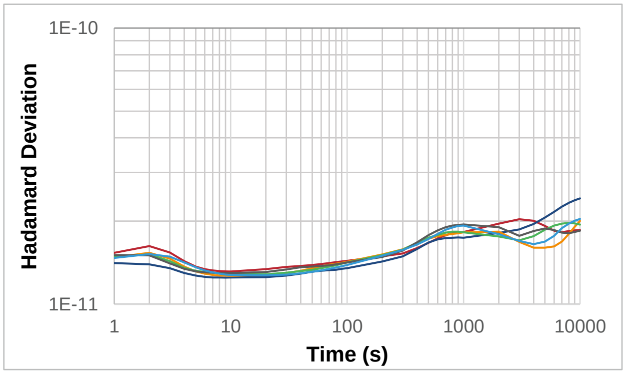



**Figure 17. HDEV Still Air**

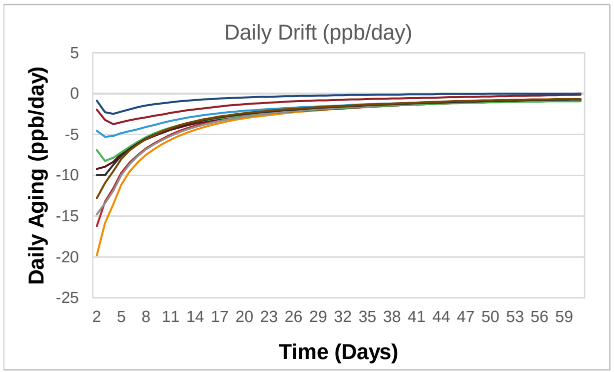
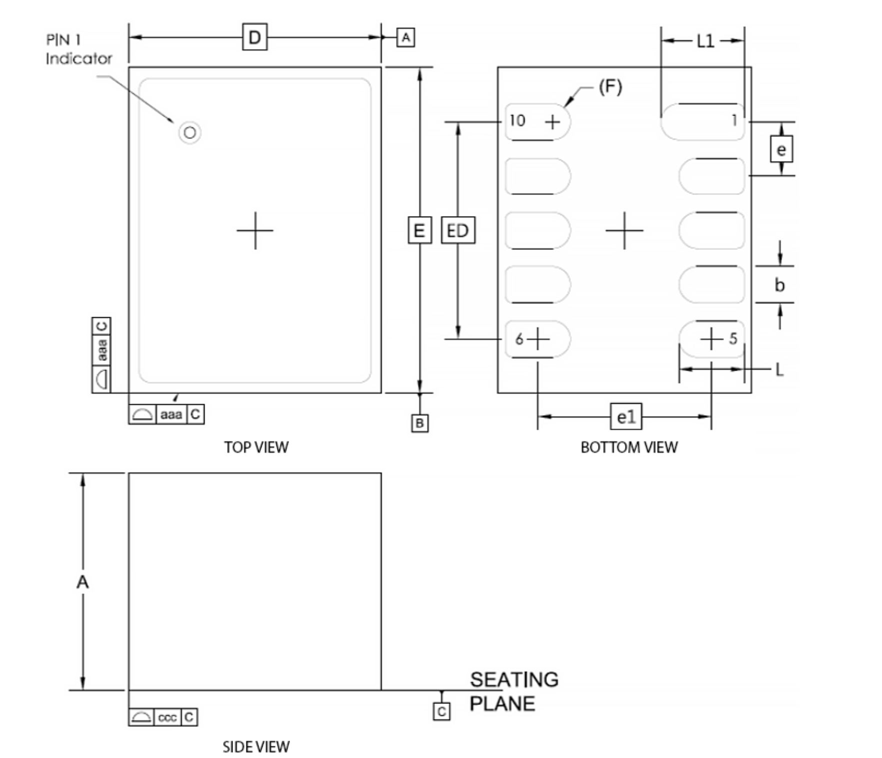



**Figure 18. Daily Aging (50°C)**

## Dimensions and Patterns — 9 mm x 7 mm package

**Package Size – Dimensions (Unit: mm)**

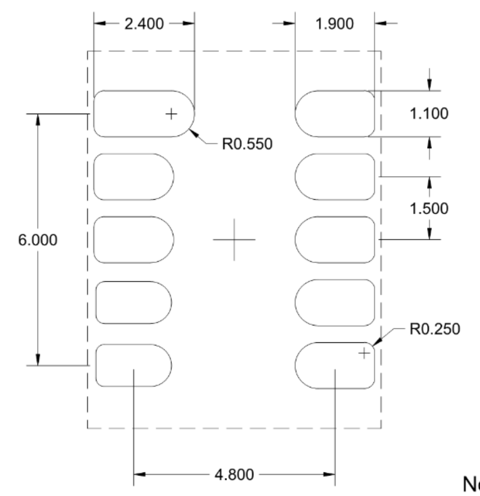



| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| PACKAGE THICKNESS | | A | 5.010 | 5.600 | 6.190 |
| BODY SIZE | X | D | | 7.000 BSC | |
| | Y | E | | 9.000 BSC | |
| LEAD WIDTH | | b | 0.950 | 1.000 | 1.050 |
| LEAD LENGTH | | L | 1.750 | 1.800 | 1.850 |
| | | L1 | 2.250 | 2.300 | 2.350 |
| LEAD PITCH | | e | | 1.500 BSC | |
| | | e1 | | 4.800 BSC | |
| RADIUS | | F | | 0.500 REF | |
| EDGE LEAD TO LEAD | | ED | | 6.000 BSC | |
| PACKAGE TOLERANCE | | aaa | | 0.15 | |
| COPLANRITY | | ccc | | 0.08 | |

Notes
1. All dimensions are in millimeters

| Package Outline | |
|---|---|
| 10L PCBA | POD-051-PCBA-010-X09070 |
| 9.00x7.00x5.6 mm | SiTime |
| REV E00 Jul-28-2020 | |

**Recommended Land Pattern (Top View)**




Note : All units in mm.

| SiTime | PKG INFO | SPL DRAWING NO. | |
|---|---|---|---|
| | | SPL-051-PCBA-010-X09070 | |
| DATE | 10L PCBA<br>9.000x7.000 mm | REV | SHEET |
| 2022/05/20 | | G00 | 00 |

## Layout Guidelines

- SiT5721 uses internal regulators to minimize the impact of the power supply noise. For further reduction of noise, it is essential to use two bypass capacitors (0.1 µF and 10 µF). Place the bypass capacitors as close to the VDD pin as possible, typically within 1 to 2 mm. Ensure 0.1 uF cap is placed closest to the device VDD and power pins.
- SiT5721 is engineered to have superior performance when compared to quartz OCXOs in the presence of ambient disturbers such as airflow and temperature transients. Therefore, the use of a metal cover typical for quartz OCXOs can often be avoided.
- For additional layout recommendations, refer to the Best Design Layout Practices.

## Manufacturing Guidelines

- No Ultrasonic or Megasonic Cleaning: Do not subject the SiT5721 to an ultrasonic or megasonic cleaning environment. Permanent damage or long-term reliability issues to the device may occur in such an event.
- After the surface mount (SMT)/reflow process, solder flux residues may be present on the PCB and around the pads of the device. Excess residual solder flux may lead to problems such as pad corrosion, elevated leakage currents, increased frequency aging, or other performance degradation. For optimal device performance and long-term reliability, it is recommended to use “no clean” flux. Do not subject SiT5721 to liquid based cleaning processes.
- Reflow profile, per JESD22-A113D.
- For additional manufacturing guidelines and marking/ tape-reel instructions, refer to SiTime Manufacturing Notes.

## Additional Information

### Table 11. Additional Information

| Document | Description |
|---|---|
| **ECCN #: EAR99** | Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes. |
| **HTS Classification Code: 8542.39.0000** | A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods. |
| **SiT6731 EVB** | Evaluation board, contact SiTime |
| **Manufacturing Notes** | Tape & Reel dimension, reflow profile and other manufacturing related info |
| **Qualification Reports** | RoHS report, Reliability reports, Composition reports |
| **Performance Reports** | Additional performance data such as phase noise, current consumption, and jitter for selected frequencies |
| **Termination Techniques** | Termination design recommendations |
| **Layout Techniques** | Layout recommendations |
| **Other Quality Documents** | ISO certificate, materials declarations, environmental policy, warranty on date code |

## Revision History

### Table . Revision History

| Version | Release Date | Change Summary |
|---|---|---|
| 0.83 | 17-Sep-2019 | First release, preliminary information |
| 0.84 | 30-Oct-2019 | Changed Rise/Fall time condition for Clipped Sinewave Output Characteristics<br>Other minor changes |
| 0.85 | 20-Apr-2020 | Updated various specifications and conditions after characterization<br>Updated package drawings and pinouts view |
| 0.9 | 10-Aug-2020 | Added Appendix: Emerald™ DCOCXO Programming Guide<br>Updated ordering information |
| 0.92 | | Updated pin description and package drawings<br>Updated conditions for initial tolerance<br>Updated minimum and maximum storage<br>Updated dimensions and patterns<br>Updated layout guidelines<br>Updated Figure 12 and data format section in appendix |
| 0.93 | 24-Aug-2021 | Updated various electrical specifications after further characterization.<br>Updated minimum order quantity for tape and reel packaging<br>Added thermal considerations<br>Updated recommended land pattern<br>Resolved typographical error on page 21 |
| 1.0 | 7-Jun-2022 | Updated the product description<br>Changed the name of pin 7 to “DNC” for added clarity<br>Updated the aging, Allan deviation, and phase noise specifications with the latest characterization data<br>Updated the thermal considerations and guidelines<br>Added test circuit and waveform diagrams<br>Added Allan deviation, Hadamard deviation, and daily aging performance plots<br>Added, lot number, serial number, and fabrication date, and aging compensation registers to the appendix<br>Added temperature error register and status flag reset instructions to the appendix<br>Added schematic for digitally controlled OCXO to the appendix |

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# Appendix

## Introduction

This programing guide is applicable to SiTime's Emerald digitally controlled OCXO (DCOCXO). It provides system developers with the necessary design information including $I^2C$ interface timing, $I^2C$ data format, register definition and register read/write access.

The SiT5721 (1 to 60 MHz) Emerald DCOCXO supports unique features such as

- Digital frequency pulling with ±5 ppt resolution
- Adjust frequency-pull ramp rate
- Temperature read-back
- Error status flag

These features allow system designers to enhance system robustness by eliminating output frequency sensitivity to board level noise and enabling device status monitoring. By reading and writing to the registers through the $I^2C$ interface, the guide supports designers in utilizing the distinct features SiT5721 has to offer, including adjusting frequency pull and ramp rate, reading temperature, and checking error status flags.

## Register Definitions and Descriptions

SiT5721 provides three categories of registers with read/write accessibility via $I^2C$:

- **Description Registers** – read only registers that provide information about the specific part.
- **Control Registers** – read/write registers that allow for controlling the behavior of the part.
- **Status Registers** – read only registers that provide current operating values of the part.

The details of these registers are defined in the following sections. Many of the registers use a single precision floating point (binary 32 IEEE 754-2008 standard) data type. Details on the float point approach can be found in Floating Point Interface section.

Examples of writing and reading registers can be found in I2C Read and Write Example section.

Refer to the SiT5721 datasheet for other device information such as pin map and description, electrical spec and package dimensions.

### Description Registers

| Description Registers (1024 Byte Block) | | | | | | |
|---|---|---|---|---|---|---|
| Register Address | Name | Size (bytes) | Format | Units | Read/Write | Default |
| 0x50 | Part Number | 256 | ASCII | - | R | Factory Set |
| 0x51 | Reserved | - | - | - | - | - |
| 0x52 | Nominal Frequency | 32 | ASCII | MHz | R | Factory Set |
| 0x53 | Reserved | - | - | - | - | - |
| 0x54 | Reserved | - | - | - | - | - |
| 0x55 | Reserved | - | - | - | - | - |
| 0x56 | Lot and Serial Numbers | 32 | ASCII | - | R | Factory Set |
| 0x57 | Fabrication Date | 32 | ASCII | - | R | Factory Set |

Each of the header registers returns ASCII values representing the header attribute (e.g. Part Number = "SiT5721AC-KW333JT-19.123456T"). The first returned byte that is equal to 0 indicates the end of the ASCII string.

**Nominal Frequency:**

Register 0x52 contains the nominal frequency at the output.

**Lot and Serial Numbers and Fabrication Date**

Registers 0x56 and 0x57 contain the part lot information, serial numbers, and fabrication date. These registers are read only.

## Control Registers

The SiT5721 DCOCXO enables control of the frequency pull, maximum frequency-pull ramp rate, and aging compensation. The following table defines the locations and parameters of each register.

| Control Registers (1024 Byte Block) | | | | | | |
|---|---|---|---|---|---|---|
| Register Address | Name | Size (bytes) | Format | Units | Read/Write | Default |
| 0x60 | Reserved | - | - | - | - | - |
| 0x61 | Pull Value | 4 | Float | ± Fractional Offset | R/W | 0 |
| 0x62 | Pull Range | 4 | Float | Fractional Offset | R/W | 10E-06 |
| 0x63 | Aging Compensation | 4 | Float | ± Fraction/Second | R/W | 0 |
| 0x64 | Max. Frequency Ramp Rate | 4 | Float | Fraction/Second | R/W | 1.00E-05 |
| 0x65 | Reserved | - | - | - | - | - |
| 0x66 | Reserved | - | - | - | - | - |
| 0x67 | Reserved | - | - | - | - | - |
| 0x68 | Reserved | - | - | - | - | - |
| 0x69 | Reserved | - | - | - | - | - |
| 0x6A | Reserved | - | - | - | - | - |
| 0x6B | Reserved | - | - | - | - | - |
| 0x6C | Reserved | - | - | - | - | - |
| 0x6D | Reserved | - | - | - | - | - |
| 0x6E | Reserved | - | - | - | - | - |
| 0x6F | Reserved | - | - | - | - | - |

### Pull Value:

The pull value is the adjustment that the designer desires to make to the factory programmed center frequency, where the center frequency is the device frequency with the Pull Value set to 0. It is a fractional offset in the form of a 32-bit float. For a desired shift of +1 ppm, the designer would write the value of 1.00E-06 to the register address 0x61. A desired shift of 1 ppm lower than the factory programmed frequency would be entered into the register as -1.00E-06. However, the set pull value is not persistent; the output will return to the factory programmed frequency during power cycles. The designer can read from as well as write to this register and the factory default is no frequency offset.

### Pull Range:

The pull range is the limit above and below the center frequency to which the center frequency can be pulled. This value and any value written to this register are absolute; it is the value in the register above and below zero. For example, if the designer writes 3.0E-06 to the register, the pull range would be -3E-06 to +3E-06 relative to the center frequency. The designer can read from and write to this register.

### Aging Compensation

Aging compensation reflects the fractional offset per second with reference to the nominal output frequency. For example, 2E-14 corresponds to an aging compensation rate of 0.02 ppt per second, approximately 1.7 ppb per day. A positive value increases the output frequency, compensating for a negative aging trend. The aging compensation register is volatile and resets to 0 upon power cycling. This is a read/write register.

### Maximum Frequency Ramp Rate:

The maximum frequency ramp rate is the maximum rate at which the output frequency will adjust until it meets the set pull value or hits the set pull range. It is a 32-bit float value which is set in the unit of fraction per second. The maximum and default rate which can be set is 10 ppm per second. For example, if the desired maximum ramp rate is 1 ppm per second, 1.00E-06 would be written to the register address 0x64.

## Status Registers

Status registers are used to monitor the operation of the Emerald. Status registers that can be read are the time since start register, resonator temperature register, and the error status flag. All status registers are read only and updated at 1 kHz.

| Status Registers (512 Byte Block) | | | | | |
|---|---|---|---|---|---|
| Register Address | Name | Size (bytes) | Format | Units | Read/Write |
| 0xA0 | Time Since Power Up | 4 | Unsigned Int. | Seconds | R |
| 0xA1 | Resonator Temperature | 4 | Float | Degrees C | R |
| 0xA2 | Reserved | - | - | - | - |
| 0xA3 | Microcontroller Supply Voltage | 4 | Float | Volts | R |
| 0xA4 | Reserved | - | - | - | - |
| 0xA5 | Reserved | - | - | - | - |
| 0xA6 | Reserved | - | - | | - |
| 0xA7 | Heater Power | 4 | Float | Watts | R |
| 0xA8 | Reserved | - | - | - | - |
| 0xA9 | Reserved | - | - | - | - |
| 0xAA | Reserved | - | - | - | - |
| 0xAB | Total Offset Written | 4 | Float | ± Fractional Offset | R |
| 0xAC | Reserved | - | - | - | - |
| 0xAD | Reserved | - | - | - | - |
| 0xAE | Error Status Flag | 4 | Unsigned Int. | Bit Field | R |
| 0xAF | Stability Flag | 4 | Unsigned Int. | - | R |
| 0xB0 | Temperature Error | 4 | Float | Degrees C | R |
| 0xB1 | Power Target | 4 | Float | Watts | R |

**Total Offset:**

The total offset register indicates the total offset written into the device in units of fractional frequency. It includes both the pull value and aging compensation.

**Stability Flag:**

A high stability flag of “1” indicates that the internal oven has stabilized and that the device is in oven control.

**Temperature Error:**

The temperature error register indicates the current error in the temperature control loop as a delta from target temperature in degrees centigrade.

**Power Target:**

The power target register indicates the target power input into the heater control loop

**Error Status Flag:**

In addition to the error status pin, the error status flag alerts the user of any errors during operation. A register value of 7 represents normal operation. This is as non-volatile register and will not change until reset. The following procedure resets the error status flag.

Master write:

- Write address 0xE1
- Data: 0x64 0x01 (2 bytes of data)
- Stop

## I²C Interface Configuration Description

### Serial Interface Configuration Description

Emerald includes an I²C interface to access registers that control the DCOCXO frequency pull range, and frequency pull value. The SiT5721 I²C is a slave-only interface with clock stretch and clock speeds up to 400 kHz. Emerald, during the transaction, can hold SCL LOW to force the master into a wait state until it has performed internal operations. Therefore, clock stretching support by the master is required. The I²C module is based on the I²C specification, UM1024 (Rev.6 April 4, 2014 of NXP Semiconductor).

### Serial Signal Format

The SDA line must be stable during the high period of the SCL. SDA transitions are allowed only during SCL low level for data communication. Only one transition is allowed during the low SCL state to communicate one bit of data. Figure 19 shows the detailed timing diagram.

An idle I²C bus state occurs when both SCL and SDA are not being driven by any master and are therefore in a logic HI state due to the pull up resistors. Every transaction begins with a START (S) signal and ends with a STOP (P) signal. A START condition is defined by a high to low transition on the SDA while SCL is high. A STOP condition is defined by a low to high transition on the SDA while SCL is high. START and STOP conditions are always generated by the master. This slave module also supports repeated START (Sr) condition which is same as START condition instead of STOP condition (the blue-color line shows repeated START in Figure 20).

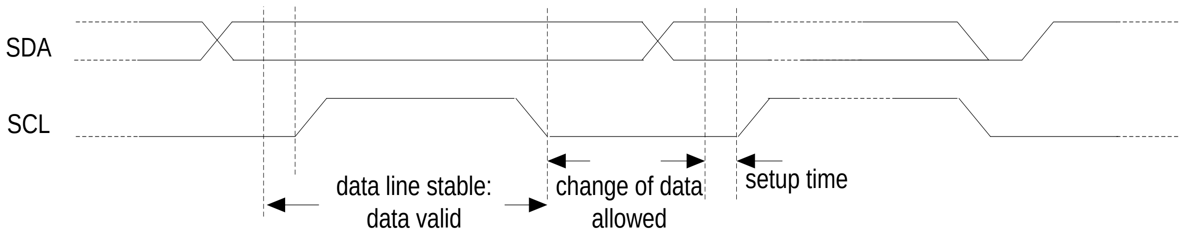


**Figure 19. Data and clock timing relation in I²C bus**

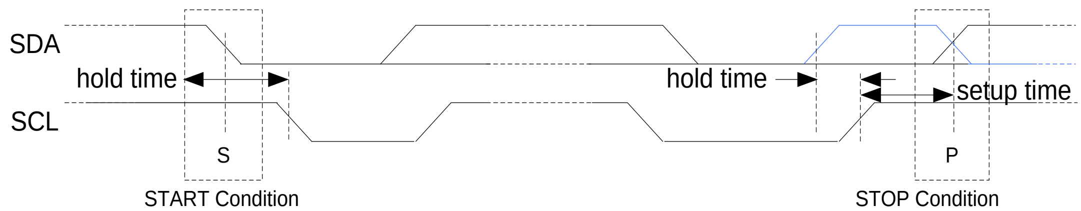


**Figure 20. START and STOP (or repeated START, blue line) condition**

**Byte Format**

Every data byte is 8 bits long. The number of bytes that can be transmitted per transfer is defined by the address being written. Data is transferred with the LSB (Least Significant Byte) first. The detailed data transfer format is shown in Figure 22 below.

## Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge bit must occur after every byte transfer and it allows the receiver to signal the transmitter that the byte was successfully received, and another byte may be sent. The acknowledge signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. Setup and hold times must also be taken into account. When SDA remains high during this ninth clock pulse, this is defined as the Not-Acknowledge signal (NACK). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer. The only condition that leads to the generation of NACK from Emerald is when the transmitted address does not match the slave address. When the master is reading data from the device, SiT5721 expects the ACK from the master at the end of received data, so that the slave releases the SDA line and the master can generate the STOP or repeated START.

## Data Format

This I$^2$C slave module supports 7-bit device addressing format. The 8th bit is a read/write bit and "1" indicates a read transaction and a "0" indicates a write transaction. The register addresses are 8-bits long with an address range of 0 to 255 (0x00 to 0xFF). Auto register address incrementing is supported for read operation only and within one register group. This allows data to be transferred to contiguous addresses without the need to write each address beyond the first address. For a read operation, the starting register address must be written first. The data format is based on the register being accessed (ASCII, 32 bit float, 32 bit ints). Float and Int values are set least significant byte first (little endian).

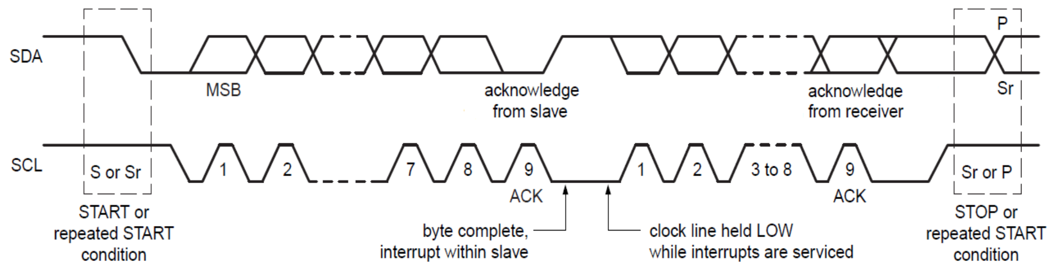


**Figure 21. Parallel signaling format**

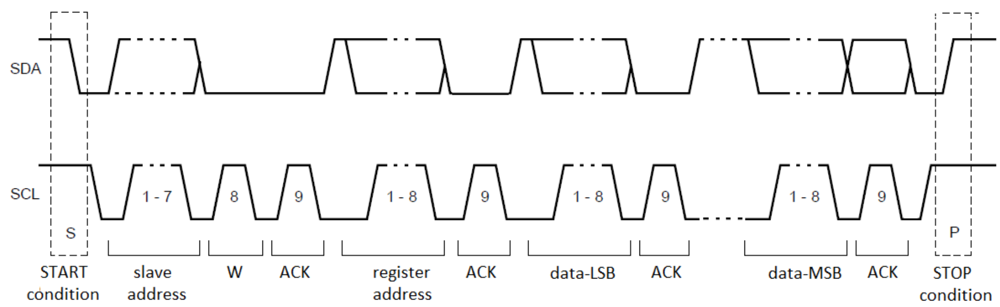


**Figure 22. Parallel data byte format, write operation**

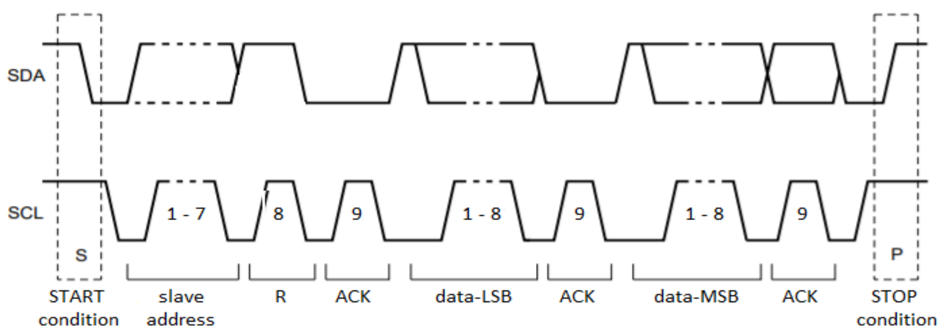


**Figure 23. Parallel data byte format, read operation**

### $I^2C$ Timing Specification

The below timing diagram and Table 12 illustrate the timing relationships for both master and slave.

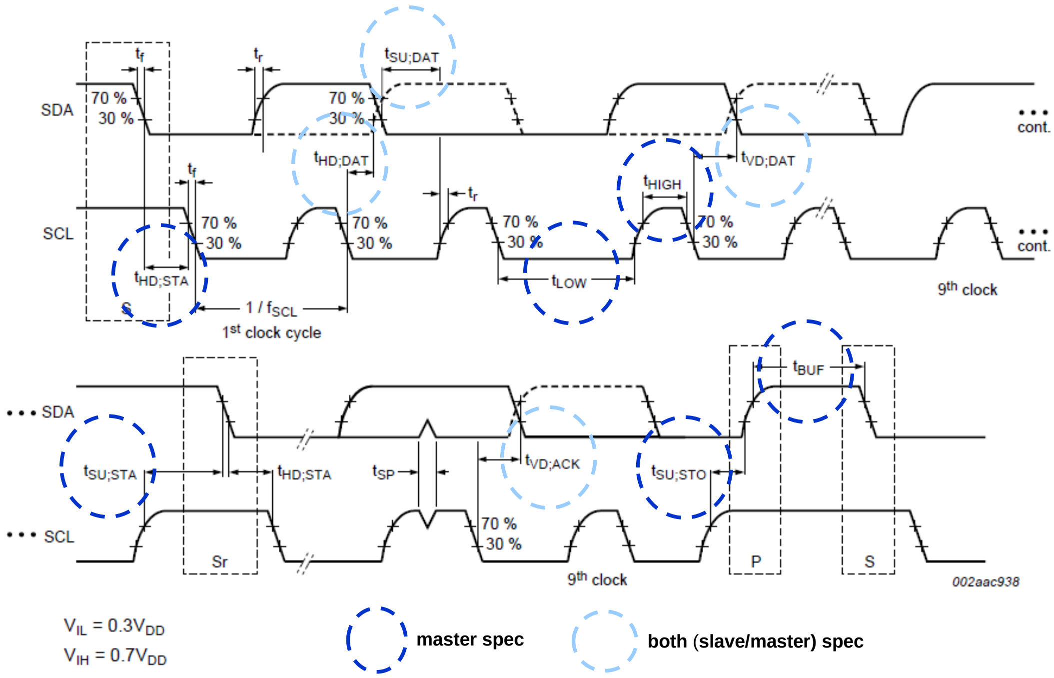


**Figure 24. $I^2C$ Timing Diagram**

**Table 12. $I^2C$ Timing Requirements for Fast Mode (FM) and Standard Mode (SM)**

| Parameter | Speed Mode | Minimum Value | Unit |
|---|---|---|---|
| $t_{SU;DAT}$ | FM (400 KHz) | >100 | ns |
| | SM (100 KHz) | >250 | ns |
| $t_{HD;DAT}$ | FM (400 KHz) | >0 | ns |
| | SM (100 KHz) | >0 | ns |

## Programming Guide and Examples

This section of the document provides a guide on how to program SiT5721. The first subsection provides details on floating point numbers and how to convert between binary and floating point. The second subsection describes how to use the floating point interface to communicate the desired frequency pull. Finally, the last subsection provides examples of how to read to and write from the SiT5721 registers.

### Floating Point Interface

Emerald uses 32-bit single precision floating-point numbers for some of the register values as specified by IEEE-754-2008 and repeated below for convenience:

| 31 | 30 … 23 | 22 … 0 |
|---|---|---|
| S | Exponent | Fraction (mantissa) |

**Bit 31 is the sign bit with the following definition:**

0 = Positive number
1 = Negative Number

Bits 30:23 contain the exponent value and bits 22:0 contain the fractional value.

**The conversion formula to decimal in normalized form is:**

$$= (-1)^{S} \times (1 + Fraction) \times 2^{(Exponent-127)}$$

The normalized form is used to express most values except 0. As an example, if:

- S = 1b
- Exponent = 1000 0010b
- Fraction = 011 1000 0000 0000 0000 0000b

Then the binary fraction would be converted to decimal:

011 1000 0000 0000 0000 0000b = $\frac{0}{2^1} + \frac{1}{2^2} + \frac{1}{2^3} + \frac{1}{2^4}$ = 0.4375d

Similarly, the exponent would be converted to decimal:

1000 0010b = $2^1 + 2^7$ = 130d

Finally, by substituting the calculated values into the formula provide above, the total decimal value would be:

$$= (-1)^{1} \times (1 + 0.4375) \times 2^{(130-127)} = (-1) \times 1.4375 \times 2^{3} = -11.5d$$

### Frequency Control Using Floating Point Numbers

To clarify how the frequency control operates, the floating-point value sets the offset in fractional frequency units. For instance, +1.00e-6 is 1.00 ppm higher frequency shift, and -1.23456e-9 is 1.23456 ppb lower frequency. These values must be written to the control registers using the proper IEEE-754-2008 format described in Floating Point Interface section.

The fractional part of the single-precision floating point number (mantissa) is 23 bits and the frequency resolution is therefore 1 part in $2^{23}$, or approximately 0.0000012. The following two examples demonstrate a couple of frequency resolution cases.

| Frequency Pull Value | Resolution of Pull Value |
|---|---|
| 5 ppm | 0.6 ppt |
| 0.1 ppm | 0.01 ppt |

These values are below the Emerald noise floor and therefore do not contribute additional noise.

## I$^2$C Read and Write Example

The address of the part is based on the part number that was ordered.

SiT5721AC-KW333-T-19.123456T

**I$^2$C Address Mode**

Values: 0,1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F

Set bits 3:0 of device I$^2$C address to the Hex value of the ordering code.

| I$^2$C Address Ordering Code | Device I$^2$C Address |
|---|---|
| 0 | 1100000 (0x60) |
| 1 | 1100001 (0x61) |
| 2 | 1100010 (0x62) |
| 3 | 1100011 (0x63) |
| 4 | 1100100 (0x64) |
| 5 | 1100101 (0x65) |
| 6 | 1100110 (0x66) |
| 7 | 1100111 (0x67) |
| 8 | 1101000 (0x68) |
| 9 | 1101001 (0x69) |
| A | 1101010 (0x6A) |
| B | 1101011 (0x6B) |
| C | 1101100 (0x6C) |
| D | 1101101 (0x6D) |
| E | 1101110 (0x6E) |
| F | 1101111 (0x6F) |

Values of format type float and integers are sent in little endian format (MSB last).

### Example Read Description Register

Emerald provides a register based I$^2$C interface for accessing data from the device. The description, status, and control registers can all be read. Data is returned in the size and format listed in the table for each register. The address associated with SiT5721 is based on the part number that was ordered. The sequence to read an I$^2$C register is to first write the register number to the SiT5721 I$^2$C address and then read back the data from the same address (read/write transaction).

**Read Nominal Frequency Example:**

- SiT5721 I$^2$C order code: 2 – converts to I$^2$C slave address of 0x62
- Register read: Nominal Frequency – register 0x52
- Master write:
  - Write address 0x62
  - Data: 0x52
  - Stop
- Master read:
  - Read address 0x62
  - Read 32 bytes
    - SiT5721 returns "20.000000MHz" (followed by 0x00 24 times)
  - Stop

**Write Control Register Example**

The control registers of the I$^2$C interface are writable for changing operating parameters in the Emerald. Data size and format are listed in the control register table.

**Example Write Pull Value**

- Emerald I2C order code: 4 – converts to I2C slave address of 0x64
- Register read: Pull Value – register 0x61
- Value: Change frequency by +1 ppm. In floating point this is +1.00e-6, which as a 32 bit float is 0x358637BD.
- Master write:
  - Write address 0x64
  - Data: 0x61 (register), followed by 0xBD 0x37 0x86 0x35 (little endian send of 1.00e-6)
  - Stop

## Schematic Example

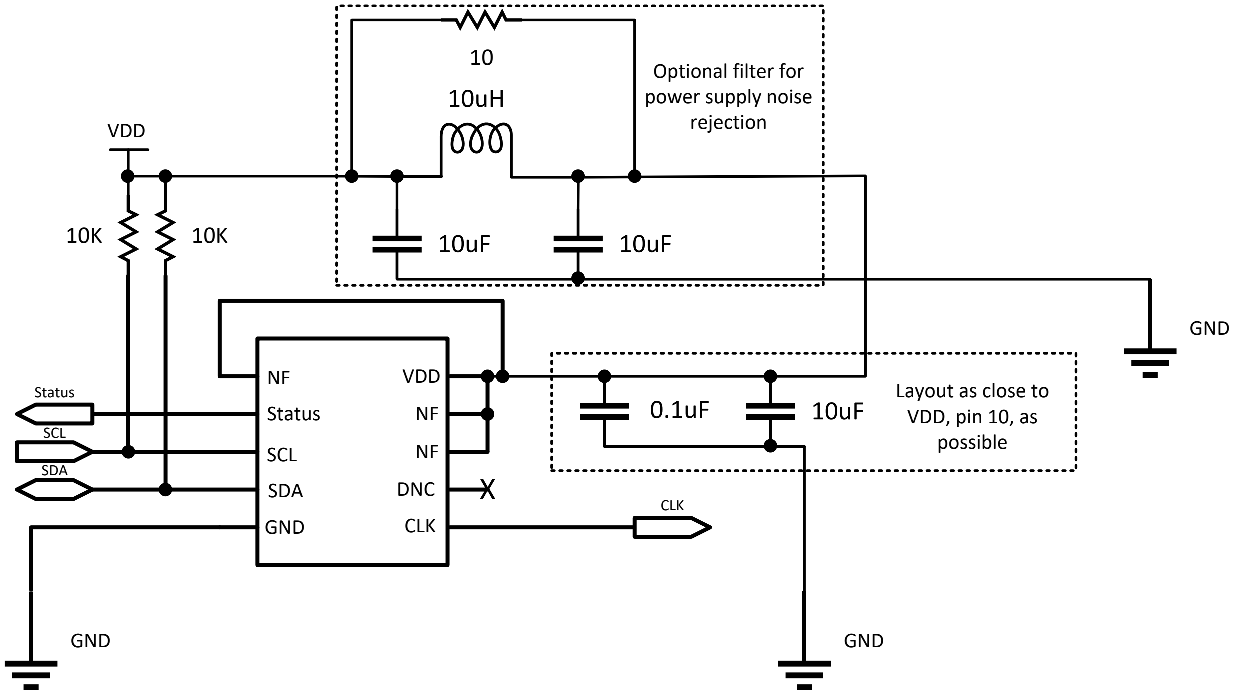


**Figure 25. DCOCXO schematic example**