4.5-V TO 16-V INPUT, HIGH CURRENT, SYNCHRONOUS STEP DOWN DUAL BUCK CONVERTER WITH INTEGRATED FETS

Check for Samples: TPS65253

FEATURES

- **Wide Input Supply Voltage Range: 4.5 V - 16 V**
- **Output Range: 0.8 V to ~V_{IN}-1 V**
- **Fully Integrated Dual Buck, 3.5-A/2.5-A Continuous Current (4-A/3-A Maximum Current)**
- **High Efficiency**
- **300-kHz - 1.2-MHz Switching Frequency Set by External Resistor**
- **External Eenable/Sequencing Pins**
- **Adjustable Cycle-by-Cycle Current Limit Set by External Resistor**
- **Soft-Start Pins**
- **Current-Mode Control With Simple Compensation Circuit**
- **Power Good and Reset Generator**
- **Low Power Mode Set By External Signal**
- **Supervisory Circuit**
- **QFN Package, 28-Pin 5 mm x 5 mm RHD**

APPLICATIONS

- **DTV**
- **DSL Modems**
- **Cable Modems**
- **Set Top Boxes**
- **Car DVD Players**
- **Home Gateway and Access Point Networks**
- **Wireless Routers**

DESCRIPTION/ORDERING INFORMATION

The TPS65253 features two synchronous wide input range high efficiency buck converters. The converters are designed to simplify product application while giving designers the options to optimize their usage according to the target application.

The converters can operate in 5-, 9- and 12-V systems and have integrated power transistors. The output voltage can be set externally using a resistor divider to any value between 0.8 V and the input supply minus 1 V. Each converter features an enable pin that allows a delayed start-up for sequencing purposes, soft-start pin that allows adjustable soft-start time by choosing the soft-start capacitor, and a current limit (RLIMx) pin that enables designer to adjust current limit by selecting an external resistor and optimize the choice of inductor. The CMP pin allows optimizing transient versus dc accuracy response with a simple RC compensation.

The switching frequency of the converters is set by an external resistor connected to R_{OSC} pin. The switching regulators are designed to operate from 300 kHz to 1.2 MHz. The converters operate with 180° phase between then to minimize the input filter requirements.

TPS65253 also features a low power mode enabled by an external signal, which allows for a reduction on the input power supplied to the system when the host processor is in stand-by (low activity) mode.

TPS65253 features a supervisor circuit that monitors both converters and provides a PGOOD signal (End of Reset) with a 32-ms timer.

TPS65253 is packaged in a small, thermally efficient 28-pin QFN package.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	28-Pin (QFN) - RHD	TPS65253RHD	TPS65253

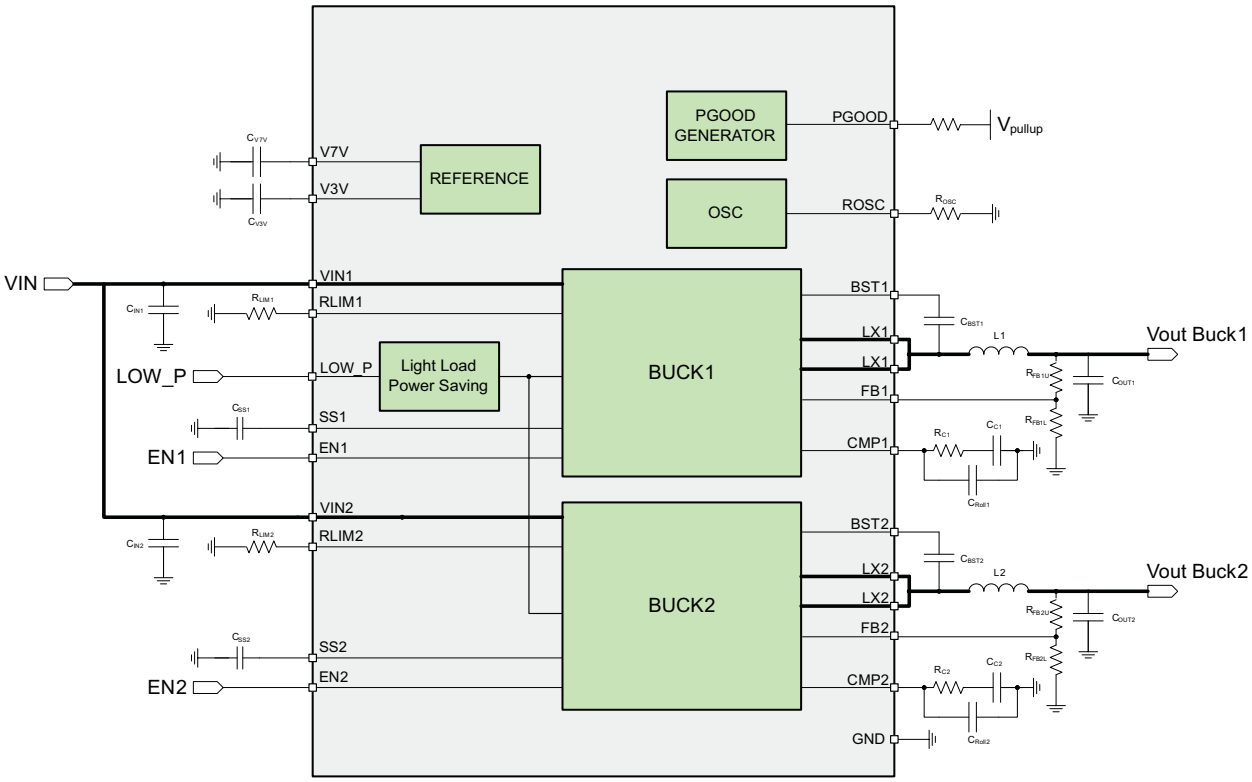
(1) For the most current packaging and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

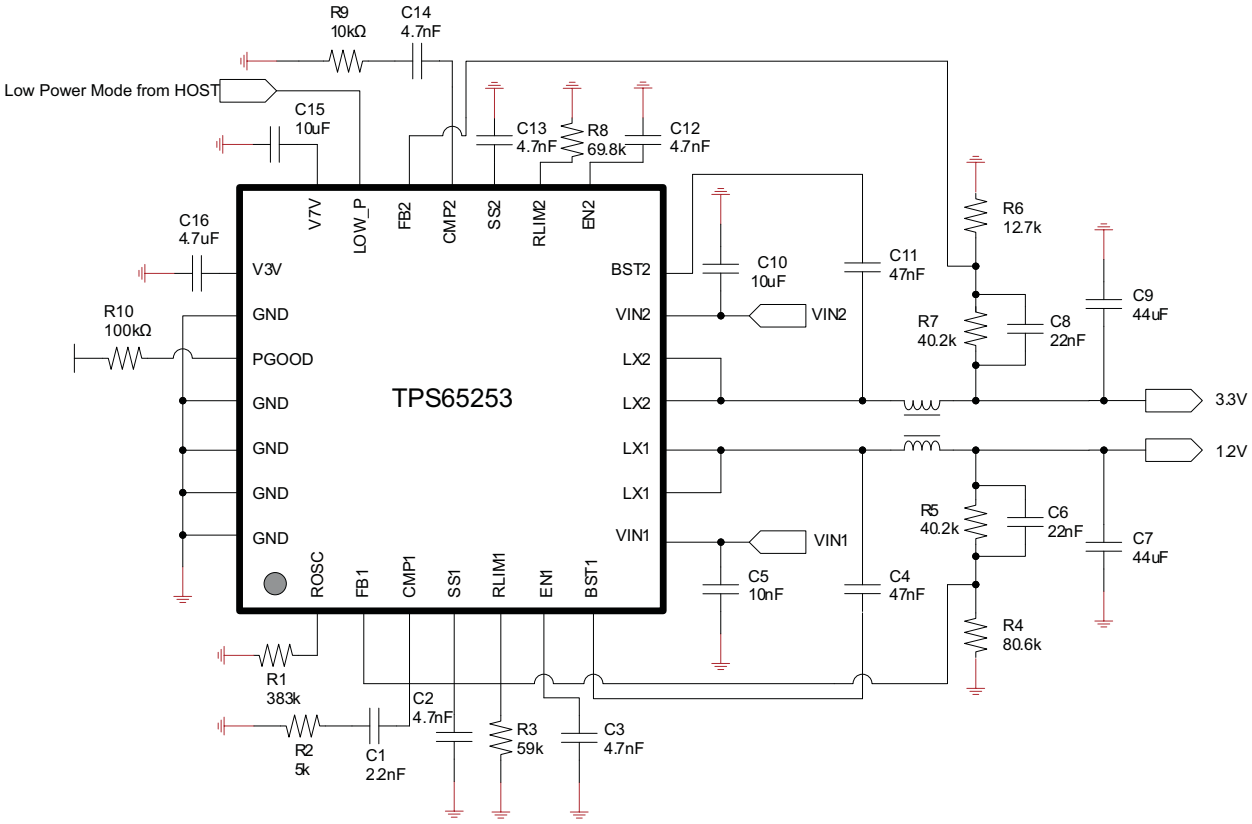
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM

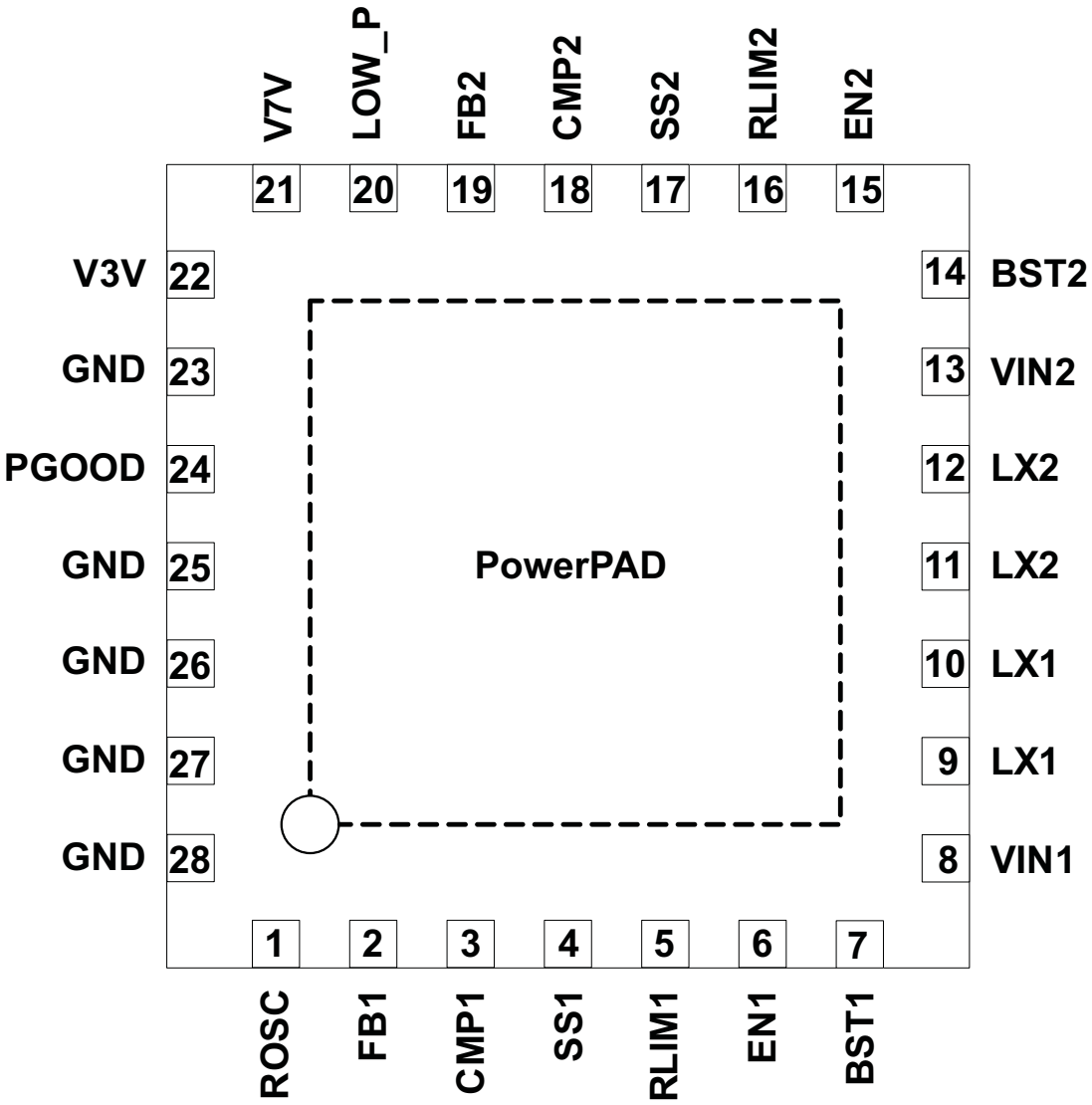


TYPICAL APPLICATION



PIN OUT

RHD PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

NAME	NO.	I/O	DESCRIPTION
ROSC	1	I	Oscillator set. This resistor sets the frequency of internal autonomous clock.
FB1	2	I	Feedback pin for Buck 1. Connect a divider set to 0.8 V from the output of the converter to ground.
CMP1	3	O	Compensation pin for Buck 1. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
SS1	4	I	Soft-start pin for Buck 1. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
RLIM1	5	I	Current limit setting pin for Buck 1. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
EN1	6	I	Enable pin for Buck 1. A high signal on this pin enables the regulator Buck. For a delayed start-up add a small ceramic capacitor from this pin to ground.
BST1	7	I	Bootstrap capacitor for Buck 1. Fit a 47-nF ceramic capacitor from this pin to the switching node.
VIN1	8	I	Input supply for Buck 1. Fit a 10-µF ceramic capacitor close to this pin.
LX1	9, 10	O	Switching node for Buck 1
LX2	11, 12	O	Switching node for Buck 2
VIN2	13	I	Input supply for Buck 2. Fit a 10-µF ceramic capacitor close to this pin.
BST2	14	I	Bootstrap capacitor for Buck 1. Fit a 47-nF ceramic capacitor from this pin to the switching node.
EN2	15	I	Enable pin for Buck 2. A high signal on this pin enables the regulator Buck. For a delayed start-up add a small ceramic capacitor from this pin to ground.
RLIM2	16	I	Current limit setting pin for Buck 2. Fit a resistor from this pin to ground to set the peak current limit on the output inductor.
SS2	17	I	Soft-start pin for Buck 2. Fit a small ceramic capacitor to this pin to set the converter soft-start time.
CMP2	18	O	Compensation pin for Buck 2. Fit a series RC circuit to this pin to complete the compensation circuit of this converter.
FB2	19	I	Feedback pin for Buck 2. Connect a divider set to 0.8 V from the output of the converter to ground.
LOW_P	20	I	Low power operation mode (active high) input for TPS65253
V7V	21	O	Internal supply. Connect a 4.7-µF to 10-µF ceramic capacitor from this pin to ground.
V3V	22	O	Internal supply. Connect a 3.3-µF to 10-µF ceramic capacitor from this pin to ground.
GND	23, 25, 26, 27, 28		Ground
PGOOD	24	O	Open drain power good output
PowerPAD			PowerPAD. Connect to system ground for electrical and thermal connection.

ABSOLUTE MAXIMUM RATINGS (1)

over operating free-air temperature range (unless otherwise noted)

	Voltage range at VIN1,VIN2, LX1, LX2	–0.3 to 18	V
	Voltage range at LX1, LX2 (maximum withstand voltage transient < 20 ns)(2)	–3 to 18	V
	Voltage at BST1, BST2, referenced to LX pin	–0.3 to 7	V
	Voltage at V7V, CMP1, CMP2	–0.3 to 7	V
	Voltage at V3V, RLIM1, RLIM2, EN1, EN2, SS1, SS2, FB1, FB2, PGOOD, ROSC, LOW_P	–0.3 to 3.6	V
	Voltage at GND	–0.3 to 0.3	V
T_J	Operating virtual junction temperature range	–40 to 125	°C
T_{STG}	Storage temperature range	–55 to 150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) Excessive parasitic inductance may cause deeper negative voltage for less than 20 ns. To minimize this undershoot tight board layout is recommended.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input operating voltage	4.5		16	V
T_A	Junction temperature	–40		85	°C

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

	MIN	MAX	UNIT
Human body model (HBM)	2000		V
Charge device model (CDM)	500		V

PACKAGE DISSIPATION RATINGS(1)

PACKAGE	θ_{JA} (°C/W)	T_A = 25°C POWER RATING (W)	T_A = 55°C POWER RATING (W)
RHD	34 (Simulated)	2.9	2

(1) Based on JEDEC 51.5 HIGH K environment measured on a 76.2 x 114 x 0.6-mm board with the following layer arrangement:
(a) Top layer: 2 Oz Cu, 6.7% coverage
(b) Layer 2: 1 Oz Cu, 90% coverage
(c) Layer 3: 1 Oz Cu, 90% coverage
(d) Bottom layer: 2 Oz Cu, 20% coverage

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, VIN = 12 V, L_O = 2.2 µH, f_{SW} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY UVLO AND INTERNAL SUPPLY VOLTAGE						
VIN	Input voltage range		4.5		16	V
IDD_{SDN}	Shutdown	EN pin = low for all converters		0.4		mA
IDD_Q	Quiescent, low power disabled	Converters enabled, no load Buck 1 = 1.2 V Buck 2 = 3.3 V		40		mA
$IDD_{Q\_LOW\_P}$	Quiescent, low power enabled	Converters enabled, no load Buck 1 = 1.2 V Buck 2 = 3.3 V		0.6		mA
$UVLO_{VIN}$	V_{IN} under voltage lockout	Rising V_{IN}		4.22		V
		Falling V_{IN}		4.1		
$UVLO_{DEGLITCH}$		Both edges		110		µs
V3V	Internal supply output voltage			3.3		V
	External load for 3.15 V < V3V < 3.4 V				10	mA
V7V	Internal supply output voltage			6.25		V
	External load for 5.8 V < V3V < 6.56 V	V_{IN} = 12 V			25	mA
$V7V_{UVLO}$	UVLO for internal V7V rail	Rising V7V		3.8		V
		Falling V7V		3.6		
$V7V_{UVLO\_DEGLITCH}$		Falling edge		110		µs
BUCK CONVERTERS (ENABLE CIRCUIT, CURRENT LIMIT, SOFT-START, SWITCHING FREQUENCY AND LOW POWER MODE)						
V_{IH_ENx}	Enable threshold high	V3p3 = 3.2 V - 3.4 V, V_{ENx} rising	0.66 x V3p3			V
V_{IL_ENx}	Enable treshold Low	V3p3 = 3.2 V - 3.4 V, V_{ENx} falling			0.33 x V3p3	V
ICH_{EN}	Pull up current enable pin			1.1		µA
t_D	Discharge time enable pins	Power-up		10		ms
I_{SS}	Soft-start pin current source			5		µA
F_{SW_BK}	Converter switching frequency range	Set externally with resistor	0.3		1.2	MHz
R_{FSW}	Frequency setting resistor		140		600	kΩ
f_{SW_TOL}	Internal oscillator accuracy	f_{SW} = 800 kHz	-10		10	%
VIH_{LOW_P}	Low power mode threshold high	V3p3 = 3.3 V	0.66 x V3p3			V
VIL_{LOW_P}	Low power mode treshold Low	V3p3 = 3.3 V			0.33 x V3p3	V
FEEDBACK, REGULATION, OUTPUT STAGE						
V_{FB}	Feedback voltage	V_{IN} = 12 V , T_A = 25°C	-1%	0.8	1%	V
		V_{IN} = 4.5 V to 16 V	-2%	0.8	2%	
t_{ON_MIN}	Minimum on time (current sense blanking)			100	135	ns
I_{LIMIT1}	Peak inductor current limit range	V_{IN} = 12 V, V_{OUT} = 3.3 V, T_J = 25°C, L_O = 2.2 µH, R_{LIM1} = 59 kΩ, R_{LIM2} = 69.8 kΩ	-10%	5	10%	A
I_{LIMIT2}	Peak inductor current limit range	V_{IN} = 12 V, V_{OUT} = 3.3 V, T_J = 25°C, L_O = 2.2 µH, R_{LIM1} = 59 kΩ, R_{LIM2} = 69.8 kΩ	-15%	4.25	15%	A
MOSFET (BUCK 1)						
H.S. Switch	On resistance of high side FET on CH1	25°C, BOOT = 6.5 V		90		mΩ
L.S. Switch	On resistance of low side FET on CH1	25°C, VIN = 12 V		45		mΩ

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, VIN = 12 V, L_O = 2.2 µH, f_{SW} = 500 kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MOSFET (BUCK 2)						
H.S. Switch	On resistance of high side FET on CH2	25°C, BOOT = 6.5 V		115		mΩ
L.S. Switch	On resistance of low side FET on CH2	25°C, VIN = 12 V		75		mΩ
ERROR AMPLIFIER						
Error amplifier transconductance		-2 µA < ICOMP < 2 µA		130		µ℧
CMP to I_{LX} gm		I_{LX} = 0.5 A		12		A/V
POWER GOOD RESET GENERATOR						
VUV_{BUCKX}	Threshold voltage for buck under voltage	Output falling		85		%
		Output rising (PG will be asserted)		90		
$t_{UV\_deglitch}$	Deglitch time (both edges)			11		ms
t_{ON_HICCUP}	Hiccup mode ON time	VUV_{BUCKX} asserted		12		ms
t_{OFF_HICCUP}	Hiccup mode OFF time	All converters disabled. Once t_{OFF_HICCUP} elapses, all converters will go through sequencing again.		20		ms
VOV_{BUCKX}	Threshold voltage for buck over voltage	Output rising (high side FET will be forced off)		109		%
		Output falling (high side FET will be allowed to switch)		107		
t_{RP}	minimum reset period	Measured after the later of Buck 1 or Buck 2 power-up successfully		32		ms
THERMAL SHUTDOWN						
T_{TRIP}	Thermal shut down trip point	Rising temperature		160		°C
T_{HYST}	Thermal shut down hysteresis	Device re-starts		20		°C
$T_{TRIP\_DEGLITCH}$	Thermal shut down deglitch		100		120	µs

TYPICAL CHARACTERISTICS

V_{IN} = 12 V, f_{SW} = 500 kHz, L_O = 2.2 µH, DCR = 15 mΩ, C_O = 44 µF (unless otherwise specified)

Buck 1 Efficiency vs V_{OUT}

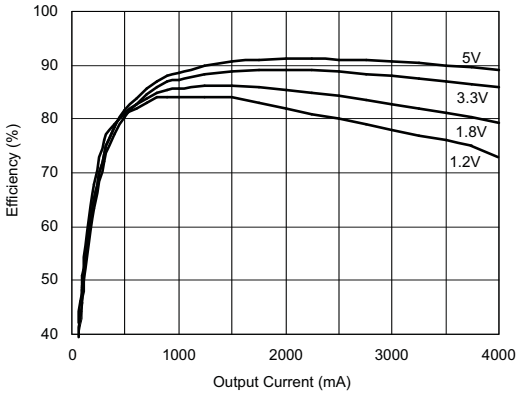


Figure 1.

Buck 2 Efficiency vs V_{OUT}

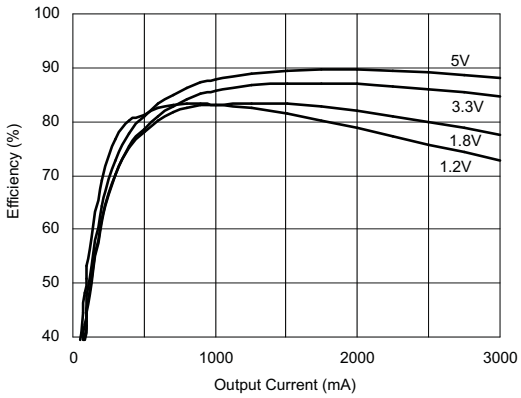


Figure 2.

Buck 1 (1.8 V) Efficiency vs V_{IN}

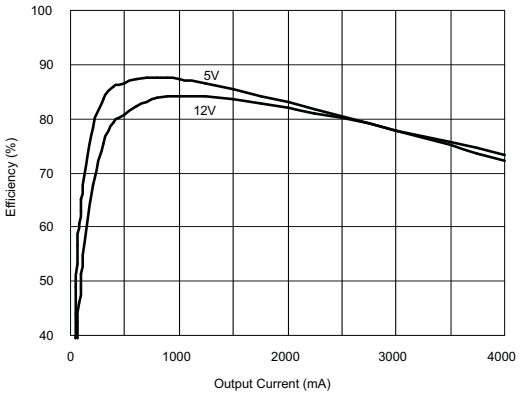


Figure 3.

. Buck 2 (3.3 V) Efficiency vs V_{IN}

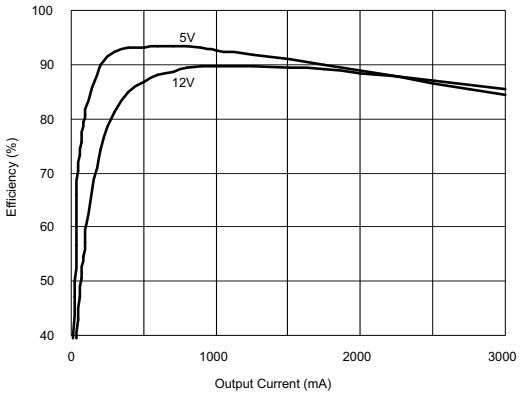


Figure 4.

Buck 1 Load Regulation vs V_{OUT}

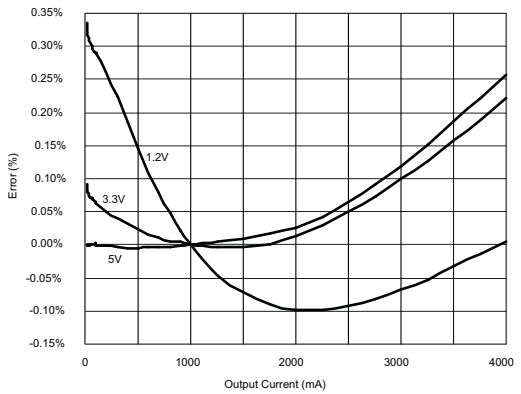


Figure 5.

Buck 2 Load Regulation vs V_{OUT}

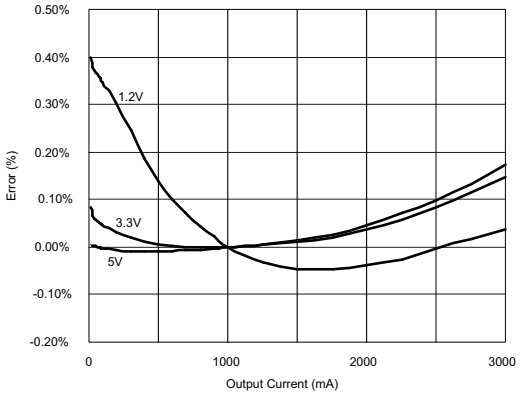


Figure 6.

TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, f_{SW} = 500 kHz, L_O = 2.2 µH, DCR = 15 mΩ, C_O = 44 µF (unless otherwise specified)

Buck 1 Output Ripple vs V_{OUT}

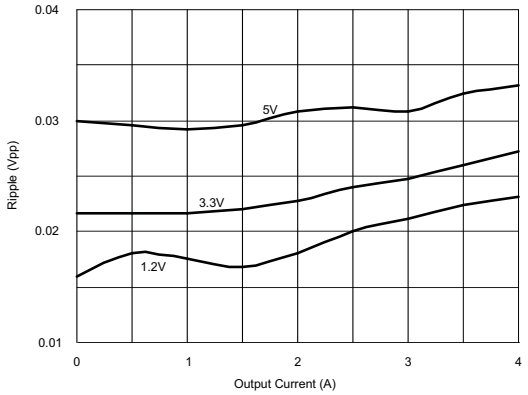


Figure 7.

Buck 2 Output Ripple vs V_{OUT}

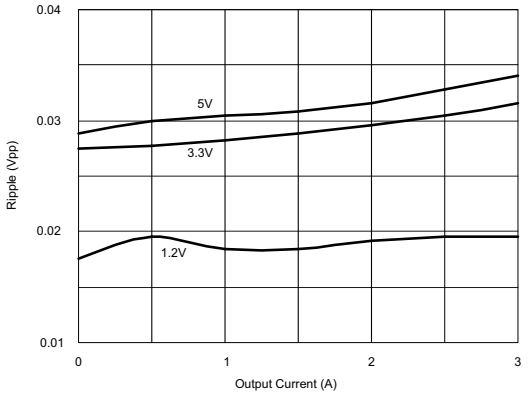


Figure 8.

Output Voltage (1.2 V) vs T_A

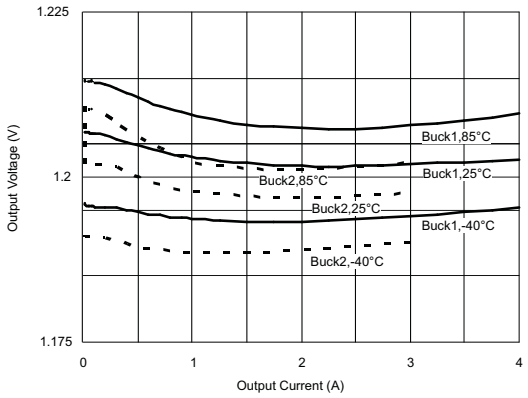


Figure 9.

Output Voltage (1.8 V) vs T_A

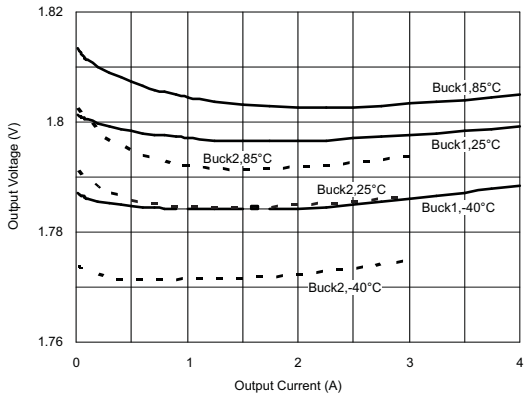


Figure 10.

Output Voltage (3.3 V) vs T_A

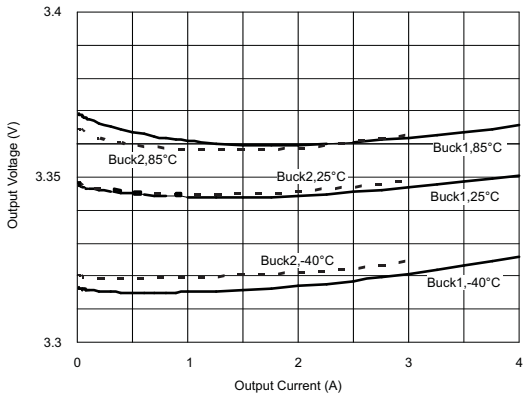


Figure 11.

Output Voltage (5 V) vs T_A

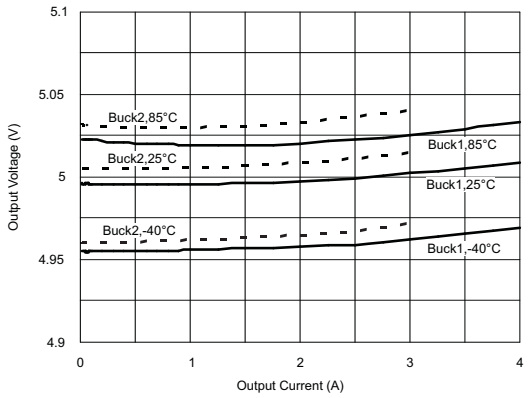


Figure 12.

TYPICAL CHARACTERISTICS (continued)

V_{IN} = 12 V, f_{SW} = 500 kHz, L_O = 2.2 µH, DCR = 15 mΩ, C_O = 44 µF (unless otherwise specified)

Details on Soft-Start, 1 ms/div

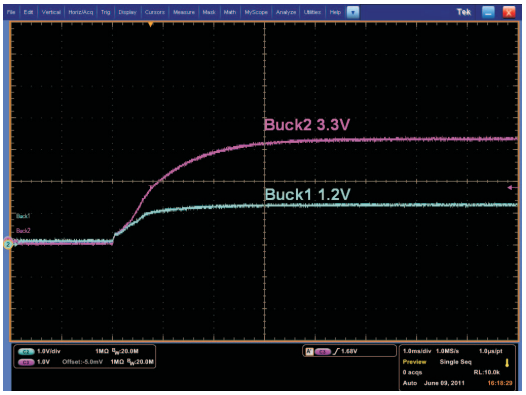


Figure 13.

Buck 1 (1.2 V) Ripple at Output Load of 4 A, 20 mV/div

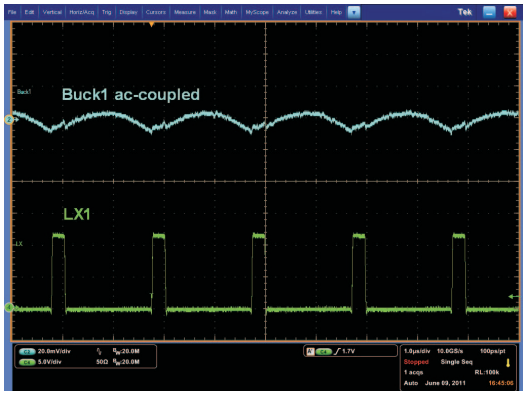


Figure 14.

Buck 2 (3.3 V) Ripple at Output Load of 3 A, 20 mV/div

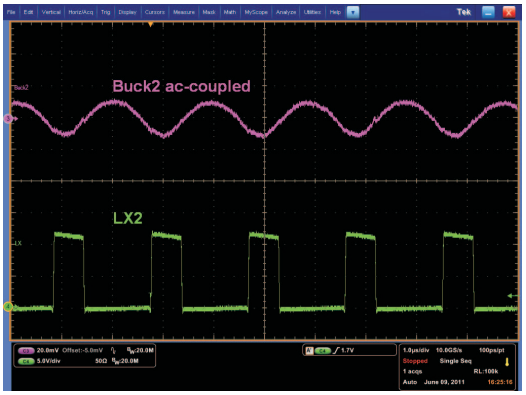


Figure 15.

Buck 1 Transient Load Response (1-A to 3-A Step), 30 mV/div

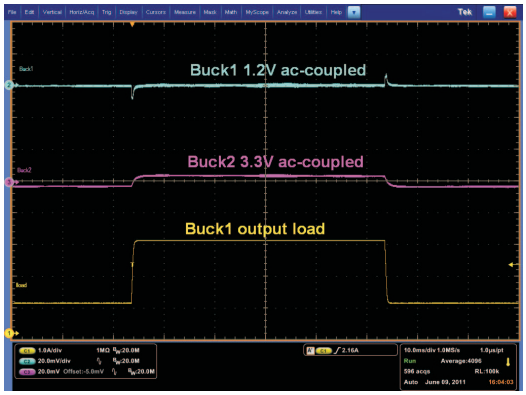


Figure 16.

Buck 2 Transient Load Response (0.75-A to 2.25-A Step), 30 mV/div

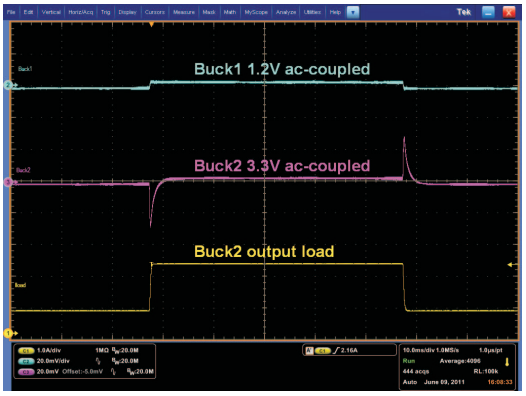


Figure 17.

Ripple With LOW_P = 1, Each Buck is Loaded With 10 mA, 100 mV/div

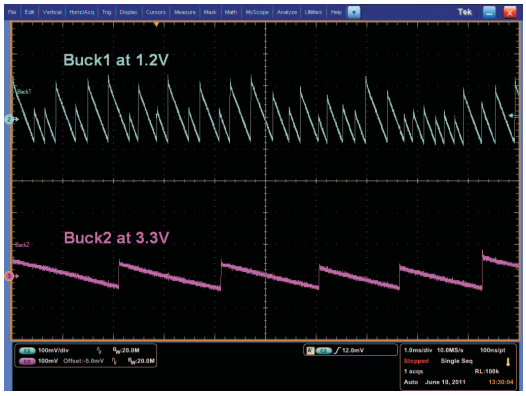


Figure 18.

OVERVIEW

TPS65253 is a power management IC with two step-down buck converters. Both high-side and low-side MOSFETs are integrated to provide fully synchronous conversion with higher efficiency. TPS65253 can support 4.5-V to 16-V input supply, high load current, 300-kHz to 1.2-MHz clocking. The buck converters have an optional PFM mode, which can improve power dissipation at light loads. Alternatively, the device implements a constant frequency mode by connecting the LOW_P pin to ground. The wide switching frequency of 300 kHz to 1.2 MHz allows for efficiency and size optimization. The switching frequency is adjustable by selecting a resistor to ground on the ROSC pin. Input ripple is reduced by 180° out-of-phase operation between Buck 1 and Buck 2.

Both buck converters have peak current mode control which simplifies external frequency compensation. A traditional type II compensation network can stabilize the system and achieve fast transient response. Moreover, an optional capacitor in parallel with the upper resistor of the feedback divider provides one more zero and makes the crossover frequency over 100 kHz.

Each buck converter has an individual current limit, which can be set up by a resistor to ground from the RLIMx pin. The adjustable current limiting enables high efficiency design with smaller and less expensive inductors.

The device has two built-in LDO regulators. During a standby mode, the 3.3-V LDO and the 6.5-V LDO can be used to drive MCU and other active loads. By this, the system is able to turn of the two buck converters and improve the standby efficiency.

The device has a power good comparator monitoring the output voltage. Each converter has its own soft-start and enable pin, which provide independent control and programmable soft-start.

DETAILED DESCRIPTION

Adjustable Switching Frequency

To select the internal switching frequency, connect a resistor from ROSC to ground. Figure 19 shows the required resistance for a given switching frequency.

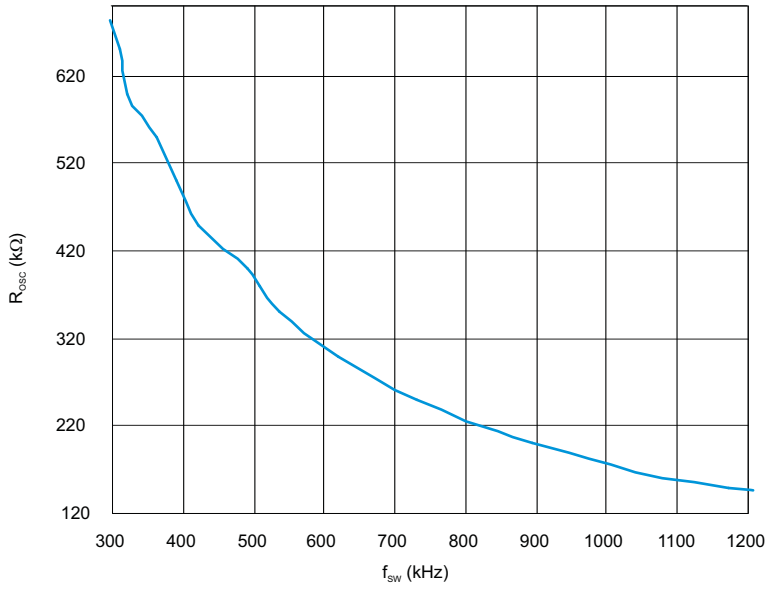


Figure 19. ROSC vs Switching Frequency

$$R_{OSC}(k\Omega) = 174 \bullet f_{SW}^{-1.122} \quad (1)$$

Out-of-Phase Operation

In order to reduce input ripple current, Buck 1 and Buck 2 operate 180° out-of-phase. This enables the system having less input ripple, then to lower component cost, save board space and reduce EMI.

Startup and Sequencing

If a delayed start-up is required on any of the buck converters fit a ceramic capacitor to the ENx pins. The delay added is ~1.7 ms per nF connected to the pin. Note that the EN pins have a weak 1-MΩ pull-up to the 3V3 rail. Figure 20 describes startup sequencing and PGOOD generation.

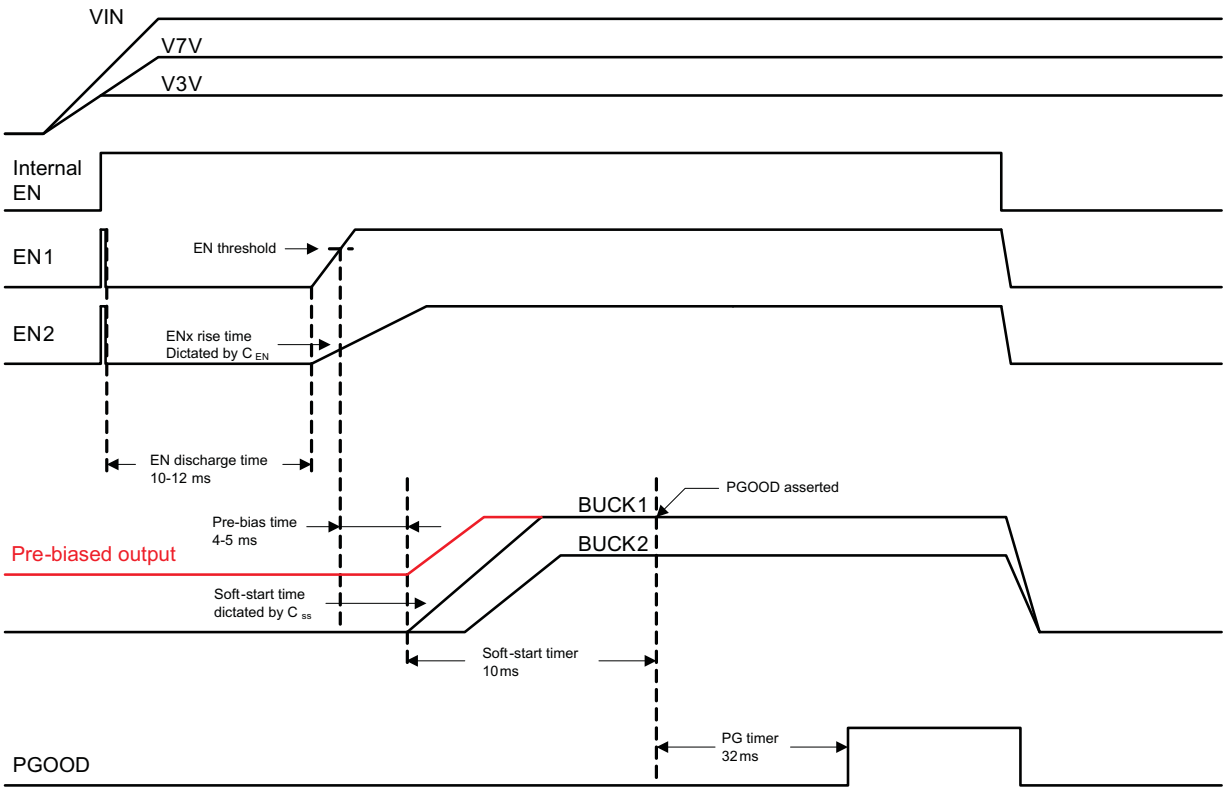


Figure 20. Startup Sequence of Dual Bucks

Soft-Start Time

The device has an internal pull-up current source of 5 µA that charges an external soft-start capacitor to implement a slow start time. Equation 2 shows how to select a soft-start capacitor based on an expected slow start time. The voltage reference (V_{REF}) is 0.8 V and the soft-start charge current (I_{SS}) is 5 µA. The soft-start circuit requires 1 nF per around 160 µs to be connected at the SS pin. A 0.8-ms soft-start time is implemented for all converters fitting 4.7 nF to the relevant SS pin.

$$T_{ss}(ms) = V_{REF}(V) \bullet \left(\frac{C_{ss}(nF)}{I_{ss}(\mu A)} \right) \quad (2)$$

The Power Good circuit for the bucks has a 10-ms watchdog. Therefore the soft-start time should be lower than this value. It is recommended not to exceed 5 ms.

Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. In order to improve efficiency at light load, start with a value close to 40 kΩ for the R1 resistor and use Equation 3 to calculate R2.

$$R2 = R1 \cdot \left(\frac{0.8V}{V_O - 0.8V} \right) \quad (3)$$

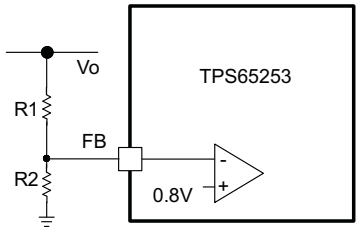


Figure 21. Voltage Divider Circuit

Loop Compensation

TPS65253 is a current mode control DC/DC converter. The error amplifier is a transconductance of 130 µA/V. A typical compensation circuit could be type II (R_c and C_c) to have a phase margin above 45°, or type III (R_c and C_c and C_{ff} to improve the converter transient response. Optional C_{Roll} adds a high frequency pole to attenuate high-frequency noise when needed. It may also prevent noise coupling from other rails if there is possibility of cross coupling in between rails when layout is very compact.

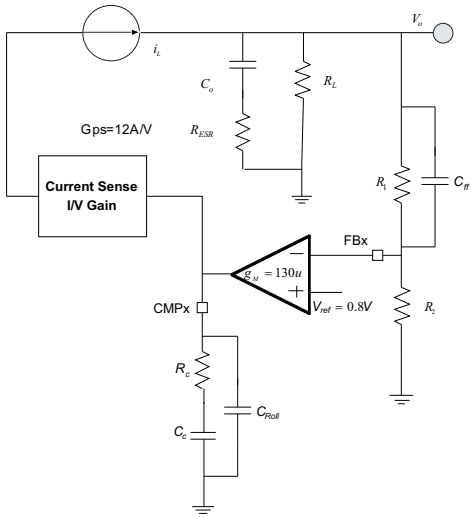


Figure 22. Loop Compensation Scheme

To calculate the external compensation components follow the following steps:

	TYPE II CIRCUIT	TYPE III CIRCUIT
Select switching frequency that is appropriate for application depending on L, C sizes, output ripple, EMI concerns and etc. Switching frequencies around 500 kHz yield best trade off between performance and cost. When using smaller L and C, switching frequency can be increased. To optimize efficiency, switching frequency can be lowered.		Use type III circuit for switching frequencies higher than 500 kHz.
Select cross over frequency (f_c) to be at least 1/5 to 1/10 of switching frequency (f_s).	Suggested $f_c = f_s/10$	Suggested $f_c = f_s/10$
Set and calculate R_c.	$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$	$R_C = \frac{2\pi \cdot fc \cdot Vo \cdot Co}{g_M \cdot Vref \cdot gm_{ps}}$
Calculate C_c by placing a compensation zero at or before the converter dominant pole $fp = \frac{1}{C_O \cdot R_L \cdot 2\pi}$	$C_c = \frac{R_L \cdot Co}{R_c}$	$C_c = \frac{R_L \cdot Co}{R_c}$
Add C_{Roll} if needed to remove large signal coupling to high impedance CMP node. Make sure that $fp_{Roll} = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_{Roll}}$ is at least twice the cross over frequency.	$C_{Roll} = \frac{\mathrm{Re}sr \cdot Co}{R_C}$	$C_{Roll} = \frac{\mathrm{Re}sr \cdot Co}{R_C}$
Calculate C_{ff} compensation zero at low frequency to boost the phase margin at the crossover frequency. Make sure that the zero frequency (fz_{ff}) is smaller than equivalent soft-start frequency ($1/T_{ss}$).	NA	$C_{ff} = \frac{1}{2 \cdot \pi \cdot fz_{ff} \cdot R_1}$

Slope Compensation

The device has a built-in slope compensation ramp. The slope compensation can prevent sub harmonic oscillations in peak current mode control.

Input Capacitor

Use at least 10-µF X7R/X5R ceramic capacitors at the input of the converter inputs. These capacitors should be connected as close as physically possible to the input pins of the converters.

Bootstrap Capacitor

The device has two integrated boot regulators and requires a small ceramic capacitor between the BST and LX pins to provide the gate drive voltage for the high side MOSFET. The value of the ceramic capacitor should be 0.047 µF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

Power Good

The PGOOD pin is an open drain output. The PGOOD pin is pulled low when any buck converter is pulled below 85% of the nominal output voltage. The PGOOD is pulled up when both buck converters' outputs are more than 90% of its nominal output voltage.

The default reset time is 32 ms. The polarity of the PGOOD is active high.

Current Limit Protection

The TPS65253 current limit trip is set by the following formula for Buck 1:

$$I_{LIM1}(A) = \frac{252}{R_{LIM1}(k\Omega)} + 0.6 \quad (4)$$

and for Buck 2:

$$I_{LIM2}(A) = \frac{236}{R_{LIM2}(k\Omega)} + 0.56 \quad (5)$$

All converters operate in hiccup mode: Once an over-current lasting more than 12 ms is sensed in any of the converters, they will shut down for 20 ms and then the start-up sequencing will be tried again. If the overload has been removed, the converter will ramp up and operate normally. If this is not the case the converter will see another over-current event and shuts-down again repeating the cycle (hiccup) until the failure is cleared.

If an overload condition lasts for less than 12 ms, only the relevant converter affected will shut-down and re-start and no global hiccup mode will occur.

Overvoltage Transient Protection

The device incorporates an overvoltage transient protection (OVP) circuit to minimize voltage overshoot. The OVP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVTP threshold which is 109% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the FB voltage drops lower than the OVTP threshold which is 107%, the high side MOSFET is allowed to turn on the next clock cycle.

Low Power Mode Operation

By pulling high the Low_P pin all converters will operate in pulse-skipping mode, greatly reducing the overall power consumption at light and no load conditions. Although each buck converter has a skip comparator that makes sure regulation is not lost when a heavy load is applied and low power mode is enabled, system design needs to make sure that the LP pin is pulled low for continuous loading in excess of 100 mA.

When low power is implemented, the peak inductor current used to charge the output capacitor is:

$$I_{LIMIT} = 0.25 \bullet T_{SLEEP\_CLK} \bullet \frac{V_{IN} - V_{OUT}}{L} \quad (6)$$

Where T_{SLEEP_CLK} is half of the converter switching period, $2/f_{SW}$.

The size of the additional ripple added to the output is:

$$\Delta V_{OUT} = \frac{1}{C} \bullet \left(\frac{L \bullet I_{LIMIT}^{2}}{2} \bullet \frac{V_{IN}}{V_{OUT} \bullet (V_{IN} - V_{OUT})} - \frac{I_{LOAD}}{f_{SLEEP\_CLK}} \right) \quad (7)$$

And the peak output voltage during low power operation is (see Figure 23):

$$V_{OUT\_PK} = V_{OUT} + \frac{\Delta V_{OUT}}{2} \quad (8)$$

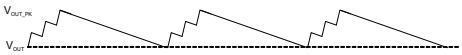


Figure 23. Peak Output Voltage During Low Power Operation

Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 160°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. Once the die temperature decreases below 140°C, the device reinitiates the power up sequence. The thermal shutdown hysteresis is 20°C.

3.3-V and 6.5 LDO Regulators

The following ceramic capacitor (X7R/X5R) should be connected as close as possible to the described pins:

- 4.7 µF to 10 µF for V7V pin 21
- 3.3 µF or larger for V3V pin 229

Layout Recommendation

Layout is a critical portion of PMIC designs.

- Place tracing for output voltage and LX on the top layer and an inner power plane for VIN.
- For best thermal performance, pins 25, 26, 27, and 28 should be connected to GND on the top PCB layer as well as inner GND plane by through-hole connections.
- The top layer ground area should be connected to the internal ground layer(s) using vias at the input bypass capacitor, the output filter capacitor and directly under the TPS65253 device to provide a thermal path from the PowerPad land to ground.
- For operation at full rated load, the top side ground area together with the internal ground plane, must provide adequate heat dissipating area.
- There are several signals paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. To help eliminate these problems, the VIN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with X5R or X7R dielectric. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the ground connections. Since the LX connection is the switching node, the output inductor should be located close to the LX pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling.
- The output filter capacitor ground should use the same power ground trace as the VIN input bypass capacitor. Try to minimize this conductor length while maintaining adequate width.
- The compensation should be as close as possible to the CMPx pins. The CMPx and ROSC pins are sensitive to noise so the components associated to these pins should be located as close as possible to the IC and routed with minimal lengths of trace.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS65253RHDR	Active	Production	VQFN (RHD) | 28	3000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65253
TPS65253RHDT	Active	Production	VQFN (RHD) | 28	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS 65253

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

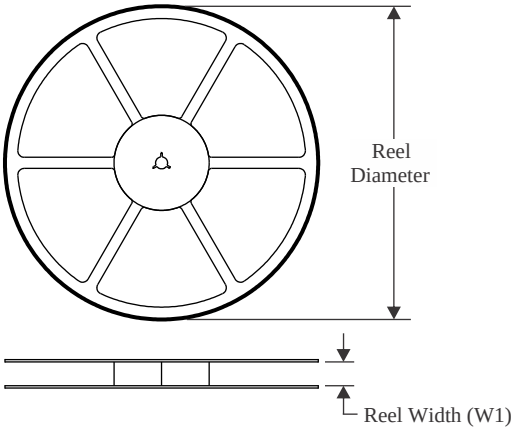
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

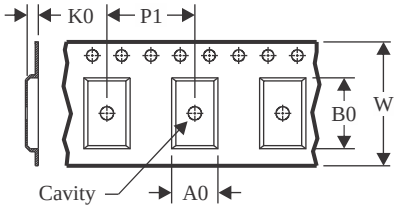
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

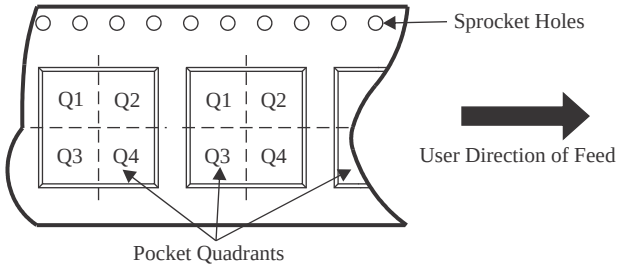


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

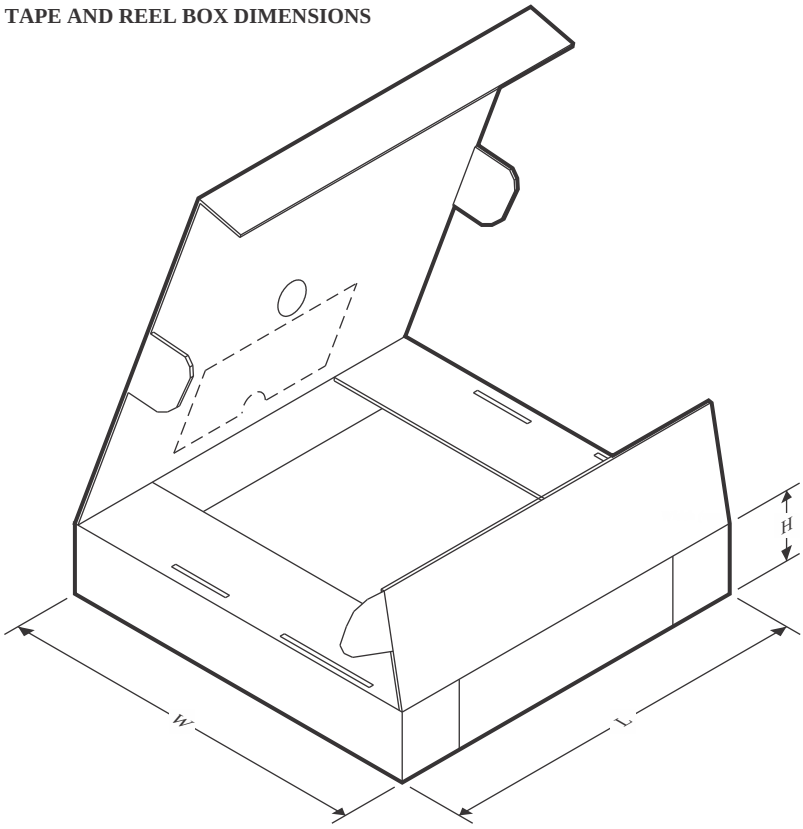
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65253RHDR	VQFN	RHD	28	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS65253RHDT	VQFN	RHD	28	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65253RHDR	VQFN	RHD	28	3000	346.0	346.0	33.0
TPS65253RHDT	VQFN	RHD	28	250	210.0	185.0	35.0

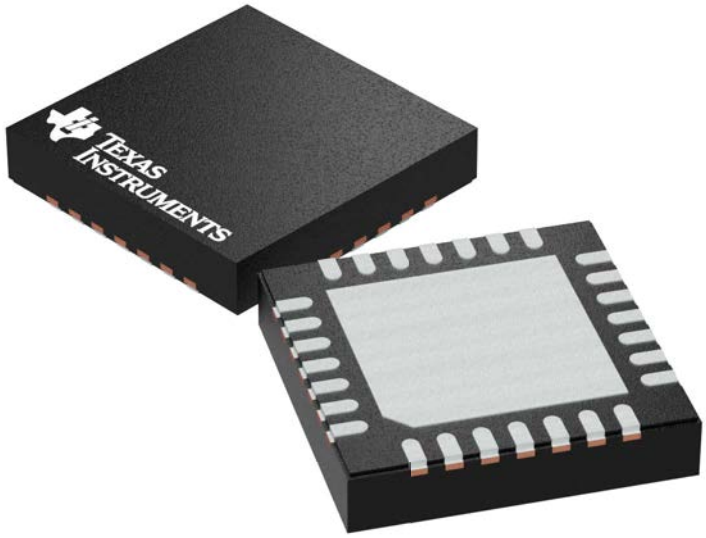
GENERIC PACKAGE VIEW

RHD 28

VQFN - 1 mm max height

5 x 5 mm, 0.5 mm pitch

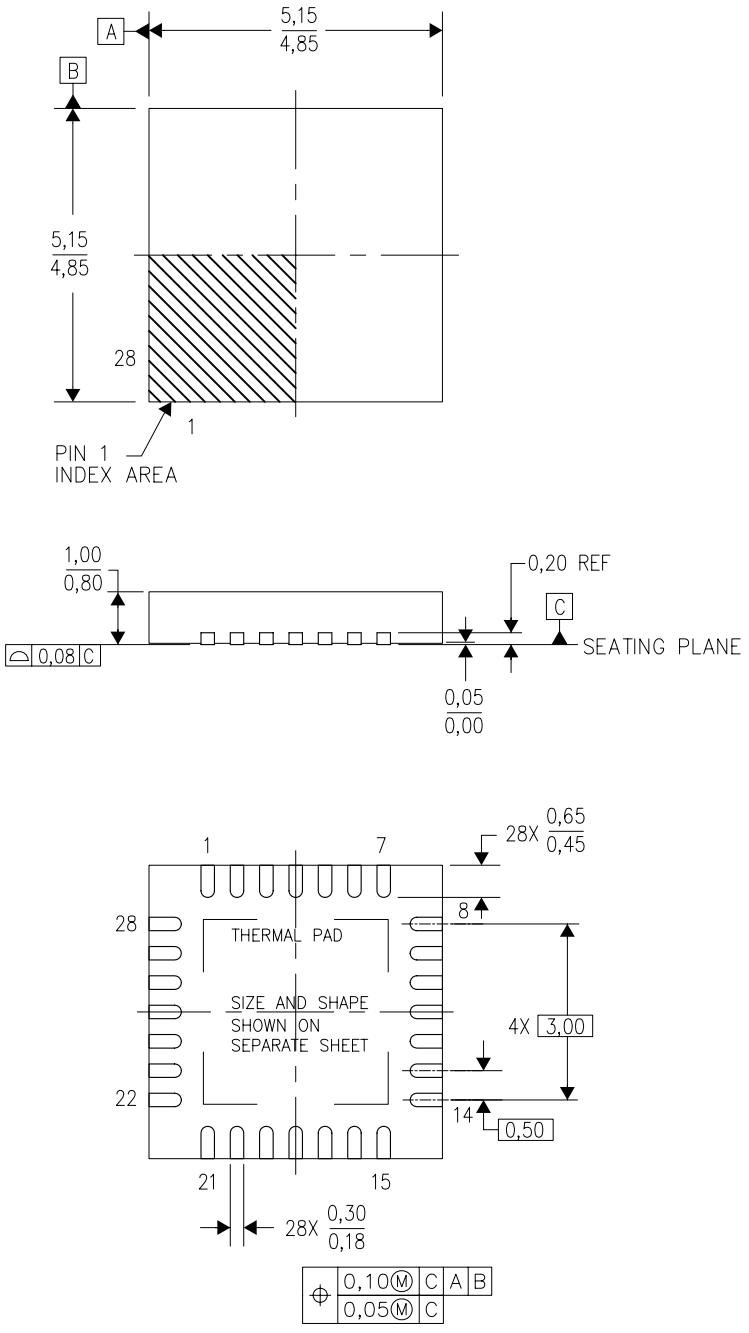
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204400/G

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



4204400/F 09/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

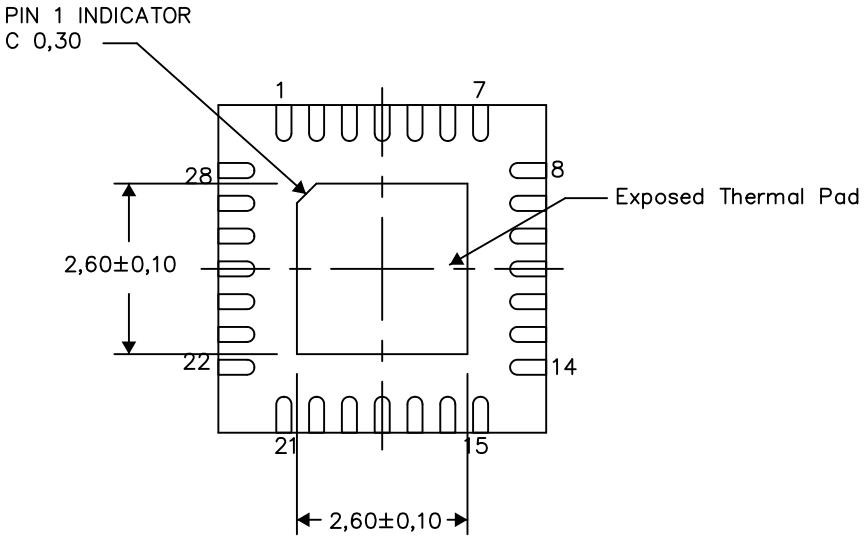
RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



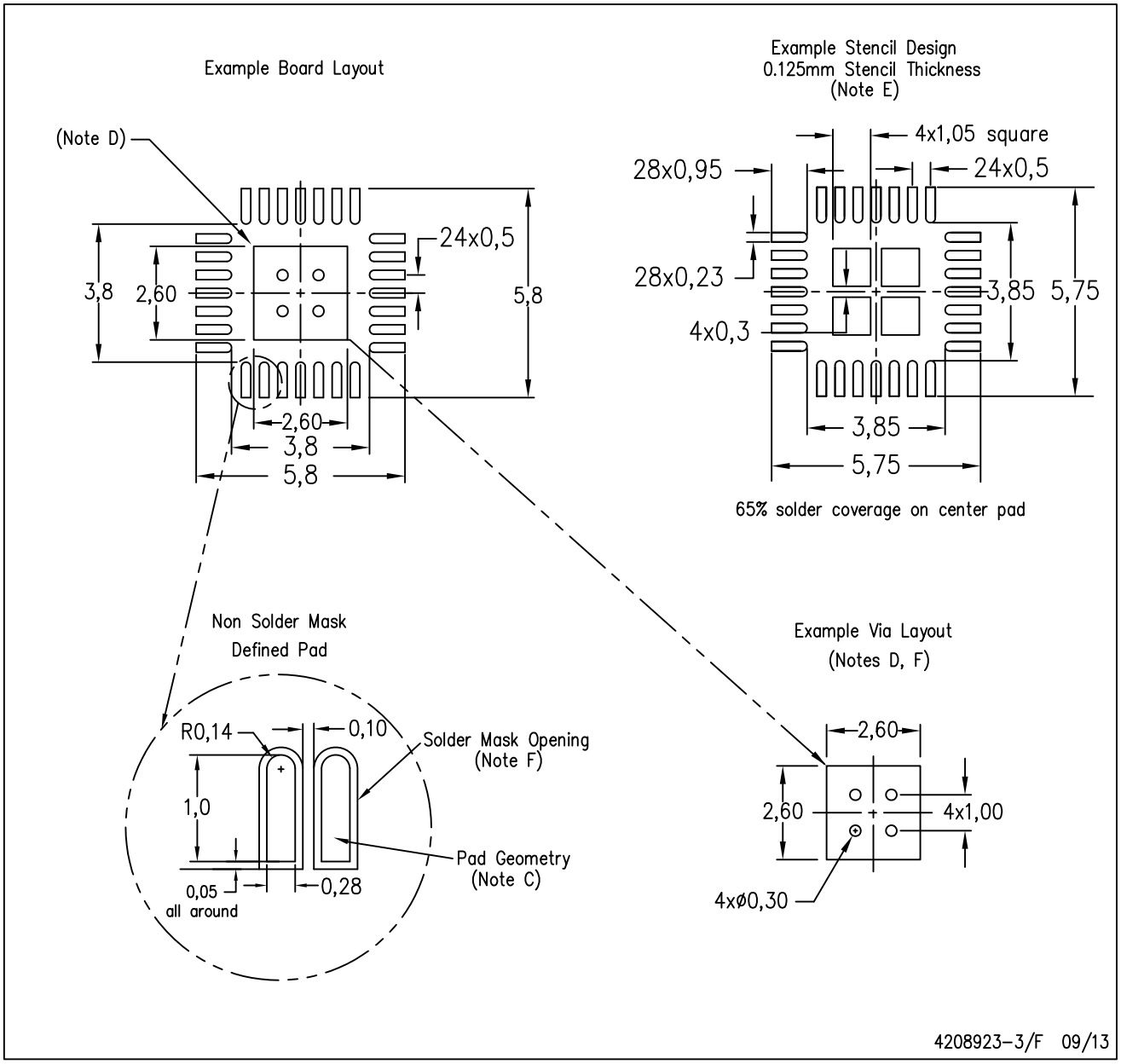
Bottom View

Exposed Thermal Pad Dimensions

4206358–3/L 05/15

NOTE: All linear dimensions are in millimeters

RHD (S–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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