



Is Now Part of

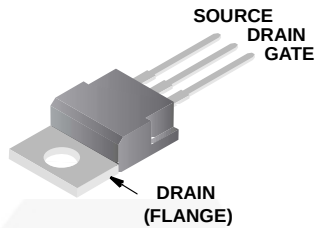
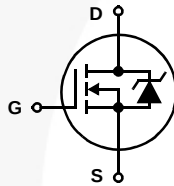


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N-Channel Logic Level UltraFET Power MOSFET
60 V, 33 A, 35 mΩ
Packaging
JEDEC TO-220AB

Symbol

Features

- Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.030\Omega$, $V_{GS} = 10V$
 - $r_{DS(ON)} = 0.035\Omega$, $V_{GS} = 5V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER™ Electrical Models
 - Spice and SABER Thermal Impedance Models
 - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs R_{GS} Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF76423P3	TO-220AB	76423P

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

	HUF76423P3	UNITS
Drain to Source Voltage (Note 1)	60	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	60	V
Gate to Source Voltage	± 16	V
Drain Current		
Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 5V$)	33	A
Continuous ($T_C = 25^\circ\text{C}$, $V_{GS} = 10V$) (Figure 2)	35	A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 5V$)	23	A
Continuous ($T_C = 100^\circ\text{C}$, $V_{GS} = 4.5V$) (Figure 2)	22	A
Pulsed Drain Current	Figure 4	
Pulsed Avalanche Rating	Figures 6, 17, 18	
Power Dissipation	85	W
Derate Above 25°C	0.567	W/ $^\circ\text{C}$
Operating and Storage Temperature	-55 to 175	$^\circ\text{C}$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief TB334.	260	$^\circ\text{C}$

NOTES:

1. $T_J = 25^\circ\text{C}$ to 150°C .

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Product reliability information can be found at <http://www.fairchildsemi.com/products/discrete/reliability/index.html>

For severe environments, see our Automotive HUFA series.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

HUF76423P3

Electrical Specifications $T_C = 25^{\circ}\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 12)	60	-	-	V	
		I _D = 250μA, V _{GS} = 0V , T _C = -40 ⁰ C (Figure 12)	55	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 55V, V _{GS} = 0V	-	-	1	μA	
		V _{DS} = 50V, V _{GS} = 0V, T _C = 150 ⁰ C	-	-	250	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±16V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 11)	1	-	3	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 35A, V _{GS} = 10V (Figures 9, 10)	-	0.025	0.030	Ω	
		I _D = 23A, V _{GS} = 5V (Figure 9)	-	0.029	0.035	Ω	
		I _D = 22A, V _{GS} = 4.5V (Figure 9)	-	0.032	0.038	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R _{θJC}	TO-220	-	-	1.76	⁰ C/W	
Thermal Resistance Junction to Ambient	R _{θJA}		-	-	62	⁰ C/W	
SWITCHING SPECIFICATIONS (V _{GS} = 4.5V)							
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D = 22A V _{GS} = 4.5V, R _{GS} = 10Ω (Figures 15, 21, 22)	-	-	245	ns	
Turn-On Delay Time	t _{d(ON)}		-	12	-	ns	
Rise Time	t _r		-	147	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	32	-	ns	
Fall Time	t _f		-	50	-	ns	
Turn-Off Time	t _{OFF}		-	-	125	ns	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 30V, I _D = 35A V _{GS} = 10V, R _{GS} = 10Ω (Figures 16, 21, 22)	-	-	140	ns	
Turn-On Delay Time	t _{d(ON)}		-	7	-	ns	
Rise Time	t _r		-	85	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	47	-	ns	
Fall Time	t _f		-	76	-	ns	
Turn-Off Time	t _{OFF}		-	-	185	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 10V	V _{DD} = 30V, I _D = 23A, I _{g(REF)} = 1.0mA (Figures 14, 19, 20)	-	28	34	nC
Gate Charge at 5V	Q _{g(5)}	V _{GS} = 0V to 5V		-	15	18	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 1V		-	1.2	1.5	nC
Gate to Source Gate Charge	Q _{gs}			-	3.5	-	nC
Gate to Drain “Miller” Charge	Q _{gd}			-	7	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 13)	-	1060	-	pF	
Output Capacitance	C _{OSS}		-	315	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	65	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 23\text{A}$	-	-	1.25	V
		$I_{SD} = 11.5\text{A}$	-	-	1.0	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 23\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	80	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 23\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	205	nC

Typical Performance Curves

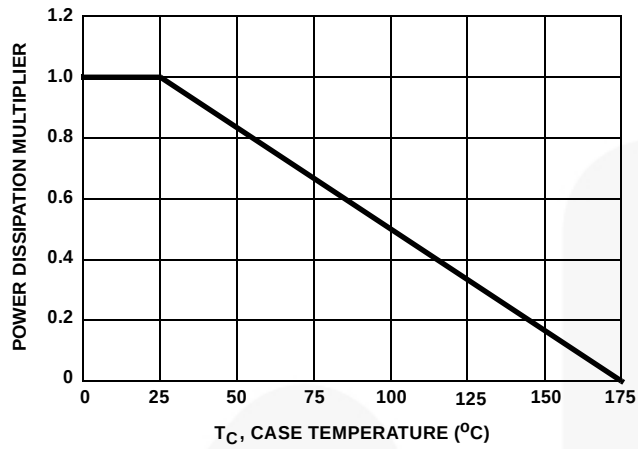


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

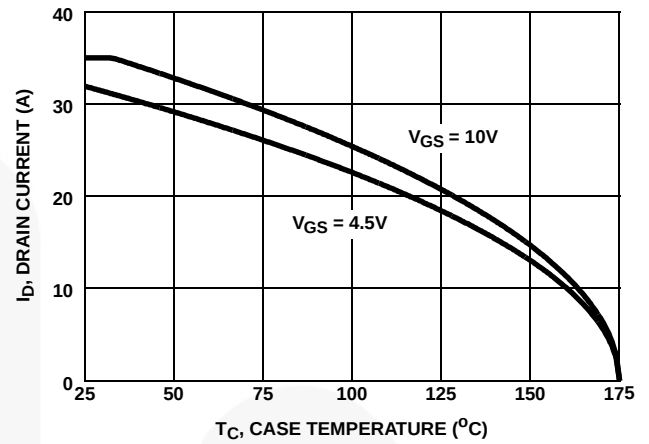


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

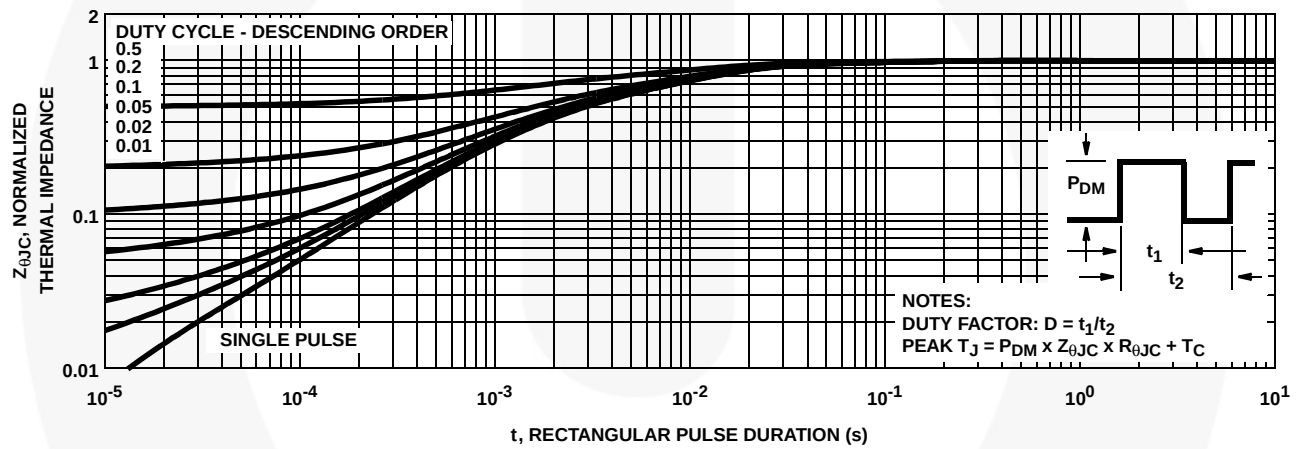


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

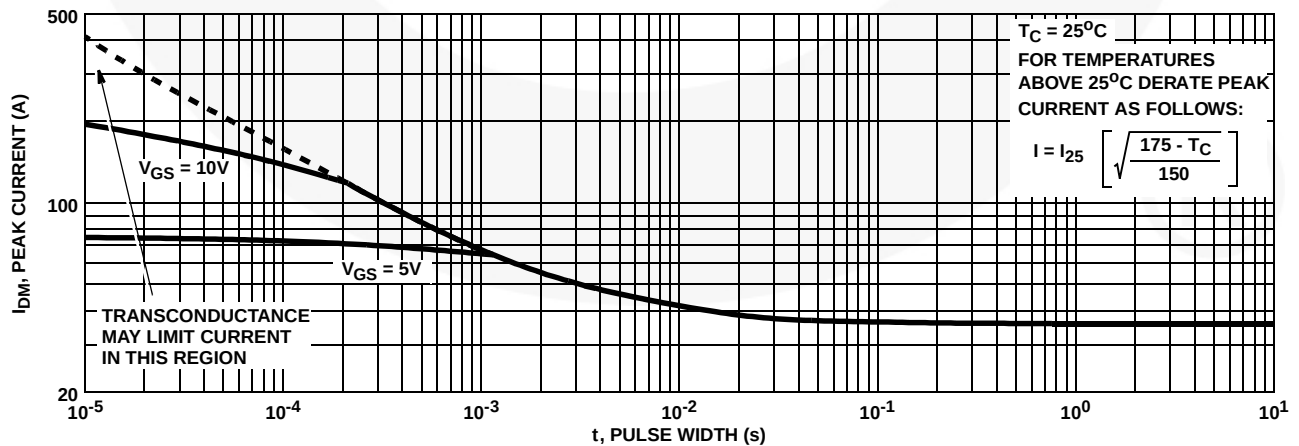


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

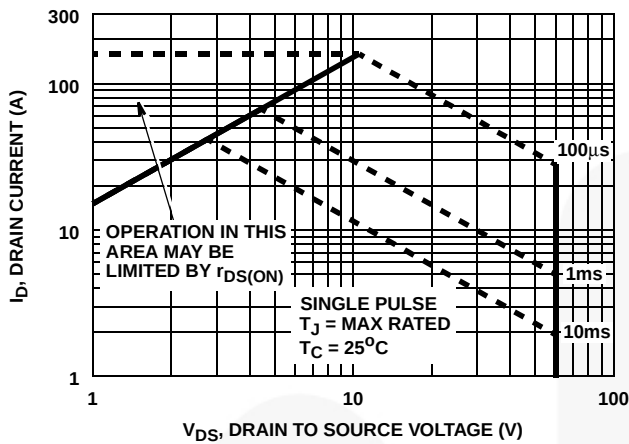
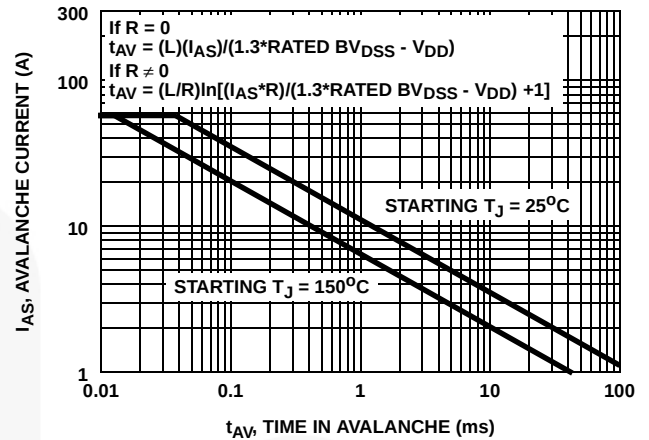


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

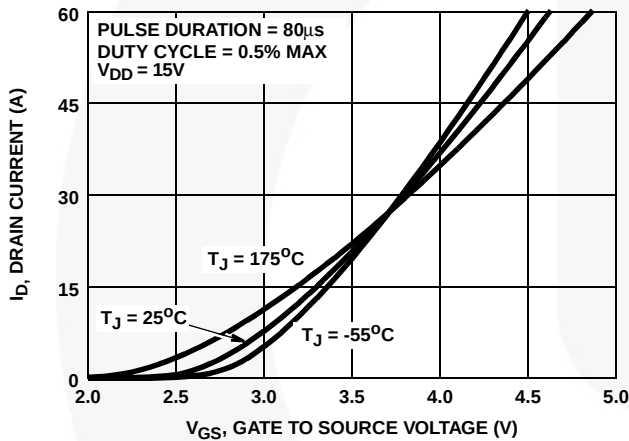


FIGURE 7. TRANSFER CHARACTERISTICS

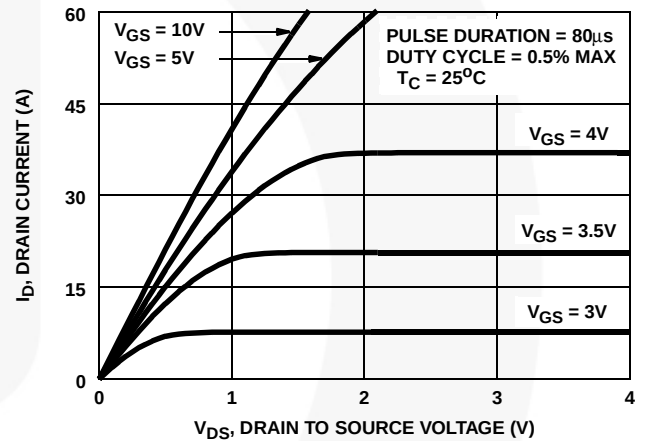


FIGURE 8. SATURATION CHARACTERISTICS

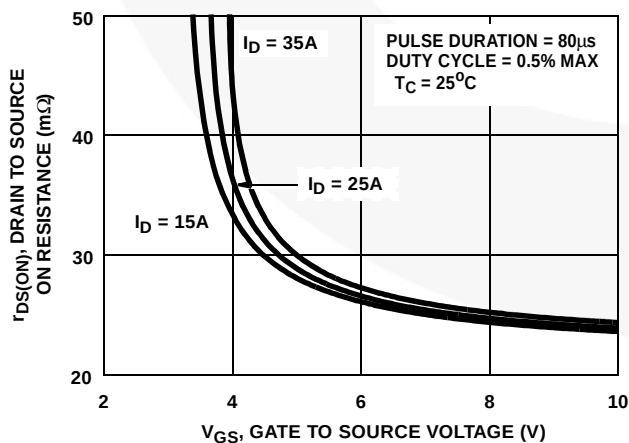


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs. GATE VOLTAGE AND DRAIN CURRENT

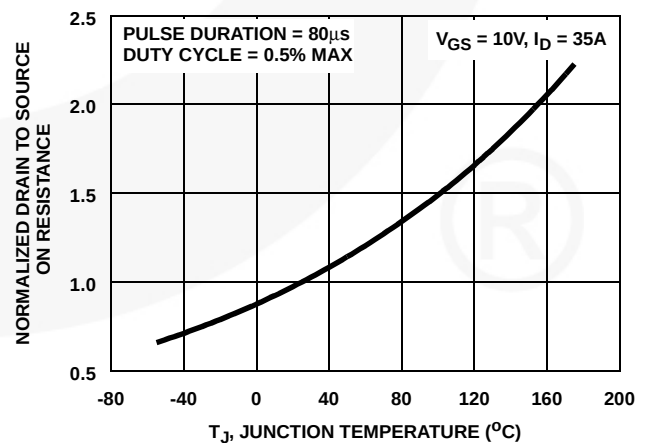


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs. JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

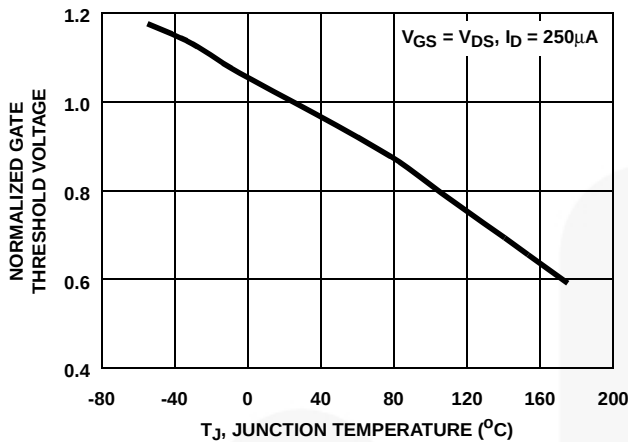


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

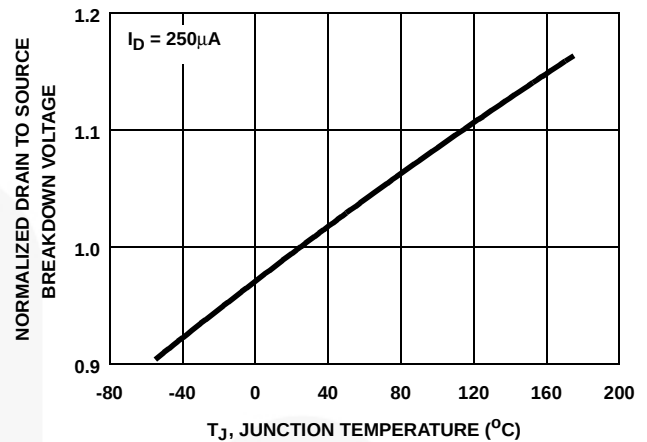


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

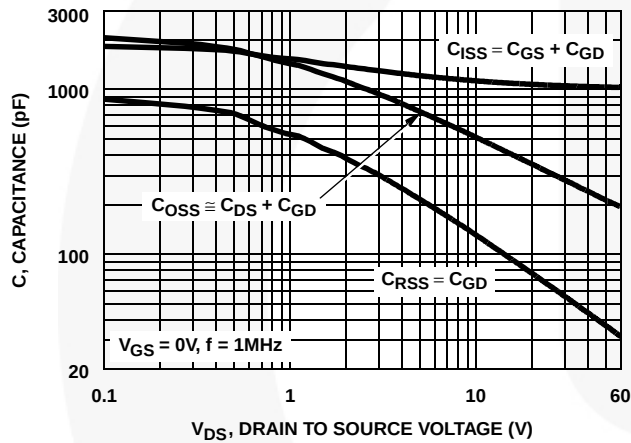
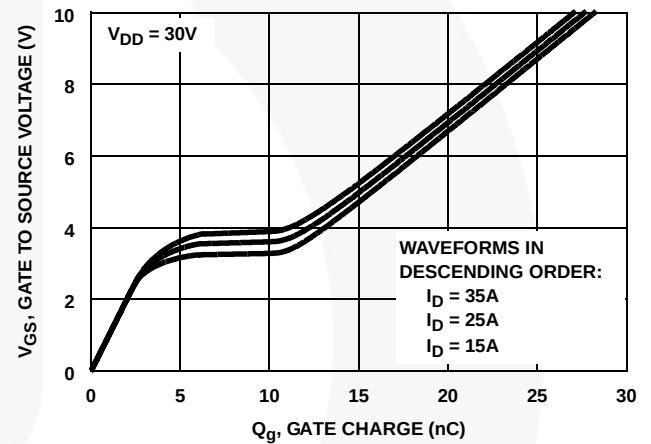


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

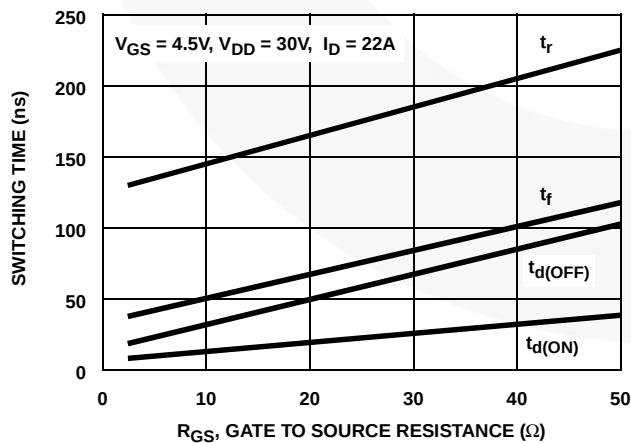


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

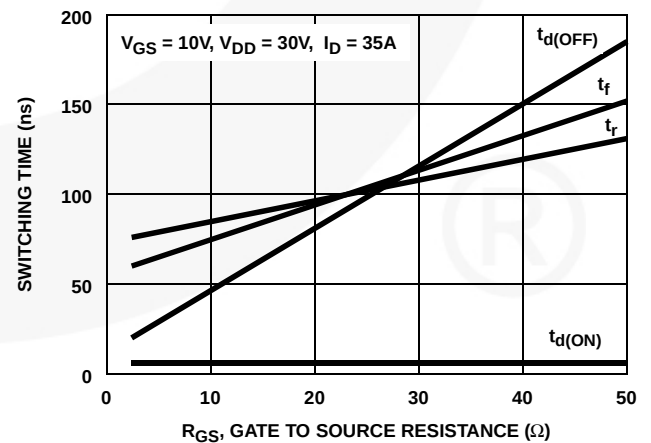


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

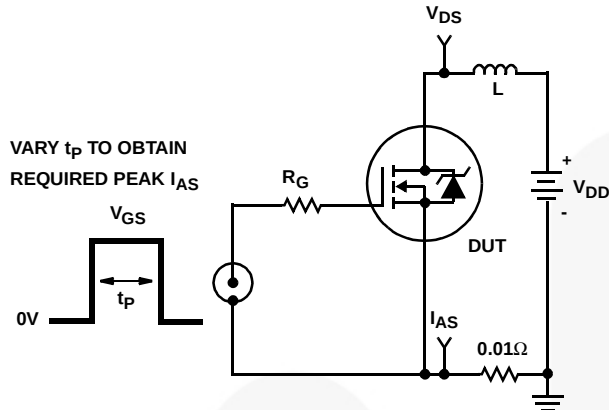


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

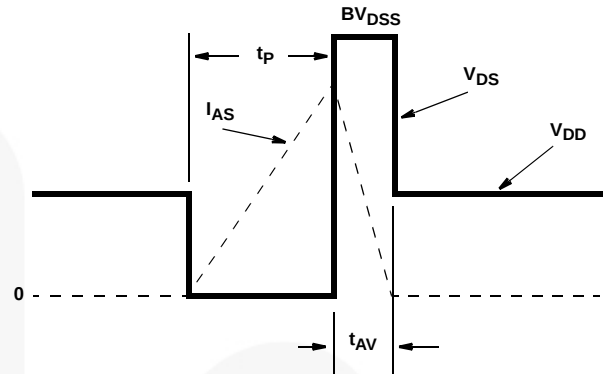


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

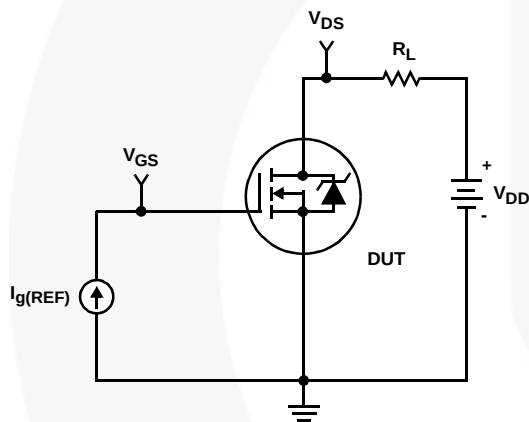


FIGURE 19. GATE CHARGE TEST CIRCUIT

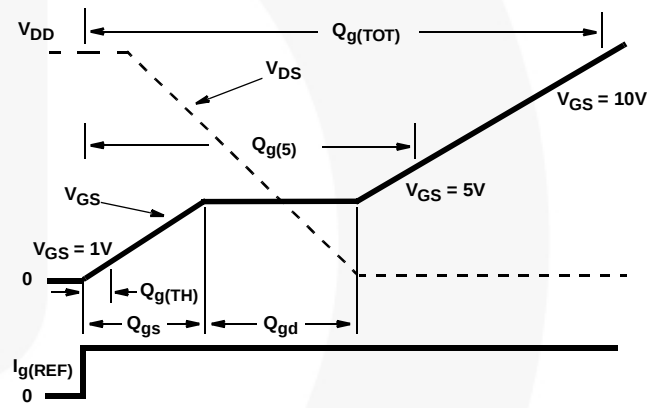


FIGURE 20. GATE CHARGE WAVEFORMS

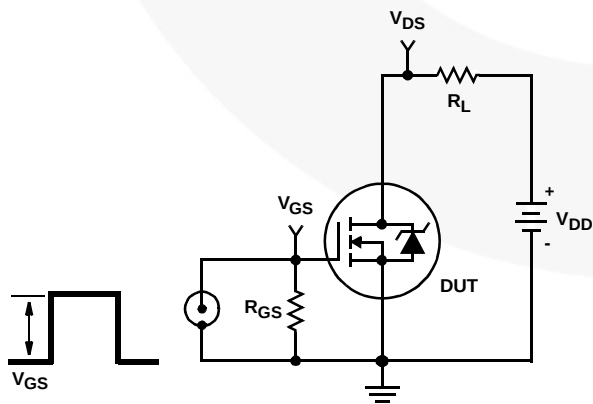


FIGURE 21. SWITCHING TIME TEST CIRCUIT

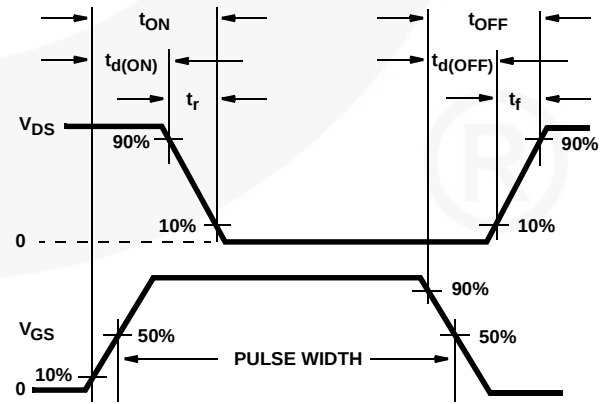


FIGURE 22. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

.SUBCKT HUF76423 2 1 3 ; rev 7 September 1999

CA 12 8 1.46e-9
 CB 15 14 1.46e-9
 CIN 6 8 1.0e-9

DBODY 7 5 DBODYMOD
 DBREAK 5 11 DBREAKMOD
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 66.0
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 6 10 6 8 1
 EVTHRES 6 21 19 8 1
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
 LGATE 1 9 5.5e-9
 LSOURCE 3 7 4.4e-9

MMED 16 6 8 8 MMEDMOD
 MSTRO 16 6 8 8 MSTROMOD
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
 RDRAIN 50 16 RDRAINMOD 7.0e-3
 RGATE 9 20 3.6
 RLDRAIN 2 5 10
 RLGATE 1 9 55
 RLSOURCE 3 7 44
 RSLC1 5 51 RSLCMOD 1e-6
 RSLC2 5 50 1e3
 RSOURCE 8 7 RSOURCEMOD 1.45e-2
 RVTHRES 22 8 RVTHRESMOD 1
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

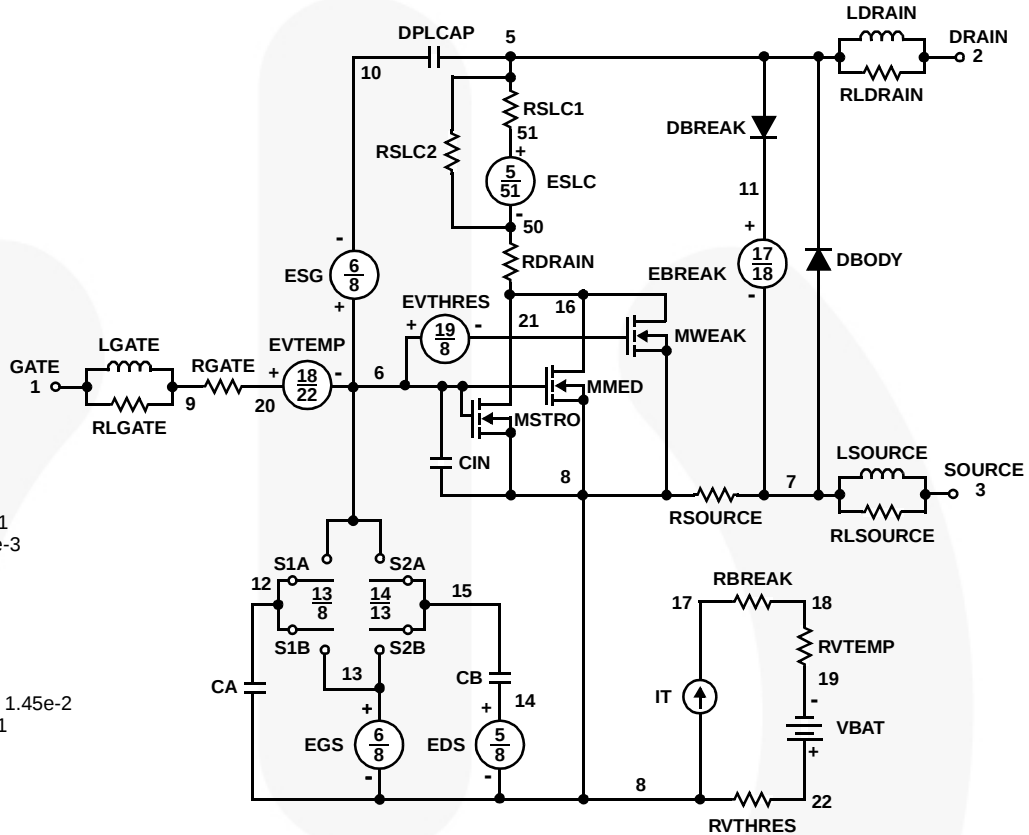
ESLC 51 50 VALUE={ (V(5,51)/ABS(V(5,51))) * (PWR(V(5,51)/(1e-6*100),3.5)) }

.MODEL DBODYMOD D (IS = 6.3e-13 RS = 6.8e-3 TRS1 = 1e-3 TRS2 = 1e-6 XTI = 4.3 CJO = 1.28e-9 TT = 5.1e-8 M = 0.5)
 .MODEL DBREAKMOD D (RS = 2.9e-1 TRS1 = 1e-4 TRS2 = 0)
 .MODEL DPLCAPMOD D (CJO = 9.5e-1 OIS = 1e-3 ON = 10 M = 0.82)
 .MODEL MMEDMOD NMOS (VTO = 2.10 KP = 6 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.6)
 .MODEL MSTROMOD NMOS (VTO = 2.45 KP = 60.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
 .MODEL MWEAKMOD NMOS (VTO = 1.79 KP = 0.13 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 36 RS = 0.1)
 .MODEL RBREAKMOD RES (TC1 = 1.2e-3 TC2 = -5e-7)
 .MODEL RDRAINMOD RES (TC1 = 1.3e-2 TC2 = 3.1e-5)
 .MODEL RSLCMOD RES (TC1 = 5.5e-3 TC2 = 7e-6)
 .MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
 .MODEL RVTHRESMOD RES (TC1 = -1.8e-3 TC2 = -5.8e-6)
 .MODEL RVTEMPMOD RES (TC1 = -1.7e-3 TC2 = 8e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.8 VOFF = -2.8)
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.8 VOFF = -4.8)
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.6 VOFF = 0.5)
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -0.6)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SPICE Thermal Model

REV 1 September 1999

HUF76423T

CTHERM1 th 6 1.40e-3
 CHERM2 6 5 8.30e-3
 CHERM3 5 4 7.00e-3
 CHERM4 4 3 3.20e-3
 CHERM5 3 2 1.50e-2
 CHERM6 2 tl 1.10

RHERM1 th 6 1.20e-2
 RHERM2 6 5 2.99e-2
 RHERM3 5 4 8.43e-2
 RHERM4 4 3 4.73e-1
 RHERM5 3 2 7.14e-1
 RHERM6 2 tl 9.47e-2

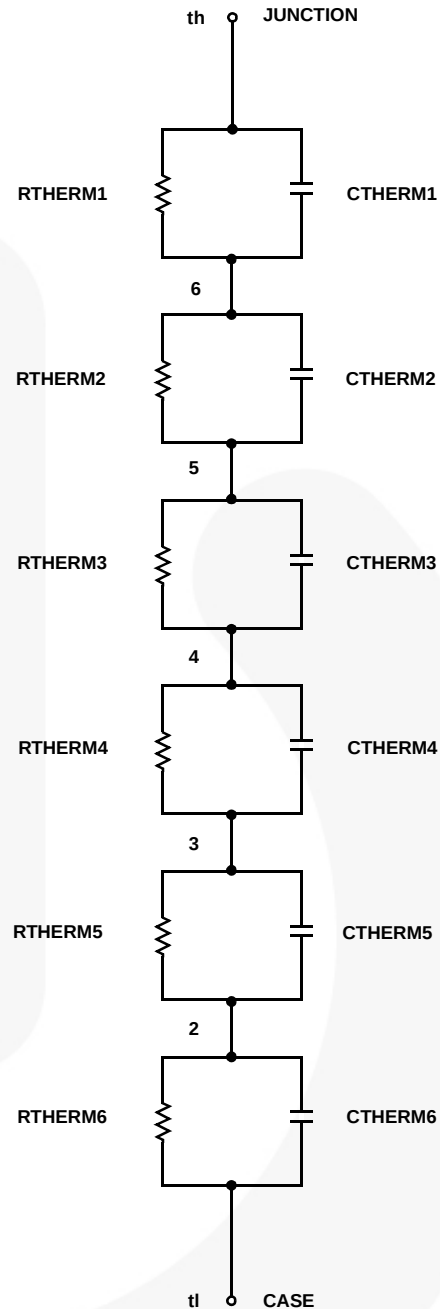
SABER Thermal Model

SABER thermal model HUF76423T

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  ctherm.ctherm2 6 5 = 8.30e-3
  ctherm.ctherm3 5 4 = 7.00e-3
  ctherm.ctherm4 4 3 = 3.20e-3
  ctherm.ctherm5 3 2 = 1.50e-2
  ctherm.ctherm6 2 tl = 1.10

  rtherm.rtherm1 th 6 = 1.20e-2
  rtherm.rtherm2 6 5 = 2.99e-2
  rtherm.rtherm3 5 4 = 8.43e-2
  rtherm.rtherm4 4 3 = 4.73e-1
  rtherm.rtherm5 3 2 = 7.14e-1
  rtherm.rtherm6 2 tl = 9.47e-2
}
  
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CorePOWER™	Green FPS™ e-Series™	Quiet Series™	TinyLogic®
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CTL™	GTO™	Saving our world, 1mW/W/kW at a time™	TinyPower™
Current Transfer Logic™	IntelliMAX™	SignalWise™	TinyPWM™
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EfficientMax™	MICROCOUPLER™	SPM®	TRUECURRENT®*
ESBC™	MicroFET™	STEALTH™	µSerDes™
	MicroPak™	SuperFET®	
Fairchild®	MicroPak2™	SuperSOT™-3	UHC®
Fairchild Semiconductor®	MillerDrive™	SuperSOT™-6	Ultra FRFET™
FACT Quiet Series™	MotionMax™	SuperSOT™-8	UniFET™
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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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