

## P-channel 40 V, 0.0175 $\Omega$ typ.,36 A, STripFET™ F6 Power MOSFET in a DPAK package

Datasheet - production data

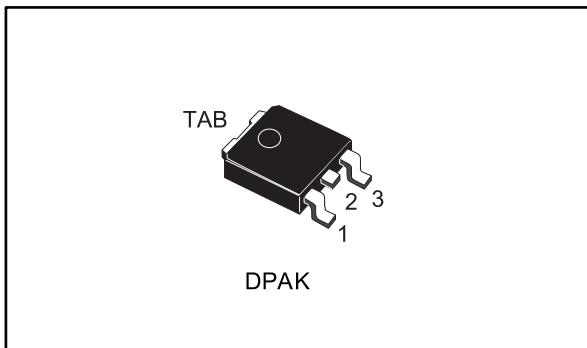
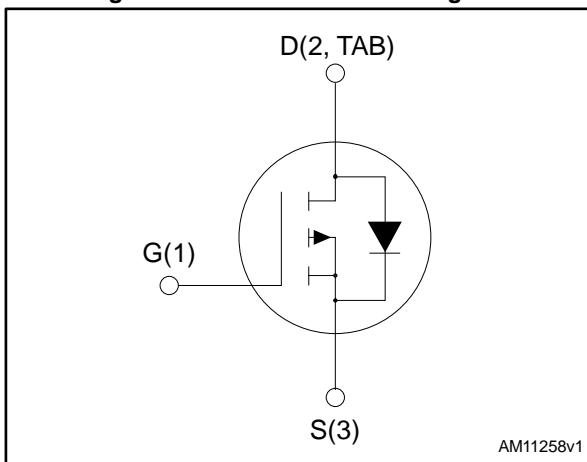


Figure 1: Internal schematic diagram



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max.	$I_D$	$P_{TOT}$
STD36P4LLF6	40 V	0.0205 $\Omega$	36 A	60 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low  $R_{DS(on)}$  in all packages.



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

Table 1: Device summary

Order code	Marking	Package	Packaging
STD36P4LLF6	36P4LLF6	DPAK	Tape and reel

## Contents

<b>1</b>	<b>Electrical ratings .....</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics .....</b>	<b>4</b>
2.1	Electrical characteristics (curves).....	6
<b>3</b>	<b>Test circuits .....</b>	<b>8</b>
<b>4</b>	<b>Package information .....</b>	<b>9</b>
4.1	DPAK (TO-252) type A2 package information.....	10
4.2	Packing information.....	13
<b>5</b>	<b>Revision history .....</b>	<b>15</b>

# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_c = 25^\circ\text{C}$	36	A
$I_D$	Drain current (continuous) at $T_c = 100^\circ\text{C}$	26	A
$I_{DM}^{(1)}$	Drain current (pulsed)	144	A
$P_{TOT}$	Total dissipation at $T_c = 25^\circ\text{C}$	60	W
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_j$	Maximum junction temperature	175	$^\circ\text{C}$

**Notes:**

<sup>(1)</sup> Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.5	$^\circ\text{C}/\text{W}$



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

## 2 Electrical characteristics

( $T_C = 25^\circ\text{C}$  unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$	40			V
$I_{\text{DSS}}$	Zero gate voltage Drain current	$V_{\text{GS}} = 0 \text{ V}$ , $V_{\text{DS}} = 40 \text{ V}$			1	$\mu\text{A}$
		$V_{\text{GS}} = 0 \text{ V}$ , $V_{\text{DS}} = 40 \text{ V}$ , $T_C = 125^\circ\text{C}$			10	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-body leakage current	$V_{\text{DS}} = 0 \text{ V}$ , $V_{\text{GS}} = \pm 20 \text{ V}$			$\pm 100$	nA
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_D = 250 \mu\text{A}$	1		2.5	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{\text{GS}} = 10 \text{ V}$ , $I_D = 18 \text{ A}$		0.0175	0.0205	$\Omega$
		$V_{\text{GS}} = 4.5 \text{ V}$ , $I_D = 18 \text{ A}$		0.024	0.029	

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{iss}}$	Input capacitance	$V_{\text{DS}} = 25 \text{ V}$ , $f = 1 \text{ MHz}$ , $V_{\text{GS}} = 0 \text{ V}$	-	2850	-	pF
$C_{\text{oss}}$	Output capacitance		-	270	-	pF
$C_{\text{rss}}$	Reverse transfer capacitance		-	180	-	pF
$Q_g$	Total gate charge	$V_{\text{DD}} = 20 \text{ V}$ , $I_D = 36 \text{ A}$ , $V_{\text{GS}} = 4.5 \text{ V}$ (see <a href="#">Figure 14: "Gate charge test circuit"</a> )	-	22	-	nC
$Q_{\text{gs}}$	Gate-source charge		-	9.4	-	nC
$Q_{\text{gd}}$	Gate-drain charge		-	7.3	-	nC
$R_G$	Gate input resistance	$I_D = 0 \text{ A}$ , gate DC bias = 0 V, $f = 1 \text{ MHz}$ , magnitude of alternative signal = 20 mV	-	1.4	-	$\Omega$

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d}(\text{on})}$	Turn-on delay time	$V_{\text{DD}} = 20 \text{ V}$ , $I_D = 18 \text{ A}$ $R_G = 4.7 \Omega$ , $V_{\text{GS}} = 10 \text{ V}$ (see <a href="#">Figure 13: "Switching times test circuit for resistive load"</a> )	-	43	-	ns
$t_r$	Rise time		-	47	-	ns
$t_{\text{d}(\text{off})}$	Turn-off-delay time		-	148	-	ns
$t_f$	Fall time		-	19	-	ns

 For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 18 \text{ A}$ $I_{SD} = 36 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 32 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <i>Figure 15: "Test circuit for inductive load switching and diode recovery times"</i> )	-		1.1	V
$t_{rr}$	Reverse recovery time		-	26		ns
$Q_{rr}$	Reverse recovery charge		-	21		nC
$I_{RRM}$	Reverse recovery current		-	1.7		A

**Notes:**

<sup>(1)</sup>Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

 For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

## 2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

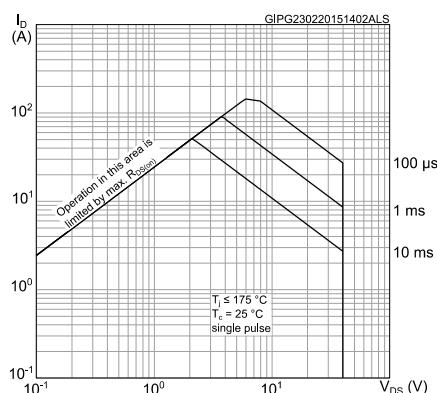


Figure 3: Thermal impedance

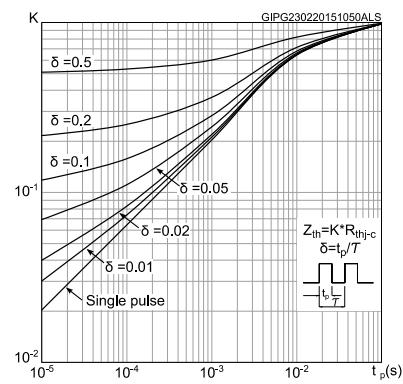


Figure 4: Output characteristics

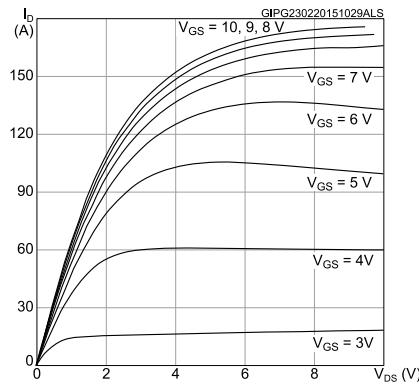


Figure 5: Transfer characteristics

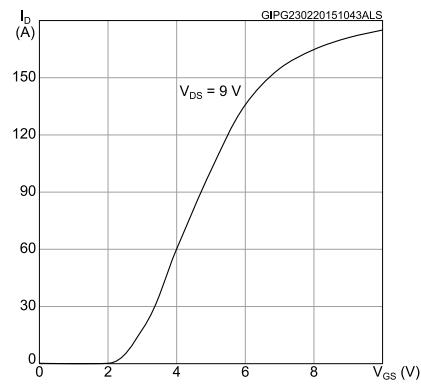


Figure 6: Normalized gate threshold voltage vs temperature

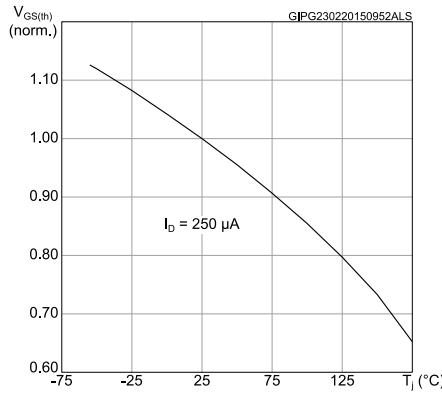


Figure 7: Normalized V(BR)DSS vs temperature

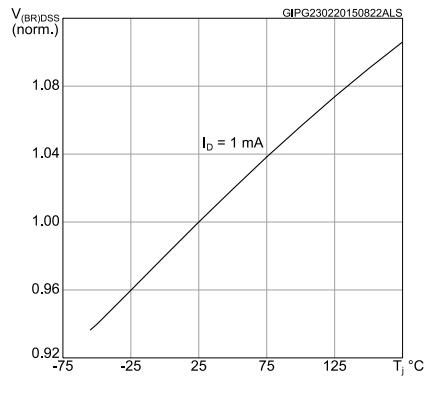


Figure 8: Static drain-source on-resistance

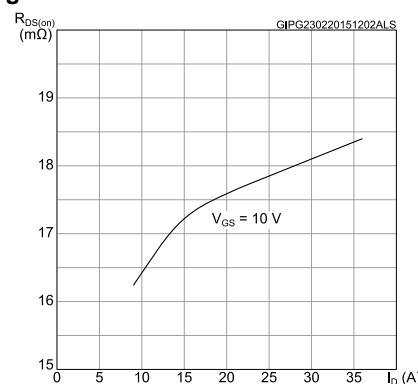


Figure 9: Normalized on-resistance vs. temperature

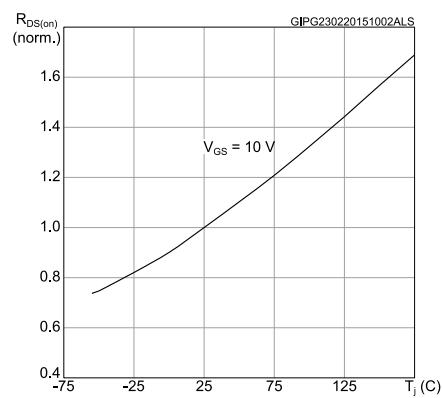


Figure 10: Gate charge vs gate-source voltage

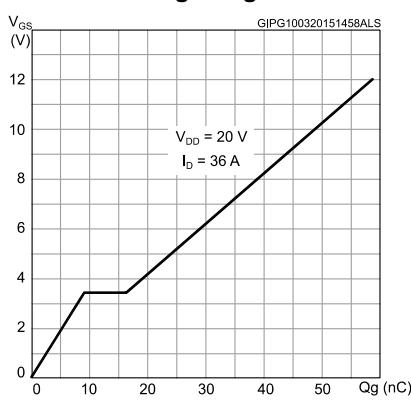


Figure 11: Capacitance variations voltage

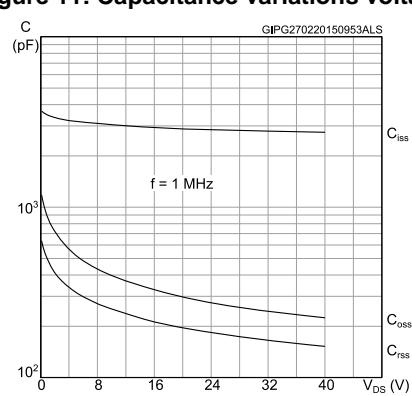
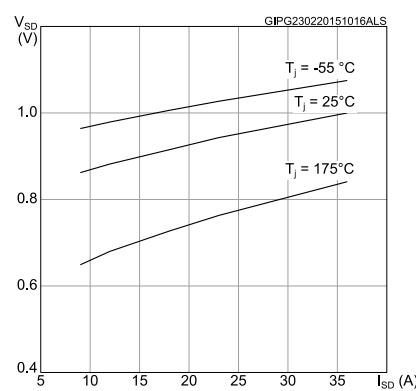


Figure 12: Source-drain diode forward characteristics



### 3 Test circuits

Figure 13: Switching times test circuit for resistive load

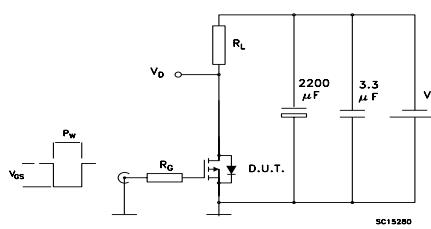


Figure 14: Gate charge test circuit

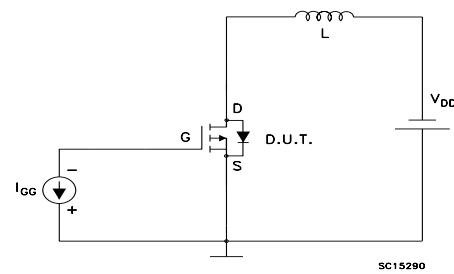
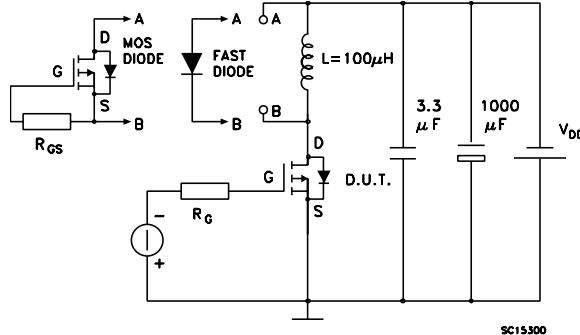


Figure 15: Test circuit for inductive load switching and diode recovery times



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

## 4.1 DPAK (TO-252) type A2 package information

Figure 16: DPAK (TO-252) type A2 package outline

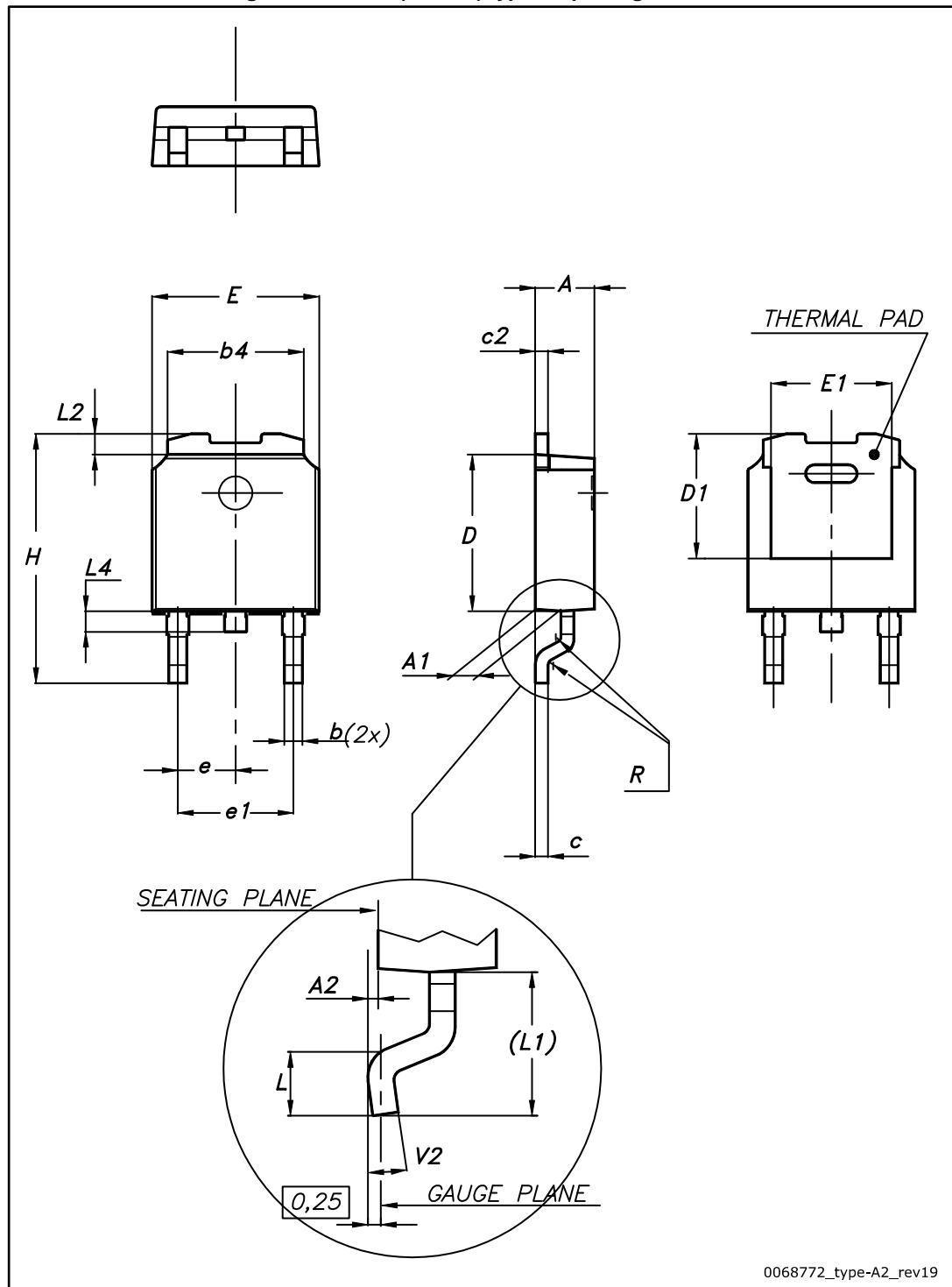
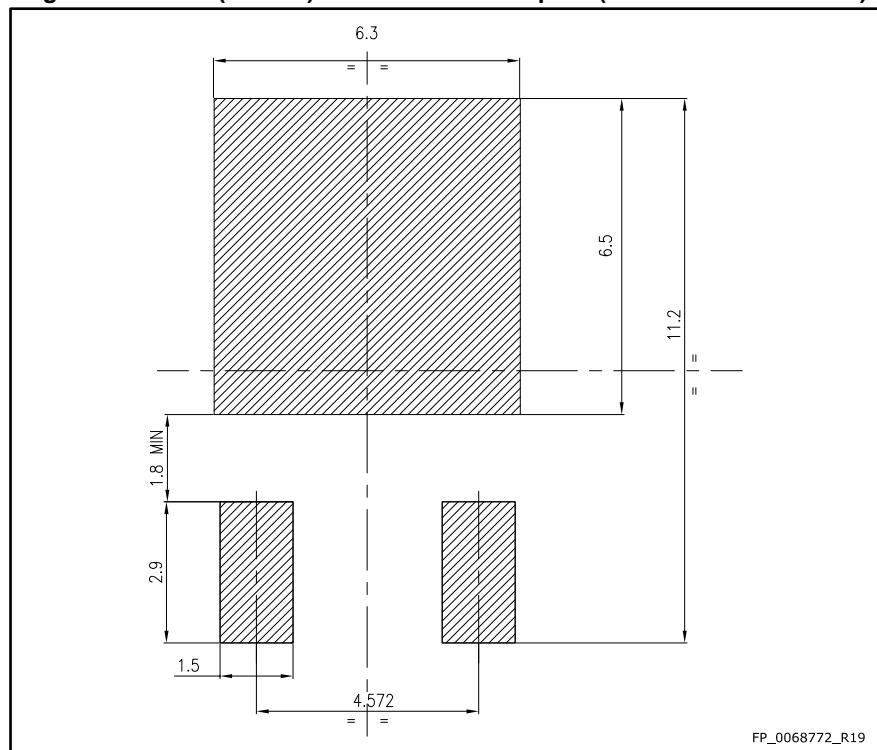


Table 8: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 17: DPAK (TO-252) recommended footprint (dimensions are in mm)



## 4.2 Packing information

Figure 18: Tape for DPAK (TO-252)

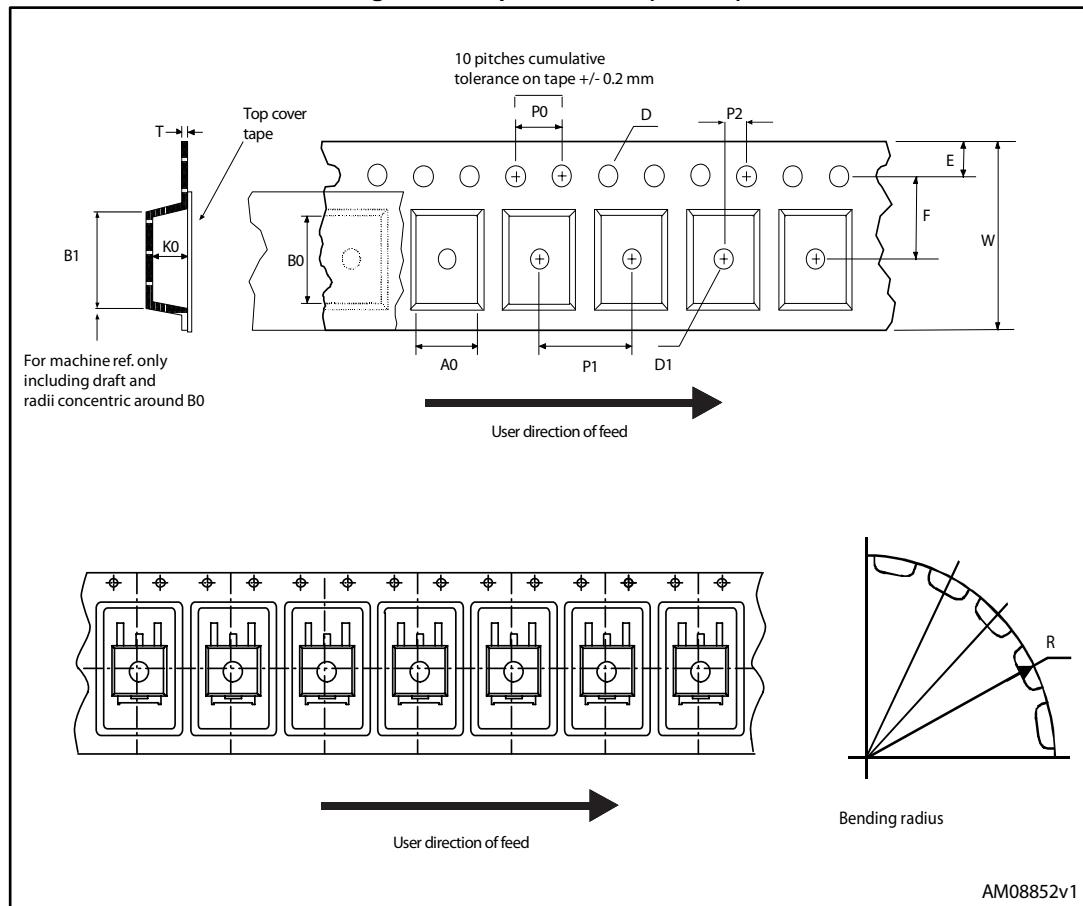


Figure 19: Reel for DPAK (TO-252)

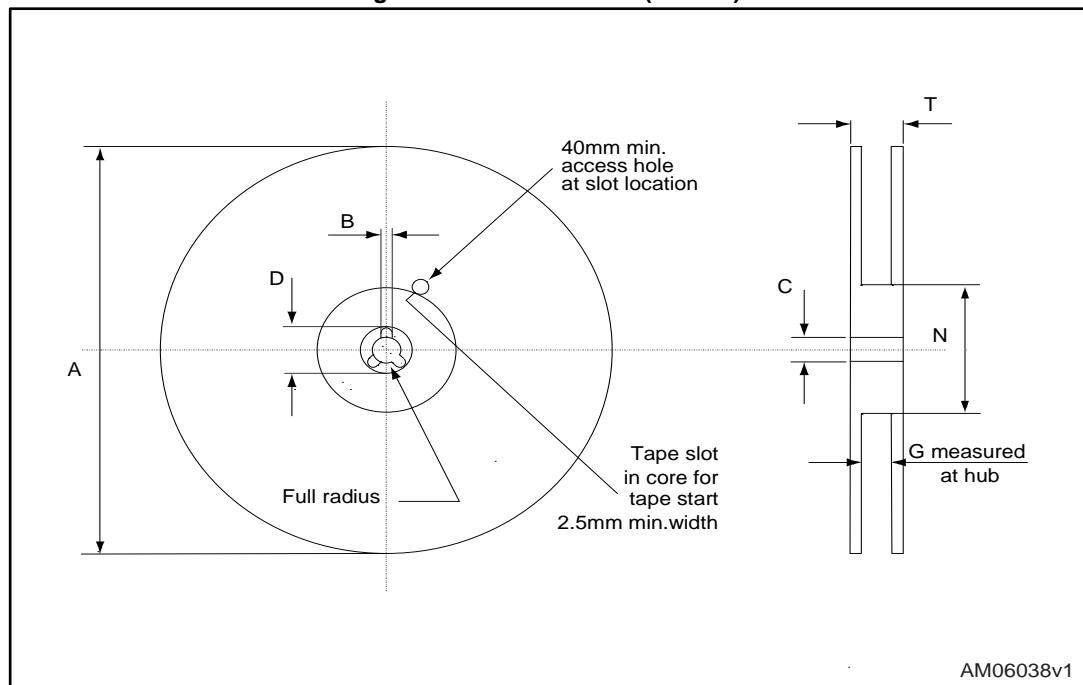


Table 9: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
10-Dec-2013	1	First revision.
24-Mar-2015	2	Text edits throughout document On cover page, updated title, applications, description and features table Updated Table 4: Static Updated Table 5: Dynamic Updated Table 6: Switching times Updated Table 7: Source-drain diode Added Section 2.1: Electrical characteristics (curves) Minor text changes

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved