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MC14043B, MC14044B

CMOS MSI

Quad R–S Latches

The MC14043B and MC14044B quad R–S latches are constructed with MOS P–Channel and N–Channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three–state buffers having a common enable input. The outputs are enabled with a logical "1" or high on the enable input; a logical "0" or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

Features

- Double Diode Input Protection
- Three–State Outputs with Common Enable
- Outputs Capable of Driving Two Low–power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable
- These Devices are Pb–Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to $+18.0$	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to $+125$	°C
T_{stg}	Storage Temperature Range	-65 to $+150$	°C
T_L	Lead Temperature (8–Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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SOIC–16
D SUFFIX
CASE 751B

SOEIAJ–16
F SUFFIX
CASE 966

MARKING DIAGRAMS

16

140xxBG
AWLYWW

1

SOIC–16

16

MC14043B
ALYWG

1

SOEIAJ–16
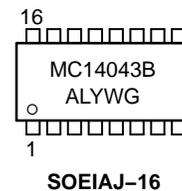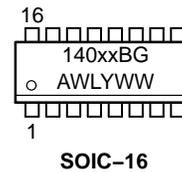
xx	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G	= Pb–Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

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PIN ASSIGNMENT

MC14043B

Q3	1 ●	16	V$_{DD}$
Q0	2	15	R3
R0	3	14	S3
S0	4	13	NC
E	5	12	S2
S1	6	11	R2
R1	7	10	Q2
V$_{SS}$	8	9	Q1

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Q3	1 ●	16	V$_{DD}$
NC	2	15	$\overline{S3}$
$\overline{S0}$	3	14	$\overline{R3}$
$\overline{R0}$	4	13	Q0
E	5	12	$\overline{R2}$
$\overline{R1}$	6	11	$\overline{S2}$
$\overline{S1}$	7	10	Q2
V$_{SS}$	8	9	Q1
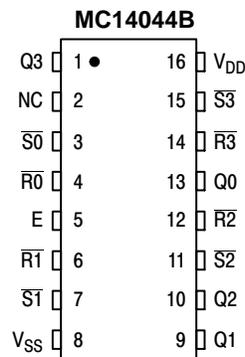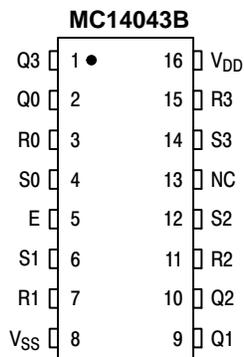
NC = NO CONNECTION
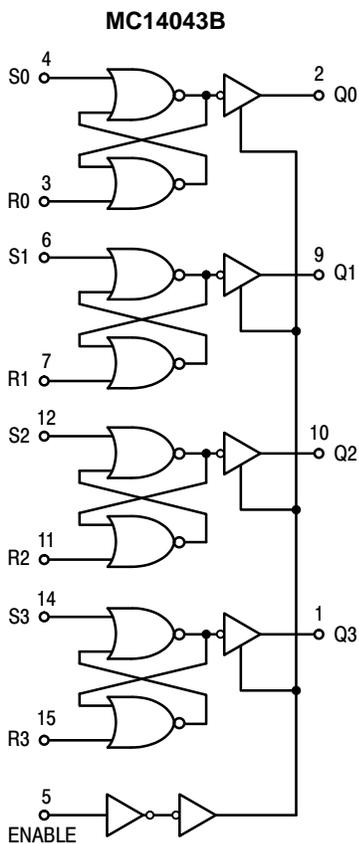
MC14043B

V$_{DD}$ = PIN 16
V$_{SS}$ = PIN 8
NC = PIN 13

TRUTH TABLE

S	R	E	Q
X	X	0	High Impedance
0	0	1	No Change
0	1	1	0
1	0	1	1
1	1	1	1

X = Don't Care
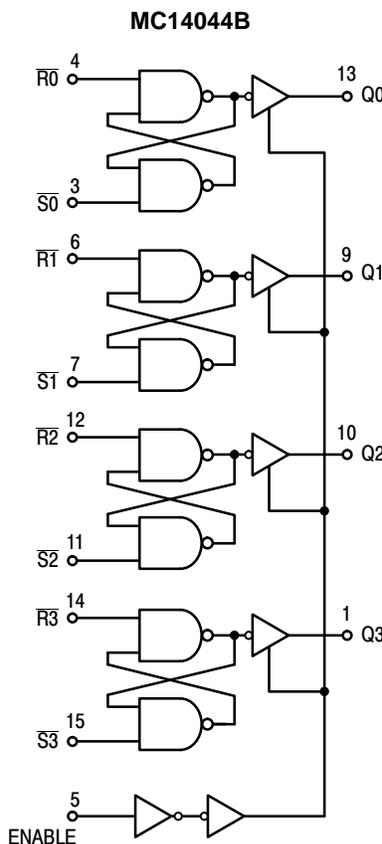
MC14044B

V$_{DD}$ = PIN 16
V$_{SS}$ = PIN 8
NC = PIN 2

TRUTH TABLE

$\overline{S}$	$\overline{R}$	E	Q
X	X	0	High Impedance
0	0	1	0
0	1	1	1
1	0	1	0
1	1	1	No Change

X = Don't Care

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	mAdc
		5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
		10	−1.6	–	−1.3	−2.25	–	−0.9	–	
		15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) (V_{OL} = 1.5 Vdc)	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	
		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	1.0	–	0.002	1.0	–	30	μAdc
		10	–	2.0	–	0.004	2.0	–	60	
		15	–	4.0	–	0.006	4.0	–	120	
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs all buffers switching)	I_T	5.0 10 15	$I_T = (0.58\ \mu A/kHz)\ f + I_{DD}$; $I_T = (1.15\ \mu A/kHz)\ f + I_{DD}$; $I_T = (1.73\ \mu A/kHz)\ f + I_{DD}$							μAdc
Three−State Output Leakage Current	I_{TL}	15	–	±0.1	–	±0.0001	±0.1	–	±3.0	μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.004.

## SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time t_{TLH} = (1.35 ns/pF) C_L + 32.5 ns t_{TLH} = (0.60 ns/pF) C_L + 20 ns t_{TLH} = (0.40 ns/pF) C_L + 20 ns	t_{TLH}	 5.0 10 15	 – – –	 100 50 40	 200 100 80	ns
Output Fall Time t_{THL} = (1.35 ns/pF) C_L + 32.5 ns t_{THL} = (0.60 ns/pF) C_L + 20 ns t_{THL} = (0.40 ns/pF) C_L + 20 ns	t_{THL}	 5.0 10 15	 – – –	 100 50 40	 200 100 80	ns
Propagation Delay Time t_{PLH} = (0.90 ns/pF) C_L + 130 ns t_{PLH} = (0.36 ns/pF) C_L + 57 ns t_{PLH} = (0.26 ns/pF) C_L + 47 ns	t_{PLH}	 5.0 10 15	 – – –	 175 75 60	 350 175 120	ns
t_{PHL} = (0.90 ns/pF) C_L + 130 ns t_{PHL} = (0.90 ns/pF) C_L + 57 ns t_{PHL} = (0.26 ns/pF) C_L + 47 ns	t_{PHL}	5.0 10 15	– – –	175 75 60	350 175 120	ns
Set, $\overline{Set}$ Pulse Width	t_W	5.0 10 15	200 100 70	80 40 30	– – –	ns
Reset, $\overline{Reset}$ Pulse Width	t_W	5.0 10 15	200 100 70	80 40 30	– – –	ns
Three–State Enable/Disable Delay	t_{PLZ}, t_{PHZ}, t_{PZL}, t_{PZH}	5.0 10 15	– – –	150 80 55	300 160 110	ns

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

AC WAVEFORMS
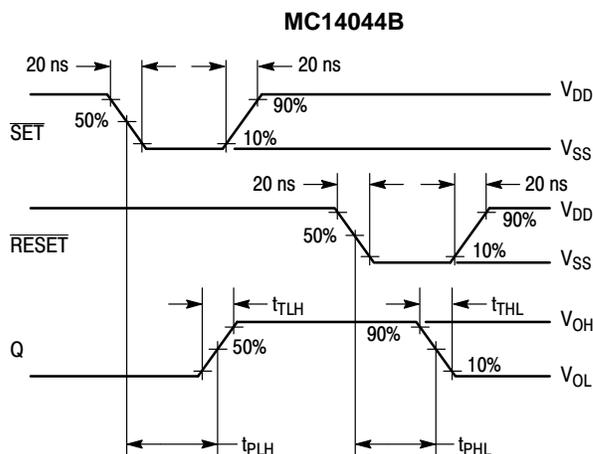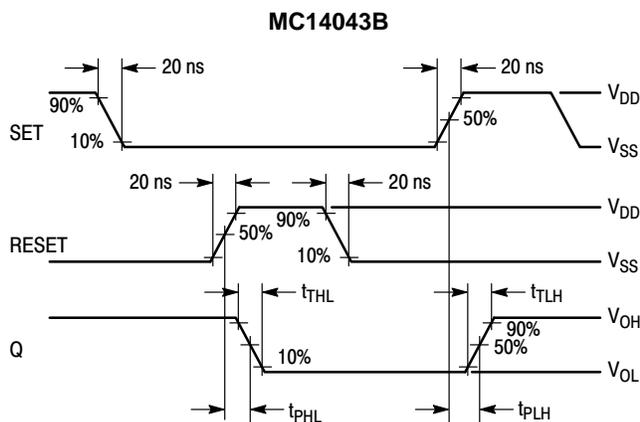
MC14043B

MC14044B

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THREE−STATE ENABLE/DISABLE DELAYS

Set, Reset, Enable, and Switch Conditions for 3−State Tests

					MC14043B		MC14044B	
Test	**Enable**	**S1**	**S2**	**Q**	**S**	**R**	**$\overline{S}$**	**$\overline{R}$**
t_{PZH}	⤒	Open	Closed	A	V_{DD}	V_{SS}	V_{SS}	V_{DD}
t_{PZL}	⤒	Closed	Open	B	V_{SS}	V_{DD}	V_{DD}	V_{SS}
t_{PHZ}	⤓	Open	Closed	A	V_{DD}	V_{SS}	V_{SS}	V_{DD}
t_{PLZ}	⤓	Closed	Open	B	V_{SS}	V_{DD}	V_{DD}	V_{SS}
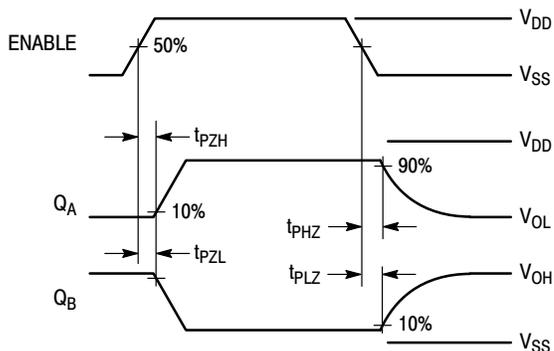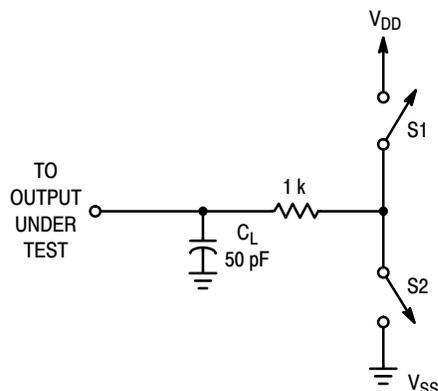
ORDERING INFORMATION

Device	Package	Shipping†
MC14043BDG	SOIC−16 (Pb−Free)	48 Units / Rail
NLV14043BDG*	SOIC−16 (Pb−Free)	48 Units / Rail
MC14043BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14043BDR2G*	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
MC14043BFELG	SOEIAJ−16 (Pb−Free)	2000 Units / Tape & Reel

Device	Package	Shipping†
MC14044BDG	SOIC−16 (Pb−Free)	48 Units / Rail
NLV14044BDG*	SOIC−16 (Pb−Free)	48 Units / Rail
MC14044BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14044BDR2G*	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MC14043B, MC14044B

PACKAGE DIMENSIONS

SOIC−16
D SUFFIX
CASE 751B−05
ISSUE K
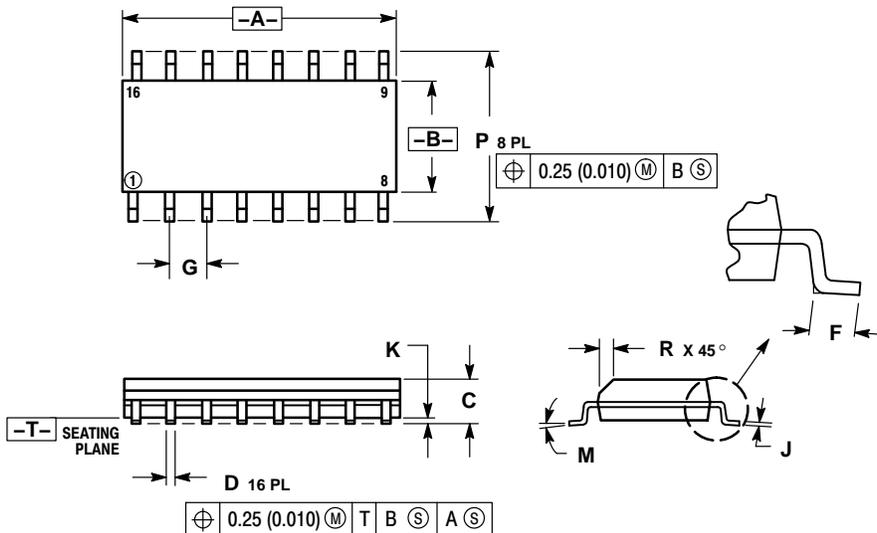
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS
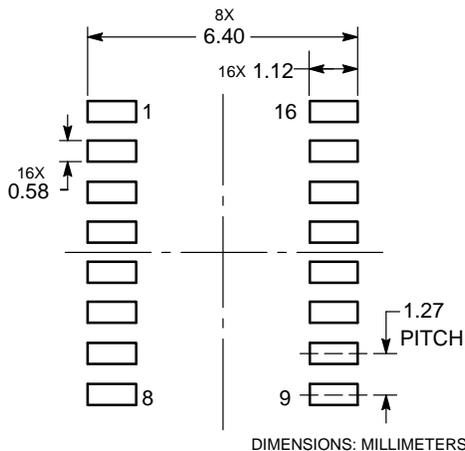
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC14043B, MC14044B

PACKAGE DIMENSIONS

SOEIAJ−16
F SUFFIX
CASE 966
ISSUE A
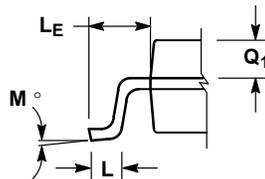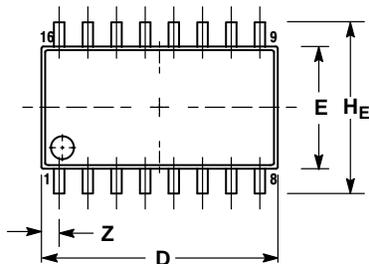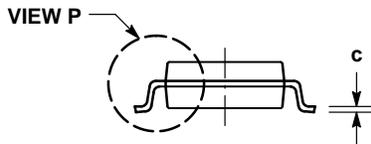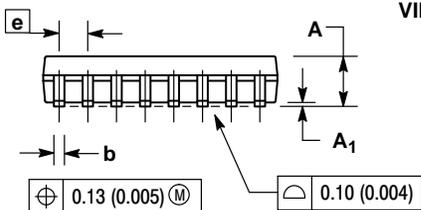
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	---	2.05	---	0.081
A₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

MC14043B/D