AT25QF128A

128-Mbit Serial NOR Flash Memory with Dual and Quad I/O Support

Features

- Single voltage operation with range of 2.7V to 3.6V
- 128-Mbit (32 x 4 Mbit physical block) Flash Memory
- Default Operating Mode is SPI Quad I/O
- Serial Peripheral Interface (SPI) compatible support
  - Supports SPI modes 0 and 3
  - Supports Dual Output and Quad Output read
  - Supports Dual I/O and Quad I/O read
- Maximum Operating Frequency
  - 133 MHz maximum operating frequency at 85 °C
  - 120 MHz maximum operating frequency at 105 °C
- Read Operations
  - 70 MHz SPI normal read
  - 120 MHz SPI fast read
  - 133 MHz Quad Output fast read at 85 °C
  - Dual I/O data transfer rate up to 240 Mbps
  - Quad I/O data transfer rate up to 480 Mbps
  - Quad Output data transfer rate up to 532 Mbps
  - Continuous read with 8/16/32/64-byte wrap
- Flexible programming
  - Byte/Page program (1 to 256 Bytes)
  - Program suspend and resume
- Fast program and erase times
  - 0.6 ms typical page (256 byte) program time
  - 70 ms typical 4-Kbyte block erase time
  - 150 ms typical 32-Kbyte block erase time
  - 250 ms typical 64-Kbyte block erase time
  - Full chip erase: 30 s typical
- Hardware and software Write Protection
  - Hardware-controlled locking of protected sector via $\overline{WP}$ pin
  - Three 256-byte OTP-capable security registers
  - Write protect all or part of memory via software with top/bottom block selection
- Serial Flash Discoverable Parameter (SFDP) register
- Low power dissipation
  - 13 µA standby current at 85 °C
  - 20 µA standby current at 105 °C
  - 2 µA deep power-down current at 85 °C
  - 5 µA deep power-down current at 105 °C
- Endurance:
  - 100K program/erase cycles at 85 °C
  - 10K program/erase cycles at 105 °C
- Data Retention:
  - 20 years at 85 °C
  - 10 years at 105 °C
- Temperature Range:
  - Industrial: -40 °C to 85 °C
  - Extended Temperature Range: -40 °C to 105 °C
- Industry standard green (Pb/Halide-free/RoHS compliant) package options
  - 8-lead 0.208” Wide SOIC
  - 8-pad (5 x 6 x 0.6 mm) UDFN

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1. Product Overview

The AT25QF128A is a 128-Mbit Serial Peripheral Interface (SPI) Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the AT25QF128A is ideal for data storage as well, eliminating the need for additional data storage devices.

The SPI clock supports a maximum frequency of 133 MHz, enabling data transfers up to 532 Mbits/s for Quad Output operations.

The AT25QF128A array is organized into 65,536 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program commands. Pages can be erased in 4 kB, 32 kB, or 64 kB blocks, or the entire chip.

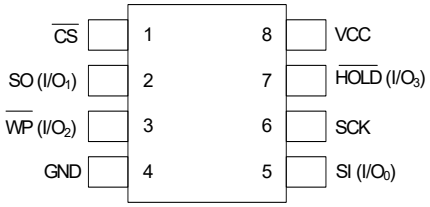
The devices operate on a single 2.7V to 3.6V power supply with current consumption as low as 2 µA for Deep Power-Down at 85 °C. All devices offered in space-saving packages. The device supports JEDEC standard manufacturer and device identification with three 256-byte secure OTP registers.

The physical block size for this device is 4 Mbit.

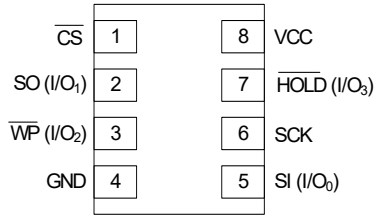
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2. Package Pinouts

Figure 1 show the package pinouts for the following devices.



8-lead 8S1 SOIC Package (208-mil)



8-pad UDFN Package

Figure 1. AT25QF128A Flash Memory Package Types

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3. Pin Descriptions

During all operations, VCC must be held stable and within the specified valid range: VCC (min) to VCC (max).

All of the input and output signals must be held high or low (according to voltages of VIH, VOH, VIL or VOL, see Section 9.6, DC Electrical Characteristics). These pins are described below.

3.1 Pin Summary

Table 1. AT25QF128A Pin Names

Pin Name	I/O	Description
$\overline{CS}$	I	Chip select.
SO (IO_1)	I/O	Serial Output for single bit data commands. IO_1 for dual or quad commands.
$\overline{WP}$ (IO_2)	I/O	Write Protect in single bit or dual data commands. IO_2 in quad mode. The signal has an internal pull-up resistor and can be left unconnected in the host system if not used for quad commands.
GND		Ground.
SI (IO_0)	I/O	Serial input for single bit data commands. IO_0 for dual or quad commands.
SCK	I	Serial clock.
$\overline{HOLD}$ (IO_3)	I/O	Hold (pause) serial transfer in single bit or dual data commands. IO_3 in Quad-I/O mode. The signal has an internal pull-up resistor and can be left unconnected in the host system if not used for Quad commands.
VCC		Core and I/O power supply.

3.2 Chip Select ($\overline{CS}$)

The chip select signal indicates when a command for the device is in process and the other signals are relevant for the memory device. When the $\overline{CS}$ signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal *Program*, *Erase* or *Write Status Registers* embedded operation is in progress, the device remains in the Standby Power mode. Driving the $\overline{CS}$ input to logic low state enables the device, placing it in the *Active Power* mode. After Power Up, a falling edge on $\overline{CS}$ is required prior to the start of any command.

3.3 Serial Clock (SCK)

This input signal provides the synchronization reference for the SPI interface. Commands, addresses, or data input are latched on the rising edge of the SCK signal. Data output changes after the falling edge of SCK.

3.4 Serial Input (SI or I/O_0)

This input signal is used to transfer data serially into the device. It receives commands, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal.

SI becomes I/O_0 an input and output during Dual and Quad commands for receiving commands, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

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3.5 Serial Data Output (SO or I/O_1)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal.

The SO pin becomes an I/O pin (I/O_1) during Dual and Quad commands for receiving commands, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

3.6 Write Protect ($\overline{WP}$ or I/O_2)

When $\overline{WP}$ is driven low, while the Status Register Protect bits (SRP1 and SRP0) of the Status Registers are set to 0 and 1 respectively, it is not possible to write to the Status Registers. This prevents any alteration of the Status Registers. As a consequence, all the data bytes in the memory area that are protected by the Block Protect, TB, SEC, and CMP bits in the status registers, are also hardware protected against data modification while $\overline{WP}$ remains low. The $\overline{WP}$ function is not available when the Quad mode is enabled. In the AT25QF128A, the QE bit in Status Register 2 is set to 1 after power-on.

The $\overline{WP}$ function is replaced by I/O_2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK). $\overline{WP}$ has an internal pull-up resistance; when unconnected; $\overline{WP}$ is at VIH and can be left unconnected in the host system if not used for Quad mode.

3.7 Hold ($\overline{HOLD}$ or I/O_3)

The $\overline{HOLD}$ function is only available when the Quad Enable (QE) bit in Status Register 2 = 0. If QE = 1, The $\overline{HOLD}$ function is disabled and the pin acts as dedicated data I/O pin. Note that the AT25QF128A device ships with the QE bit set at the factory, causing the device to power up in Quad mode.

The $\overline{HOLD}$ signal goes low to stop any serial communication with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

3.8 VCC Power Supply

VCC is the supply voltage. It is the single voltage used for all device functions including read, program, and erase.

3.9 GND Ground

GND is the ground reference for the VCC supply voltage.

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4. Block/Sector Addresses

Table 2. Block/Sector Addresses of AT25QF128A

Memory Density	Block (64k byte)	Block (32k byte)	Sector No.	Sector Size (kB)	Address Range
128 Mbit	Block 0	Half block 0	Sector 0	4	000000h - 000FFFh
			:	:	:
			Sector 7	4	007000h - 007FFFh
		Half block 1	Sector 8	4	008000h - 008FFFh
			:		:
			Sector 15	4	00F000h - 00FFFFh
	Block 1	Half block 2	Sector 16	4	010000h - 010FFFh
			:	:	:
			Sector 23	4	017000h - 017FFFh
		Half block 3	Sector 24	4	018000h - 018FFFh
			:	:	:
			Sector 31	4	01F000h - 01FFFFh
	:	:	:	:	:
	Block 254	Half block 508	Sector 4064	4	FE0000h - FE0FFFh
			:	:	:
			Sector 4071	4	FE7000h - FE7FFFh
		Half block 509	Sector 4072	4	FE8000h - FE8FFFh
			:	:	:
			Sector 4079	4	FEF000h - FEFFFFh
	Block 255	Half block 510	Sector 4080	4	FF0000h - FF0FFFh
			:	:	:
			Sector 4087	4	FF7000h - FF7FFFh
		Half block 511	Sector 4088	4	FF8000h - FF8FFFh
			:	:	:
			Sector 4095	4	FFF000h - FFFFFFh

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5. SPI Operation

5.1 Standard SPI Commands

The AT25QF128A features a 4-pin serial peripheral interface on 4 signals bus: Serial Clock (SCK), Chip Select ($\overline{CS}$), Serial Data Input (SI) and Serial Data Output (SO). SPI bus modes 0 and 3 are supported. Input data is latched on the rising edge of SCK and data shifts out on the falling edge of SCK.

5.2 Dual SPI Commands

The AT25QF128A supports Dual SPI operation when using the *Dual Output Fast Read* (3BH), *Dual I/O Fast Read* (BBH) and *Read Manufacture ID/Device ID Dual I/O* (92H) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: I/O_0 and I/O_1, respectively.

5.3 Quad SPI Commands

The AT25QF28A device ships with the Quad Enable (QE) bit set in the Status Register. This causes the device to power-up in SPI Quad I/O mode.

The AT25QF128A supports Quad SPI operation when using the *Quad Output Fast Read* (6BH), *Quad I/O Fast Read* (EBH), *Quad I/O Word Fast Read* (E7h), *Read Manufacture ID/Device ID Quad I/O* (94H) and *Quad Page Program* (32H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: I/O_0 and I/O_1, and /WP and $\overline{HOLD}$ pins become I/O_2 and I/O_3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

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6. Operating Features

6.1 Supply Voltage

6.1.1 Operating Supply Voltage

Prior to selecting the memory and issuing commands to it, a valid and stable VCC voltage within the specified VCC (min) / VCC (max) range must be applied. In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a 1 µF low-ESR ceramic decoupling capacitor, placed as close as possible to the VCC/GND package pins. This voltage must remain stable and valid until the end of the transmission of the command and, for a Write command, until the completion of the internal write cycle (t_W).

6.1.2 Power-up Conditions

When the power supply is turned on, VCC rises continuously from GND to VCC. During this time, the Chip Select ($\overline{CS}$) line is not allowed to float but should follow the VCC voltage, it is therefore recommended to connect the $\overline{CS}$ line to VCC via a pull-up resistor.

In addition, the $\overline{CS}$ input is both edge sensitive and level sensitive. After power-up, the device does not become selected until a falling edge is first detected on $\overline{CS}$. This ensures that $\overline{CS}$ must have been High, prior to going low to start the first operation.

6.1.3 Device Reset

In order to prevent inadvertent Write operations during power-up (continuous rise of VCC), a power on reset (POR) circuit is included. At Power-up, the device does not respond to any command until VCC has reached the power on reset threshold voltage (this threshold is lower than the minimum VCC operating voltage defined by the DC operating ranges).

When VCC has passed the POR threshold, the device is reset.

6.1.4 Power-down

At Power-down (continuous decrease in VCC), as soon as VCC drops from the normal operating voltage to below the power on reset threshold voltage, the device stops responding to any command sent to it. During Power-down, the device must be deselected (Chip Select, $\overline{CS}$, must be allowed to follow the voltage applied on VCC) and in Standby Power mode (no internal Write cycle in progress).

6.2 Active Power and Standby Power Modes

When Chip Select ($\overline{CS}$) is low, the device is selected and in the Active Power mode and consuming current (ICC).

When Chip Select ($\overline{CS}$) is high, the device is deselected. If a Write cycle is not currently in progress, the device enters the Standby Power mode, and the current consumption drops to ICC1.

6.3 Hold Condition

The $\overline{HOLD}$ signal pauses any serial communications with the device without resetting the clocking sequence. During a Hold, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCK) are don't care. Note that the HOLD function can only be used with the QE bit of the Status Register = 0.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{CS}$) low. Normally, the device remains selected for the duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold ($\overline{HOLD}$) signal is driven low at the same time as Serial Clock (SCK) already being low (as shown in Figure 2).

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The Hold condition ends when the Hold ($\overline{HOLD}$) signal is driven High at the same time as Serial Clock (C) already being low. Figure 2 also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (SCK) being low.

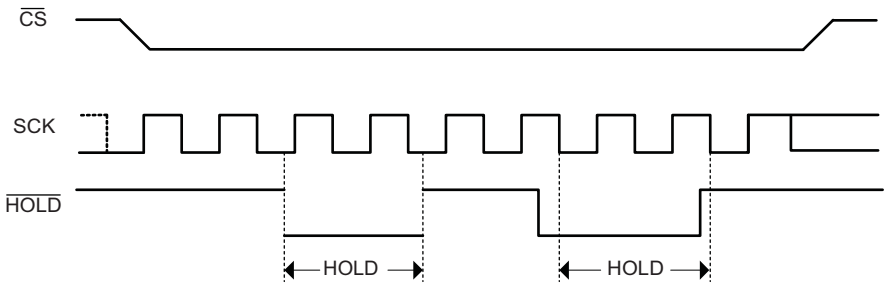


Figure 2. Hold Condition Activation

6.4 Status Register

The AT25QF128A contains three Status registers. Each byte is written or read using specific commands. For a read operation, the 05h, 35h, and 15h commands are used to access the S7 - S0, S15 - S8, and S23 - S16 bytes respectively. For a write operation, the 01h, 31h, and 11h commands are used as shown in Table 11.

The tables show the layout of the Status Register bits.

Table 3. Status Register 3

S23	S22	S21	S20	S19	S18	S17	S16
Reserved	DRV1	DRV0	Reserved	Reserved	Reserved	Reserved	Reserved

Table 4. Status Register 2

S15	S14	S13	S12	S11	S10	S9	S8
SUS1	CMP	LB3	LB2	LB1	SUS2	QE	SRP1

Table 5. Status Register 1

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP

6.4.1 Status Register Bit Definitions

6.4.1.1 WIP bit (S0)

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

6.4.1.2 WEL bit (S1)

The Write Enable Latch bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

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6.4.1.2.1 BP4, BP3, BP2, BP1, BP0 Bits (S6 - S2)

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register command.

- When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory becomes protected against Page Program, Sector Erase and Block Erase commands.
- The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.
- The Chip Erase (CE) command is executed if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP = 0 or the Block Protect (BP2, BP1, BP0) bits are 1 and CMP = 1.

6.4.1.3 SRP1, SRP0 Bits (S8 - S7)

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, or power supply lock-down.

6.4.1.4 QE Bit (S9)

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is cleared to 0, the $\overline{WP}$ and $\overline{HOLD}$ pins are enabled. When the QE pin is set to 1 (default), the Quad I/O_2 and I/O_3 pins are enabled. Note that the QE bit should never be set to 1 during standard SPI or Dual SPI operation if the $\overline{WP}$ or $\overline{HOLD}$ pins are connected directly to the power supply or ground. Note that if these pins are connected to power or ground, software must first clear the QE bit.

6.4.1.5 SUS1/SUS2 Bits (S15, S10)

The SUS1 and SUS2 bits are read only bits in the status register2 (S15 and S10) that are set to 1 after executing an Erase/Program Suspend (75h) command (The Erase Suspend sets SUS1 to 1, and the Program Suspend sets SUS2 to 1). The SUS1 and SUS2 bits are cleared to 0 by Erase/Program Resume (7Ah) command as well as a power-down, power-up cycle.

6.4.1.6 LB3/LB2/LB1 bit (S13 - S11)

The LB bits are non-volatile One Time Program (OTP) bits in Status Register (S13 - S11) that provide the write protect control and status to the Security Registers. The default state of LBx is 0, the security registers are unlocked. The LBx bits can be set to 1 individually using the Write Register command. The LBx bits are One Time Programmable. Once they are set to 1, the Security Registers become read-only permanently.

6.4.1.7 CMP Bit (S14)

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the SEC and BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP = 0.

6.4.1.8 DRV1/DRV0 Bits (S22, S21)

The DRV1 and DRV0 bits are used to determine the output driver strength for the Read command. m

Table 6. DRV1 / DRV0 Bit Encoding

DRV1, DRV0	Driver Strength
00	100% (default)
01	75%
10	50%
11	25%

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6.4.2 Status Register Protect Table

The Status Register Protect (SRP1 and SRP0) bit are non-volatile Read/Write bits in the Status Register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

Table 7. Status Register Protect Table

SRP1	SRP0	$\overline{WP}$	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL = 1 (Factory Default).
0	1	0	Hardware Protected	$\overline{WP}$ = 0, the Status Register locked and cannot be written.
0	1	1	Hardware Unprotected	$\overline{WP}$ = 1, the Status Register is unlocked and can be written to after a Write Enable command, WEL = 1.
1	0	X	Power Supply Lock-Down [1]	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X		Not allowed.

1. When SRP1, SRP0 = (1, 0), a Power-Down, Power-Up cycle change SRP1, SRP0 to (0, 0) state.

6.4.3 Write Protect Features

1. Software Protection: The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.
2. Hardware Protection: $\overline{WP}$ going low to protected the writable bits of Status Register.
3. Deep Power-Down: In Deep Power-Down mode, all commands are ignored except the *Release from Deep Power-Down Mode* command.
4. Write Enable: The Write Enable command is set the Write Enable Latch (WEL) bit. The WEL bit is reset under any of the following conditions:
   - Power -up
   - Write Disable
   - Write Status Register
   - Page Program
   - Sector Erase/Block Erase/Chip Erase
   - Software Reset

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6.4.4 Status Register Memory Protection

Table 8. AT25QF128A Status Register Memory Protection (CMP = 0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	252 to 255	FC0000h - FFFFFFh	256 kB	Upper 1/64
0	0	0	1	0	248 to 255	F80000h - FFFFFFh	512 kB	Upper 1/32
0	0	0	1	1	240 to 255	F00000h - FFFFFFh	1 MB	Upper 1/16
0	0	1	0	0	224 to 255	E00000h - FFFFFFh	2 MB	Upper 1/8
0	0	1	0	1	192 to 255	C00000h - FFFFFFh	4 MB	Upper 1/4
0	0	1	1	0	128 to 255	800000h - FFFFFFh	8 MB	Upper 1/2
0	1	0	0	1	0 to 3	000000h - 03FFFFh	256 kB	Upper 1/64
0	1	0	1	0	0 to 7	000000h - 07FFFFh	512 kB	Upper 1/32
0	1	0	1	1	0 to 15	000000h - 0FFFFFh	1 MB	Upper 1/16
0	1	1	0	0	0 to 31	000000h - 1FFFFFh	2 MB	Upper 1/8
0	1	1	0	1	0 to 63	000000h - 3FFFFFh	4 MB	Upper 1/4
0	1	1	1	0	0 to 127	000000h - 7FFFFFh	8 MB	Upper 1/2
X	X	1	1	1	0 to 255	000000h - FFFFFFh	16 MB	ALL
1	0	0	0	1	255	FFF000h - FFFFFFh	4 kB	Top Block
1	0	0	1	0	255	FFE000h - FFFFFFh	8 kB	Top Block
1	0	0	1	1	255	FFC000h - FFFFFFh	16 kB	Top Block
1	0	1	0	X	255	FF8000h - FFFFFFh	32 kB	Top Block
1	0	1	1	0	255	FF8000h - FFFFFFh	32 kB	Top Block
1	1	0	0	1	0	000000h - 000FFFh	4 kB	Bottom Block
1	1	0	1	0	0	000000h - 001FFFh	8 kB	Bottom Block
1	1	0	1	1	0	000000h - 003FFFh	16 kB	Bottom Block
1	1	1	0	X	0	000000h - 007FFFh	32 kB	Bottom Block
1	1	1	1	0	0	000000h - 007FFFh	32 kB	Bottom Block

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Table 9. AT25QF128A Status Register Memory Protection (CMP = 1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	0 to 255	000000h - FFFFFFh	ALL	ALL
0	0	0	0	1	0 to 251	000000h - FBFFFFh	16128 kB	Lower 63/64
0	0	0	1	0	0 to 247	000000h - F7FFFFh	15872 kB	Lower 31/32
0	0	0	1	1	0 to 239	000000h - EFFFFFh	15 kB	Lower 15/16
0	0	1	0	0	0 to 223	000000h - DFFFFFh	14 MB	Lower 7/8
0	0	1	0	1	0 to 191	000000h - BFFFFFh	12 MB	Lower 3/4
0	0	1	1	0	0 to 127	000000h - 7FFFFFh	8 MB	Lower 1/2
0	1	0	0	1	4 to 255	040000h - FFFFFFh	16,128 kB	Upper 63/64
0	1	0	1	0	8 to 255	080000h - FFFFFFh	15,872 kB	Upper 31/32
0	1	0	1	1	16 to 255	100000h - FFFFFFh	15 kB	Upper 15/16
0	1	1	0	0	32 to 255	200000h - FFFFFFh	14 MB	Upper 7/8
0	1	1	0	1	64 to 255	400000h - FFFFFFh	12 MB	Upper 3/4
0	1	1	1	0	128 to 255	800000h - FFFFFFh	8 MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 255	000000h - FFEFFFh	16380 kB	L-4095/4096
1	0	0	1	0	0 to 255	000000h - FFDFFFh	16376 kB	L-2047/2048
1	0	0	1	1	0 to 255	000000h - FFBFFFh	16368 kB	L-1023/1024
1	0	1	0	X	0 to 255	000000h - FF7FFFh	16352 kB	L-511/512
1	0	1	1	0	0 to 255	000000h - FF7FFFh	16352 kB	L-511/512
1	1	0	0	1	0 to 255	001000h - FFFFFFh	16380 kB	U-4095/4096
1	1	0	1	0	0 to 255	002000h - FFFFFFh	16376 kB	U-2047/2048
1	1	0	1	1	0 to 255	004000h - FFFFFFh	16368 kB	U-1023/1024
1	1	1	0	X	0 to 255	008000h - FFFFFFh	16352 kB	U-511/512
1	1	1	1	0	0 to 255	008000h - FFFFFFh	16352 kB	U-511/512

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7. Device Identification

Three legacy commands are supported to access device identification that can indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information shown in Table 10.

Table 10. AT25QF128A ID Definition table

Operating Code	M7-M0	ID15-ID8	ID7-ID0
9Fh	1Fh	89h	01h
90h/92h/94h	1Fh		17h
ABh			17h

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8. Command Descriptions

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCK after $\overline{CS}$ is driven low. Then, the one byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCK.

See Table 11, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, data bytes, both, or none. The $\overline{CS}$ pin must be driven high after the last bit of the command sequence has been shifted in.

For the *Read*, *Fast Read*, *Read Status Register*, *Release from Deep Power-Down*, and *Read Device ID* commands, the shifted-in command sequence is followed by a data out sequence. The $\overline{CS}$ pin can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, $\overline{CS}$ must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is $\overline{CS}$ must driven high when the number of clock pulses after $\overline{CS}$ being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing happens, and WEL is not reset.

Table 11. Command Set

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	N-Bytes
Write Enable	06h						
Write Disable	04h						
Read Status Register-1	05h	(S7 - S0)					continuous
Read Status Register-2	35h	(S15 - S8)					continuous
Read Status Register-3	15h	(S23 - S16)					continuous
Write Enable for Volatile Status Register	50h						
Write Status Register-1	01h	(S7 - S0)					
Write Status Register-2	31h	(S15 - S8)					
Write Status Register-3	11h	(S23 - S16)					
Read Data	03h	A23 - A16	A15 - A8	A7 - A0	(D7 - D0)	Next byte	continuous
Fast Read	0Bh	A23 - A16	A15 - A8	A7 - A0	dummy	(D7 - D0)	continuous
Dual Output Fast Read	3Bh	A23 - A16	A15 - A8	A7 - A0	dummy	(D7 - D0) [1]	continuous
Dual I/O Fast Read	BBh	A23 - A8 [2]	A7 - A0 M7 - M0 [2]	(D7 - D0) [1]	Next byte	Next byte	continuous
Quad Output Fast Read	6Bh	A23 - A16	A15 - A8	A7 - A0	dummy	(D7 - D0) [3]	continuous
Quad I/O Fast Read	EBh	A23 - A0 M7 - M0 [4]	dummy [5]	(D7 - D0) [3]	Next byte	Next byte	continuous
Quad I/O Word Fast Read [7]	E7h	A23 - A0 M7 - M0 [4]	dummy [6]	(D7 - D0)(3)	Next byte	Next byte	continuous
Page Program	02h	A23 - A16	A15 - A8	A7 - A0	(D7 - D0)	Next byte	continuous
Quad Page Program	32h	A23 - A16	A15 - A8	A7 - A0	(D7 - D0) [3]	Next byte	continuous
Fast Page Program	F2h	A23 - A16	A15 - A8	A7 - A0	(D7 - D0)	Next byte	continuous
Sector Erase	20h	A23 - A16	A15 - A8	A7 - A0			
Block Erase(32K)	52h	A23 - A16	A15 - A8	A7 - A0			
Block Erase (64K)	D8h	A23 - A16	A15 - A8	A7 - A0			
Chip Erase	C7/60h						
Enable Reset	66h						
Reset	99h						
Set Burst with Wrap	77h	dummy [6] W7 - W0					

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Table 11. Command Set *(continued)*

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	N-Bytes
Program/Erase Suspend	75h						
Program/Erase Resume	7Ah						
Deep Power-Down	B9h						
Release From Deep Power-Down, And Read Device ID	ABh	dummy	dummy	dummy	(ID7 - ID0)		continuous
Release From Deep Power-Down	ABh						
Manufacturer/ Device ID	90h	dummy	dummy	00H	(MID7 - MID0)	(ID7 - ID0)	continuous
Manufacturer/ Device ID by Dual I/O	92h	A23 - A8	A7 - A0, dummy	(MID7 - MID0), (DID7 -DID0)			continuous
Manufacturer/ Device ID by Quad I/O	94h	A23 - A0, dummy	dummy [10] (MID7 - MID0) (DID7 - DID0)				continuous
JEDEC ID	9Fh	MID7 - MID0	ID15 - ID8	ID7-ID0			continuous
Read Serial Flash Discoverable Parameter	5Ah	A23 - A16	A15 - A8	A7-A0	Dummy	D7 - D0	continuous
Erase Security Registers [8]	44h	A23 - A16	A15 - A8	A7-A0			
Program Security Registers [8]	42h	A23 - A16	A15 - A8	A7-A0	(D7 - D0)	(D7 - D0)	continuous
Read Security Registers [8]	48h	A23 - A16	A15 - A8	A7-A0	dummy	(D7 - D0)	continuous

1. Dual Output data
   IO_0 = (D6, D4, D2, D0)
   IO_1 = (D7, D5, D3, D1)
2. Dual Input Address
   IO_0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO_1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3,M1
3. Quad Output Data
   IO_0 = (D4, D0,…..)
   IO_1 = (D5, D1,…..)
   IO_2 = (D6, D2,…..)
   IO_3 = (D7, D3,…..)
4. Quad Input Address
   IO_0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO_1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO_2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO_3 = A23, A19, A15, A11, A7, A3, M7, M3
5. Fast Read Quad I/O Data
   IO_0 = (x, x, x, x, D4, D0,…)
   IO_1 = (x, x, x, x, D5, D1,…)
   IO_2 = (x, x, x, x, D6, D2,…)
   IO_3 = (x, x, x, x, D7, D3,…)
6. Fast Word Read Quad I/O Data
   IO_0 = (x, x, D4, D0,…)
   IO_1 = (x, x, D5, D1,…)
   IO_2 = (x, x, D6, D2,…)
   IO_3 = (x, x, D7, D3,…)
7. Fast Word Read Quad I/O Data; the lowest address bit must be 0.

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8. Security Registers Address:

   Security Register 1: A23 - A16 = 00h, A15 - A8 = 00010000b, A7 - A0 = Byte Address;
   Security Register 2: A23 - A16 = 00h, A15 - A8 = 00100000b, A7 - A0 = Byte Address;
   Security Register 3: A23 - A16 = 00h, A15 - A8 = 00110000b, A7 - A0 = Byte Address;

9. Dummy bits and Wraps Bits

   IO_0 = (x, x, x, x, x, x, w4, x)
   IO_1 = (x, x, x, x, x, x, w5, x)
   IO_2 = (x, x, x, x, x, x, w6, x)
   IO_3 = (x, x, x, x, x, x, x, x)

10. Address, continuous Read Mode bits, Dummy bits, Manufacture ID and Device ID

    IO_0 = (A20, A16, A12, A8, A4, A0, M4, M0, x, x, x, x, MID4, MID0, DID4, DID0)
    IO_1 = (A21, A17, A13, A9, A5, A1, M5, M1, x, x, x, x, MID5, MID1, DID5, DID1)
    IO_2 = (A22, A18, A14, A10, A6, A2, M6, M2, x, x, x, x, MID6, MID2, DID6, DID2)
    IO_3 = (A23, A19, A15, A11, A7, A3, M7, M3, x, x, x, x, MID7, MID3, DID7, DID3)

8.1 Configuration and Status Commands

8.1.1 Write Enable (06h)

The Write Enable command is for setting the Write Enable Latch (WEL) bit. The WEL bit must be set prior to every *Page Program*, *Sector Erase*, *Block Erase*, *Chip Erase*, *Write Status Register*, and *Erase/Program Security Registers* command.

The Write Enable command sequence: $\overline{CS}$ goes low sending the Write Enable command $\overline{CS}$ goes high.

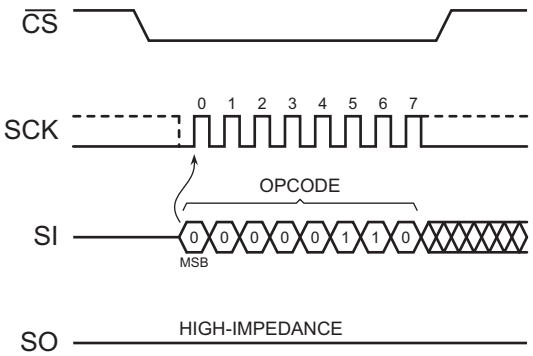


Figure 3. Write Enable Sequence Diagram

8.1.2 Write Disable (04h)

The Write Disable command is for resetting the Write Enable Latch bit. The Write Disable command sequence: $\overline{CS}$ goes low → sending the Write Disable command → $\overline{CS}$ goes high. The WEL bit is reset by following condition: Power-up and upon completion of the *Write Status Register*, *Page Program*, *Sector Erase*, *Block Erase*, *Chip Erase*, *Erase/Program Security Registers,* and *Reset* commands.

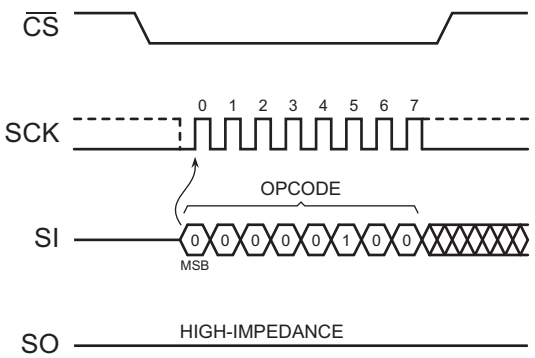


Figure 4. Write Disable Sequence Diagram

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8.1.3 Read Status Register (05h or 35h or 15h)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register can be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code 05h, the SO outputs Status Register bits S7 - S0. For command code 35h, the SO outputs Status Register bits S15 - S8. For command code 15h, the SO outputs Status Register bits S23 - 16.

Figure 5 shows a Read Status Register operation for Status Register 1 (05h). The Read Status Register 2 and 3 operations would be the same, but with a different opcode in the first eight clocks.

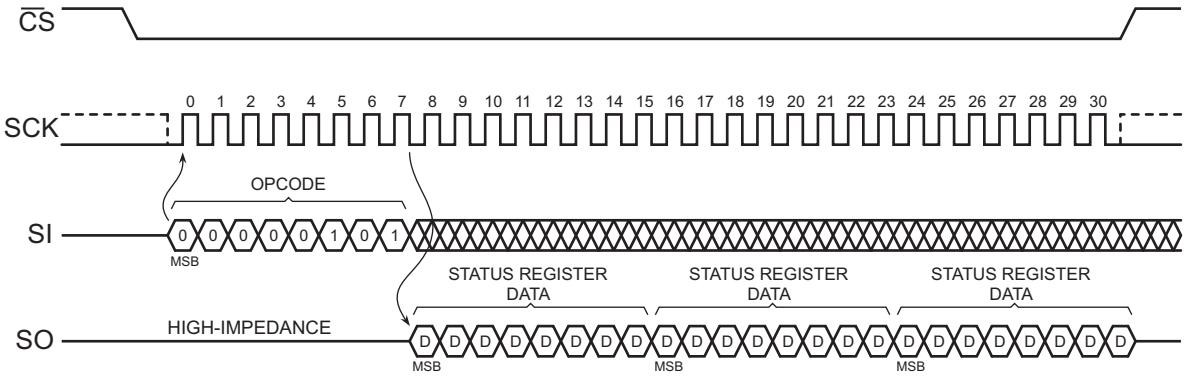


Figure 5. Read Status Register Sequence Diagram

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8.1.4 Write Status Register (01h or 31h or 11h)

The Write Status Register command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable command must previously have been executed. After the Write Enable command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register command has no effect on S23, S20, S19, S18, S17, S16, S15, S1 and S0 of the Status Register. $\overline{CS}$ must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register can still be read to check the value of the Write in Progress (WIP) bit. This bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the WEL bit is reset.

The Write Status Register command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only. The Write Status Register command also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect ($\overline{WP}$) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect ($\overline{WP}$) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register command is not executed once the Hardware Protected Mode is entered.

Figure 6 shows a Write Status Register operation for Status Register 1 (01h). The Write Status Register 2 and 3 operations would be the same, but with a different opcode in the first eight clocks.

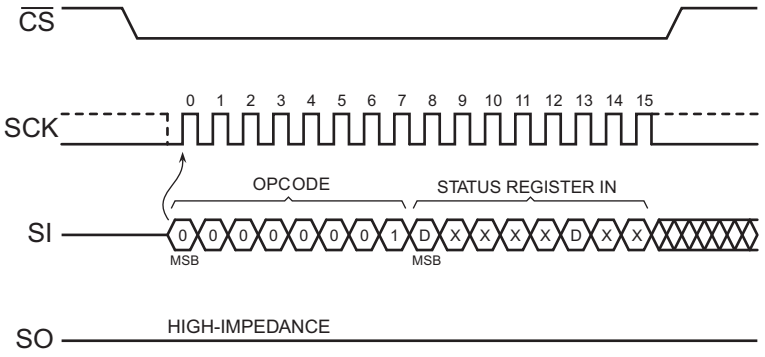


Figure 6. Write Status Register Sequence Diagram

8.1.5 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command does not set the Write Enable Latch bit, it is only valid for the Write Status Registers command to change the volatile Status Register bit values.

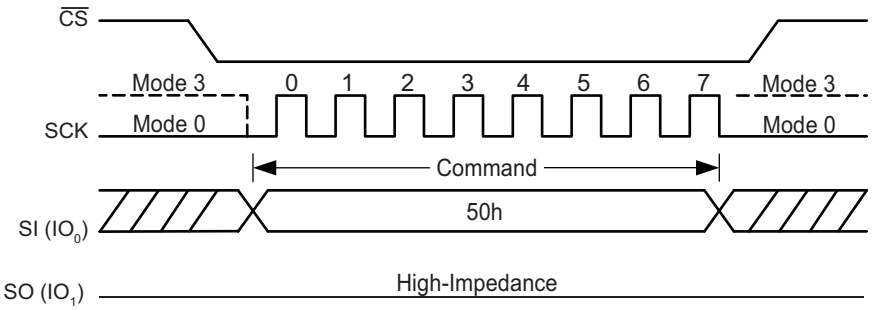


Figure 7. Write Enable for Volatile Status Register

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8.2 Read Commands

8.2.1 Read Data (03h)

The Read Data command is followed by a 3-byte address (A23 - A0), each bit being latched-in during the rising edge of SCK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_{C2}, during the falling edge of SCK. The address automatically increments to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues. The command is completed by driving $\overline{CS}$ high. The whole memory can be read with a single Read Data Bytes (READ) command. Any *Read Data* command attempting to execute while an *Erase*, *Program* or *Write* cycle is in progress, is rejected without having any effects on the cycle that is in progress.

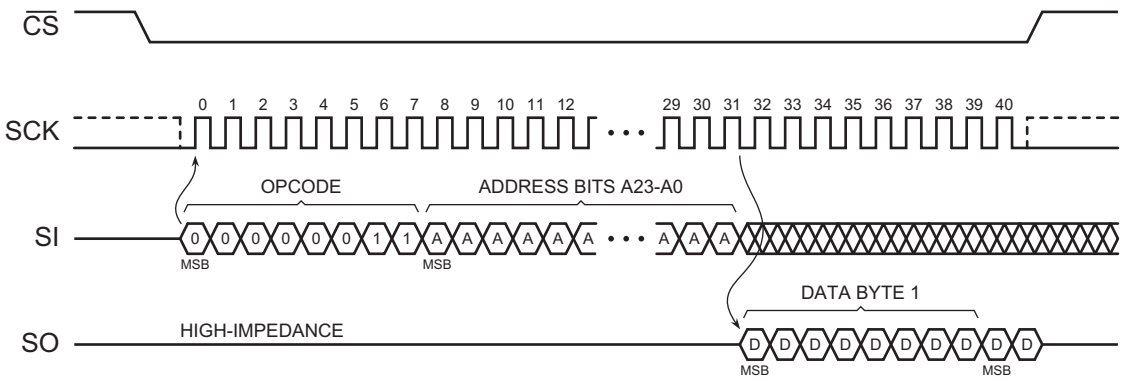


Figure 8. Read Data Bytes Sequence Diagram

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8.2.2 Fast Read (0Bh)

The Read Data at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a three-byte address (A23 - A0) and a dummy byte, each bit being latched-in during the rising edge of SCK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency of f_{C4} during the falling edge of SCK. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out.

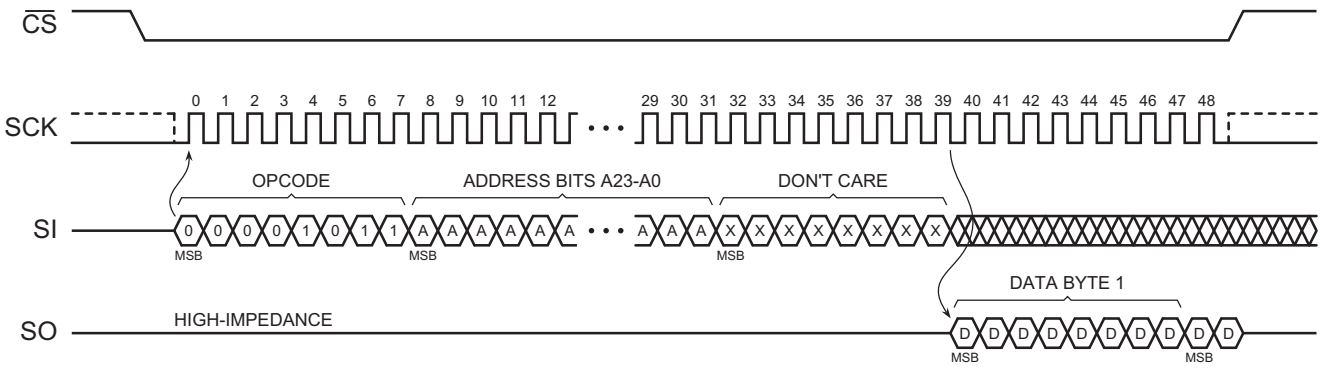


Figure 9. Fast Read Sequence Diagram

8.2.3 Dual Output Fast Read (3Bh)

The Dual Output Fast Read command is followed by 3-byte address (A23 - A0) and a dummy byte, each bit being latched in during the rising edge of SCK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out.

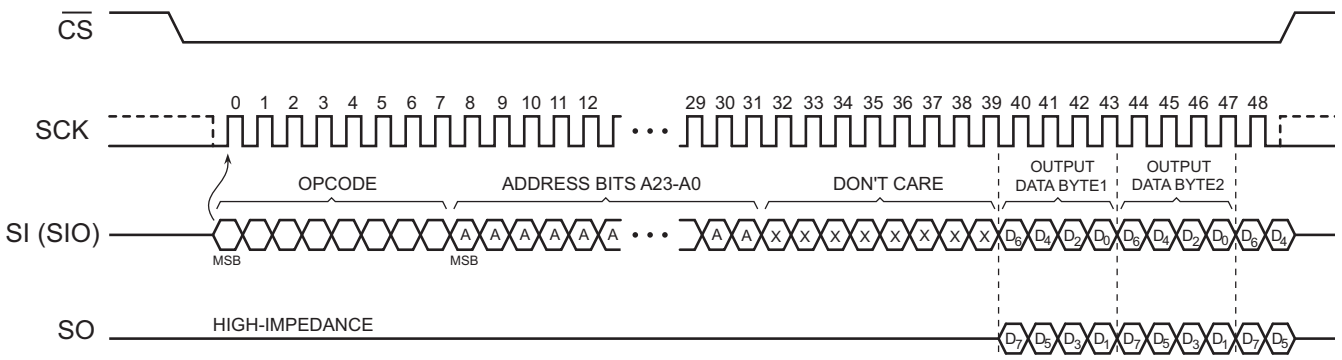


Figure 10. Dual Output Fast Read Sequence Diagram

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8.2.4 Quad Output Fast Read (6Bh)

The Quad Output Fast Read command is followed by 3-byte address (A23 - A0) and a dummy byte, each bit being latched in during the rising edge of SCK, then the memory contents are shifted out 4-bit per clock cycle from IO_3, IO_2, IO_1 and IO_0. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out.

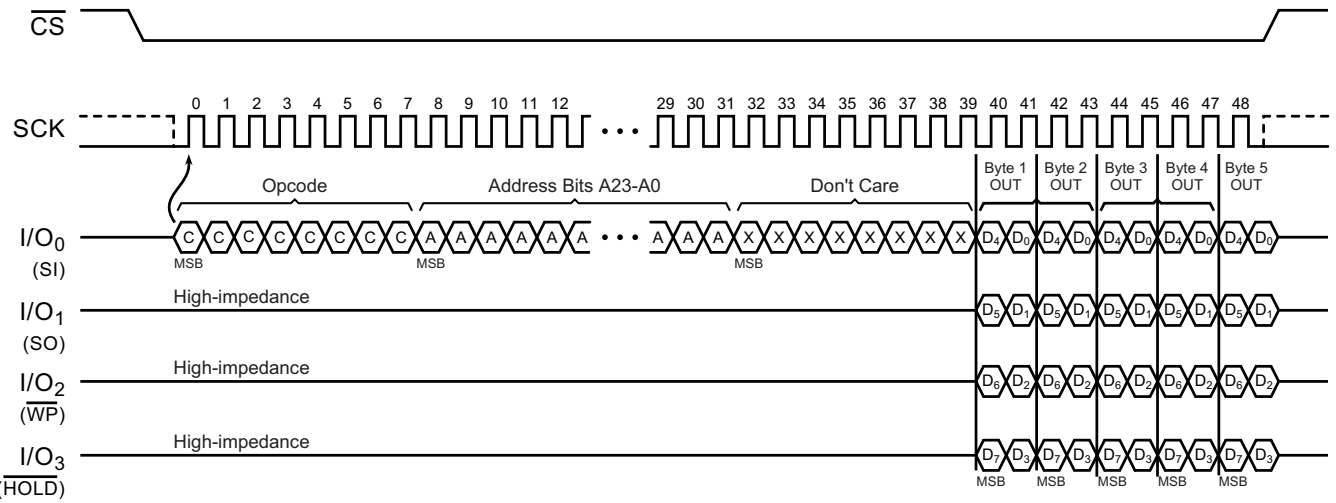


Figure 11. Quad Output Fast Read Sequence Diagram

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8.2.5 Dual I/O Fast Read (BBh)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23 - 0) and a Continuous Read Mode byte 2-bits per clock by SI and SO, each bit being latched in during the rising edge of SCK, then the memory contents are shifted out two bits per clock cycle on the SI and SO pins. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read with Continuous Read Mode

The Dual I/O Fast Read command can further reduce command overhead through setting the Continuous Read Mode bits (M7 - 4) after the inputs 3-byte address A23 - A0).

If the Continuous Read Mode bits (M5:M4) do not equal (1,0), the next command requires the first BBh command code, thus returning to normal operation. A Continuous Read Mode Reset command can be used to reset (M5:M4) before issuing normal command. The command sequence is shown in the following Figure 12.

If the Continuous Read Mode bits (M5:M4) = (1, 0), then the next Dual I/O fast Read command (after $\overline{CS}$ is raised and then lowered) does not require the BBh command code. The command sequence is shown in the following Figure 13.

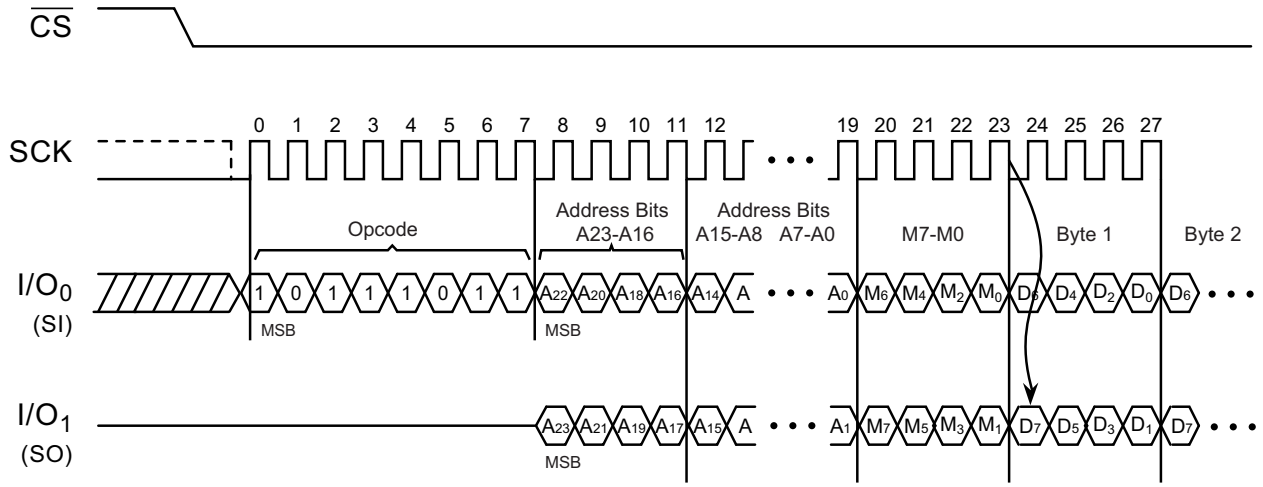


Figure 12. Dual I/O Fast Read Sequence Diagram (Initial command or previous (M5:4) ≠ (1,0))

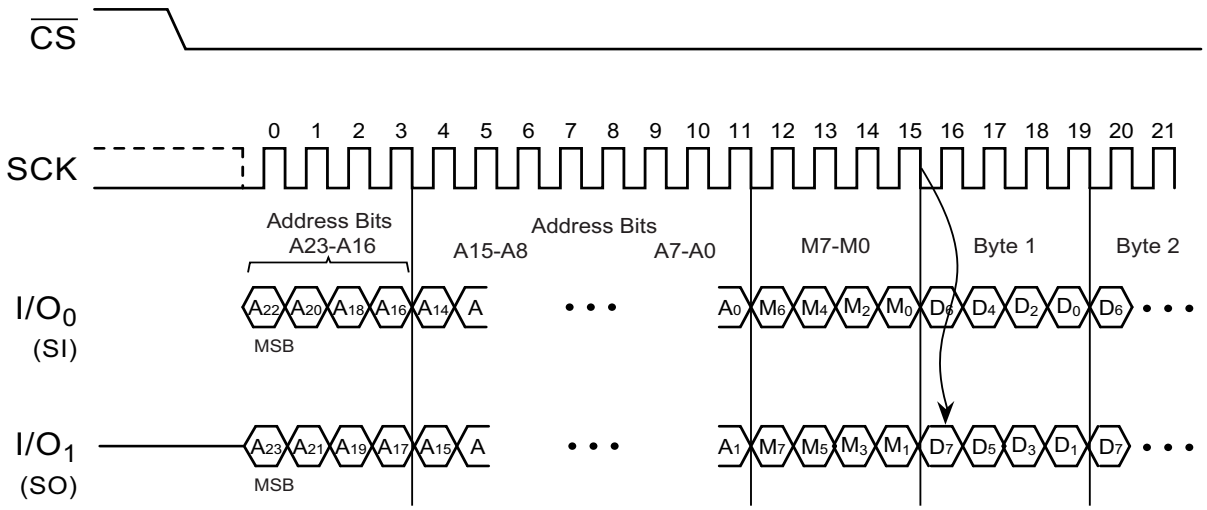


Figure 13. Dual I/O Fast Read Sequence Diagram (Previous command set (M5:4) = (1,0))

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8.2.6 Quad I/O Fast Read (EBh)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a Continuous Read Mode byte and four dummy clocks, each bit being latched in during the rising edge of SCK, then the memory contents are shifted out 4-bit per clock cycle from IO_0, IO_1, IO_2, IO_3. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register must be set to enable for the Quad I/O Fast read command.

Quad I/O Fast Read with Continuous Read Mode

The Quad I/O Fast Read command can further reduce command overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23-0).

If the Continuous Read Mode bits M5-4 do not equal to (1,0), the next command requires the first EBh command code, thus returning to normal operation. A Continuous Read Mode Reset command can also be used to reset (M5-4) before issuing normal command. The command sequence is shown in the followed Figure 14.

If the Continuous Read Mode bits (M5-4) = (1,0), then the next Fast Read Quad I/O command (after $\overline{CS}$ is raised and then lowered) does not require the EBh command code. The command sequence is shown in the followed Figure 15.

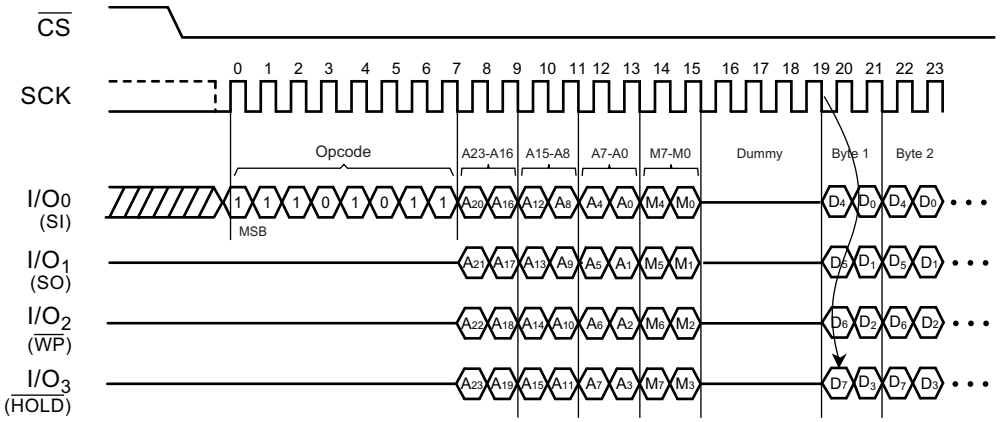


Figure 14. Quad I/O Fast Read Sequence Diagram (Initial command or previous (M5-4) ≠ (1,0))

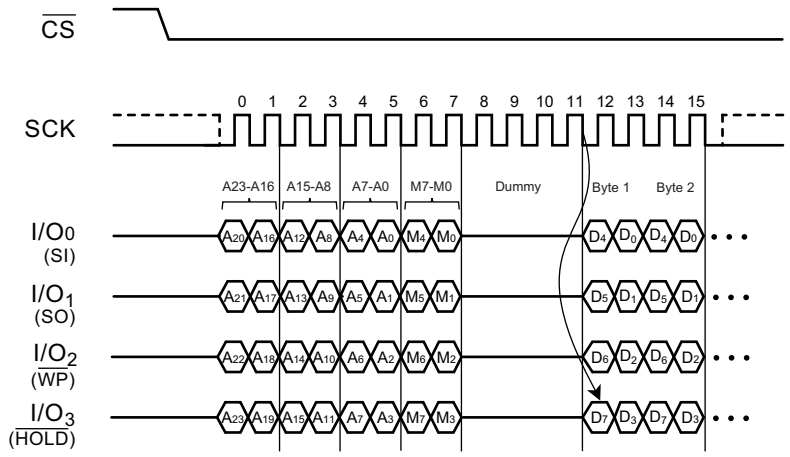


Figure 15. Quad I/O Fast Read Sequence Diagram (Previous command set (M5-4) = (1,0))

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Quad I/O Fast Read with 8/16/32/64-Byte Wrap Around

The Quad I/O Fast Read command can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) command prior to EBh. The Set Burst with Wrap (77h) command can either enable or disable the Wrap Around feature for the following EBh commands.

When Wrap Around is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The Set Burst with Wrap command allows three Wrap Bits, W6-4 to be set. The W4 bit is used to enable or disable the Wrap Around operation while W6-5 are used to specify the length of the wrap around section within a page.

8.2.7 Quad I/O Word Fast Read (E7h)

The Quad I/O Word Fast Read command is similar to the Quad Fast Read command, except that the lowest address bit (A0) must be 0 and there are two dummy clocks. The address automatically increments to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast Read command.

Quad I/O Word Fast Read with Continuous Read Mode

The Quad I/O Word Fast Read command can further reduce command overhead through setting the Continuous Read Mode bits (M7-0) after the input three-byte Address bits (A23-0).

If the Continuous Read Mode bits M5-4 do not equal to (1,0), the next command requires the first E7h command code, thus returning to normal operation. A Continuous Read Mode Reset command can also be used to reset (M5-4) before issuing normal command. The command sequence is shown in the followed Figure 16.

If the Continuous Read Mode bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after $\overline{CS}$ is raised and then lowered) does not require the E7h command code, the command sequence is shown in the followed Figure 17.

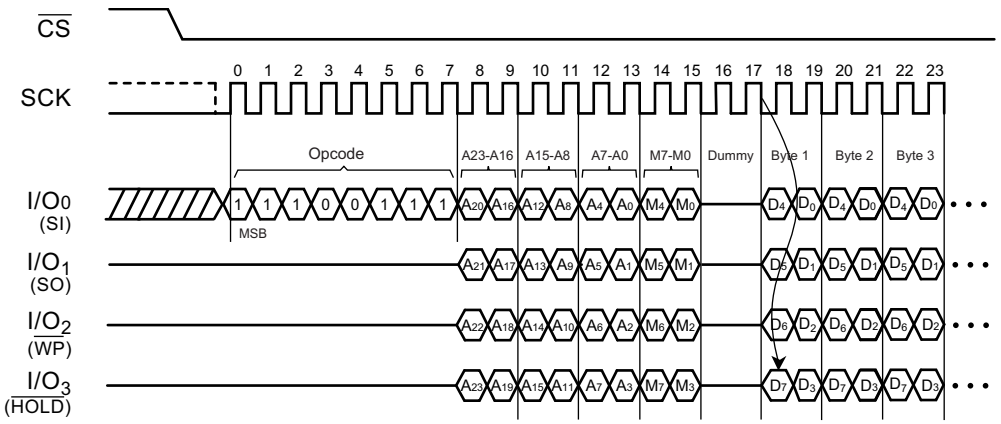


Figure 16. Quad I/O Word Fast Read Sequence Diagram (Initial command or previous (M5-4) ≠ (1,0))

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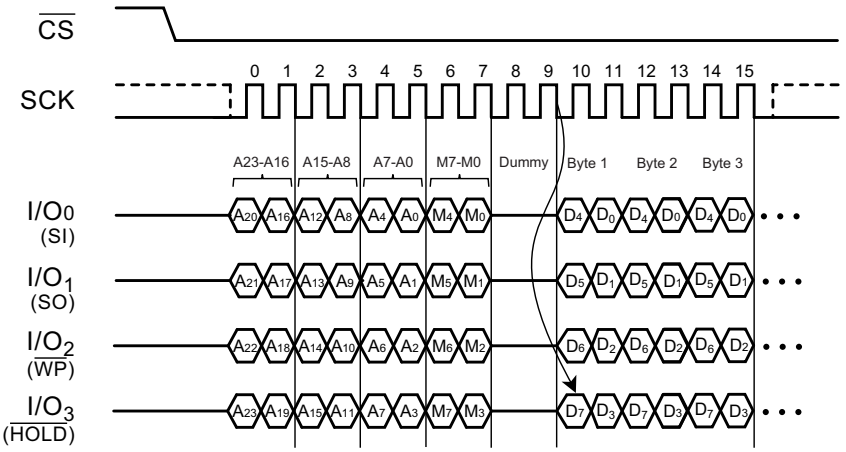


Figure 17. Quad I/O Word Fast Read Sequence Diagram (Previous command set (M5-4) = (1,0))

Quad I/O Word Fast Read with 8/16/32/64-Byte Wrap Around in Standard SPI Mode

The Quad I/O Fast Read command can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) command prior to E7h. The Set Burst with Wrap (77h) command can either enable or disable the Wrap Around feature for the following E7h commands. When Wrap Around is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The Set Burst with Wrap command allows three Wrap Bits, W6-4 to be set. The W4 bit is used to enable or disable the Wrap Around operation while W6-5 are used to specify the length of the wrap around section within a page.

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8.2.8 Set Burst with Wrap (77h)

The Set Burst with Wrap command is used in conjunction with Quad I/O Fast Read and Quad I/O Word Fast Read command to access a fixed length of 8/16/32/64-byte section within a 256-byte page in standard SPI mode. The Set Burst with Wrap command sequence is as follows: $\overline{CS}$ goes low → Send Set Burst with Wrap command → Send 24 Dummy bits → Send 8 Wrap bits → $\overline{CS}$ goes high.

If W6-4 is set by a Set Burst with Wrap command, all the following Fast Read Quad I/O and Word Read Quad I/O commands use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the Wrap Around function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4 = 1. The default value of W4 upon power on is 1.

Table 12. Set Burst with Wrap

W6, W5	W4 = 0		W4 = 1 (Default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

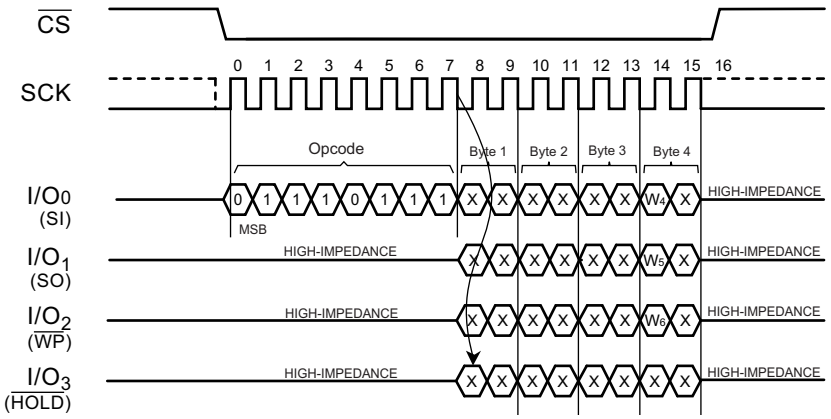


Figure 18. Set Burst with Wrap Sequence Diagram

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8.3 ID and Security Commands

8.3.1 Read Manufacture ID/ Device ID (90h)

The Read Manufacturer/Device ID command is an alternative to the Release from Power-Down/Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 90h followed by a 24-bit address (A23-A0) of 000000h. If the 24-bit address is initially set to 000001h, the Device ID is read first.

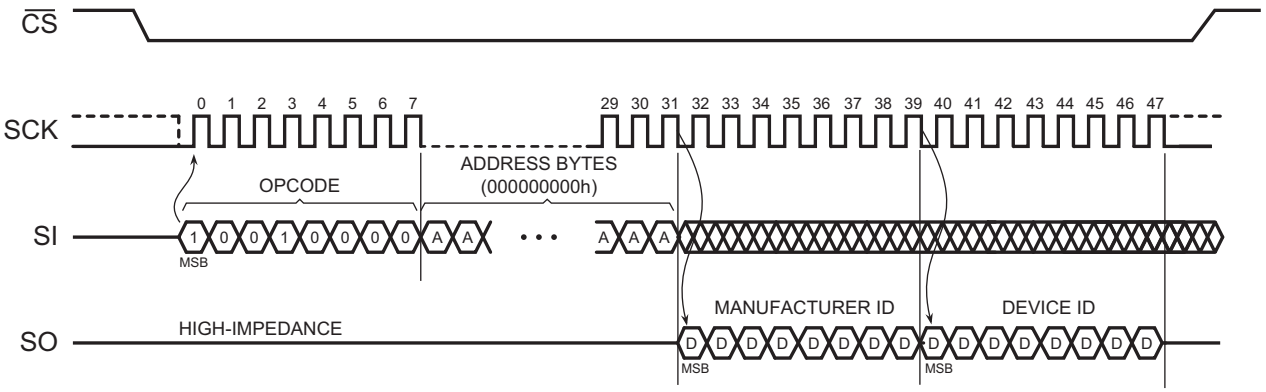


Figure 19. Read Manufacture ID/ Device ID Sequence Diagram

8.3.2 Dual I/O Read Manufacture ID/ Device ID (92h)

The Dual I/O Read Manufacturer/Device ID command is an alternative to the Release from Power-Down/Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by Dual I/O.

The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 92h followed by a 24-bit address (A23 - A0) of 000000h. If the 24-bit address is initially set to 000001h, the Device ID is read first.

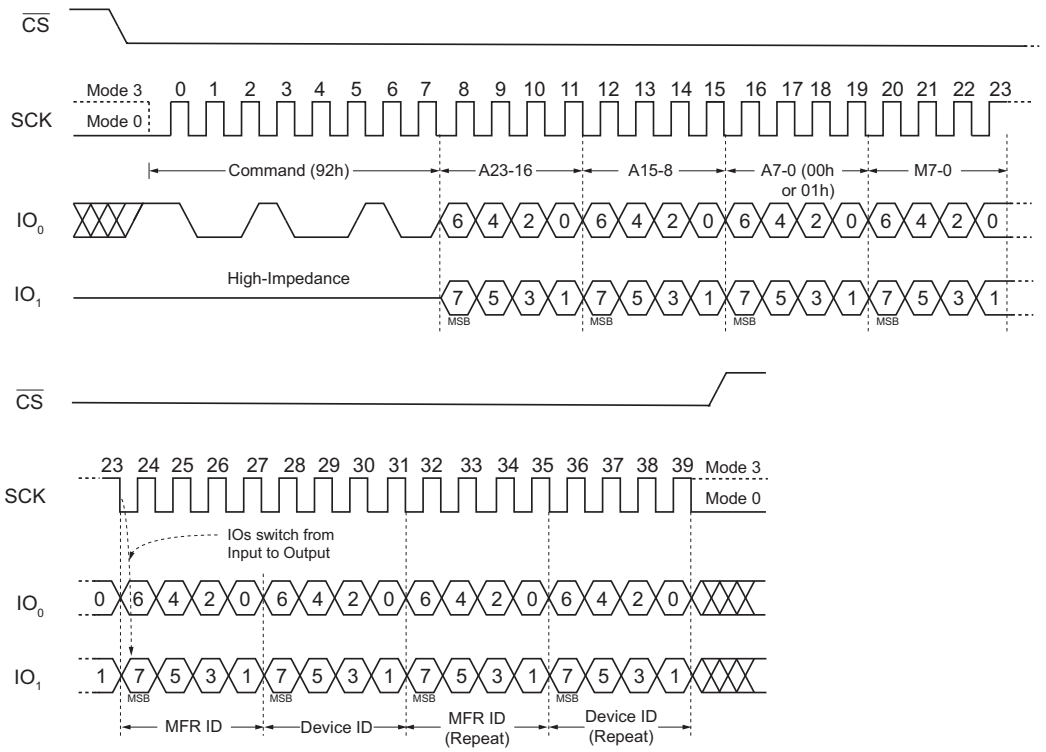


Figure 20. Dual I/O Read Manufacture ID/ Device ID Sequence Diagram

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8.3.3 Quad I/O Read Manufacture ID/ Device ID (94h)

The Quad I/O Read Manufacturer/Device ID command is an alternative to the Release from Power-Down/Device ID command that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O.

The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 94h followed by a 24-bit address (A23 - A0) of 000000h and four dummy clocks. If the 24-bit address is initially set to 000001h, the Device ID is read out first.

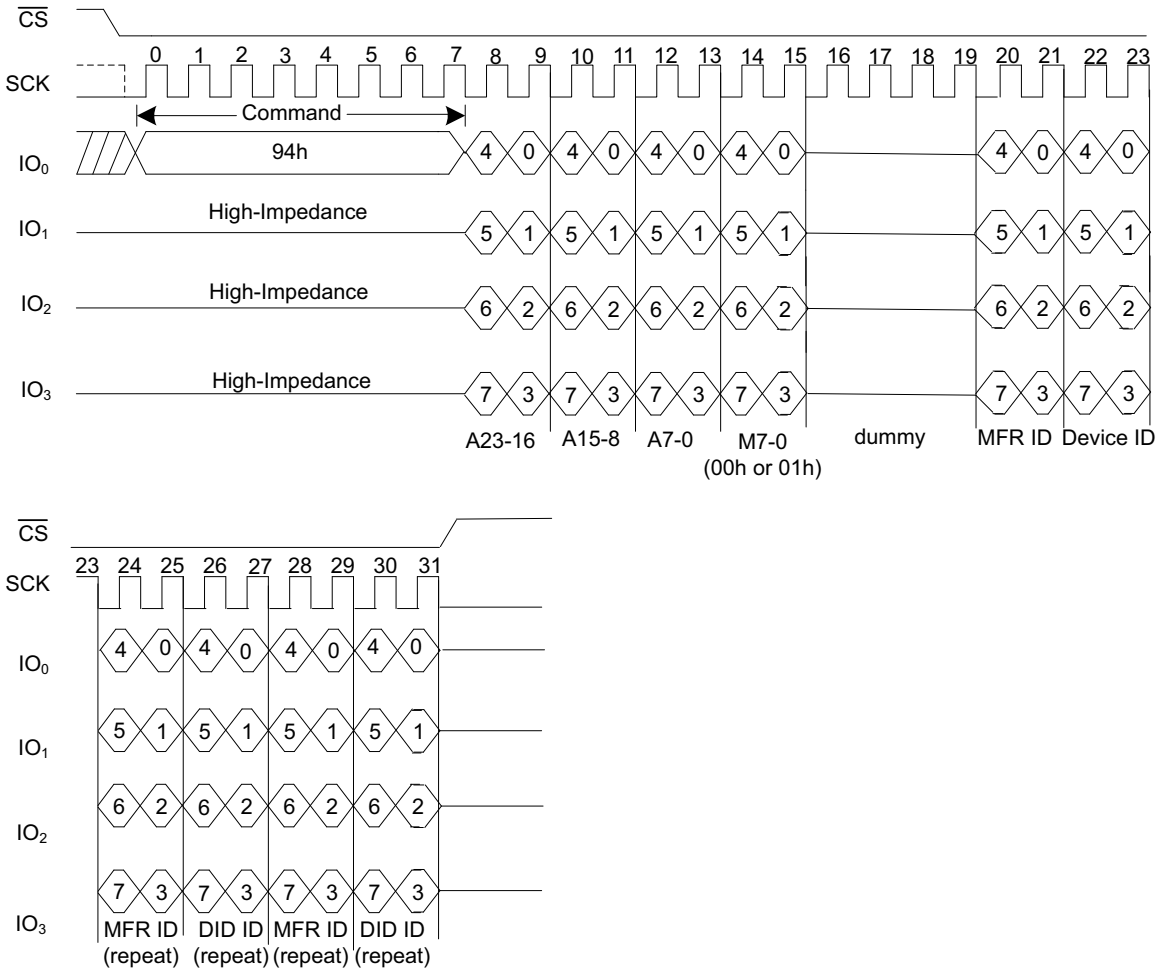


Figure 21. Quad I/O Read Manufacture ID / Device ID Sequence Diagram

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8.3.4 Read JEDEC ID (9Fh)

The JEDEC ID command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. JEDEC ID command while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The JEDEC ID command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving $\overline{CS}$ to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The JEDEC ID command is terminated by driving $\overline{CS}$ to high at any time during data output. When $\overline{CS}$ is driven high, the device is put in the Standby Mode. Once in Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

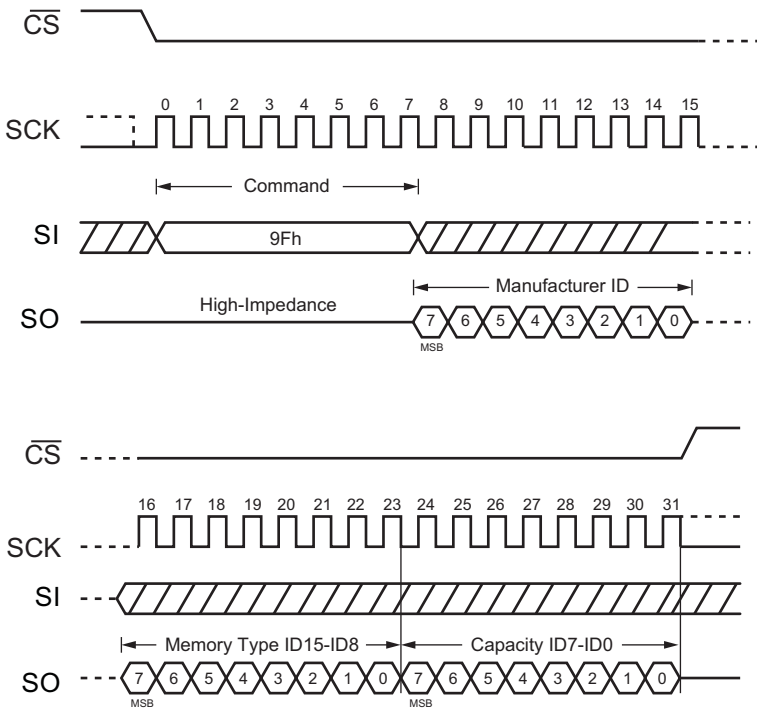


Figure 22. JEDEC ID Sequence Diagram

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8.3.5 Read Unique ID Number (4Bh)

The Read Unique ID Number command accesses a factory-set read-only 64-bit number that is unique to each AT25QF128A device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 4Bh followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of SCK, as shown in Figure 23.

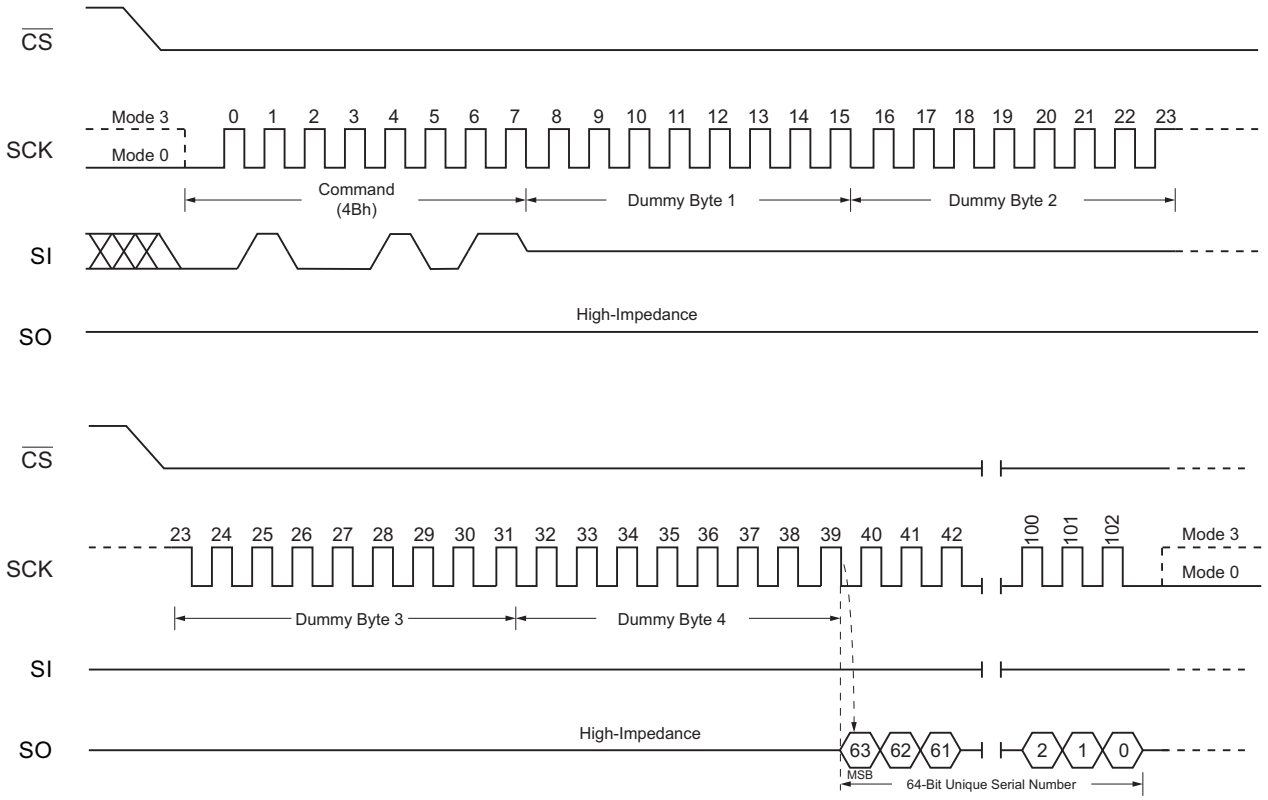


Figure 23. Read Unique ID Sequence Diagram

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8.3.6 Deep Power-Down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down command. The lower power consumption makes the Deep Power-down (DPD) command especially useful for battery powered applications (see ICC1 and ICC2). The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code B9h, as shown in Figure 24.

The $\overline{CS}$ pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power-Down command is not executed. After $\overline{CS}$ is driven high, the power-down state is entered within the time t_{DP}. While in the power-down state, only the Release from Deep Power-down / Device ID command, which restores the device to normal operation, is recognized. All other Commands are ignored. This includes the Read Status Register command, which is always available during normal operation. Ignoring all but one command also makes the Power-Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

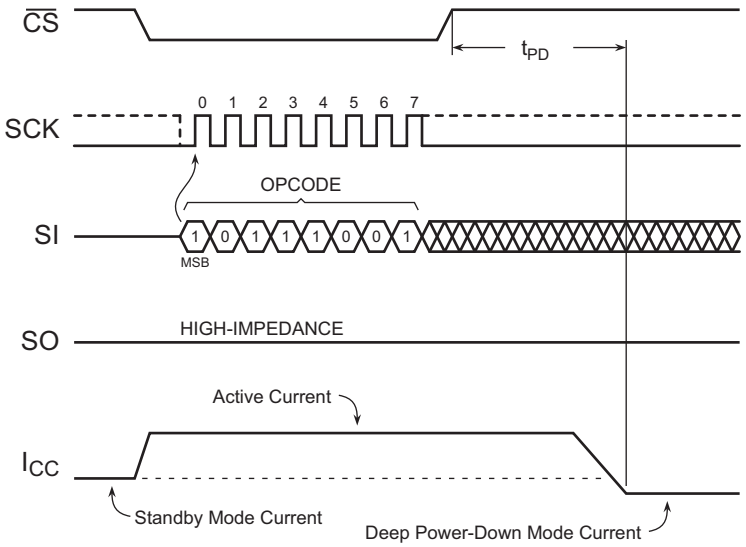


Figure 24. Deep Power-Down Sequence Diagram

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8.3.7 Release from Deep Power-Down/Read Device ID (ABh)

The Release from Power-Down or Device ID command is a multi-purpose command. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

To release the device from the Power-Down state, the command is issued by driving the $\overline{CS}$ pin low, shifting the command code ABh and driving $\overline{CS}$ high Release from Power-Down takes time t_{RES1} (see Section 9.8, AC Electrical Characteristics) before the device resumes normal operation and other command are accepted. The $\overline{CS}$ pin must remain high during t_{RES1}.

When used only to obtain the Device ID while not in the Power-Down state, the command is initiated by driving the $\overline{CS}$ pin low and shifting the command code ABh followed by three dummy bytes. The Device ID bits are then shifted out on the falling edge of SCK with most significant bit (MSB) first, as shown in Figure 25. The Device ID value for the AT25QF128A is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving $\overline{CS}$ high.

When used to release the device from the Power-Down state and obtain the Device ID, the command is the same as previously described, and shown in Figure 25, except that after $\overline{CS}$ is driven high it must remain high for a time of t_{RES2} (see Section 9.8, AC Electrical Characteristics), as shown in Figure 26. After this time, the device resumes normal operation and other commands are accepted. If the Release from Power-Down/Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and does not effect the current cycle.

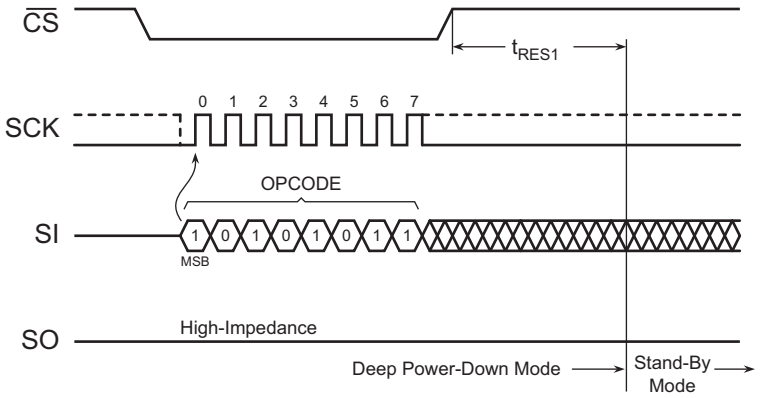


Figure 25. Release Power-Down Sequence Diagram

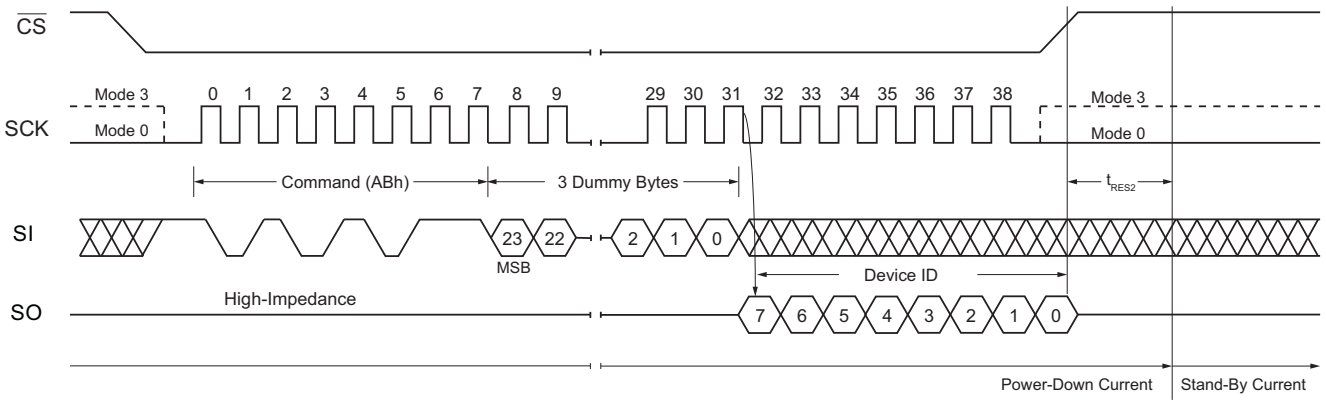


Figure 26. Release Power-Down and Read Device ID Sequence Diagram

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8.3.8 Read Security Registers (48h)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23 - A0) and a dummy byte, each bit being latched-in during the rising edge of SCK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C, during the falling edge of SCK. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out. Once the A7 - A0 address reaches the last byte of the register (Byte FFh), it resets to 000h, the command is completed by driving $\overline{CS}$ high.

Table 13. Read Security Registers

Address	A23-A16	A15-A12	A11-A8	A7-A0
Security Registers 1	00h	0001	0000	Byte Address
Security Registers 2	00h	0010	0000	Byte Address
Security Registers 3	00h	0011	0000	Byte Address

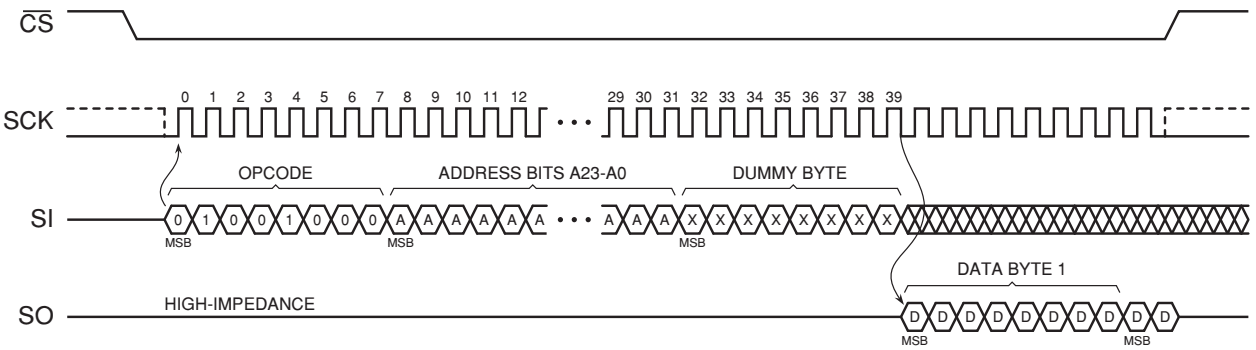


Figure 27. Read Security Registers Command Sequence Diagram

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8.3.9 Erase Security Registers (44h)

The AT25QF128A provides three 256-byte Security Registers which can be erased and programmed individually. These registers can be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable command must previously have been executed to set the Write Enable Latch bit.

The Erase Security Registers command sequence: $\overline{CS}$ goes low → sending Erase Security Registers command → $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the command code has been latched in otherwise the Erase Security Registers command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Erase Security Registers cycle (whose duration is t_{SE}) is initiated. While the Erase Security Registers cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers are permanently locked; the Erase Security Registers command is ignored.

Table 14. Erase Security Registers

Address	A23 - A16	A15 - A12	A11 - A8	A7 - A0
Security Registers 1	00h	0001	0000	Byte Address
Security Registers 2	00h	0010	0000	Byte Address
Security Registers 3	00h	0011	0000	Byte Address

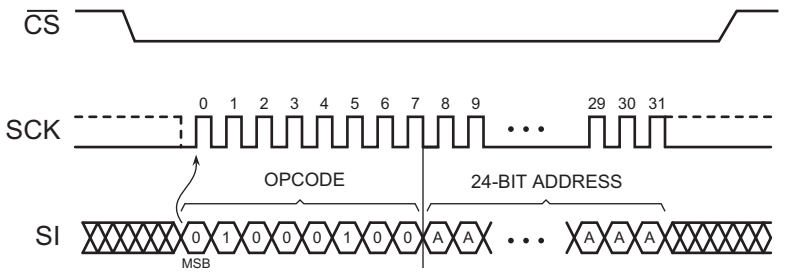


Figure 28. Erase Security Registers Command Sequence Diagram

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8.3.10 Program Security Registers (42h)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 256 bytes Security Registers data to be programmed. A Write Enable command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command.

The Program Security Registers command is entered by driving $\overline{CS}$ low, followed by the command code (42h), a 3-byte address and at least one data byte on the SI pin. As soon as $\overline{CS}$ is driven high, the self-timed Program Security Registers cycle (whose duration is t_{PP}) is initiated. While the Program Security Registers cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

If the Security Registers Lock Bit (LB3/LB2/LB1) bits are set to 1, the Security Registers are permanently locked. The Program Security Registers command is ignored.

Table 15. Program Security Registers

Address	A23 - A16	A15 - A12	A11 - A8	A7 - A0
Security Registers 1	00h	0001	0000	Byte Address
Security Registers 2	00h	0010	0000	Byte Address
Security Registers 3	00h	0011	0000	Byte Address

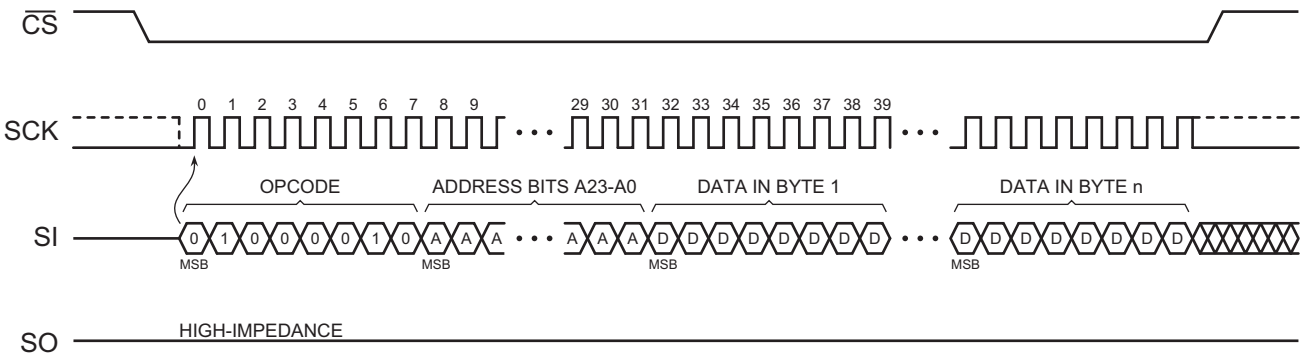


Figure 29. Program Security Registers Command Sequence Diagram

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8.3.11 Enable Reset (66h) and Reset Device (99h)

Because of the small package and the limitation on the number of pins, the AT25QF128A provides a software Reset command instead of a dedicated RESET pin. Once the software Reset command is accepted, any on-going internal operations are terminated and the device returns to its default power-on state and loses all of the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).

To avoid accidental reset, both Enable Reset (66h) and Reset (99h) commands must be issued in sequence. Any other commands other than Reset (99h) after the Enable Reset (66h) command disable the Reset Enable state. A new sequence of Enable Reset (66h) and Reset (99h) is needed to reset the device. Once the Reset command is accepted by the device, the device takes approximately 30 µs to reset. During this period, no commands are accepted.

The Enable Reset (66h) and Reset (99h) command sequence is shown in Figure 30.

Data corruption can happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

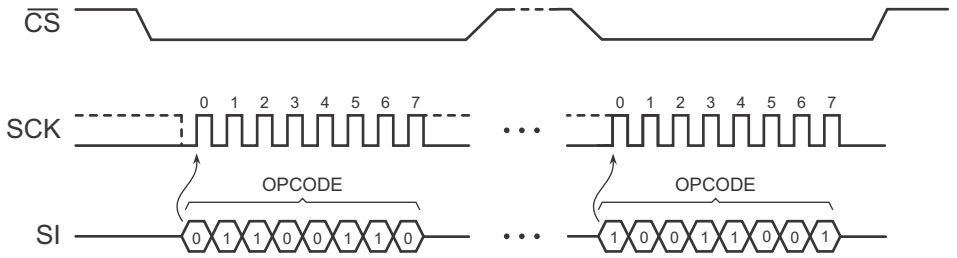


Figure 30. Enable Reset (66h) and Reset (99h) Command Sequence

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8.4 Program and Erase Commands

8.4.1 Page Program (02h)

The Page Program command is for programming the memory. A Write Enable command must previously have been executed to set the Write Enable Latch bit before sending the Page Program command.

The Page Program command is entered by driving $\overline{CS}$ low, followed by the command code, 3-byte address and at least one data byte on SI. If the 8 least significant address bits (A7 - A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7 - A0) are all zero). $\overline{CS}$ must be driven low for the entire duration of the sequence. The Page Program command sequence: $\overline{CS}$ goes low → sending Page Program command → 3-byte address on SI → at least 1 byte of data on SI → $\overline{CS}$ goes high.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. $\overline{CS}$ must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program command is not executed.

As soon as $\overline{CS}$ is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register can be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

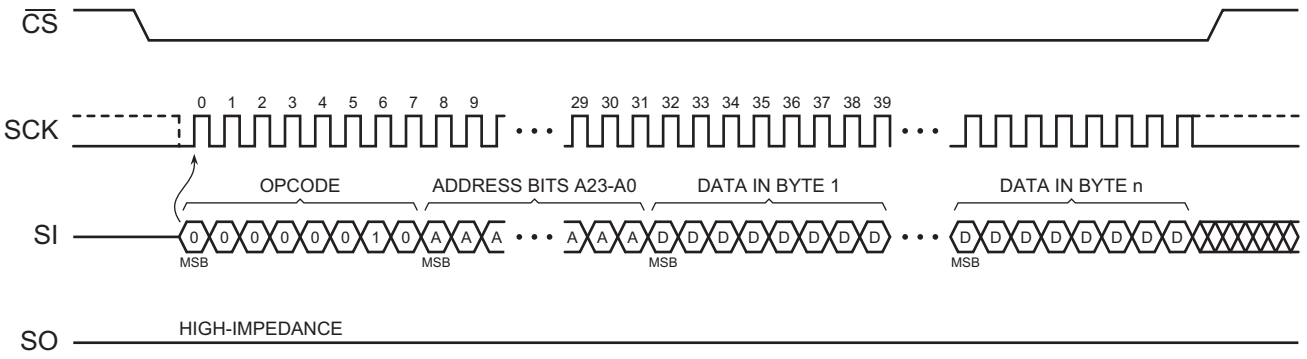


Figure 31. Page Program Sequence Diagram

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8.4.2 Quad Page Program (32h)

The Quad Page Program command is for programming the memory using for pins: IO_0, IO_1, IO_2 and IO_3. To use Quad Page Program the Quad Enable (QE) bit in the Status register must be set (QE = 1). A Write Enable command must previously have been executed to set the Write Enable Latch bit before sending the Page Program command. The Quad Page Program command is entered by driving $\overline{CS}$ low, followed by the command code (32h), three address bytes and at least one data byte on IO pins.

The command sequence is shown in Figure 32. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. $\overline{CS}$ must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program command is not executed.

As soon as $\overline{CS}$ is driven high, the self-timed Quad Page Program cycle (whose duration is t_{PP}) is initiated. While the Quad Page Program cycle is in progress, the Status Register can be read to check the value of the Write in Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

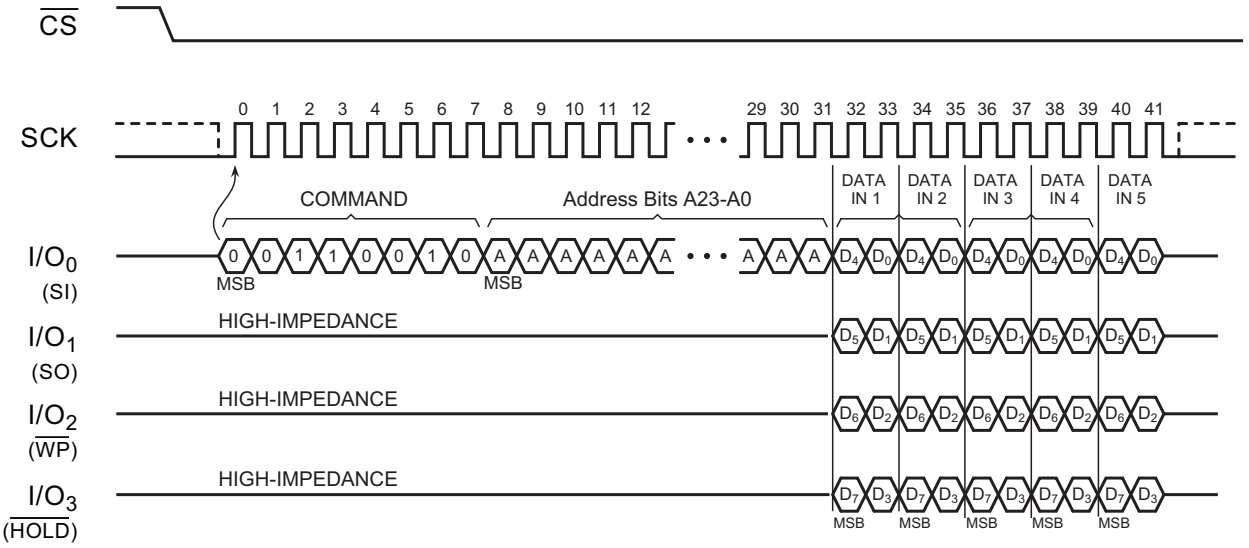


Figure 32. Quad Page Program Sequence Diagram

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8.4.3 Fast Page Program (F2h)

The Fast Page Program command is used to program the memory. A Write Enable command must previously have been executed to set the WEL bit before sending the Page Program command.

The Fast Page Program command is entered by driving $\overline{CS}$ low, followed by the command code, 3-byte address and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). $\overline{CS}$ must be driven low for the entire duration of the sequence.

The Fast Page Program command sequence: $\overline{CS}$ goes low → sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → $\overline{CS}$ goes high.

The command sequence is shown in Figure 33. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. $\overline{CS}$ must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Fast Page Program command is not executed.

As soon as $\overline{CS}$ is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register can be read to check the value of the Write-in-Progress (WIP) bit. The WIP bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset.

A Fast Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

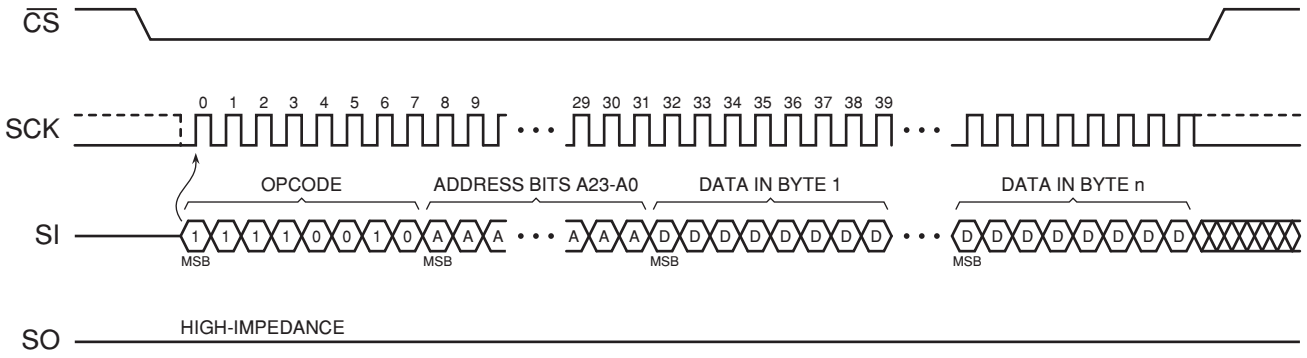


Figure 33. Fast Page Program Sequence Diagram

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8.4.4 Sector Erase (20h)

The Sector Erase command is for erasing the all data of the chosen sector. A Write Enable command must previously have been executed to set the Write Enable Latch bit. The Sector Erase command is entered by driving $\overline{CS}$ low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase command. $\overline{CS}$ must be driven low for the entire duration of the sequence.

The Sector Erase command sequence: $\overline{CS}$ goes low → sending Sector Erase command → 3-byte address on SI → $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Sector Erase cycle (whose duration is t_{SE}) is initiated. While the Sector Erase cycle is in progress, the Status Register can be read to check the value of the Write-in-Progress (WIP) bit. The WIP bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

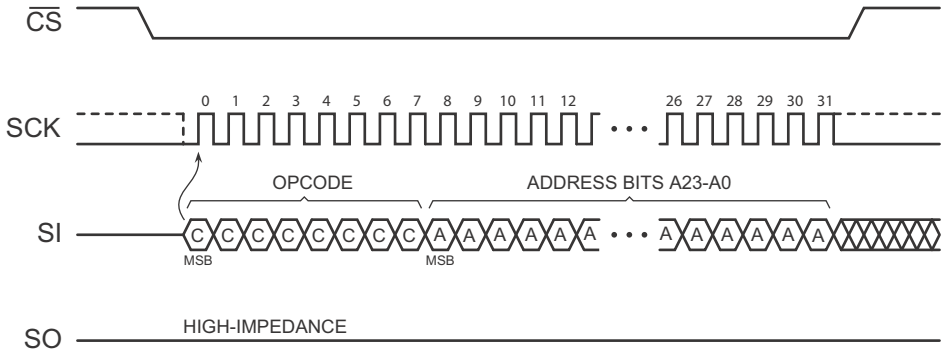


Figure 34. Sector Erase Sequence Diagram

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8.4.5 32 kB Block Erase (52h)

The 32 kB Block Erase command is for erasing all data of a chosen block. A Write Enable command must have been previously executed to set the WEL bit. The 32 kB Block Erase command is entered by driving $\overline{CS}$ low, followed by the command code, and 3-byte address on SI. Any address inside the block is a valid address for the 32 kB Block Erase command. $\overline{CS}$ must be driven low for the entire duration of the sequence.

The 32 kB Block Erase command sequence: $\overline{CS}$ goes low → sending 32 kB Block Erase command → 3-byte address on SI → $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32 kB Block Erase command is not executed.

As soon as $\overline{CS}$ is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Write-in-Progress (WIP) bit. The WIP bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32 kB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

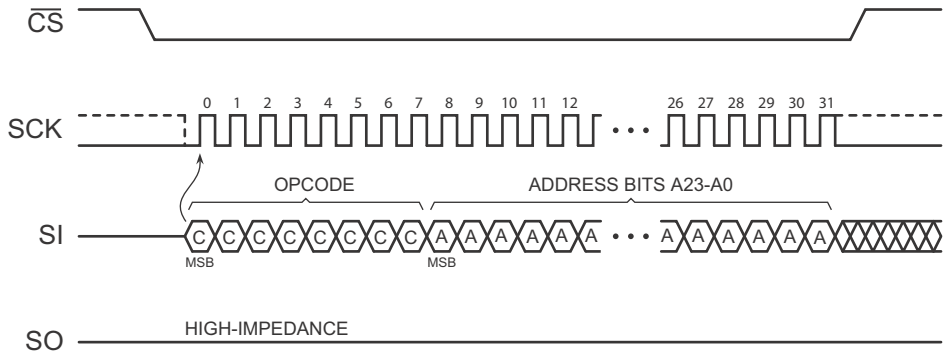


Figure 35. 32 kB Block Erase Sequence Diagram

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8.4.6 64 kB Block Erase (D8h)

The 64 kB Block Erase command is for erasing the all data of the chosen block. A Write Enable command must previously have been executed to set the WEL bit. The 64 kB Block Erase command is entered by driving $\overline{CS}$ low, followed by the command code, and 3-byte address on SI. Any address inside the block is a valid address for the 64 kB Block Erase command. $\overline{CS}$ must be driven low for the entire duration of the sequence.

The 64 kB Block Erase command sequence: $\overline{CS}$ goes low sending 64 kB Block Erase command 3-byte address on SI $\overline{CS}$ goes high. $\overline{CS}$ must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64 kB Block Erase command is not executed. As soon as $\overline{CS}$ is driven high, the self-timed Block Erase cycle (whose duration is t_{BE}) is initiated.

While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Write-in-Progress (WIP) bit. The WIP bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the WEL bit is reset. A 64 kB Block Erase command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits is not executed.

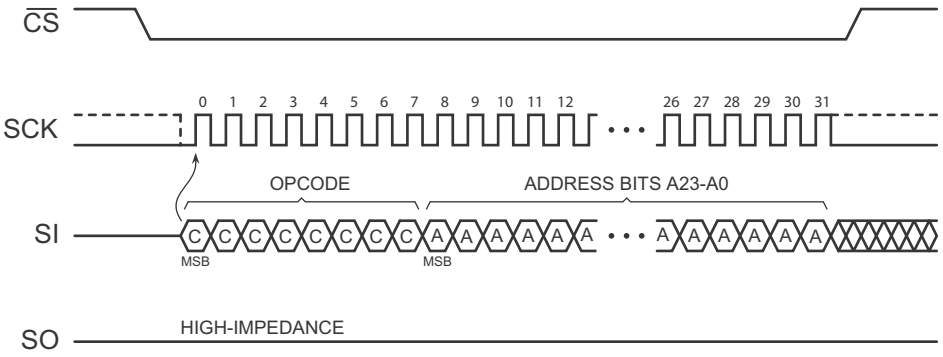


Figure 36. 64 kB Block Erase Sequence Diagram

8.4.7 Chip Erase (60/C7h)

The Chip Erase command sets all memory within the device to the erased state of all 1s (FFh). A Write Enable command must be executed before the device accepts the Chip Erase Command (Status Register bit WEL must equal 1). The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code C7h or 60h. The Chip Erase command sequence is shown in Figure 37.

The $\overline{CS}$ pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase command is not executed. After $\overline{CS}$ is driven high, the self-timed Chip Erase command commences for a time of t_{CE}. While the Chip Erase cycle is in progress, the Read Status Register command can still be accessed to check the status of the WIP bit.

The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other Commands again. After the Chip Erase cycle has finished the WEL bit in the Status Register is cleared to 0. The Chip Erase command is executed only if all Block Protect (BP2, BP1, and BP0) bits are 0. The Chip Erase command is ignored if one or more sectors are protected.

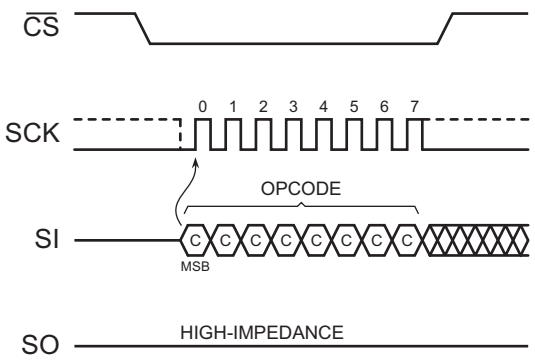


Figure 37. Chip Erase Sequence Diagram

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8.4.8 Erase / Program Suspend (75h)

The Erase/Program Suspend command allows the system to interrupt a Sector or Block Erase operation, then read from or program data to any other sector. The Erase/Program Suspend command also allows the system to interrupt a Page Program operation and then read from any other page or erase any other sector or block. The Erase/Program Suspend command sequence is shown in Figure 38.

The Write Status Registers command (01h) and Erase commands (20h, D8h, C7h, 60h, 44h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend command is ignored. The Write Status Registers command (01h), and Program commands (02h, 42h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program operation.

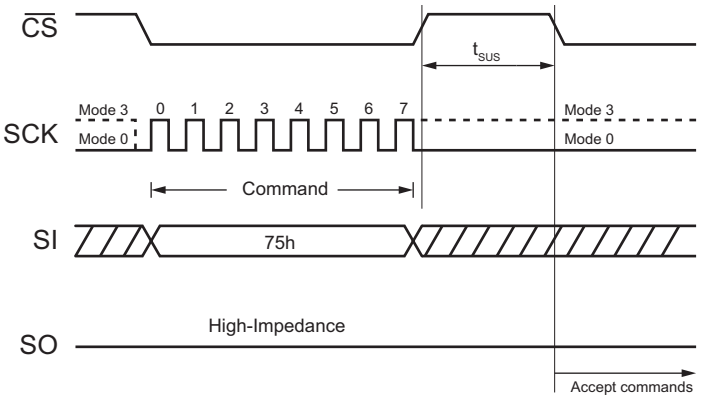


Figure 38. Erase/Program Suspend Command Sequence

Note: Repeated suspend/resume sequences might significantly impact progress of the erase or program operation. To ensure timely completion of the erase or program operation, limit the number of suspend/resume sequences during the same erase or program operation, or, alternatively, provide sufficient time (up to 60 ms) after a resume operation to allow the erase or program operation to complete.

A read operation from a physical block that includes a suspended area might provide unreliable data. For the definition of the physical block and for the techniques to ensure high data integrity, see application note AN-500.

8.4.9 Erase / Program Resume (7Ah)

The Erase/Program Resume command 7Ah must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume command 7Ah is accepted by the device only if the SUS bit in the Status Register equals to 1 and the WIP bit equals to 0.

After the Resume command is issued the SUS bit is cleared from 1 to 0 immediately, the WIP bit is set from 0 to 1 within 200 ns and the Sector or Block completes the erase operation or the page completes the program operation. If the SUS bit equals to 0 or the WIP bit equals to 1, the Resume command 7Ah is ignored by the device. The Erase/Program Resume command sequence is shown in Figure 39.

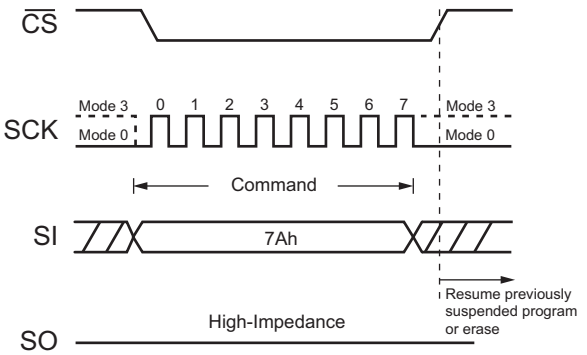


Figure 39. Erase/Program Resume Command Sequence

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8.4.10 Read Serial Flash Discoverable Parameter (5Ah)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial Flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. For more detail on the SFDP parameters, contact Renesas Electronics.

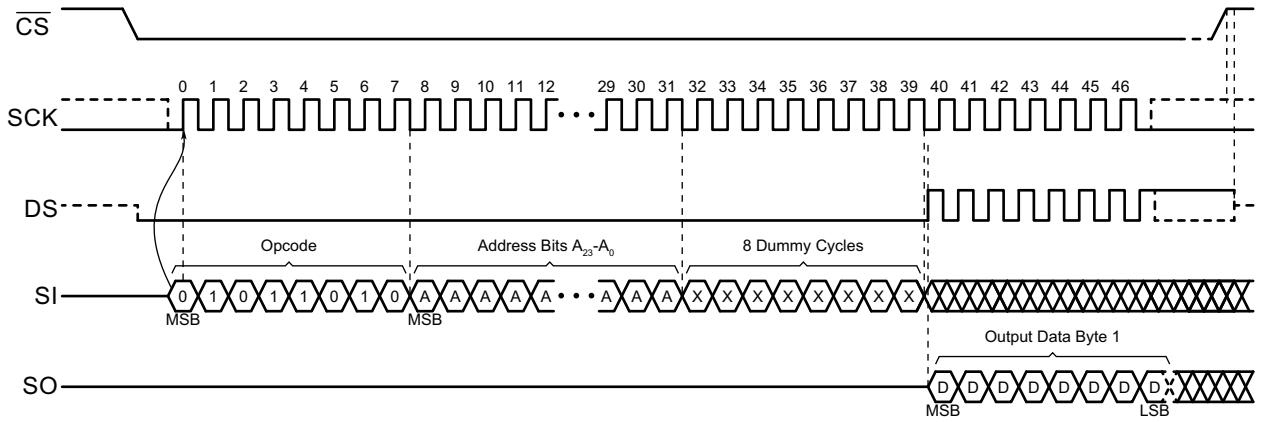


Figure 40. Read Serial Flash Discoverable Parameter Command Sequence Diagram

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9. Electrical Characteristics

9.1 Absolute Maximum Ratings

Table 16. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Range	Units
Supply Voltage	VCC		-0.5 to 4	V
Voltage Applied to Any Pin	VIO	Relative to Ground	-0.5 to 4	V
Transient Voltage on any Pin	VIOT	<20 ns Transient Relative to Ground	-2.0 to VCC + 2.0	V
Storage Temperature	TSTG		-65 to +150	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(1)	-2000 to +2000	V

1. JEDEC Std JESD22-A114 (C1 = 100 pF, R1 = 1500Ω, R2 = 500Ω).

9.2 Operating Ranges

Table 17. Operating Range

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	VCC		2.7	3.6	V
Operating Temperature	TA	Industrial	-40	+85	°C
		Extended	-40	+105	°C

9.3 Data Retention and Endurance

Table 18. Data Retention and Endurance

Parameter	Condition	Max Temperature	Min	Max	Units
Erase/Program Cycles	4 kB sector, 32/64 kB block, or full chip	85 °C	100,000		Cycles
		105 °C	10,000		Cycles
Data Retention	Full temperature range	85 °C	20		Years
		105 °C	10		Years

9.4 Latch Up Characteristics

Table 19. Latch-up Characteristics

Parameter	Min	Max
Input Voltage Respect To GND on I/O Pins	-1.0V	VCC + 1.0V
VCC Current	-100 mA	100 mA

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9.5 Power-up Timing

Table 20. Power-up Timing

Symbol	Parameter	Min	Max	Unit
t_{VSL}	VCC (min) To $\overline{CS}$ low	300		us

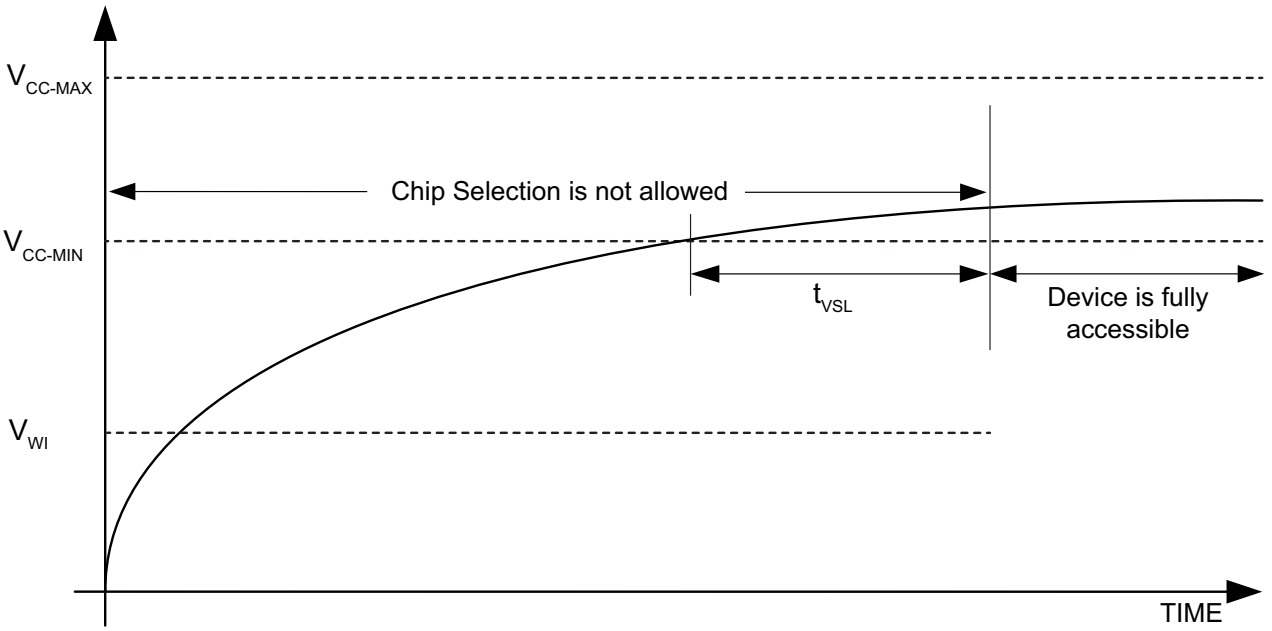


Figure 41. Power-up Timing and Voltage Levels

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9.6 DC Electrical Characteristics

Table 21 shows the DC electrical characteristics at 85 ºC.

Table 21. DC Electrical Characteristics — 85 °C

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{LI}	Input Leakage Current				±2	µA
I_{LO}	Output Leakage Current				±2	µA
ICC_1	Standby Current	$\overline{CS}$ = VCC, VIN = VCC or GND		13	25	µA
ICC_2	Deep Power-Down Current	$\overline{CS}$ = VCC, VIN = VCC or GND		2	5	µA
ICC_3	Operating Current: (Read)	SCK = 0.1VCC/0.9VCC, at 120 MHz, Q = Open (*1,*,2*4 I/O)		12	18	mA
		SCK = 0.1VCC/0.9VCC, at 80MHz,Q = Open (*1,*,2*4 I/O)		10	16	mA
ICC_4	Operating Current (Page Program)	$\overline{CS}$ = VCC		15	20	mA
ICC_5	Operating Current (WRSR)	$\overline{CS}$ = VCC			5	mA
ICC_6	Operating Current (Sector Erase)	$\overline{CS}$ = VCC		9	20	mA
ICC_7	Operating Current (Block Erase)	$\overline{CS}$ = VCC		9	20	mA
ICC_8	Operating Current (Chip Erase)	$\overline{CS}$ = VCC		9	20	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.8 VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	IOL = 100 µA			0.4	V
V_{OH}	Output High Voltage	IOH = -100 µA	VCC-0.2			V

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Table 22 shows the DC electrical characteristics at 105 °C.

Table 22. DC Electrical Characteristics — 105 °C

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
I_{LI}	Input Leakage Current				±2	µA
I_{LO}	Output Leakage Current				±2	µA
ICC_1	Standby Current	$\overline{CS}$ = VCC, VIN = VCC or GND		20	30	µA
ICC_2	Deep Power-Down Current	$\overline{CS}$ = VCC, VIN = VCC or GND		5	8	µA
ICC_3	Operating Current: (Read)	SCK = 0.1VCC/0.9VCC, at 120 MHz, Q = Open (*1,*,2*4 I/O)		12	18	mA
		SCK = 0.1VCC/0.9VCC, at 80MHz, Q = Open(*1,*,2*4 I/O)		10	16	mA
ICC_4	Operating Current (Page Program)	$\overline{CS}$ = VCC		15	20	mA
ICC_5	Operating Current (WRSR)	$\overline{CS}$ = VCC			5	mA
ICC_6	Operating Current (Sector Erase)	$\overline{CS}$ = VCC		9	20	mA
ICC_7	Operating Current (Block Erase)	$\overline{CS}$ = VCC		9	20	mA
ICC_8	Operating Current (Chip Erase)	$\overline{CS}$ = VCC		9	20	mA
V_{IL}	Input Low Voltage		-0.5		0.2VCC	V
V_{IH}	Input High Voltage		0.8VCC		VCC+0.4	V
V_{OL}	Output Low Voltage	IOL = 100 µA			0.4	V
V_{OH}	Output High Voltage	IOH = -100 µA	VCC-0.2			V

9.7 AC Measurement Conditions

Table 23. AC Measurement Conditions

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_L	Load Capacitance			30	pF	
t_R, t_F	Input Rise and Fall time			5	ns	
V_{IN}	Input Pause Voltage	0.2VCC to 0.8VCC			V	
IN	Input Timing Reference Voltage	0.5VCC			V	
OUT	Output Timing Reference Voltage	0.5VCC			V	

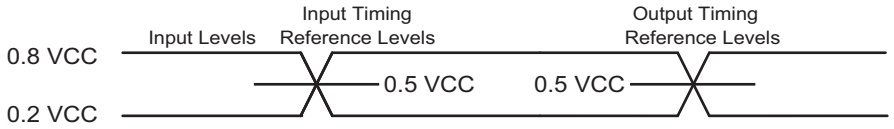


Figure 42. AC Measurement I/O Waveform

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9.8 AC Electrical Characteristics

Table 24 shows the AC electrical characteristics at 85 °C.

Table 24. AC Electrical Characteristics — 85 °C

Symbol	Parameter	Min	Typ	Max	Units
Fc_1	Clock frequency for Quad Output Fast Read (6Bh) on 3.0V - 3.6V power supply.	DC		133	MHz
Fc_2	Clock frequency for Read Data (03h) on 2.7V - 3.6V power supply.	DC		70	MHz
Fc_3	Clock frequency except for Quad Output Fast Read (6Bh) or Read Data (03h) on 3.0V - 3.6V power supply.	DC		120	MHz
Fc_4	Clock frequency except for Read Data (03h) on 2.7V - 3.6V power supply.	DC		108	MHz
t_{CLH}	Serial Clock High Time	3.75			ns
t_{CLL}	Serial Clock Low Time	3.75			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.1 [1]			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.1 [1]			V/ns
t_{SLCH}	$\overline{CS}$ Active Setup Time	5			ns
t_{CHSH}	$\overline{CS}$ Active Hold Time	5			ns
t_{SHCH}	$\overline{CS}$ Not Active Setup Time	5			ns
t_{CHSL}	$\overline{CS}$ Not Active Hold Time	5			ns
t_{SHSL}	$\overline{CS}$ High Time (read/write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	0			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}	$\overline{HOLD}$ Low Setup Time (relative to Clock)	5			ns
t_{HHCH}	$\overline{HOLD}$ High Setup Time (relative to Clock)	5			ns
t_{CHHL}	$\overline{HOLD}$ High Hold Time (relative to Clock)	5			ns
t_{CHHH}	$\overline{HOLD}$ Low Hold Time (relative to Clock)	5			ns
t_{HLQZ}	$\overline{HOLD}$ Low To High-Z Output			6	ns
t_{HHQX}	$\overline{HOLD}$ Low To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid			7	ns
t_{WHSL}	Write Protect Setup Time Before $\overline{CS}$ Low	20			ns
t_{SHWL}	Write Protect Hold Time After $\overline{CS}$ High	100			ns
t_{DP}	$\overline{CS}$ High To Deep Power-Down Mode			20	µs
t_{RES1}	$\overline{CS}$ High To Standby Mode Without Electronic Signature Read			20	µs
t_{RES2}	$\overline{CS}$ High To Standby Mode With Electronic Signature Read			20	µs
t_{SUS}	$\overline{CS}$ High To Next Command After Suspend			20	µs
t_{RST_R}	$\overline{CS}$ High To Next Command After Reset (from read)			20	
t_{RST_P}	$\overline{CS}$ High To Next Command After Reset (from program)			20	
t_{RST_E}	$\overline{CS}$ High To Next Command After Reset (from erase)			12	
t_W	Write Status Register Cycle Time		5	30	ms
t_{BP1}	Byte Program Time (First Byte)		30	50(2)	µs
t_{BP2}	Additional Byte Program Time (After First Byte)		2.5	12(2)	µs
t_{PP}	Page Programming Time		0.6	2.4	ms
t_{SE}	Sector Erase Time		70	300	ms
t_{BE}	Block Erase Time (32K Bytes/64K Bytes)		0.15/0.25	1.6/2.0	sec
t_{CE}	Chip Erase Time		30	120	sec

1. Tested with clock frequency lower than 50 MHz.
2. For multiple bytes after first byte within a page, $t_{BPn} = t_{BP1} + t_{BP2} * N$, where N is the number of bytes programmed.

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Table 25 shows the AC electrical characteristics at 105 °C.

Table 25. AC Electrical Characteristics — 105 °C

Symbol	Parameter	Min	Typ	Max	Units
Fc_1	Clock frequency for Quad Output Fast Read (6Bh) on 3.0V - 3.6V power supply.	DC		120	MHz
Fc_2	Clock frequency for Read Data (03h) on 2.7V - 3.6V power supply.	DC		70	MHz
Fc_3	Clock frequency except for Quad Output Fast Read (6Bh) or Read Data (03h) on 3.0V - 3.6V power supply.	DC		120	MHz
Fc_4	Clock frequency except for Read Data (03h) on 2.7V - 3.6V power supply.	DC		108	MHz
t_{CLH}	Serial Clock High Time	4			ns
t_{CLL}	Serial Clock Low Time	4			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.1(1)			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.1(1)			V/ns
t_{SLCH}	$\overline{CS}$ Active Setup Time	5			ns
t_{CHSH}	$\overline{CS}$ Active Hold Time	5			ns
t_{SHCH}	$\overline{CS}$ Not Active Setup Time	5			ns
t_{CHSL}	$\overline{CS}$ Not Active Hold Time	5			ns
t_{SHSL}	$\overline{CS}$ High Time (read/write)	20			ns
t_{SHQZ}	Output Disable Time			6	ns
t_{CLQX}	Output Hold Time	0			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	2			ns
t_{HLCH}	$\overline{HOLD}$ Low Setup Time (relative to Clock)	5			ns
t_{HHCH}	$\overline{HOLD}$ High Setup Time (relative to Clock)	5			ns
t_{CHHL}	$\overline{HOLD}$ High Hold Time (relative to Clock)	5			ns
t_{CHHH}	$\overline{HOLD}$ Low Hold Time (relative to Clock)	5			ns
t_{HLQZ}	$\overline{HOLD}$ Low To High-Z Output			6	ns
t_{HHQX}	$\overline{HOLD}$ Low To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid			7	ns
t_{WHSL}	Write Protect Setup Time Before $\overline{CS}$ Low	20			ns
t_{SHWL}	Write Protect Hold Time After $\overline{CS}$ High	100			ns
t_{DP}	$\overline{CS}$ High To Deep Power-Down Mode			20	µs
t_{RES1}	$\overline{CS}$ High To Standby Mode Without Electronic Signature Read			20	µs
t_{RES2}	$\overline{CS}$ High To Standby Mode With Electronic Signature Read			20	µs
t_{SUS}	$\overline{CS}$ High To Next Command After Suspend			20	µs
t_{RST_R}	$\overline{CS}$ High To Next Command After Reset (from read)			20	
t_{RST_P}	$\overline{CS}$ High To Next Command After Reset (from program)			20	
t_{RST_E}	$\overline{CS}$ High To Next Command After Reset (from erase)			12	
t_W	Write Status Register Cycle Time		5	30	ms
t_{BP1}	Byte Program Time (First Byte)		30	50(2)	µs
t_{BP2}	Additional Byte Program Time (After First Byte)		2.5	12(2)	µs
t_{PP}	Page Programming Time		0.6	2.4	ms
t_{SE}	Sector Erase Time		70	300	ms
t_{BE}	Block Erase Time (32K Bytes/64K Bytes)		0.15/ 0.25	1.6/2.0	sec
t_{CE}	Chip Erase Time		60	120	sec

1. Tested with clock frequency lower than 50 MHz.
2. For multiple bytes after first byte within a page, $t_{BPn} = t_{BP1} + t_{BP2} * N$, where N is the number of bytes programmed.

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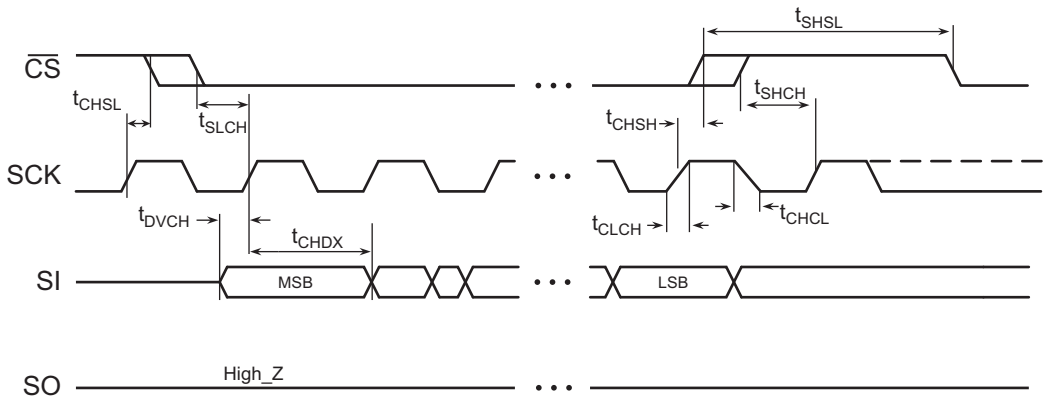


Figure 43. Serial Input Timing

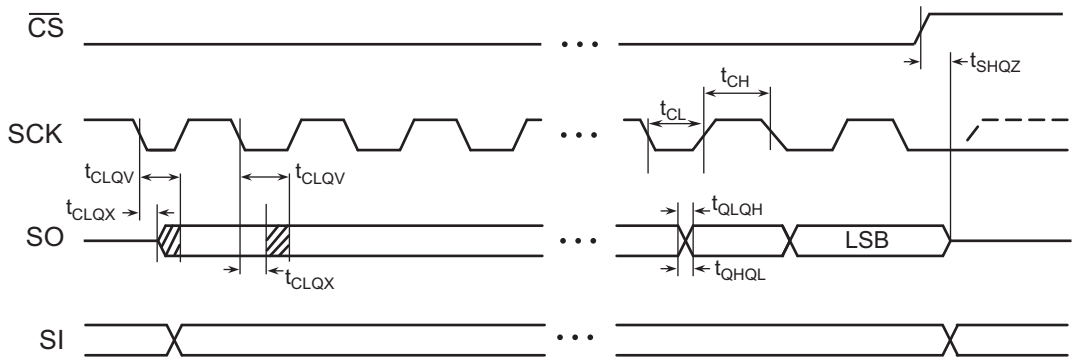


Figure 44. Output Timing

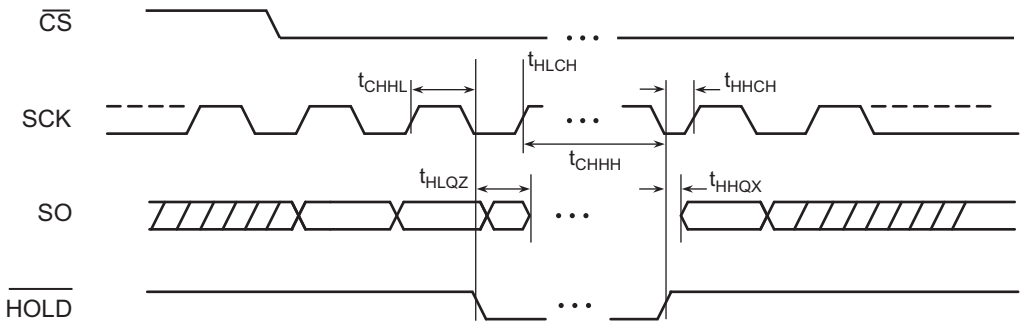


Figure 45. $\overline{\text{HOLD}}$ Timing

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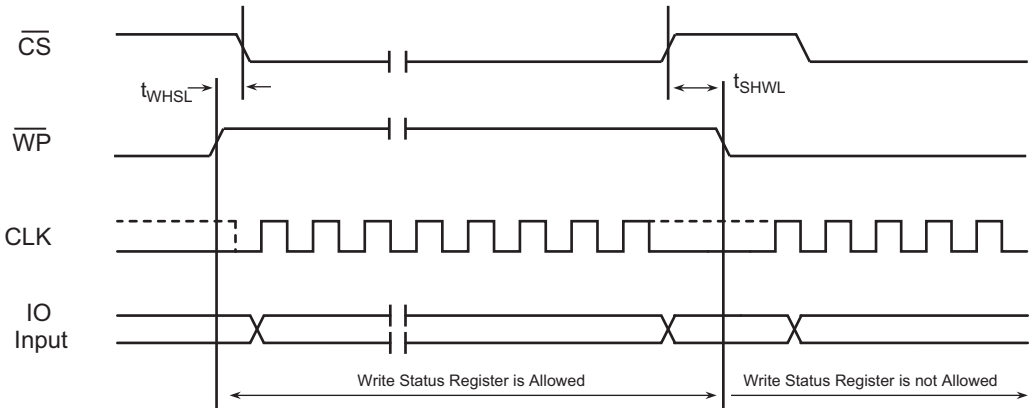


Figure 46. $\overline{WP}$ Timing

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10. Ordering Information

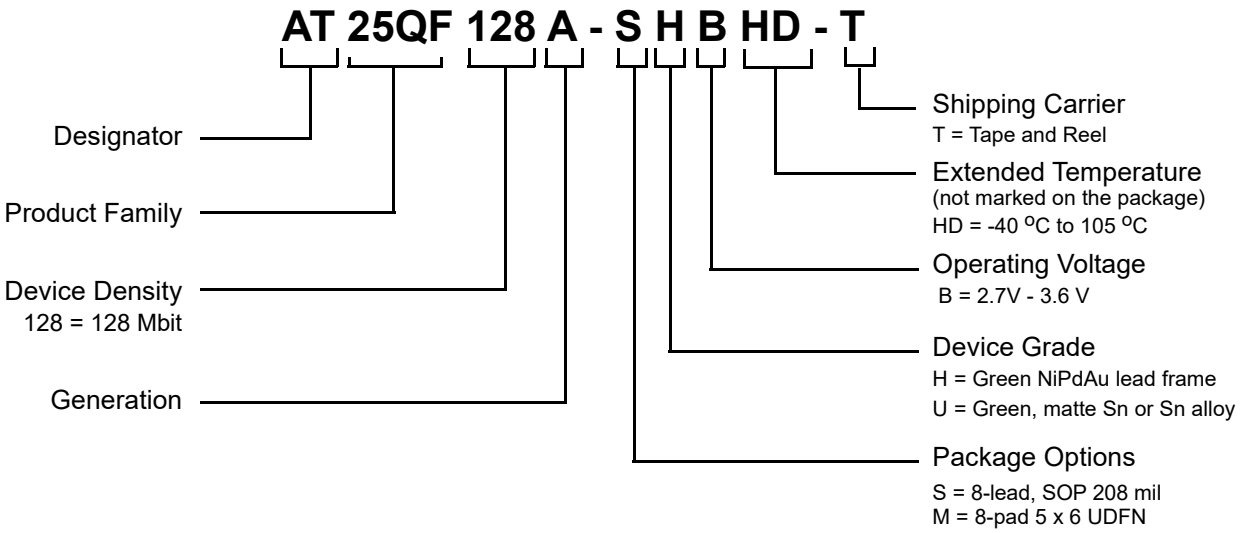


Table 26. Ordering Codes

Ordering Code	Package Type	Lead Finish	Operating Voltage	Maximum Frequency	Operating Range
AT25QF128A-SHB-T	8S2	NiPdAu	2.7 - 3.6V	133 MHz[1]	-40 °C to 85 °C
AT25QF128A-MHB-T	8MA1				
AT25QF128A-SHBHD-T	8S2			120 MHz	-40 °C to 105 °C

1. Only for Quad Output Fast Read (6Bh) command with 3.0V - 3.6V power supply.

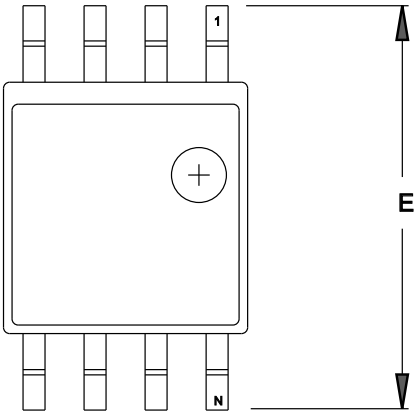
Table 27. Package Description

Package Type	
8S2	8-lead, 0.208" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
8MA1	8-pad (5 x 6 x 0.6 mm body), Thermally Enhanced Plastic Ultra-Thin Dual Flat No-lead (UDFN)

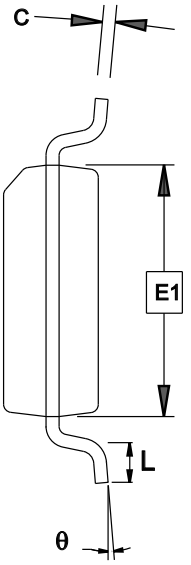
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11. Package Information

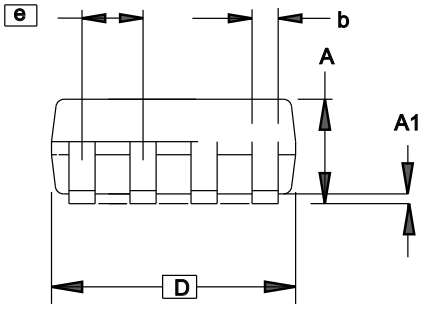
11.1 8-Pin SOP 208-mil



TOP VIEW



END VIEW



SIDE VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.70		2.16	
A1	0.05		0.25	
b	0.35		0.48	4
C	0.15		0.35	4
D	5.13		5.35	
E1	5.18		5.40	2
E	7.70		8.26	
L	0.51		0.85	
θ	0°		8°	
e	1.27 BSC			3

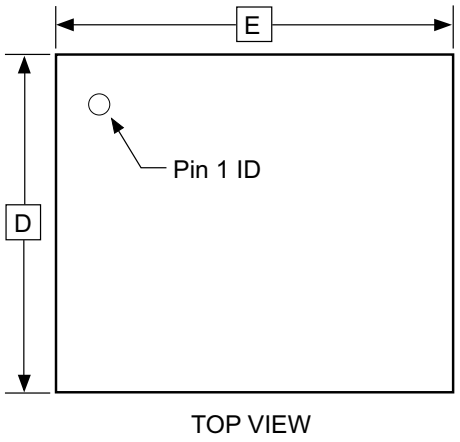
Notes: 1. This drawing is for general information only; refer to EIAJ Drawing EDR-7320 for additional information.
2. Mismatch of the upper and lower dies and resin burrs aren't included.
3. Determines the true geometric position.
4. Values b,C apply to plated terminal. The standard thickness of the plating layer shall measure between 0.007 to .021 mm.

4/15/08

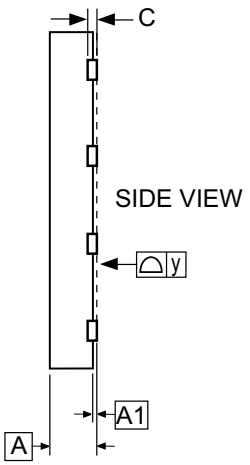
	TITLE	GPC	REV.
RENESAS	8-lead, 208-mil Body, Plastic Small Outline Package (EIAJ)	STN	F

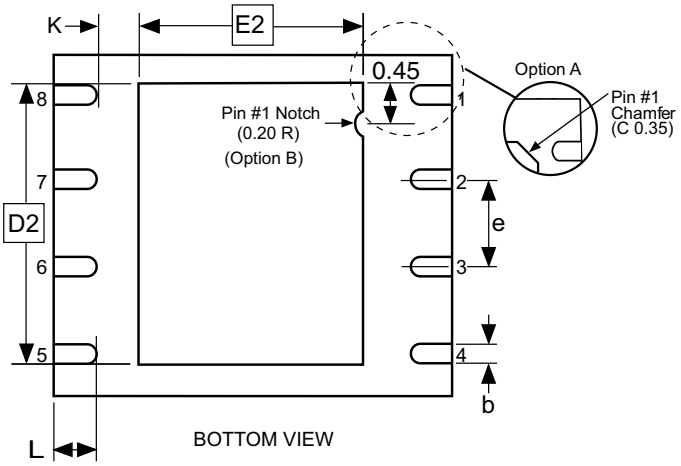
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11.2 8 UDFN



TOP VIEW





BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.45	0.55	0.60	
A1	0.00	0.02	0.05	
b	0.35	0.40	0.48	
C		0.152 REF		
D	4.90	5.00	5.10	
D2	3.80	4.00	4.20	
E	5.90	6.00	6.10	
E2	3.20	3.40	3.60	
e		1.27		
L	0.50	0.60	0.75	
y	0.00	–	0.08	
K	0.20	–	–	

Notes: 1. This package conforms to JEDEC reference MO-229, Saw Singulation.
2. The terminal #1 ID is a Laser-marked Feature.

4/15/08

	TITLE	GPC	DRAWING NO.	REV.
RENESAS	8MA1, 8-pad (5 x 6 x 0.6 mm Body), Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	YFG	8MA1	D

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12. Revision History

Revision	Date	Change Description
A	03/2019	Initial release.
B	11/2019	Removed SFDP tables and updated Section 8.4.10, Read SFDP (5Ah). Updated text in Section 8.4.10, Read SFDP. Updated document to new Adesto template. Updated Section 3.7, HOLD. Updated definition of SRP[1:0] bits in Section 6.4.2.4. Reformatted tables in Section 6.4.1, Status registers. Updated Table 6-2, Status register protections. Added note to end of Section 8.4.8, Erase/Program Suspend (75h) Changed ICC6, ICC7, and ICC8 maximum values in Tables 9-6 and 9-7 from 15 mA to 20 mA. Clarified use of decoupling capacitors in Section 6.1.1.
C	02/2020	Changed status from PRELIMINARY DATASHEET to DATASHEET.
D	06/2020	Exchanged 35 figures with new ones to conform to Adesto standard (no change in content): 6-1, 8-1, 8-5, 8-11 through 8-38, 9-2 through 9-6. Added reference to figure 8-24 in preceding text. Replaced instances of Status Register Byte with Status Register. Replaced 8S4 reference and drawing with 8S2.
E	02/2022	Applied new corporate template. Added physical block size information to the Features list and Section 1, Product Overview. Added the following to the description of opcode 75h: “A read operation from a physical block that includes a suspended area might provide unreliable data. For the definition of the physical block and for the techniques to ensure high data integrity, see application note AN-500.”
F	11/2022	Changed the maximum frequency value in the Table 26. Ordering Codes from 108 MHz to 120 MHz.

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(Rev.1.0 Mar 2020)

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