48 Gbps HDMI 1:1 Transceiver

ADI Preliminary and Confidential

ADV7671

FEATURES

- **1-input, 1-output 1 HDMI transceiver**
  - **8k60 YCbCr 4:2:0 12-bit video support**
  - **8k30 RGB/YCbCr 4:4:4 12-bit video support**
  - **4k120 4:4:4 12-bit high frame rate video support**
- **HDMI receiver**
  - **Up to 48 Gbps FRL support**
  - **Up to 18 Gbps TMDS video support**
  - **eARC transmitter**
  - **On-chip 4 block EDID SRAM managed by internal MCU**
  - **EDID access in low power standby mode**
- **HDMI transmitter**
  - **Up to 48 Gbps FRL support**
  - **Up to 18 Gbps TMDS video support**
  - **eARC receiver**
- **High-bandwidth Digital Content Protection (HDCP)**
  - **HDCP 1.4, 2.2 and 2.3 support**
  - **Independent HDCP on each transmitter and receiver port**
  - **Fully integrated HDCP 1.4, 2.2, 2.3 repeater modes**
  - **HDCP sink mode for audio playback**
  - **On-chip key storage in OTP**
- **Audio**
  - **Audio extraction port**
  - **Audio insertion port**
  - **8-Channel 192 kHz 24-bit PCM audio support**
  - **24.576 Mb IEC61937 compressed audio support**
  - **eARC transmitter or receiver with multichannel PCM, HBR audio and ARC support**
- **Video**
  - **FRL to TMDS and TMDS to FRL modes conversion**
  - **Variable Refresh Rate (VRR), Fast Vactive (FVA) and Auto Low Latency Mode (ALLM) support**
  - **Dynamic HDR passthrough support including HDMI Dynamic HDR metadata, HDR10+ and Dolby Vision™**
  - **DSC 1.2a pass-through support**

APPLICATIONS

- **TV**
- **Home Theater**
- **Industrial Switching**

GENERAL DESCRIPTION

The ADV7671 is a High-Definition Multimedia Interface (HDMI®) transceiver.

The ADV7671 supports 48 Gbps FRL and 18 Gbps TMDS video rates and provides a HDMI receiver port, a HDMI transmitter port, an audio input port, an audio output port, and an enhanced audio return channel (eARC) interface.

The HDMI receiver and transmitter support 8k60 YCbCr 4:2:0 12-bit video, 8k30 RGB 12-bit video and 4k120 RGB 12-bit high frame rate video.

The audio input port and audio output port each support 8-channel 192 kHz PCM and compressed audio formats, including high bitrate formats.

The eARC interface can be configured as either an eARC transmitter or an eARC receiver. The eARC interface supports 8-channel 192 kHz PCM audio and high bit rate audio (HBR) compressed audio formats including Dolby TrueHD™ and DTS-HD™. Audio return channel (ARC) is also supported on the eARC interface.

The ADV7671 supports pass-through of Display Stream Compression (DSC) 1.2a data and High Dynamic Range (HDR) metadata pass-through for HDMI dynamic HDR, HDR10+ and Dolby Vision™.

The ADV7671 implements the HDCP 2.3 specification to protect the delivery of premium content. HDCP 2.3 is applied in transmitter, receiver, and repeater configurations. HDCP 2.3 is backwards compatible with HDCP 2.2. HDCP 1.4 is also supported to provide interoperability with legacy devices.

The ADV7671 is configured via I^2C using a high-level host controller interface (API).

The ADV7671 is provided in a 108-Lead Lead Frame Chip Scale Package (LFCSP) with exposed paddle and is specified over the 0°C to 70°C temperature range.

Customers that wish to sample or purchase the ADV7671 must be licensed HDMI 2.1 adopters listed at HDMI.org and licensed HDCP 2.x adopters listed at Digital-CP.com.

Rev. SPrA

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

TABLE OF CONTENTS

REVISION HISTORY

10/20—Revision SPrA: Initial Preliminary Version

FUNCTIONAL BLOCK DIAGRAM

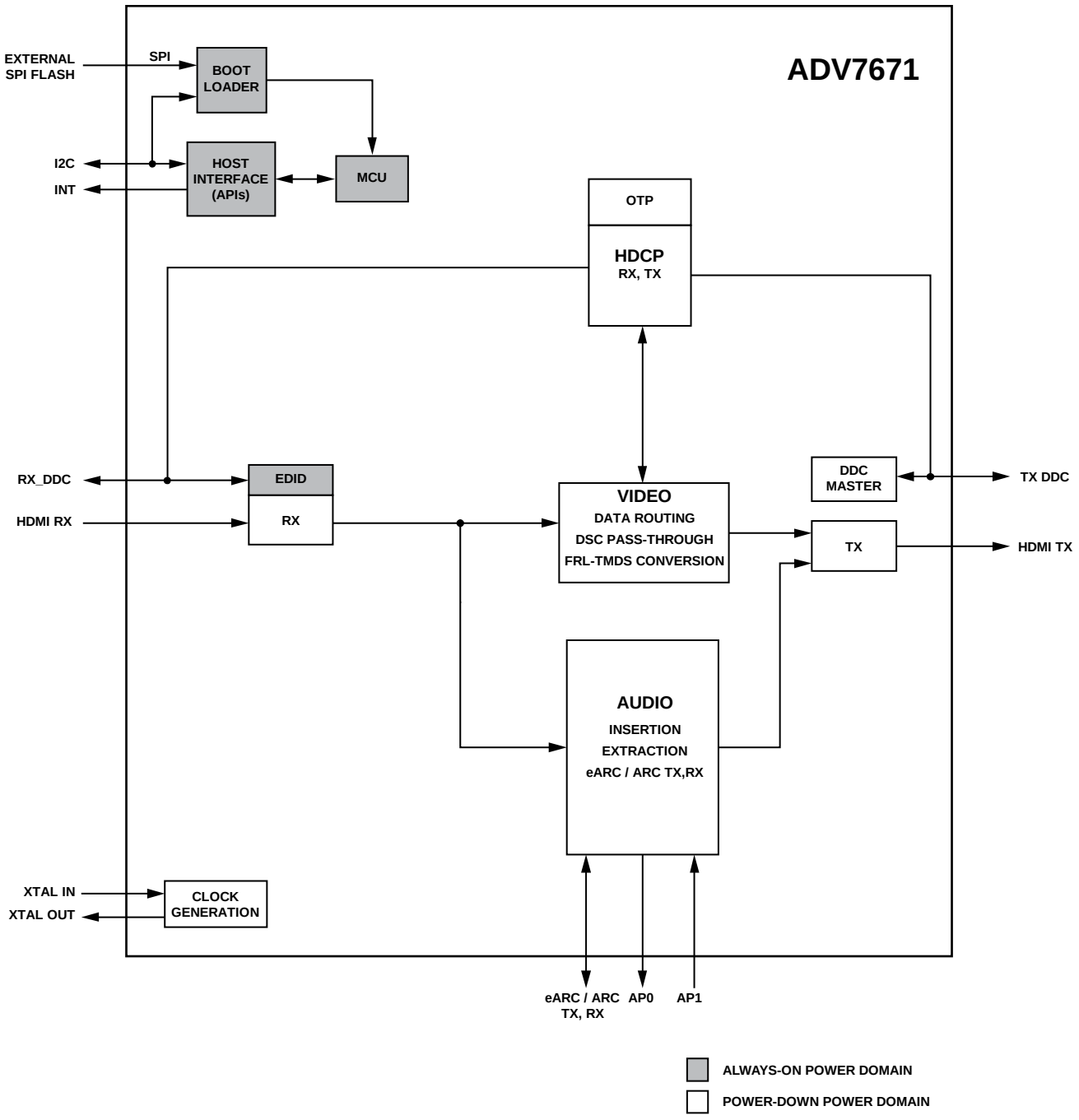


Figure 1.

SPECIFICATIONS

T_{MIN} to T_{MAX} = 0°C to +70°C.

Refer to Table 2 for V_{MIN} to V_{MAX} conditions.

All specifications are preliminary and subject to change.

DIGITAL, DC AND AC SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUTS					
Input Voltage, High (VIH)		2.0			V
Input Voltage, Low (VIL)				0.8	V
I^2C Inputs					
Low to High Threshold (V_{TH+I2C})		2.0			V
High to Low Threshold (V_{TH-I2C})				0.8	V
Display Data Channel (DDC) Inputs					
Low to High Threshold (V_{TH+DDC})		3.0			V
High to Low Threshold (V_{TH-DDC})				1.5	V
DIGITAL OUTPUTS					
Output Voltage, High (VOH)	Output high current (I_{OH}) = 8 mA	2.4			V
Output Voltage, Low (VOL)	I_{OH} = -8 mA			0.4	V
I^2C Open-Drain Outputs					
Low Level Output Voltage (V_{OL_I2C})	I_{OL} = –3 mA			0.4	V
Open Drain DDC Outputs					
Low Level Output Voltage (V_{OL_DDC})	I_{OL} = –3 mA			0.4	V
Open Drain INT Output					
Low Level Output Voltage (V_{OL_INT})	I_{OL} = –3 mA			0.4	V
DC SPECIFICATIONS					
Input Leakage Current, I_{IL}	High Impedance	–10		+10	µA
	High Impedance with pull-down resistor	–10		+100	µA
Output Leakage Current, I_{OL}	High Impedance	–10		+10	µA
	High Impedance with pull-down resistor	–10		+100	µA
	High Impedance with pull-up resistor [1]	–10		+10	µA
8 mA Digital Output Drive (LVTTL)	V_{OUT} = 2.4 V	8			mA
	V_{OUT} = 0.4 V	8			mA
AC SPECIFICATIONS					
TMDS Input Clock Frequency		25		340	MHz
TMDS Output Clock Frequency		25		340	MHz
TMDS Differential Lane Rate	One differential data lane			6	Gbps
TMDS Link Rate	Three differential data lanes			18	Gbps
FRL Differential Lane Rate	One differential data lane			12	Gbps
FRL Differential Lane Rate	Four differential data lanes			48	Gbps

[1] This condition is for the SPI_$\overline{CS}$ pin only.

POWER SPECIFICATIONS - PRELIMINARY

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
POWER SUPPLIES					
Standby Power Supply [1]	SBVCC_5V	4.5	5.0	5.5	V
RX 5 V DDC Power Input	RX_PWR_5V	4.5	5.0	5.3	V
RX 3.3 V Analog Power Supply	VDDH	3.145	3.3	3.465	V
FPLL Power Supply	FPLL_AVDD	0.95	1.0	1.05	V
eARC Power Supply	eARC_PWR	0.95	1.0	1.05	V
Crystal Oscillator Supply	XTAL_VDD_3V3	3.145	3.3	3.465	V
TX 3.3 V Analog Power Supply	TX_VDDHA	3.145	3.3	3.465	V
TX PLL Analog Power Supply	TX_VDDA_PLL	0.95	1.0	1.05	V
RX Analog 1.0 V Power Supply	AVDD	0.95	1.0	1.05	V
TX Analog Power Supply	TX_VDDAC	0.95	1.0	1.05	V
TX Analog Power Supply	TX_VDDAD	0.95	1.0	1.05	V
Digital Core Power Supply	PWR	0.95	1.0	1.05	V
CURRENT CONSUMPTION (TBD)					
Standby Power Supply	I_{SBVCC_5V}				mA
RX 5 V DDC Power Input	$I_{RX\_PWR\_5V}$				mA
RX 3.3 V Analog Power Supply	I_{VDDH}				mA
FPLL Power Supply	I_{FPLL_AVDD}				mA
eARC Power Supply	I_{eARC_PWR}				mA
Crystal Oscillator Supply	$I_{XTAL\_VDD\_3V3}$				mA
TX 3.3 V Analog Power Supply	I_{TX_VDDHA}				mA
TX PLL Analog Power Supply	$I_{TX\_VDDA\_PLL}$				mA
RX 1.0 V Analog Power Supply	I_{AVDD}				mA
TX Analog Power Supply	I_{TX_VDDAC}				mA
TX Analog Power Supply	I_{TX_VDDAD}				mA
Digital Core Power Supply	I_{PWR}				mA
Total Mode Power Dissipation					W
CURRENT CONSUMPTION (TBD)					
Standby Power Supply	I_{SBVCC_5V}				mA
RX 5 V DDC Power Input	$I_{RX\_PWR\_5V}$				mA
RX 3.3 V Analog Power Supply	I_{VDDH}				mA
FPLL Power Supply	I_{FPLL_AVDD}				mA
eARC Power Supply	I_{eARC_PWR}				mA
Crystal Oscillator Supply	$I_{XTAL\_VDD\_3V3}$				mA
TX 3.3 V Analog Power Supply	I_{TX_VDDHA}				mA
TX PLL Analog Power Supply	$I_{TX\_VDDA\_PLL}$				mA
Rx 1.0 V Analog Power Supply	I_{AVDD}				mA
TX Analog Power Supply	I_{TX_VDDAC}				mA
TX Analog Power Supply	I_{TX_VDDAD}				mA
Digital Core Power Supply	I_{PWR}				mA
Total Mode Power Dissipation					W

[1] SBVCC_5V is measured at SBVCC_5V_TP as shown in Figure 17.

TIMING SPECIFICATIONS - PRELIMINARY

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CRYSTAL		Refer to Figure 16				
External Crystal Frequency	f_{XTAL}			25		MHz
XTAL_IN Frequency Tolerance	f_{XTAL_TOL}		–150		150	ppm
Clock Duty Cycle	$\%t_{XTAL}$		40		60	% Duty Cycle
Load Capacitance	C_{LOAD}			18		pF
Feedback Resistor	$R_{FEEDBACK}$			1		MΩ
RESET TIMING						
Time from power stable to de-assertion of internal power on reset (POR)	$t_{POWER\_ON\_RESET}$				3	ms
POWER RISE TIME						
Rise time of RX_PWR_5V	t_{POWER_RISE}		50			µs
I²C, DDC		Refer to Figure 2.				
SDA Data Valid Delay from SCL Falling Edge	t_{I2CDVD}	C_L = 400 pF			700	ns
SDA Data Valid Delay from SCL Falling Edge, Receiver DDC Port	t_{I2CDVD_RXDDC}	C_L = 400 pF			1000	ns
Clock Rate on Receiver DDC Port	f_{RXDDC}	C_L = 400 pF			100	kHz
Clock Rate on Transmitter DDC Port	f_{TXDDC}	C_L = 400 pF			100	kHz
Clock Rate on I²C Port	f_{I2C}	C_L = 400 pF			1	MHz
SPI FLASH MEMORY INTERFACE		Refer to Figure 3, Figure 4.				
SPI Master (SPIM) CLK Frequency	t_{CLK_FREQ}	ISP	6		9	MHz
		Boot Loader	12		18	MHz
SPIM_$\overline{CS}$ Setup Time to SPIM_CLK Rising Edge	$t_{\overline{CS}\_SU}$		25			ns
SPIM_$\overline{CS}$ Hold Time from SPIM_CLK Rising Edge	$t_{\overline{CS}\_HD}$		220			ns
SPIM_MOSI Output Time from SPIM_CLK Falling Edge	t_{TX_OD}		0		15	ns
SPIM_MISO Setup Time to SPIM_CLK Rising Edge	t_{RX_SU}		6			ns
SPIM_MISO Hold Time to SPIM_CLK Rising Edge	t_{RX_HD}		6			ns
AUDIO PORTS, I²S INPUT		Refer to Figure 5.				
Sample Rate	f_{S_I2S}		32		192	kHz
I²S Cycle Time	t_{SCK_CYC}	C_L = 10 pF			1.0	UI
I²S Duty Cycle [1]	t_{SCK_DUTY}	C_L = 10 pF		50		% T_{SCK_CYC}
I²S Setup Time [2]	t_{I2S_SU}	C_L = 10 pF	25			ns
I²S Hold Time[2]	t_{I2S_HD}	C_L = 10 pF	0			ns
AUDIO PORTS, S/PDIF INPUT		Refer to Figure 6.				
Sample Rate	f_{IN_SPDIF}		32		192	kHz
Cycle Time [3]	$t_{IN\_SP\_CYC}$				1.0	UI
Duty Cycle[3]	$t_{IN\_SP\_DUTY}$			50		% T_{I_SPCYC}

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
AUDIO PORTS, I²S OUTPUT		Refer to Figure 7, Figure 8.				
SCK Clock Period (TX)	t_{TR}	C_L = 10 pF	20.346			ns
Setup Time, SCK to SD/WS	t_{SU}	C_L = 10 pF	0.4Tt_{TR} – 5			ns
Hold Time, SCK to SD/WS	t_{HD}	C_L = 10 pF	0.4Tt_{TR} – 5			ns
SCK Duty Cycle	t_{SCK_DUTY}	C_L = 10 pF	40		60	% t_{TR}
SCK to SD or WS Delay [4]	t_{SCK_2SD}	C_L = 10 pF	–20		+20	ns
MCLK Cycle Time	t_{MCLK_CYC}	C_L = 10 pF	20.0		250	ns
MCLK Frequency	f_{MCLK}	C_L = 10 pF	4.0		50.0	MHz
MCLK Duty Cycle	t_{MCLK_DUTY}	C_L = 10 pF	45		55	% $T_{MCLKCYC}$
AUDIO PORTS, S/PDIF OUTPUT		Refer to Figure 9.				
S/PDIF Cycle Time	t_{SP_CYC}	C_L = 10 pF		1.0		UI
S/PDIF Frequency	f_{SPDIF}		4.0		24.576	MHz
S/PDIF Duty Cycle	t_{SP_DUTY}	C_L = 10 pF		50		% T_{SPCYC}
eARC INTERFACE						
eARC Frequency	f_{CLK_eARC}		4.096		98.304	MHz

[1] Proportional to unit time (UI) according to sample rate. Refer to the I²S Specification or the S/PDIF Specification.
[2] Setup and hold minimum times are based on 13.388 MHz sampling, which is adapted from Figure 3 of the Philips I²S Specification.
[3] Proportional to unit time (UI), according to sample rate. Refer to the S/PDIF Specification.
[4] Refers to SCK to WS delay

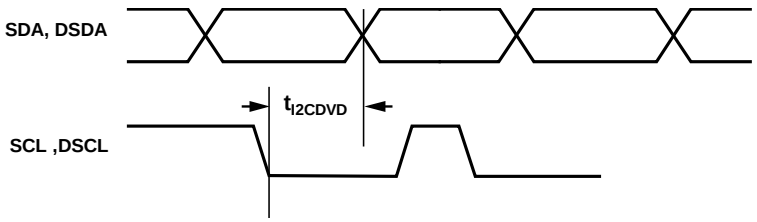


Figure 2. I²C Data Valid Delay

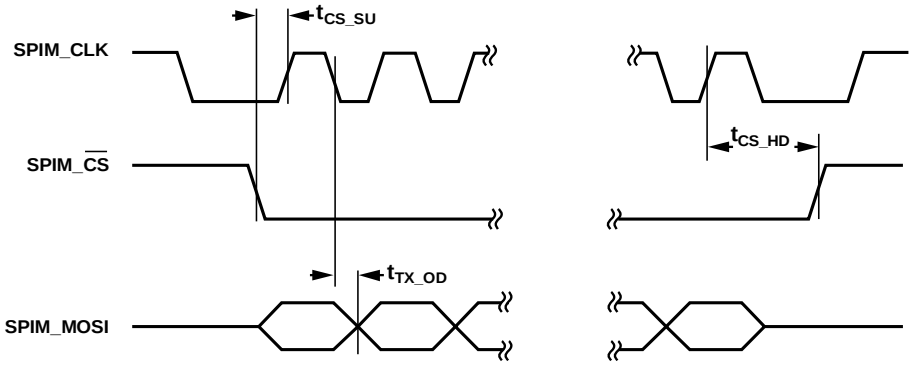


Figure 3. SPI Flash Write Timing

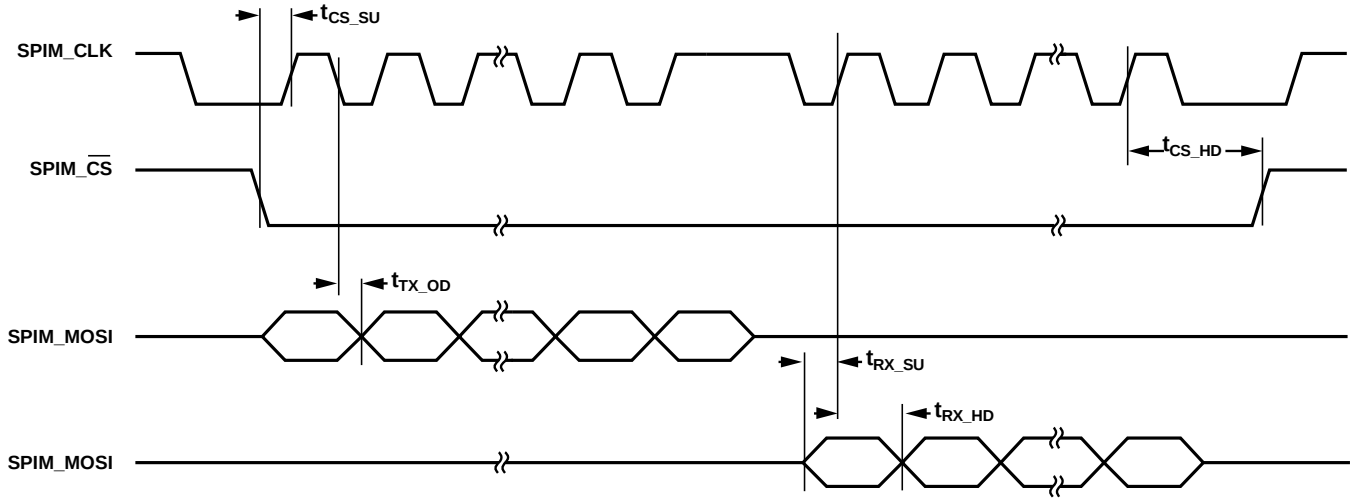


Figure 4. SPI Flash Read Timing

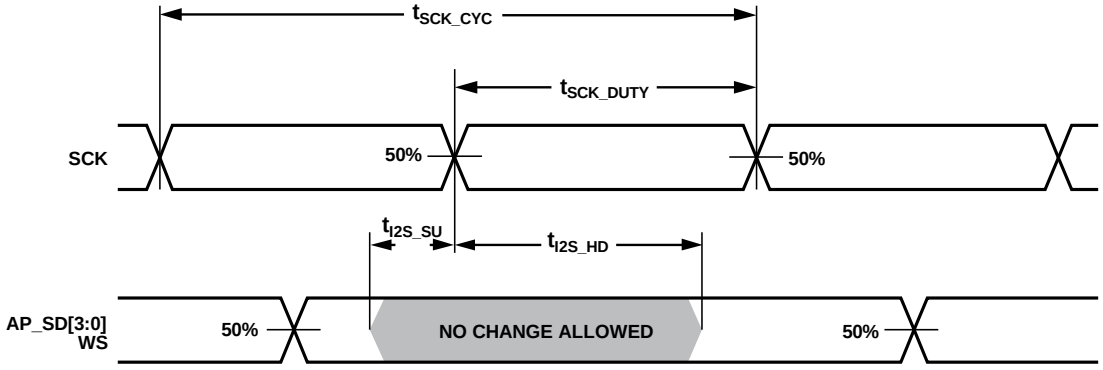


Figure 5. I²S Input Timing

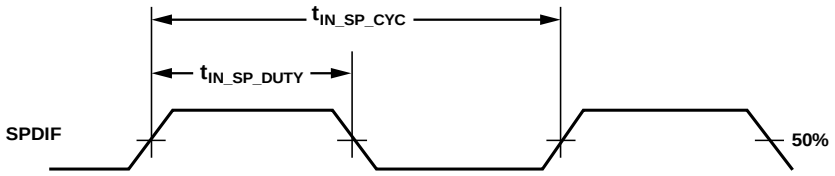


Figure 6. S/PDIF Input Timing

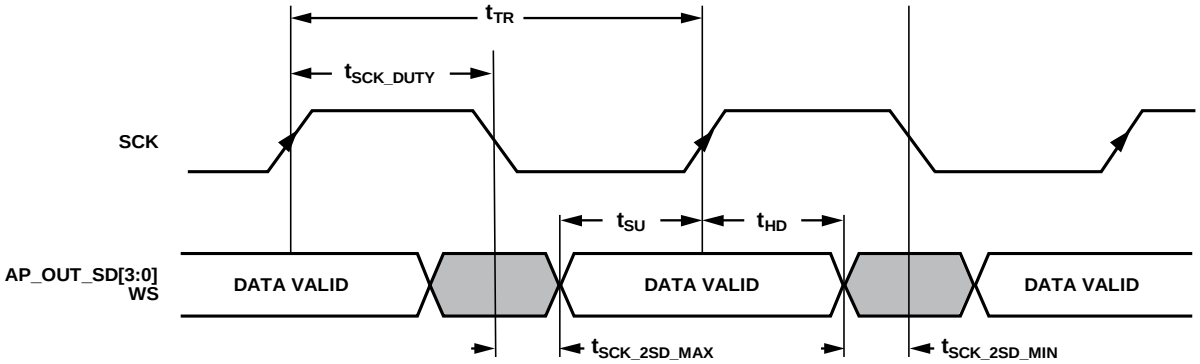


Figure 7. I²S Output Timing

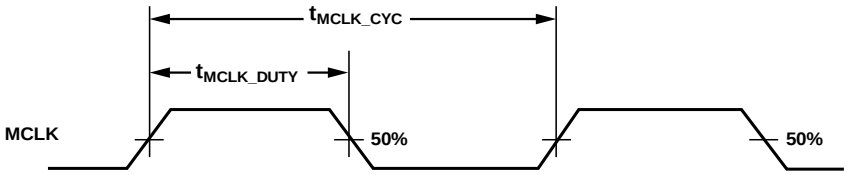


Figure 8. MCLK Timing

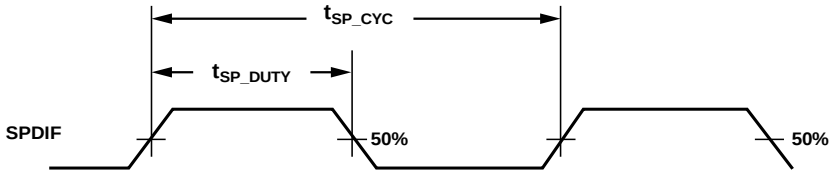


Figure 9. S/PDIF Output Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
SBVCC_5V	−0.3 V to 5.7 V
RX_PWR_5V	−0.3 V to 5.7 V
VDDH	−0.3 V to 4.0 V
FPLL_AVDD	−0.3 V to 1.5 V
eARC_PWR	−0.3 V to 1.5 V
TX_VDDHA	−0.3 V to 4.0 V
XTAL_VDD_3V3	−0.3 V to 4.0 V
TX_VDDA_PLL	−0.3 V to 1.5 V
AVDD	−0.3 V to 1.5 V
TX0_VDDAC	−0.3 V to 1.5 V
TX0_VDDAD	−0.3 V to 1.5 V
PWR	−0.3 V to 1.5 V
5 V tolerant input pins	−0.3 V to 5.7 V
Operating Temperature Range[1]	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	125°C

[1] With power applied.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 5 shows the thermal resistance for junction to ambient (θ_{JA}), junction to case top (θ_{JCtop}), junction to board (θ_{JB}), junction to top thermal characterization number (Ψ_{JT}), and junction to board thermal characterization number (Ψ_{JB}).

Table 5. Thermal Resistance

Package Type	Θ_{JA}	θ_{JCtop}	θ_{JB}	Ψ_{JT}	Ψ_{JB}	Unit
CP-108-1[1, 2]						°C/W

[1] For θ_{JC} testing, 100 µm thermal interface material (TIM) is used. TIM is assumed to have 3.6 W/mK.
[2] Using enhanced heat removal (PCB, heat sink, or airflow) technique improves thermal resistance values.

ELECTROSTATIC DISCHARGE (ESD RATINGS)

The following ESD information is provided for handling of ESD-sensitive deices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

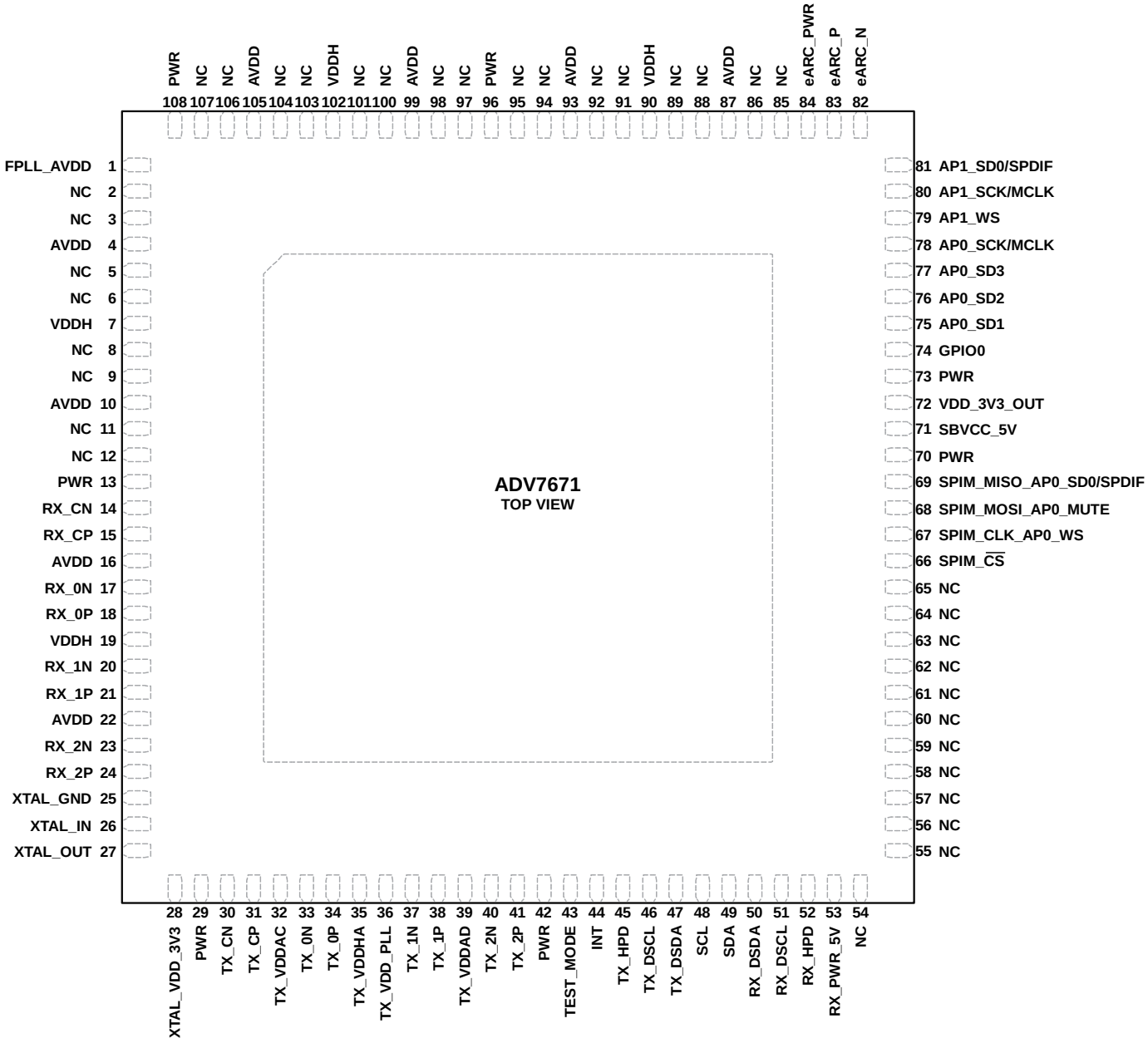
Table 6. ESD Ratings for ADV7671

ESD Model	Withstand Threshold (V)	Class
HBM	±2000	2
CDM	±500	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. THE EXPOSED PAD MUST BE SOLDERED TO A PAD THAT IS ELECTRICALLY CONNECTED TO THE GROUND PLANE OF THE PCB.

000-00000

Figure 10. ADV7671 Pin Configuration

Table 7. ADV7671 Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
HDMI Transmitter			
30	TX_CN	TX TMDS Output	TMDS TX Clock Negative Output or FRL Lane 3 Negative Output.
31	TX_CP	TX TMDS Output	TMDS TX Clock Positive Output or FRL Lane 3 Positive Output.
33	TX_0N	TX TMDS Output	TMDS TX Channel 0 Negative Output or FRL Lane 0 Negative Output.
34	TX_0P	TX TMDS Output	TMDS TX Channel 0 Positive Output or FRL Lane 0 Positive Output.
37	TX_1N	TX TMDS Output	TMDS TX Channel 1 Negative Output or FRL Lane 1 Negative Output.
38	TX_1P	TX TMDS Output	TMDS TX Channel 1 Positive Output or FRL Lane 1 Positive Output.
40	TX_2N	TX TMDS Output	TMDS TX Channel 2 Negative Output or FRL Lane 2 Negative Output.
41	TX_2P	TX TMDS Output	TMDS TX Channel 2 Positive Output or FRL Lane 2 Positive Output.
45	TX_HPD	TX Control Input	HDMI TX Hot Plug Detect (HPD). The HDMI transmitter uses this pin to detect when a Sink is connected. This pin is 5 V tolerant.
46	TX_DSCL	TX Control Input / Output	HDMI TX DDC SCL. This pin does not present a current path to GND when the device is not powered. This pin must be connected through a pull up resistor (1.5 kΩ to 2 kΩ) to DDC 5 V. Refer to the HDMI specification.
47	TX_DSDA	TX Control Input / Output	HDMI TX0 DDC SDA. This pin does not present a current path to GND when the device is not powered. This pin must be connected through a pull up resistor (1.5 kΩ to 2 kΩ) to DDC 5 V. Refer to the HDMI specification.
HDMI Receiver			
14	RX_CN	RX TMDS Input	TMDS RX Clock Negative Input or FRL Lane 3 Negative Input.
15	RX_CP	RX TMDS Input	TMDS RX Clock Positive Input or FRL Lane 3 Positive Input.
17	RX_0N	RX TMDS Input	TMDS RX Channel 0 Negative Input or FRL Lane 0 Negative Input.
18	RX_0P	RX TMDS Input	TMDS RX Channel 0 Positive Input or FRL Lane 0 Positive Input.
20	RX_1N	RX TMDS Input	TMDS RX Channel 1 Negative Input or FRL Lane 1 Negative Input.
21	RX_1P	RX TMDS Input	TMDS RX Channel 1 Positive Input or FRL Lane 1 Positive Input.
23	RX_2N	RX TMDS Input	TMDS RX Channel 2 Negative Input or FRL Lane 2 Negative Input.
24	RX_2P	RX TMDS Input	TMDS RX Channel 2 Positive Input or FRL Lane 2 Positive Input.
52	RX_HPD	RX Control Output	HDMI RX Hot Plug Detect (HPD). This pin is 5 V tolerant and has a 1 kΩ output impedance. This pin indicates that the EDID is readable.
51	RX_DSCL	RX Control Input /Output	HDMI RX DDC SCL. This pin does not present a current path to GND when the device is not powered. This pin must be connected through a 47 kΩ pull up resistor to DDC 5 V. Refer to the HDMI specification.
50	RX_DSDA	RX Control Input / Output	HDMI RX DDC SDA. This pin does not present a current path to GND when the device is not powered.

Pin No.	Mnemonic	Type	Description
Audio			
67	SPIM_CLK_AP0_WS	LVTTL Schmitt Input / Output	Audio Extraction Port AP0 I²S Word Select or SPI Flash Memory Interface Clock Output Signal. This pin is 5 V tolerant.
68	SPIM_MOSI_AP0_MUTE	LVTTL Schmitt Input / Output	Audio Extraction Port AP0 Mute Signal or SPI Flash Memory Interface Data Output. This pin is 5 V tolerant.
69	SPIM_MISO_ AP0_SD0/SPDIF	LVTTL Schmitt Input / Output	Audio Extraction Port AP0 I²S Serial Data Channel 0 or TDM data, or SPDIF signal, or SPI Flash Memory Interface Data Input Signal. This pin is 5 V tolerant.
75	AP0_SD1	LVTTL Schmitt Input / Output	Audio Extraction Port AP0 I²S Serial Data Channel 1 or TDM data. Alternatively, this pin can be configured as GPIO 1. This pin is 5 V tolerant.
76	AP0_SD2	LVTTL Schmitt Input / Output	Audio Extraction Port AP0 I²S Serial Data Channel 2 or TDM data. Alternatively, this pin can be configured as GPIO 2.
77	AP0_SD3	LVTTL Schmitt Input / Output	Audio Extraction Port AP0 I²S Serial Data Channel 3 or TDM data. Alternatively, this pin can be configured as GPIO bit 3.
78	AP0_SCK/MCLK	LVTTL Schmitt Input / Output	Audio Extraction Port AP0 I²S clock or S/PDIF MCLK. This pin is 5 V tolerant.
79	AP1_WS	LVTTL Schmitt Input / Output	Audio Insertion Port AP1 I²S Word Select, or DSD L2. This pin is 5 V tolerant.
80	AP1_SCK/MCLK	LVTTL Schmitt Input / Output	Audio Insertion Port AP1 I²S clock or S/PDIF MCLK. This pin is 5 V tolerant.
81	AP1_SD0/SPDIF	LVTTL Schmitt Input / Output	Audio Insertion Port AP1 I²S Serial Data Channel 0 or TDM data, or S/PDIF signal. This pin is 5 V tolerant.
82	eARC_N	eARC Analog Input/Output	eARC Negative Channel. This signal must be connected to the HPD pin on the HDMI connector when differential eARC or ARC is in use. Differential eARC or ARC is supported by on-board ac coupling.
83	eARC_P	eARC Analog Input / Output	eARC Positive Channel or Single-Ended ARC Signal. This signal must be AC coupled through a 1 µF external capacitor to the utility signal on the HDMI connector. In ARC receiver mode, eARC_P receives an S/PDIF signal from an ARC transmitter capable sink and outputs the signal on the audio port SPDIF pin. In ARC transmitter mode, eARC_P sends an S/PDIF audio stream from the audio port SPDIF input pin to an upstream HDMI device.
Control and Configuration			
26	XTAL_IN	LVTTL Schmitt Input	Crystal or Oscillator input. A 25 MHz crystal or oscillator clock source is required for operation.
27	XTAL_OUT	LVTTL Output	Crystal Feedback Output.
43	TEST_MODE	LVTTL Input	This pin must be driven low in normal functional operation. This pin is 5 V tolerant.
44	INT	LVTTL Schmitt Output	Interrupt Output. The INT pin power-on default is open drain and can be optionally programmed to push-pull LVTTL output. The polarity is negative by default but can be programmed to be positive asserted. This pin is 5 V tolerant.
48	SCL	LVTTL Schmitt Input / Output	I²C SCL line. This pin is 5 V tolerant.
49	SDA	LVTTL Schmitt Input / Output	I²C SDA line. This pin is 5 V tolerant.

Pin No.	Mnemonic	Type	Description
66	SPIM_$\overline{CS}$	LVTTL Schmitt Input / Output	SPI Flash Memory Interface Chip Select. Latched at power-on-reset to disable or enable SPI Master Boot : 0 = Disables SPI Master Boot, 1 = Enables SPI Master Boot. This pin is 5 V tolerant.
67	SPIM_CLK_AP0_WS	LVTTL Schmitt Input / Output	SPI Flash Memory Interface Clock Output Signal or Audio Extraction Port AP0 I^2S Word Select. This pin is 5 V tolerant.
68	SPIM_MOSI_AP0_MUTE	LVTTL Schmitt Input / Output	SPI Flash Memory Interface Data Output or Audio Extraction Port AP0 Mute Signal. Latched at power-on-reset for I^2C address select : 0 = I^2C Address is 0x40, 1 = I^2C Address is 0x44. This pin is 5 V tolerant.
69	SPIM_MISO_ AP0_SD0/SPDIF	LVTTL Schmitt Input / Output	SPI Flash Memory Interface Data Input Signal or Audio Extraction Port AP0 I^2S Serial Data Channel 0 or TDM data, or SPDIF signal. I^2C interface strapping option. This pin is 5 V tolerant.
74	GPIO0	LVTTL Schmitt Input / Output	General Purpose IO 0, or Audio Extraction Port AP0 DSD L6. This pin is 5 V tolerant.
Power and Ground			
71	SBVCC_5V	Power	Always-on Local Power System Power Supply (5.0 V).
53	RX_PWR_5V	Power	RX 5 V DDC Power Input (5.0 V).
7, 19, 90, 102	VDDH	Power	RX Analog Power Supply (3.3 V).
72	VDD_3V3_OUT	Power Output	On-Chip 3.3 V Regulator Power Output. This is a power output from the ADV7671. This pin requires an external 2.2 µF and 100 nF capacitor to ground. This pin is used to power the external SPI flash containing the ADV7671 Firmware and 3.3 V pull-ups associated with the standby power domain. Maximum output current is 30 mA.
1	FPLL_AVDD	Power	FPLL Power Supply (1.0 V).
84	eARC_PWR	Power	eARC Power Supply (1.0 V).
28	XTAL_VDD_3V3	Power	Crystal Oscillator Supply (3.3 V). Paired with XTAL_IO_GND to shield the XTAL_OUT and XTAL_IN.
35	TX_VDDHA	Power	TX Analog Power Supply (3.3 V).
36	TX_VDD_PLL	Power	TX PLL Analog Power Supply (1.0 V).
4, 10, 16, 22, 87, 93, 99, 105	AVDD	Power	Rx Analog Power Supply (1.0 V).
32	TX_VDDAC	Power	TX Analog Power Supply (1.0 V).
39	TX_VDDAD	Power	TX Analog Power Supply (1.0 V).
13, 29, 42, 70, 96, 108	PWR	Power	Digital Core Power Supply (1.0 V).
25	XTAL_IO_GND	Ground	Crystal Input / Output Ground. This pin must be connected directly to the ground plane.
	EPAD		Exposed Ground Pad. The exposed pad must be connected directly to the ground plane.
No Connect			
2, 3, 5, 6, 8. 9, 11, 12, 54, 55, 56, 57, 58, 59, 60, 61, 62, 63, 64, 65, 85, 86, 88, 89, 91, 92, 94, 95, 97, 98, 100, 101, 103, 104, 106, 107	NC	Do Not Connect	Leave these pins floating.

THEORY OF OPERATION

POWER DOMAINS

The ADV7671 provides a separate power domain to support low system power states.

The low power domain is called the AON (Always On) power domain, and the main power partition is called the PDN (Power Down) power domain.

The AON power domain derives power from the SBVCC_5V or RX_PWR_5V power input pins. Using this power source, internal voltage regulators supply the internal 3.3 V and or 1.0 V standby power for the logic and I/O. The functions powered by the AON power domain include:

- Boot loader and SPI Master (Flash Interface).
- VDD_3V3_OUT supplies 3.3 V power to external SPI flash device.
- EDID read through RX DDC.
- RX cable detection using RX_PWR_5V.
- Power on Reset.
- I^2C slave interface

The PDN domain includes all primary chip functions and is powered by the main power supply inputs when the system is in full power on state.

HDMI RECEIVER

The ADV7671 HDMI receiver supports up to 48 Gbps FRL and 18 Gbps TMDS video rates.

The receiver supports 8k30 RGB/YCbCr 4:4:4 12-bit video, 8k60 YCbCr 4:2:0 12-bit video and 4k120 RGB/YCbCr 4:4:4 12-bit high frame rate video.

The HDMI receiver accepts TMDS data and decodes the data to extract video, audio, and auxiliary data from the input stream. The-receiver Port provides a four block, 512-byte EDID.

The receiver supports HDCP 2.3, HDCP 2.2 and HDCP 1.4 decryption.

HDMI TRANSMITTER

The ADV7671 HDMI transmitter supports up to 48 Gbps FRL and 18 Gbps TMDS video rates.

The transmitter supports 8k30 RGB/YCbCr 4:4:4 12-bit video, 8k60 YCbCr 4:2:0 12-bit video and 4k120 RGB/YCbCr 4:4:4 12-bit high frame rate video.

The transmitter supports HDCP 2.3 and HDCP 2.2 and HDCP 1.4 encryption. The HDCP cipher engine allows encryption to be enabled on the Tx output.

To ease signal routing in a design, the order of the TMDS signals assigned on the transmitter port can be reversed and the polarity of the signals can be inverted

HDCP REPEATER

The ADV7671 provides HDCP 1.4 and HDCP 2.2/2.3 repeater support for up to 31 devices per receiver-transmitter path. If the total of different devices connected exceeds 31, an "HDCP MAX_DEVICES_EXCEEDED" error message is reported upstream.

HDCP

OTP

The ADV7671 is preprogrammed with production HDCP keys stored in an internal ROM. Customers that wish to sample or purchase the ADV7671 must be licensed HDCP 2.x adopters listed at Digital-CP.com.

HDCP 2.3 requires device makers to ensure that activation is performed at the site of an adopter. ADV7671 devices are shipped without the capability to display HDCP 2.3 premium until the activation step is performed.

HDCP Cores

The HDCP Cores contain the necessary logic to encrypt or decrypt HDCP audio/visual streams and support HDCP authentication and repeater checks.

The transmitter port supports HDCP 2.2/2.3 and HDCP 1.4 encryption. The transmitter port automatically selects HDCP 1.4 mode or HDCP 2.2/2.3 mode by reading the HDCP 2 version register from the downstream device over the DDC channel. The SoC application can query the HDCP status through the host interface.

AUDIO

The AP0 audio output port consists of a 4-wire I^2S interface with the SD0 pin alternatively configurable as an S/PDIF signal. The AP1 audio input port is a 1-wire I^2S or S/PDIF interface.

I^2S

The I^2S interface supports up to 8-channel PCM audio with sample rates from 32 kHz to 192 kHz. High Bitrate Audio formats, such as Dolby TrueHD™ and DTS-HD™ are also supported at sample rates of up to 768 kHz. The AP1 input on ADV7671 supports 2-channels PCM audio.

S/PDIF

The S/PDIF interface supports 2-channel PCM audio streams at sample rates from 32 kHz up to 192 kHz and low bitrate compressed formats, such as Dolby® Digital, DTS, and extensions to these formats, at up to 192 kHz sample rates.

DSD

The audio port(s) supports 6-channel, one-bit DSD audio at sample rates of 44.1 kHz and 88.2 kHz using the I^2S and S/PDIF signal pins.

eARC on AP0 and AP1

The AP0 or AP1 S/PDIF interface can be used as the audio output port for eARC, supporting 2-channel PCM audio at sample rates of up to 192 kHz.

TDM

The I²S interface also supports TDM audio with the capability to transmit or receive up to 8 audio channels distributed across 4 data lanes. The maximum sample rate supported by TDM audio is 192 kHz. Various mappings are available for the audio channels.

Audio Routing

The ADV7671 supports the following audio routing :

- Audio pass-through, from the HDMI receiver input the HDMI transmitter output.
- Audio extraction from the HDMI receiver input to the AP0 audio output port
- Audio insertion from the audio input port to the HDMI transmitter output.
- Audio from the HDMI input port to the eARC transmitter.
- Audio from the AP1 audio input port to the eARC transmitter
- Audio from the eARC interface to the audio output port.
- Audio from the S/PDIF input on the audio input port to ARC or vice versa

Figure 11 provides an overview of the audio routing supported the ADV7671. Table 8, shows the audio matrix support for the ADV7671.

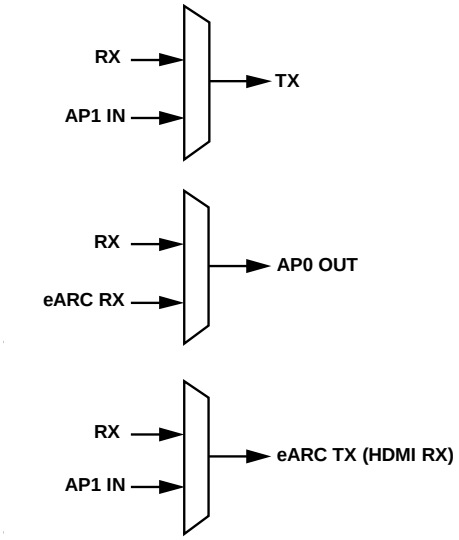


Figure 11. Audio Routing – ADV7671

Table 8. ADV7671 Audio Matrix

		AUDIO OUTPUT[1]								
		HDMI	AP0						ARC / eARC Output	
AUDIO INPUT		Tx	S/PDIF	eARC	4 x I²S	1 x TDM	4 x TDM	DSD	ARC	eARC
HDMI[2]	Rx	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
AP1[3]	S/PDIF	Yes	N/A	N/A	N/A	N/A	N/A	N/A	Yes	Yes
	1 x I²S	Yes	N/A	N/A	N/A	N/A	N/A	N/A	Yes	Yes
	1xTDM	Yes	N/A	N/A	N/A	N/A	N/A	N/A	Yes	Yes
	DSD	Yes[4]	N/A	N/A	N/A	N/A	N/A	N/A	Yes	Yes
ARC / eARC Input	ARC	N/A	Yes	N/A	N/A	N/A	N/A	N/A	N/A	N/A
	eARC	N/A	Yes	Yes	Yes	Yes	Yes	Yes	N/A	N/A

[1] N/A = Not Applicable.
[2] Audio from the RX input can be routed to the audio outputs indicated.
[3] AP1 port is 1 wire I²S/TDM interface.
[4] 2-channel support only.

AP0 and AP1 Considerations

The AP0 audio output port and the AP1 audio input output can be configured for either I²S or S/PDIF audio. They cannot be simultaneously configured for both I²S and S/PDIF.

Figure 12 shows the connections between the ADV7671 AP0 output port, AP1 audio input port and an audio processor.

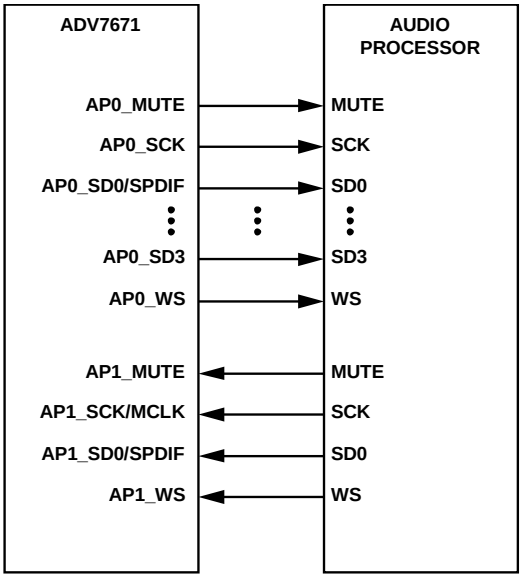


Figure 12. ADV7671 Audio Ports

eARC

The ADV7671 eARC interface can transmit or receive an audio stream over the HPD and Utility pins of the HDMI cable. The eARC_P and eARC_N pins must be AC coupled through a 1 µF capacitor to the Utility and HPD pins of the HDMI connector.

Sampling rate frequencies of 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, 176.4 kHz, 192 kHz and 768 kHz (HBR) are supported.

The eARC interface also supports legacy ARC (single-ended mode) over the HDMI connector Utility pin for backwards compatibility.

The eARC interface supports the following audio extraction / insertion modes :

- 2-channel LPCM with sample frequencies up to 192 kHz with 16-bit or 24-bit word widths.
- IEC 61937 compressed audio formats.
- Up to 8-channel LPCM with 16-bit or 24-bit word widths (eARC mode only).
- High bit rate audio (HBR) up to 768 kHz frame rate (eARC mode only).
- Up to 6-channels of DSD audio (eARC mode only).

BOOT LOADER

The Boot Loader block fetches microcode from the external flash memory. The boot sequence is triggered when power is applied to either SBVCC_5V or the RX_PWR_5Vpin. Firmware microcode can also be loaded by an external processor (SoC) from its own storage to the ADV7671 using the I²C slave interface, eliminating the need for dedicated SPI flash.

MICROCONTROLLER UNIT

The internal Microcontroller Unit (MCU) integrates all ADV7671 functions. The MCU also provides a high-level control interface to allow an external application controller to change operation modes or retrieve status information.

HOST INTERFACE

The ADV7671 I²C slave bus interface controls the active state and modes of the ADV7671.

The I²C interface supports up to 1 MHz data transfer rate. The device address of the local I²C interface can be set to 0x40 or 0x44 by strapping the SPIM_MOSI pin low or high at reset. Table 9 describes the required power-on reset level required on for each device address.

The INT pin generates a notification to the host controller of a status change in the device that requires attention from the host controller.

Table 9. I²C Device Address Configurations

Device Address	SPIM_MOSI
0x40	Low
0x44	High

ADV7671 USE CASE

ADV7671 SOUNDBAR APPLICATION

Figure 13 provides an overview of the ADV7671 used in a soundbar application.

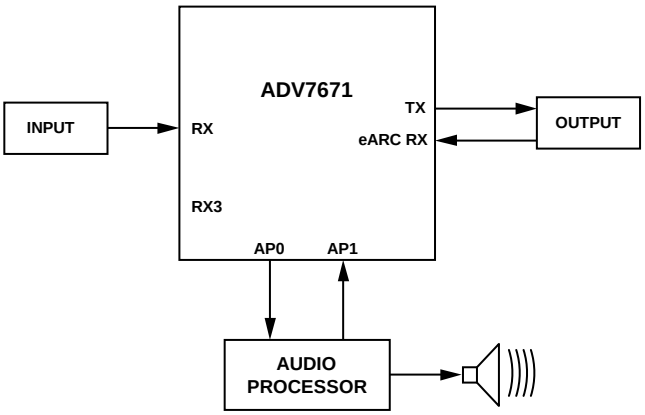


Figure 13. Example ADV7671Soundbar Application

VIDEO FORMATS

SUPPORTED VIDEO INPUT FORMATS

Table 10 and Table 11 list the video input formats supported by the ADV7671. All video formats supported in TMDS mode are also supported in FRL mode.

Table 10. Supported Video Input Formats (TMDS Mode)

Video Mode	Video Resolution	Color Space and Pixel Depth	Frame Rate (Hz)
2D	VGA[1] (640 × 480p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	59.94, 60
2D	WVGA (800 × 480p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	60
2D	SVGA (800 × 600p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	60
2D	XGA (1024 × 768p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	60
2D	SXGA (1280 × 1024p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	60
2D	UXGA (1600 × 1200p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	60
2D	WUXGA (1900 × 1200p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	60
2D	480i 2x (1440 × 480i)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	59.94, 60
2D	480i 4x (2880 × 480i)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	59.94, 60
2D	480p (720 × 480p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	59.94, 60
2D	480p 2x (1440 × 480p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	59.94, 60
2D	480p 4x (2880 × 480p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	59.94, 60
2D	576i 2x (1440 ×576i)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50
2D	576i 4x (2880 ×576i)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50
2D	576p (720 × 576p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50
2D	576p 2x (1440 × 576p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50
2D	576p 4x (2880 × 576p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50
2D	720p (1280 × 720p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	23.98, 24, 25, 29.97, 30, 50, 59.94, 60
2D	1080i (1920 × 1080i)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50, 59.94, 60
2D	1080p (1920 × 1080p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	23.98, 24, 25, 29.97, 30, 50, 59.94, 60,

Video Mode	Video Resolution	Color Space and Pixel Depth	Frame Rate (Hz)
2D	1080p (1920 × 1080p)	RGB 4:4:4 with 24 bpp YCbCr 4:4:4 with 24 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	100, 119.88, 120
2D	4k × 2k (3840 × 2160p)	RGB 4:4:4 with 24 bpp YCbCr 4:4:4 with 24 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	23.98, 24, 25, 29.97, 30, 50, 59.94, 60
2D	4k × 2k (3840 × 2160p)	YCbCr 4:2:0 with 24 bpp, 30 bpp, 36 bpp	50, 59.94, 60
2D	4k × 2k (4096 × 2160p)	RGB 4:4:4 with 24 bpp YCbCr 4:4:4 with 24 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	23.98, 24, 25, 29.97, 30, 50, 59.94, 60
2D	4k × 2k (4096 × 2160p)	YCbCr 4:2:0 with 24 bpp, 30 bpp, 36 bpp	50, 59.94, 60
3D Frame Packing	720p (1280 × 720p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50, 59.94, 60
3D Frame Packing	1080p (1920 × 1080p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	23.98, 24, 25, 29.97, 30
3D Frame Packing	1080p (1920 × 1080p)	RGB 4:4:4 with 24 bpp YCbCr 4:4:4 with 24 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50, 59.94, 60
3D Side-by-Side (Half)	1080i (1920 × 1080i)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50, 59.94, 60
3D Top-and-Bottom	720p (1280 × 720p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50, 59.94, 60
3D Top-and-Bottom	1080p (1920 × 1080p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	23.98, 24, 25, 29.97, 30, 50, 59.94, 60

[1] VGA is video graphics array, WVGA is wide VGA, SVGA is super VGA, XGA is extended GA, SXGA is super XGA, UXGA is ultra XGA, and WUXGA is widescreen UXGA.

Table 11. Supported Video Input Formats (FRL Mode)

Video Resolution	Color Space and Pixel Depth	Frame Rate (Hz)
4k× 2k (3840 × 2160)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 8, bpc 10 bpc, 12 bpc	50, 60
4k × 2k (3840 × 2160)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 8, bpc 10 bpc, 12 bpc YCbCr 4:2:2 with 8 bpc, 10 bpc, 12 bpc YCbCr 4:2:0 with 8 bpc, 10 bpc, 12 bpc	100, 120
4k × 2k (4096 × 2160)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 8, bpc 10 bpc, 12 bpc	50, 60
4k × 2k (4096 × 2160)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 8, bpc 10 bpc, 12 bpc YCbCr 4:2:2 with 8 bpc, 10 bpc, 12 bpc YCbCr 4:2:0 with 8 bpc, 10 bpc, 12 bpc	100, 120
5120 × 2160	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 8, bpc 10 bpc, 12 bpc YCbCr 4:2:2 with 8 bpc, 10 bpc, 12 bpc	50, 60
8k × 4k (7680 × 4320)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 8, bpc 10 bpc, 12 bpc YCbCr 4:2:2 with 8 bpc, 10 bpc, 12 bpc YCbCr 4:2:0 with 8 bpc, 10 bpc, 12 bpc	23.98, 24, 25, 29.97, 30
8k × 4k (7680 × 4320)	YCbCr 4:2:0 with 8 bpc, 10 bpc, 12 bpc	50, 60

SUPPORTED VIDEO OUTPUT FORMATS

The ADV7671 transmitter output supports a pixel clock frequency of up to 1188 MHz. Table 12 and Table 13 list the video output formats supported by the ADV7671.

The ADV7671 supports up to 36-bit pixel depth for RGB 4:4:4 and YCbCr 4:4:4 modes, and up to 24-bit pixel depth for YCbCr 4:2:2 mode. It also supports YCbCr 4:2:0 8, 10 and 12 bpc mode.

Table 12. Supported Video Output Formats (TMDS Mode)

Video Mode	Video Resolution	Color Space and Pixel Depth	Frame Rate (Hz)
2D	VGA[1] (640 × 480p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	59.94, 60
2D	WVGA[1] (800 × 480p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	60
2D	SVGA[1] (800 × 600p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	60
2D	XGA[1] (1024 × 768p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	60
2D	SXGA[1] (1280 × 1024p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	60
2D	UXGA[1] (1600 × 1200p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	60
2D	WUXGA[1] (1900 × 1200p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp	60
2D	480i 2x (1440 × 480i)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	59.94, 60
2D	480i 4x (2880 × 480i)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	59.94, 60
2D	480p (720 × 480p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	59.94, 60
2D	480p 2x (1440 × 480p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	59.94, 60
2D	480p 4x (2880 × 480p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	59.94, 60
2D	576i 2x (1440 × 576i)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50
2D	576i 4x (2880 × 576i)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50
2D	576p (720 × 576p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50
2D	576p 2x (1440 × 576p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50
2D	576p 4x (2880 × 576p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50
2D	720p (1280 × 720p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	23.98, 24, 25, 29.97, 30, 50, 59.94, 60
2D	1080i (1920 × 1080i)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	23.98, 24, 25, 29.97, 30, 50, 59.94, 60
2D	1080p (1920 × 1080p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	23.98, 24, 25, 29.97, 30, 50, 59.94, 60
2D	1080p (1920 × 1080p)	RGB 4:4:4 with 24 bpp YCbCr 4:4:4 with 24 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	100, 119.88, 120

Video Mode	Video Resolution	Color Space and Pixel Depth	Frame Rate (Hz)
2D	4k × 2k (3840 × 2160p)	RGB 4:4:4 with 24 bpp YCbCr 4:4:4 with 24 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	23.98, 24, 25, 29.97, 30, 50, 59.94, 60
2D	4k × 2k (3840 × 2160p)	YCbCr 4:2:0 with 24, 30, 36 bpp	50, 59.94, 60
2D	4k × 2k (4096 × 2160p)	RGB 4:4:4 with 24 bpp YCbCr 4:4:4 with 24 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	23.98, 24, 25, 29.97, 30, 50, 59.94, 60
2D	4k × 2k (4096 × 2160p)	YCbCr 4:2:0 with 24 bpp, 30 bpp, 36 bpp	50, 59.94, 60
3D Frame Packing	720p (1280 × 720p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50, 59.94, 60
3D Frame Packing	1080p (1920 × 1080p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	23.98, 24, 25, 29.97, 30
3D Frame Packing	1080p (1920 × 1080p)	RGB 4:4:4 with 24 bpp YCbCr 4:4:4 with 24 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50, 59.94, 60
3D Side-by-Side (Half)	1080i (1920 × 1080i)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50, 59.94, 60
3D Top-and-Bottom	720p (1280 × 720p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	50, 59.94, 60
3D Top-and-Bottom	1080p (1920 × 1080p)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:2:2 with 16 bpp, 20 bpp, 24 bpp	23.98, 24, 25, 29.97, 30, 50, 59.94, 60

[1] VGA is video graphics array, WVGA is wide VGA, SVGA is super VGA, XGA is extended GA, SXGA is super XGA, UXGA is ultra XGA, and WUXGA is widescreen UXGA.

Table 13. Supported Video Output Formats (FRL Mode)

Video Resolution	Color Space and Pixel Depth	Frame Rate (Hz)
4k × 2k (3840 × 2160)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 8, bpc 10 bpc, 12 bpc	50, 60
4k × 2k (3840 × 2160)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 8, bpc 10 bpc, 12 bpc YCbCr 4:2:2 with 8 bpc, 10 bpc, 12 bpc YCbCr 4:2:0 with 8 bpc, 10 bpc, 12 bpc	100, 120
4k x 2k (4096 × 2160)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 8, bpc 10 bpc, 12 bpc	50, 60
4k × 2k (4096 × 2160)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 8, bpc 10 bpc, 12 bpc YCbCr 4:2:2 with 8 bpc, 10 bpc, 12 bpc YCbCr 4:2:0 with 8 bpc, 10 bpc, 12 bpc	100, 120
5120 × 2160	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 8, bpc 10 bpc, 12 bpc YCbCr 4:2:2 with 8 bpc, 10 bpc, 12 bpc	50, 60
8k × 4k (7680 × 4320)	RGB 4:4:4 with 24 bpp, 30 bpp, 36 bpp YCbCr 4:4:4 with 8, bpc 10 bpc, 12 bpc YCbCr 4:2:2 with 8 bpc, 10 bpc, 12 bpc YCbCr 4:2:0 with 8 bpc, 10 bpc, 12 bpc	23.98, 24, 25, 29.97, 30
8k × 4k (7680 × 4320)	YCbCr 4:2:0 with 8 bpc, 10 bpc, 12 bpc	50, 60

TMDS TRANSMITTER CHANNEL SWAP AND POLARITY INVERSION

The order of the TMDS signals assigned on the transmitter port can be independently swapped to ease PCB routing when connecting to an on-board HDMI receiver. Channel swapping reverses the order of the signals on a TX output.

The channel polarity of the signals can also be inverted on the HDMI transmitter. Table 14 describes the signals assigned to each pin after channel swapping and polarity inversion.

Table 14. TMDS Transmitter Channel Swap and Polarity Inversion

Pin Number	Default TMDS Signal Assignment	TMDS Swap Signal Assignment	TMDS Polarity Inversion Signal Assignment
31	TX_CP	TX_2P	TX_2N
30	TX_CN	TX_2N	TX_2P
34	TX_0P	TX_1P	TX_1N
33	TX_0N	TX_1N	TX_1P
38	TX_1P	TX_0P	TX_0N
37	TX_1N	TX_0N	TX_0P
41	TX_2P	TX_CP	TX_CN
40	TX_2N	TX_CN	TX_CP

APPLICATIONS INFORMATION

POWER SUPPLY DECOUPLING

Decoupling and bypass capacitors must be included for each power signal in the layout as illustrated in Figure 14. Connections for an individual supply rail (such as PWR) can share C2, C3 and the ferrite, with a C1 capacitor placed as close as possible to each individual supply pin. Figure 15 shows an example implementation of power connections to the device.

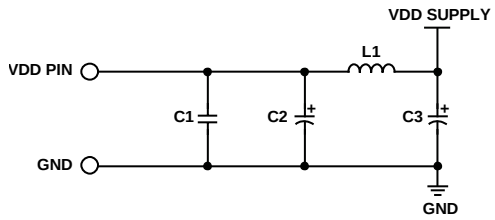


Figure 14. Decoupling and Bypass Schematic

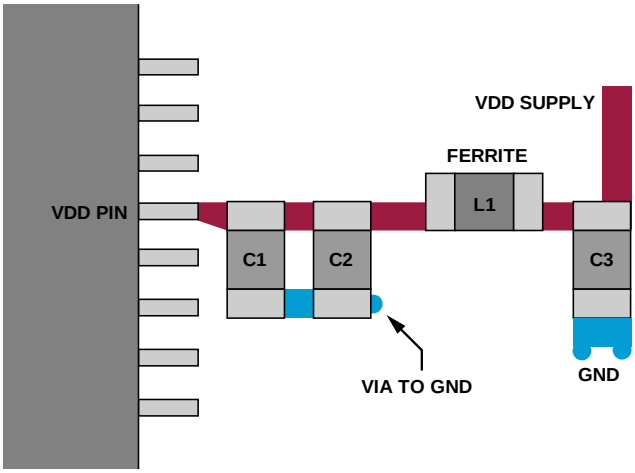


Figure 15. Decoupling and Bypass Placement

LAYOUT GUIDELINES

The following design guidelines are advised to ensure signal integrity of the system.

- Place the TMDS input and output connectors as close as possible to the chip.
- Route the TMDS differential pairs together as directly as possible from the connector to the chip.
- Route each TMDS differential pair with controlled differential impedance of 100 Ω.
- Avoid routing the TMDS signal lines through vias.
- Place external ESD devices, if used, close to the HDMI connector.
- Serpentine traces are not recommended to compensate for intra-pair and inter-pair trace skew of the TMDS signal lines.

CRYSTAL CIRCUIT

The crystal circuit required for the ADV7671 operation is shown in Figure 16.

5% tolerance for the passive devices is recommended.

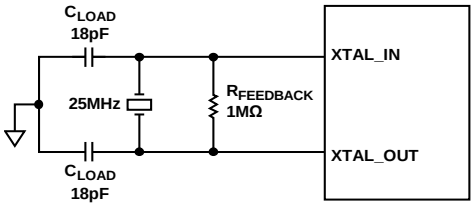


Figure 16. Crystal Circuit

SBVCC_5V MEASUREMENT

The SBVCC_5V value Table 2 in was measured at SBVCC_5V_TP, as shown in Figure 17.

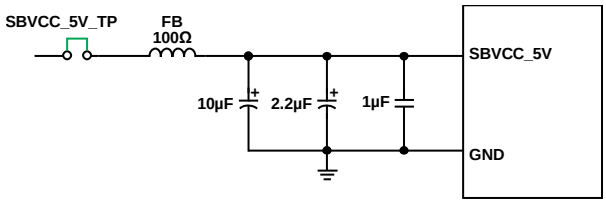


Figure 17. SBVCC_5V_TP Test Point for SBVCC_5V Measurement

ESD PROTECTION

In applications where higher protection levels are required, ESD-limiting components can be placed on the differential lines of the chip. These components typically have a capacitive effect that reduces the signal quality at higher clock frequencies. Use the lowest capacitance devices possible. ESD components must be placed as close as possible to the input or output connector. In no case can the capacitance value of these components exceed 1 pF.

EMI CONSIDERATIONS

Electromagnetic interference (EMI) is a function of board layout, shielding, receiver component operating voltage, frequency of operation, and other factors. When attempting to control emissions, it is important not to place any passive components on the differential signal lines, except the common-mode chokes and ESD protection described in the ESD Protection section. The differential signaling used in HDMI is inherently low in EMI if the routing recommendations noted in the Layout Guidelines section are followed.

The PCB ground plane should extend unbroken under as much of the transmitter chip and associated circuitry as possible, with all ground pins of the chip using a common ground.

EPAD REQUIREMENTS

The exposed paddle (ePad) of the 108-pin LFCSP package must be connected to the ground plane of the PCB to meet the package dissipation requirements at full speed operation and to correctly connect the chip circuitry to electrical ground. As a general guideline, a clearance of at least 0.25 mm should be designed on the PCB between the edge of the ePad and the inner edges of the lead pads to avoid the possibility of electrical shorts.

OUTLINE DIMENSIONS

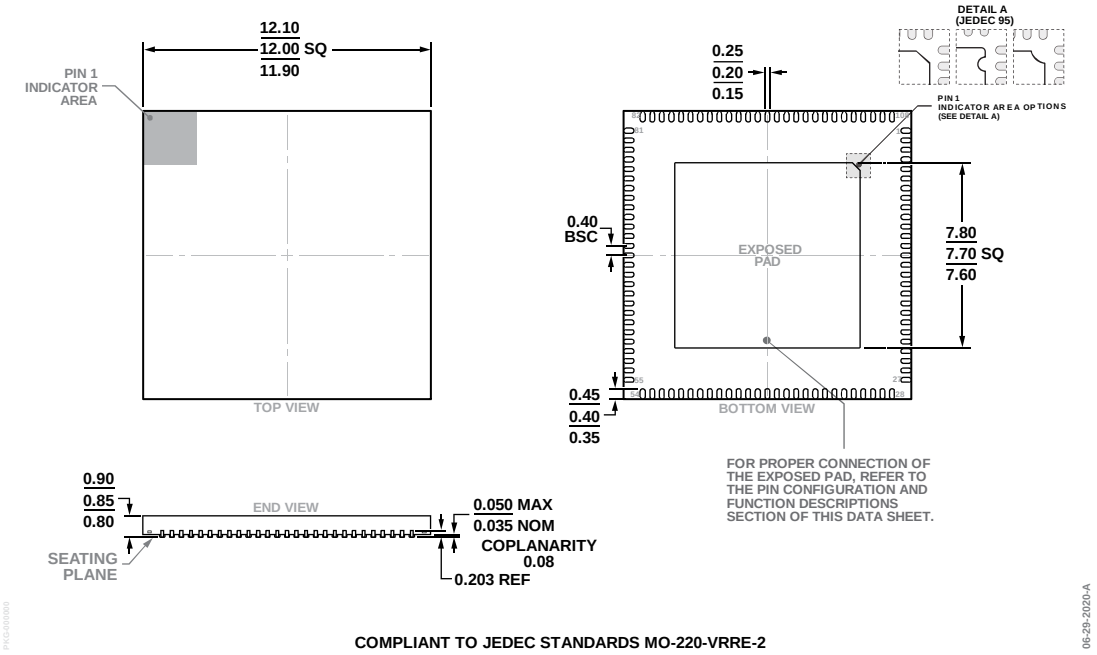


Figure 18. 108-Lead Lead Frame Chip Scale Package [LFCSP] (CP-108-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model [1,2,3]	Temperature Range	Package Description	Package Option
ADV7671JCPZ	0°C to 70°C	108-Lead Lead Frame Chip Scale Package [LFCSP]	CP-108-1
ADV7671JCPZ-RL	0°C to 70°C	108-Lead Lead Frame Chip Scale Package [LFCSP]	CP-108-1

[1] Z = RoHS-Compliant Part.
[2] Customers must have HDMI adopter status and HDMI 2.1 licensing (consult HDMI.org for adopter and licensing information) to purchase these components
[3] Customers must have HDCP adopter status and HDCP 2.x licensing (consult Digital Content Protection, LLC, for licensing requirements) to purchase these components.

NOTES

I²C refers to a communications protocol originally developed by Phillips Semiconductors (now NXP Semiconductors).

HDMI, the HDMI Logo, and High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing Administrator, Inc., in the United States and other countries.