FAIRCHILD
SEMICONDUCTOR®

February 2004

FDC796N

30V N-Channel PowerTrench® MOSFET

General Description

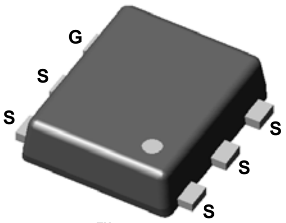
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$ and fast switching speed.

Applications

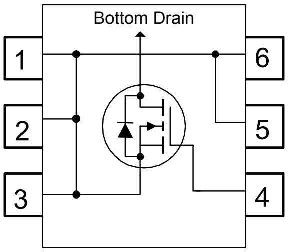
- DC/DC converter
- Power management
- Load switch

Features

- 12.5 A, 30 V. $R_{DS(ON)}$ = 9 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 12 mΩ @ V_{GS} = 4.5 V
- High performance trench technology for extremely low $R_{DS(ON)}$
- Low gate charge
- High power and current handling capability
- Fast switching speed.



SuperSOT-6™ FLMP



Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	
I_D	Drain Current – Continuous (Note 1a)	12.5	A
	– Pulsed	40	
P_D	Maximum Power Dissipation (Note 1a)	2	W
	(Note 1b)	1.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	60	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	111	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.5	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.796	FDC796N	7''	8mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		25		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			10	μA
I_{GSS}	Gate–Body Leakage	V_{GS} = ± 20 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	1	2	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C		– 5.6		mV/°C
$R_{DS(on)}$	Static Drain–Source On Resistance	V_{GS} = 10 V, I_D = 12.5 A V_{GS} = 4.5 V, I_D = 11 A V_{GS} = 10 V, I_D = 12.5 A, T_J=125°C		7.4 9.5 9	9 12 16	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 12.5 A		48.4		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		1444		pF
C_{oss}	Output Capacitance			342		pF
C_{rss}	Reverse Transfer Capacitance			135		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		1.25		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Turn–On Rise Time			3.8	7.6	ns
$t_{d(off)}$	Turn–Off Delay Time			26	42	ns
t_f	Turn–Off Fall Time			13	23	ns
Q_g	Total Gate Charge	V_{DS} = 15 V, I_D = 12.5 A, V_{GS} = 5 V		14	20	nC
Q_{gs}	Gate–Source Charge			4		nC
Q_{gd}	Gate–Drain Charge			5		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				1.5	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.5 A (Note 2)		0.73	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 12.5 A, d_{iF}/d_t = 100 A/µs		25		nS
Q_{rr}	Diode Reverse Recovery Charge			15		nC

Notes: 1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 60°C/W when mounted on a 1in^2 pad of 2 oz copper

b) 111°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

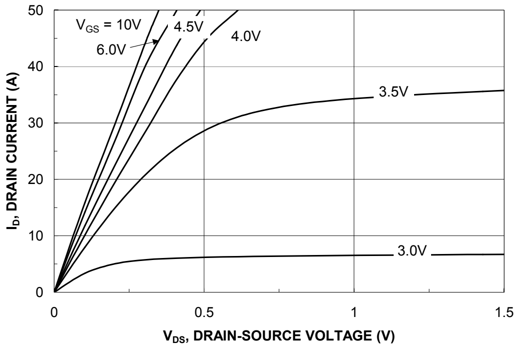


Figure 1. On-Region Characteristics.

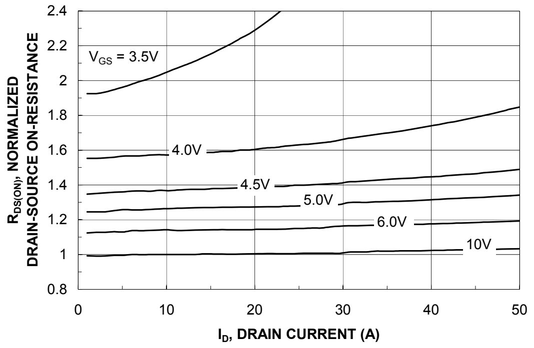


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

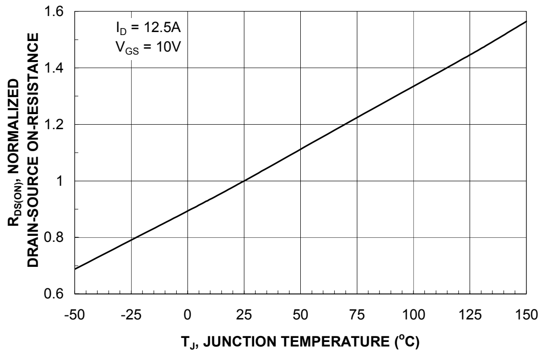


Figure 3. On-Resistance Variation with Temperature.

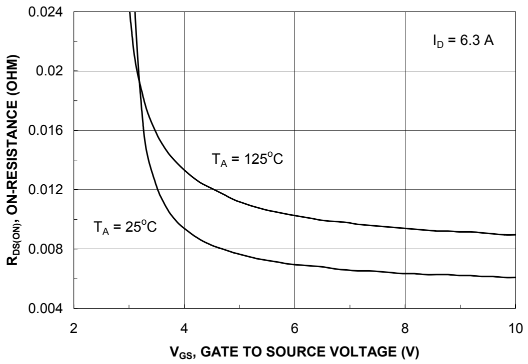


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

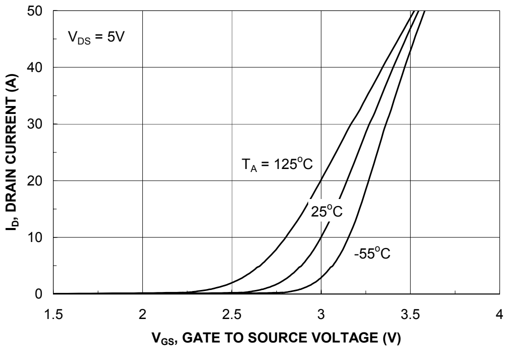


Figure 5. Transfer Characteristics.

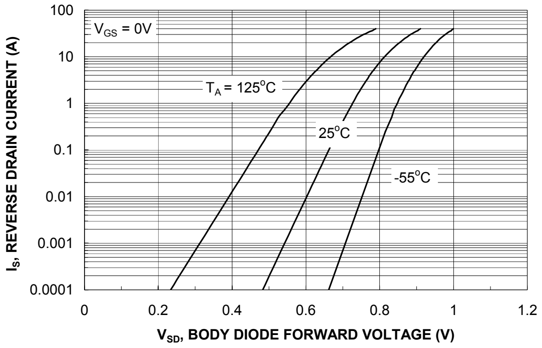


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

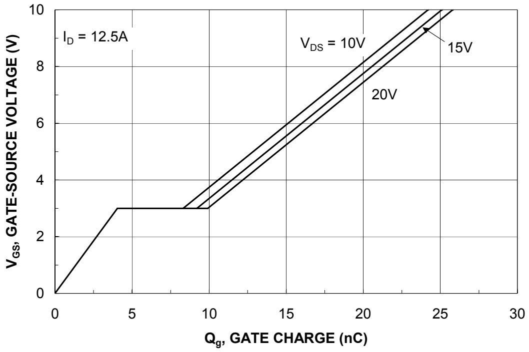


Figure 7. Gate Charge Characteristics.

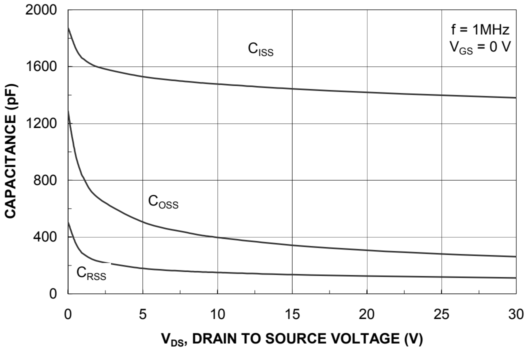


Figure 8. Capacitance Characteristics.

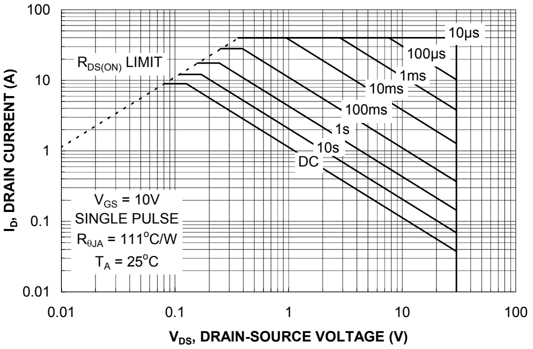


Figure 9. Maximum Safe Operating Area.

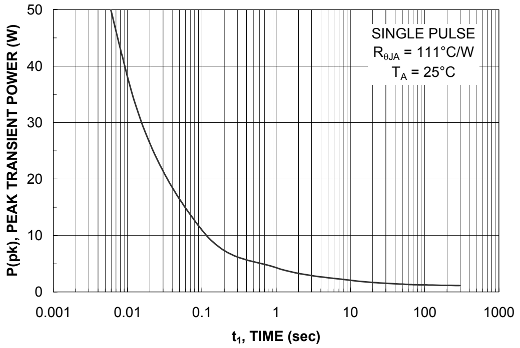


Figure 10. Single Pulse Maximum Power Dissipation.

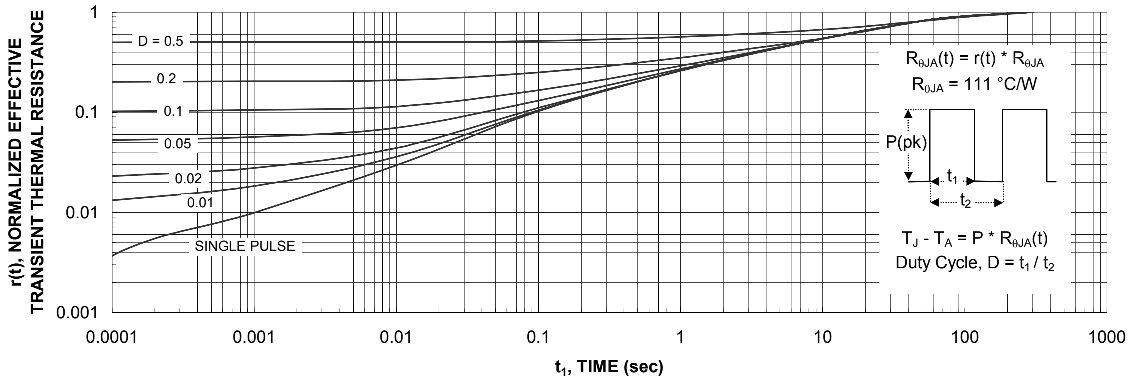
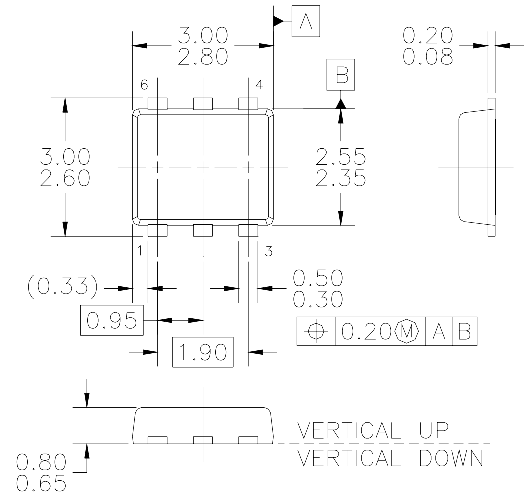
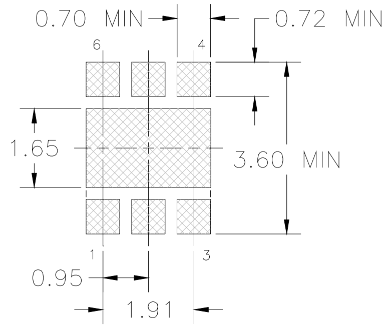


Figure 11. Transient Thermal Response Curve.

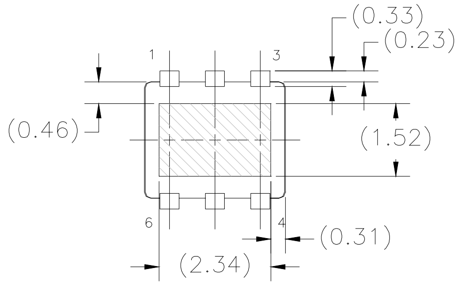
Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout

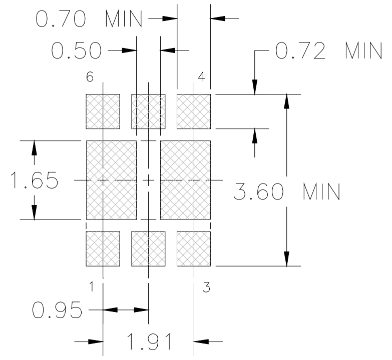




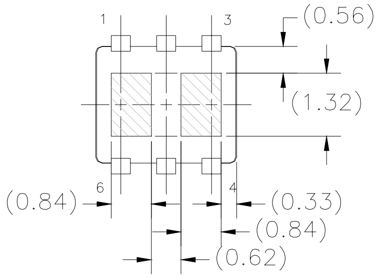
LAND PATTERN RECOMMENDATION (OPTION 01)



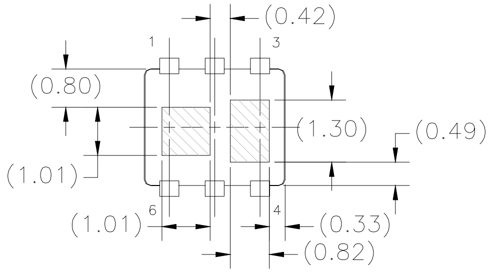
BOTTOM VIEW OPTION 01



LAND PATTERN RECOMMENDATION (OPTION 02&03)



BOTTOM VIEW OPTION 02



BOTTOM VIEW OPTION 03

NOTES: UNLESS OTHERWISE SPECIFIED

A) NO PACKAGE STANDARD REFERENCE AS OF MARCH, 2001.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH AND CUTTING BURRS.
D) LEAD TIP BURR:
   HORIZONTAL: 0.20 mm MAX
   VERTICAL UP: 0.20 mm MAX
   VERTICAL DOWN: 0.05 mm MAX

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