

EPC2046 – Enhancement-Mode Power Transistor

Preliminary Specification Sheet

Status: Engineering

Features:

- V_{DS} , 200 V
- Maximum $R_{DS(on)}$, 25 m Ω
- I_D , 11 A

Applications:

- Multi-level AC-DC Power Supplies
- Synchronous Rectification (48 V_{OUT})
- Wireless Charging
- Photovoltaic Micro Inverters
- Robotics
- Class D Audio
- Low Inductance Motor Drives



EPC2046 eGaN® FETs are supplied in passivated die form with solder bumps.

Die Size: 2.8 mm x 0.95 mm

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
I_D	Continuous ($T_A = 25^\circ\text{C}$, $R_{\theta JA} = 8^\circ\text{C/W}$)	11	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	55	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$, $I_D = 0.45 \text{ mA}$	200			V
I_{DSS}	Drain Source Leakage	$V_{DS} = 160 \text{ V}$, $V_{GS} = 0 \text{ V}$	10	150		μA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$	0.1	2		mA
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$	10	150		μA
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 7 \text{ mA}$	0.8	1.6	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$, $I_D = 20 \text{ A}$	18	25		m Ω

Thermal Characteristics			
		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2	$^\circ\text{C/W}$
$R_{\theta JB}$	Thermal Resistance, Junction to Board	13	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	72	$^\circ\text{C/W}$

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

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Dynamic Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance		285	345	pF
C_{RSS}	Reverse Transfer Capacitance		1		
C_{OSS}	Output Capacitance		145	220	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (note 2)		170		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (note 3)		220		
R_G	Gate Resistance		0.42		Ω
Q_G	Total Gate Charge	$V_{DS} = 100\text{ V}, V_{GS} = 5\text{ V}, I_D = 11\text{ A}$	2.9	3.6	nC
Q_{GS}	Gate-to-Source Charge	$V_{DS} = 100\text{ V}, I_D = 11\text{ A}$	1		
Q_{GD}	Gate-to-Drain Charge		0.6		
$Q_{G(TH)}$	Gate Charge at Threshold		0.6		
Q_{OSS}	Output Charge	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	22	33	
Q_{RR}	Source-Drain Recovery Charge		0		

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{OS} is rising from 0 to 50% BV_{DS} .

Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{OS} is rising from 0 to 50% BV_{DS} .

Figure 1: Typical Output Characteristics at 25°C

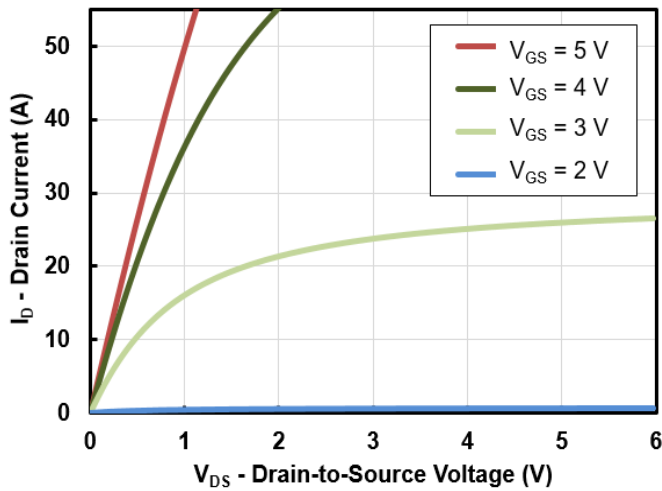
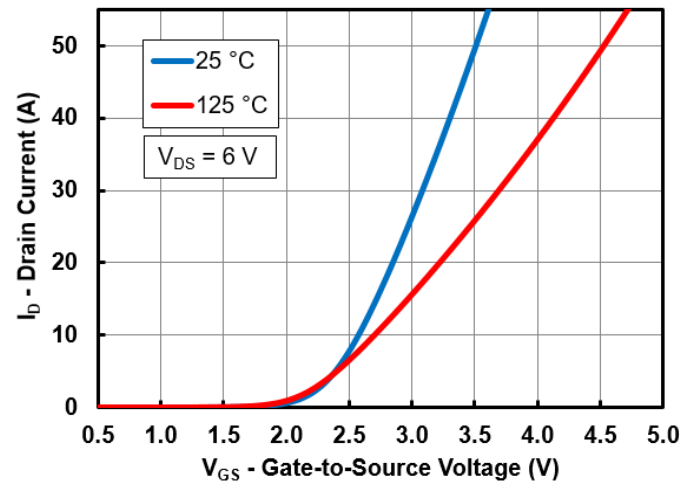


Figure 2: Transfer Characteristics



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Figure 3: $R_{DS(on)}$ vs V_{GS} for Various Drain Currents

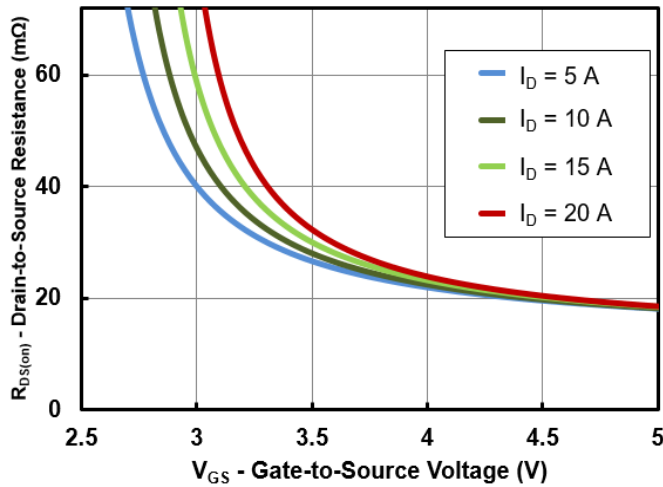


Figure 4: $R_{DS(on)}$ vs V_{GS} for Various Temperatures

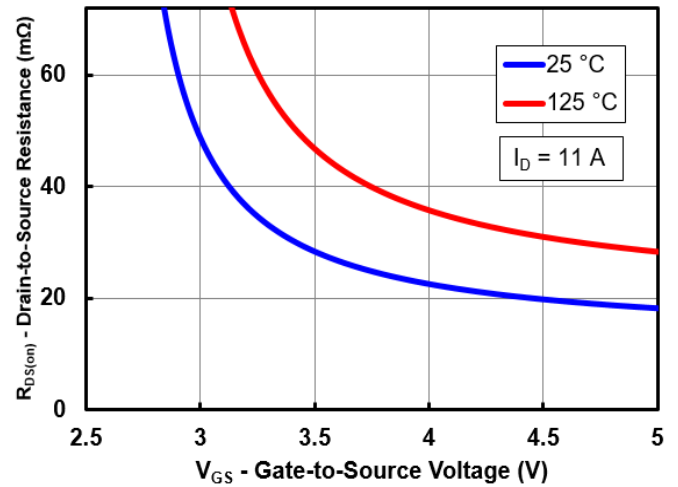


Figure 5a: Capacitance (Linear Scale)

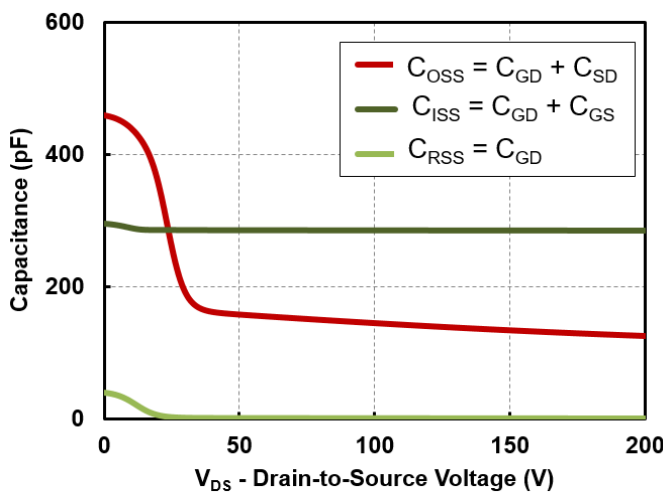


Figure 5b: Capacitance (Log Scale)

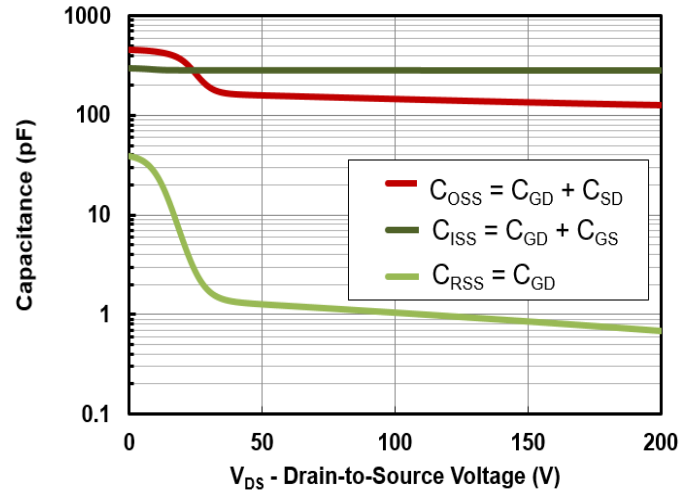


Figure 6: Output Charge Q_{OSS} and C_{OSS} Stored Energy E_{OSS}

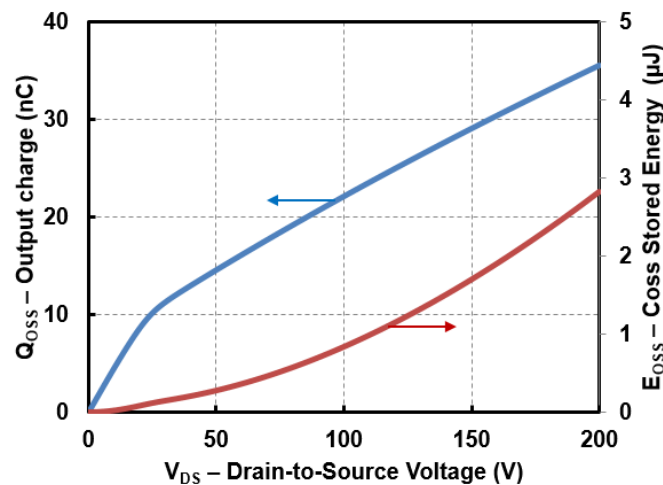
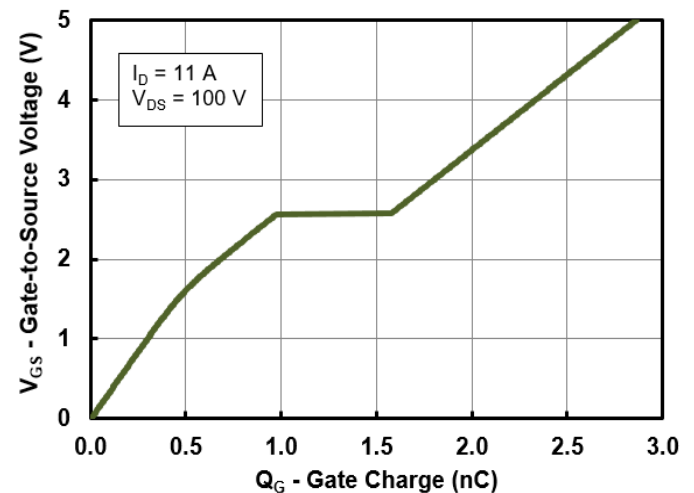


Figure 7: Gate Charge



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Figure 8: Reverse Drain-Source Characteristics

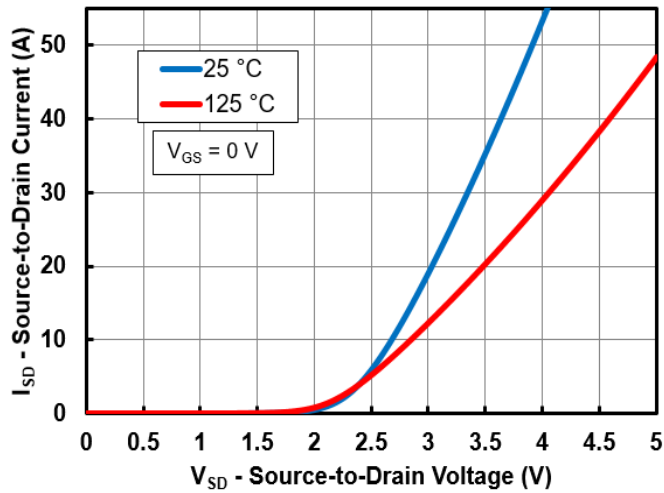


Figure 9: Normalized On-State Resistance vs Temperature

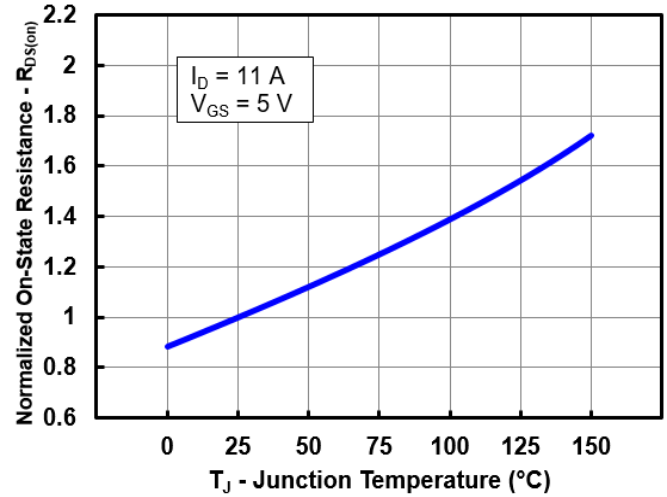


Figure 10: Normalized Threshold Voltage vs Temperature

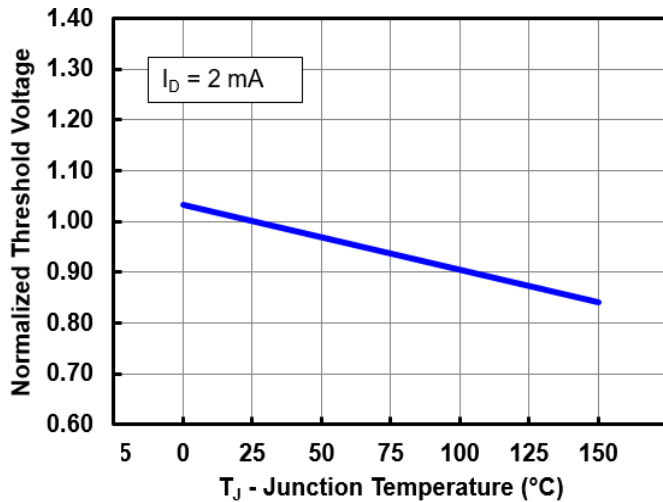
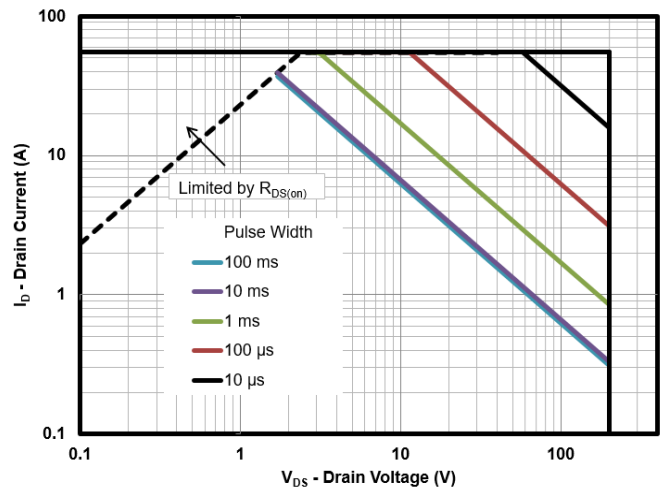


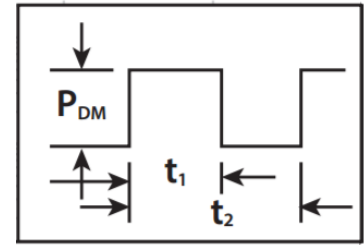
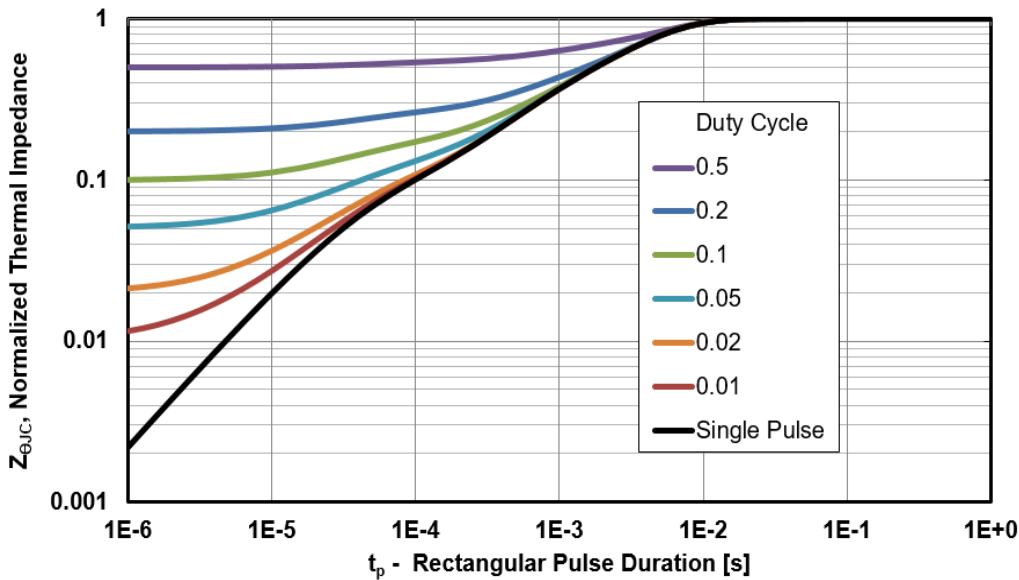
Figure 11: Safe Operating Area



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Figure 12a: Transient Thermal Response Curves (Junction-to-Case)

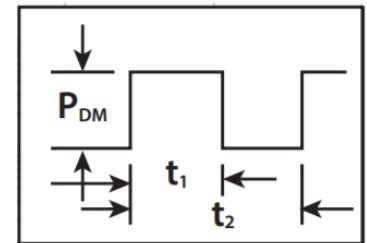
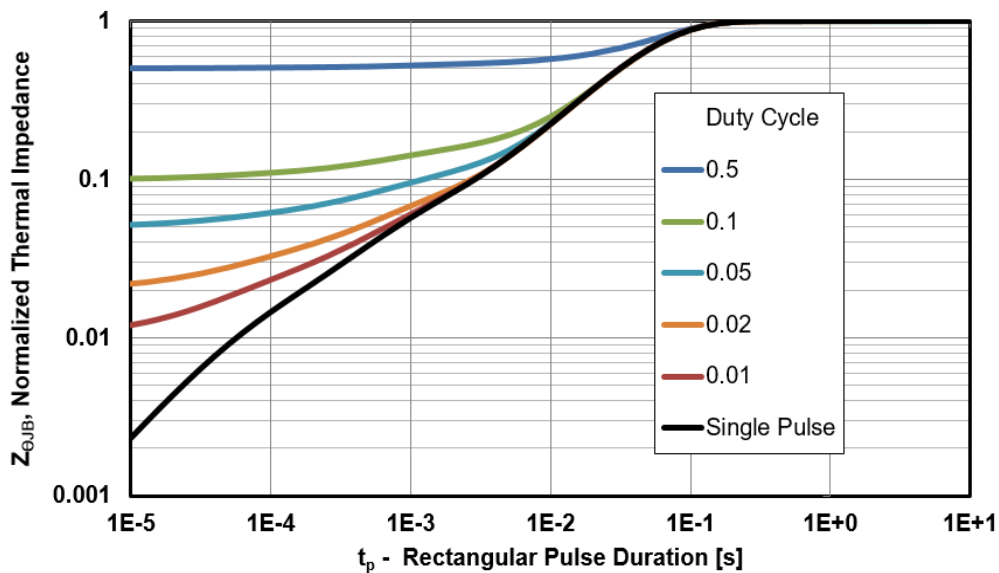


Notes:

Duty Factor: $D = t_1/t_2$

Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

Figure 12b: Transient Thermal Response Curves (Junction-to-Board)



Notes:

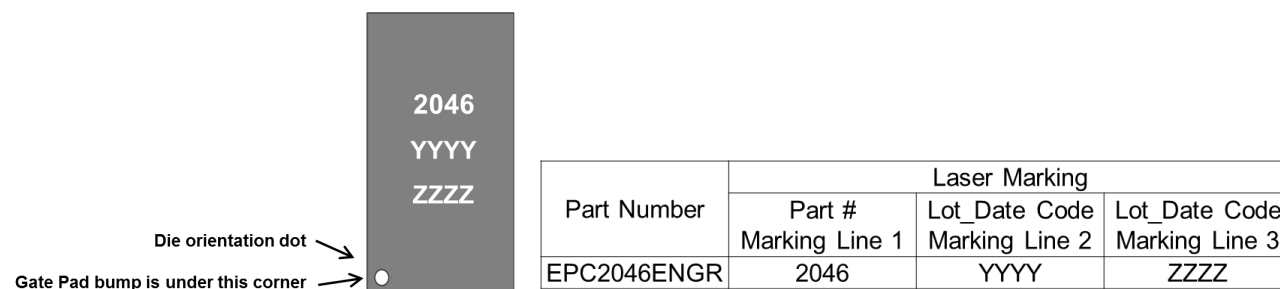
Duty Factor: $D = t_1/t_2$

Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

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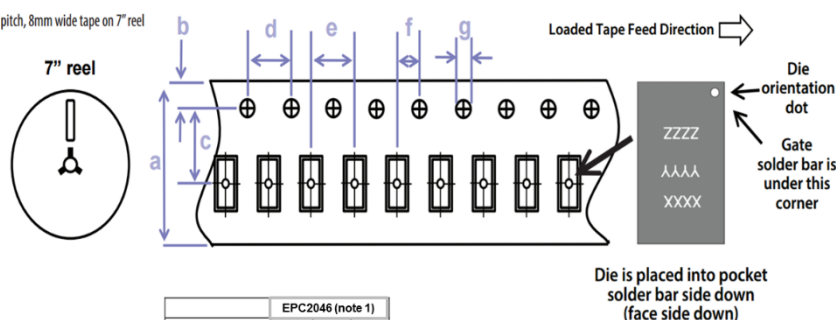
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DIE MARKINGS



TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

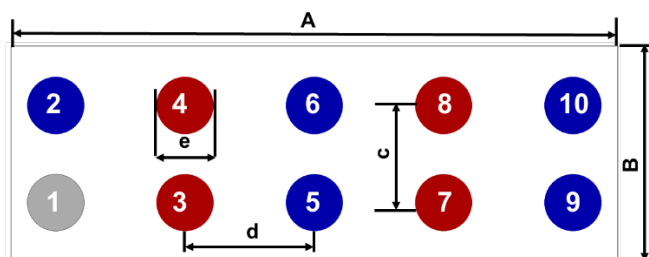


EPC2046 (note 1)			
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE OUTLINE

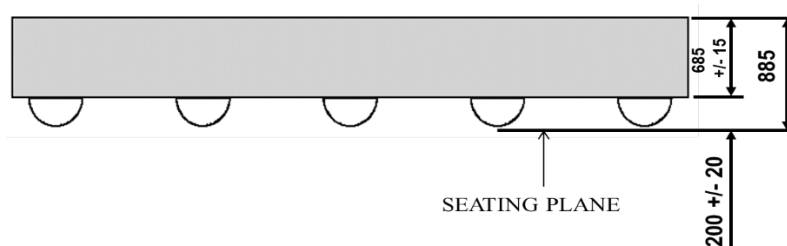
Solder Bar View



Pad 1 is Gate;
Pads 2, 5, 6, 9, 10 are Source;
Pads 3, 4, 7, 8 are Drain;

DIM	MICROMETERS		
	MIN	Nominal	MAX
A	2736	2766	2796
B	920	950	980
c		450	
d		600	
e	238	264	290

Side View

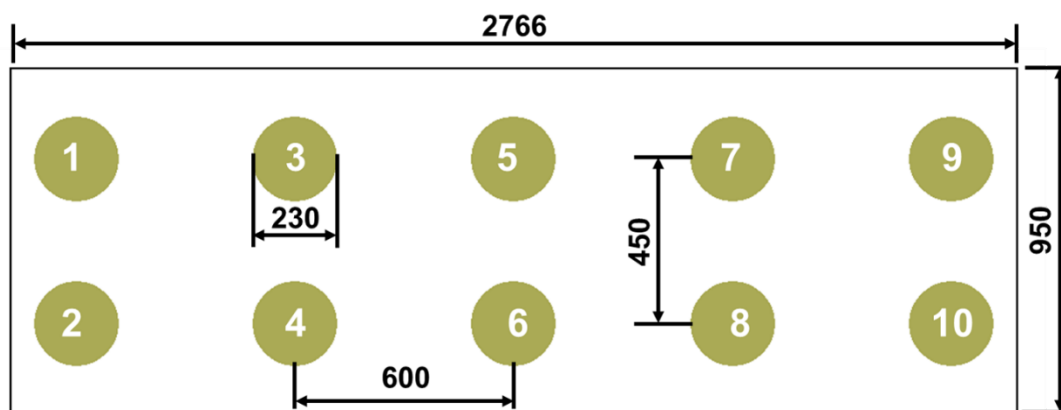


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RECOMMENDED LAND PATTERN

(measurements in μm)



Pads 1 is Gate;

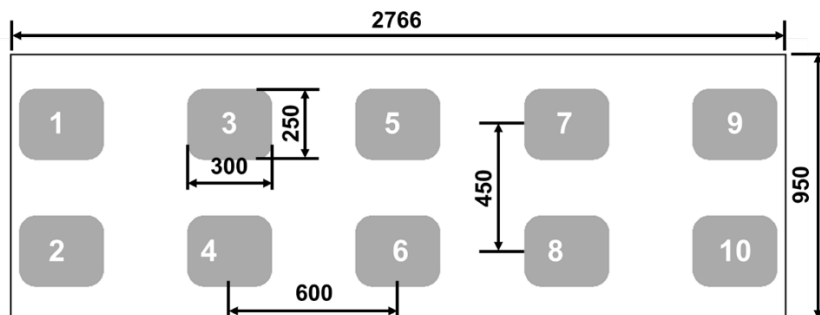
Pads 2, 3, 7, 8, 9, 13, 14, 15 are Source;

Pads 4, 5, 6, 10, 11, 12 are Drain.

The land pattern is solder mask defined
Solder mask is 10 μm smaller per side than bump

RECOMMENDED STENCIL DRAWING

(measurements in μm)



Recommended stencil should be 4mil (100 μm) thick, must be laser cut, openings per drawing.

The corner has a radius of 60 μm

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

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